

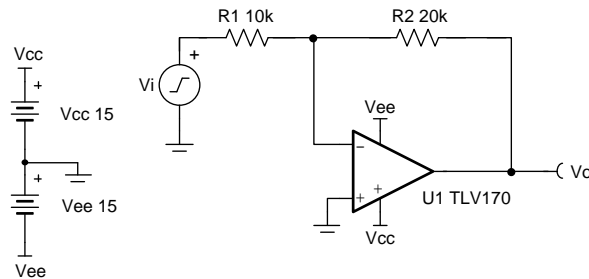
Inverting amplifier circuit

Design Goals

Input		Output		Freq.	Supply	
V_{iMin}	V_{iMax}	V_{oMin}	V_{oMax}	f	V_{cc}	V_{ee}
-7 V	7 V	-14 V	14 V	3 kHz	15 V	-15 V

Design Description

This design inverts the input signal, V_i , and applies a signal gain of -2 V/V. The input signal typically comes from a low-impedance source because the input impedance of this circuit is determined by the input resistor, R_1 . The common-mode voltage of an inverting amplifier is equal to the voltage connected to the non-inverting node, which is ground in this design.



Copyright © 2018, Texas Instruments Incorporated

Design Notes

1. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions. The common-mode voltage in this circuit does not vary with input voltage.
2. The input impedance is determined by the input resistor. Make sure this value is large when compared to the source output impedance.
3. Using high value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. Small-signal bandwidth is determined by the noise gain (or non-inverting gain) and op amp gain-bandwidth product (GBP). Additional filtering can be accomplished by adding a capacitor in parallel to R_2 . Adding a capacitor in parallel with R_2 improves stability of the circuit if high value resistors are used.
6. Large signal performance can be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth, see the Design References section.

Design Steps

The transfer function of this circuit is given below.

$$V_o = V_i \times \left(-\frac{R_2}{R_1}\right)$$

1. Determine the starting value of R_1 . The relative size of R_1 to the signal source impedance affects the gain error. Assuming the impedance from the signal source is low (for example, 100 Ω), set $R_1 = 10 \text{ k}\Omega$ for 1% gain error.

$$R_1 = 10\text{k}\Omega$$

2. Calculate the gain required for the circuit. Since this is an inverting amplifier, use $V_{i\text{Min}}$ and $V_{o\text{Max}}$ for the calculation.

$$G = \frac{V_{o\text{Max}}}{V_{i\text{Min}}} = \frac{14\text{V}}{-7\text{V}} = -2\frac{\text{V}}{\text{V}}$$

3. Calculate R_2 for a desired signal gain of -2 V/V .

$$G = -\frac{R_2}{R_1} \rightarrow R_2 = -G \times R_1 = -(-2\frac{\text{V}}{\text{V}}) \times 10\text{k}\Omega = 20\text{k}\Omega$$

4. Calculate the small signal circuit bandwidth to ensure it meets the 3 kHz requirement. Be sure to use the noise gain, or non-inverting gain, of the circuit.

$$\text{GBP}_{\text{TLV170}} = 1.2\text{MHz} \quad ($$

$$\text{NG} = 1 + \frac{R_2}{R_1} = 3\frac{\text{V}}{\text{V}}$$

$$\text{BW} = \frac{\text{GBP}}{\text{NG}} = \frac{1.2\text{MHz}}{3\text{V/V}} = 400\text{kHz}$$

5. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$V_p = \frac{\text{SR}}{2 \times \pi \times f} \rightarrow \text{SR} > 2 \times \pi \times f \times V_p$$

$$\text{SR} > 2 \times \pi \times 3\text{kHz} \times 14\text{V} = 263.89\frac{\text{kV}}{\text{s}} = 0.26\frac{\text{V}}{\mu\text{s}}$$

- $\text{SR}_{\text{TLV170}} = 0.4\text{V}/\mu\text{s}$, therefore it meets this requirement.

6. To avoid stability issues, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2 \times \pi \times (C_{\text{cm}} + C_{\text{diff}}) \times (R_2 \parallel R_1)} > \frac{\text{GBP}}{\text{NG}}$$

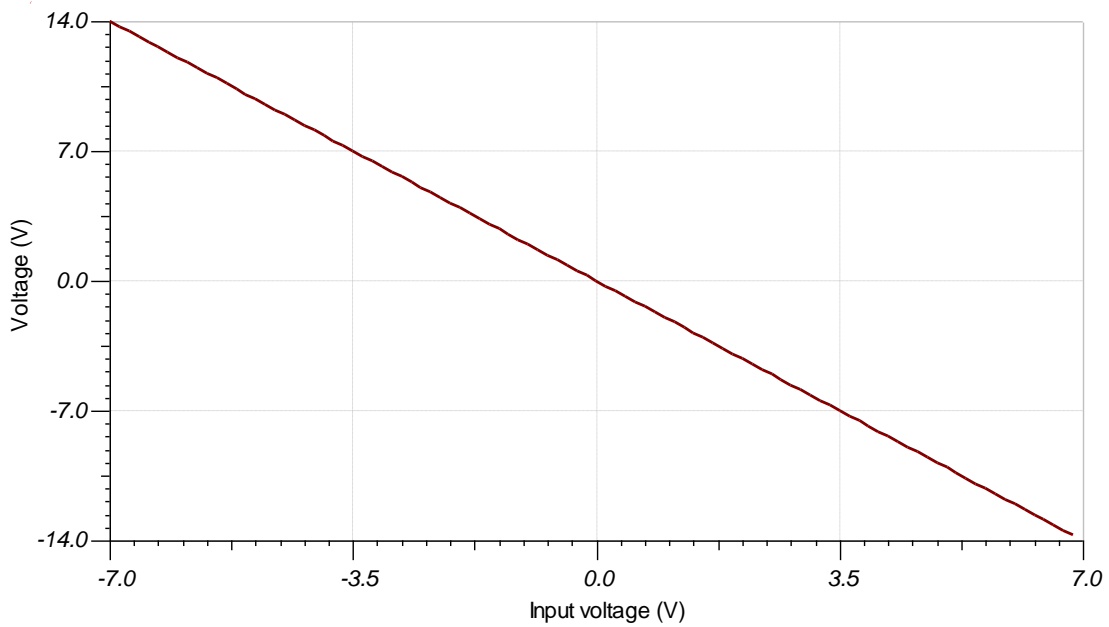
$$\frac{1}{2 \times \pi \times 3\text{pF} + 3\text{pF} \times \frac{20\text{k}\Omega \times 10\text{k}\Omega}{20\text{k}\Omega + 10\text{k}\Omega}} > \frac{1.2\text{MHz}}{3\text{V/V}}$$

$$43.77\text{MHz} > 400\text{kHz}$$

- C_{cm} and C_{diff} are the common-mode and differential input capacitances of the TLV170, respectively.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

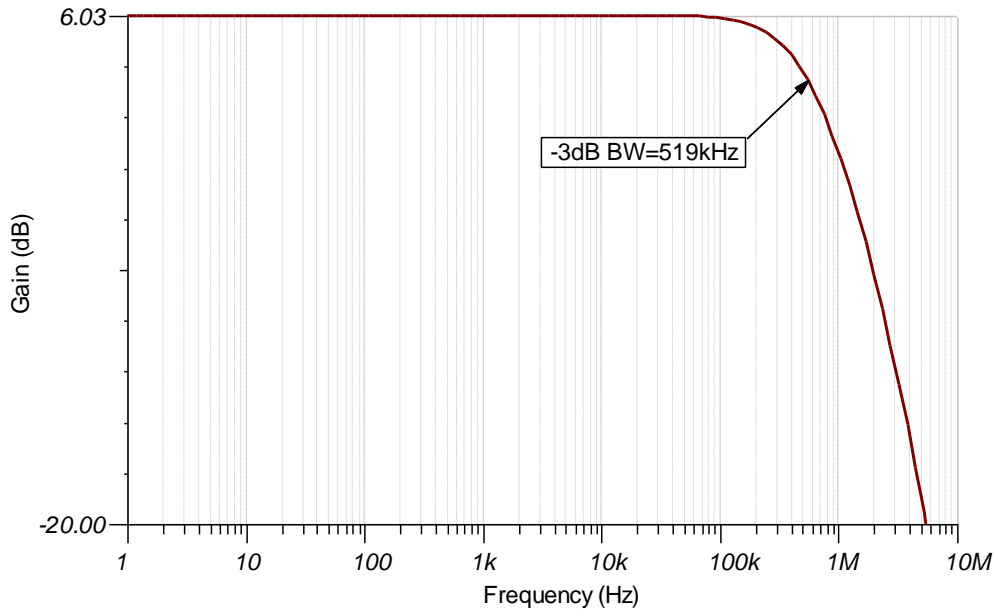
Design Simulations

DC Simulation Results



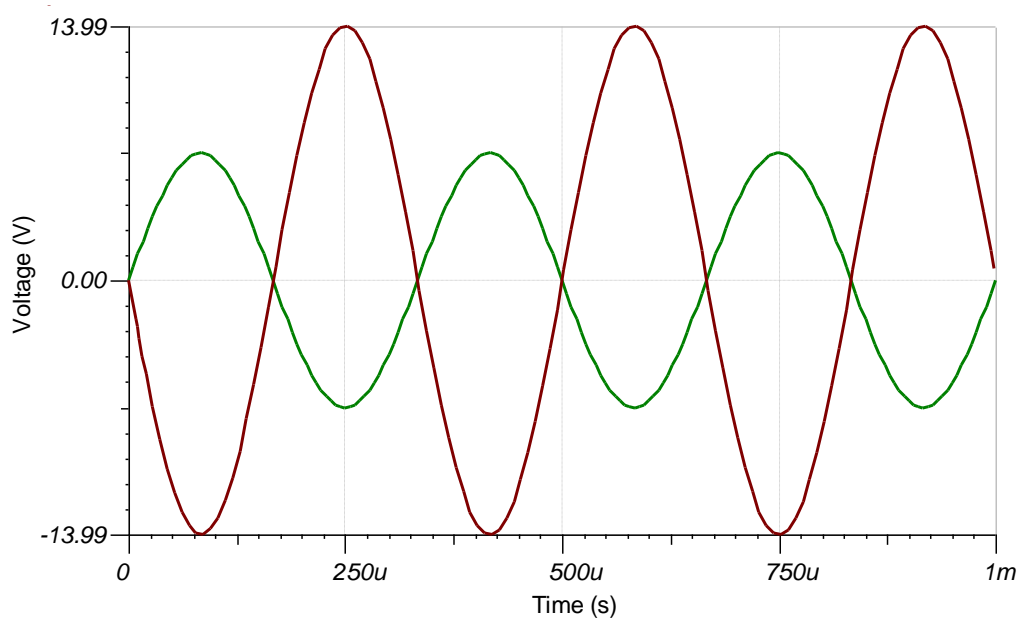
AC Simulation Results

The bandwidth of the circuit depends on the noise gain, which is 3 V/V. The bandwidth is determined by looking at the -3dB point, which is located at 3dB given a signal gain of 6dB . The simulation sufficiently correlates with the calculated value of 400 kHz .



Transient Simulation Results

The output is double the magnitude of the input and inverted.



References:

1. [Analog Engineer's Circuit Cookbooks](#)
2. SPICE Simulation File [SBOC492](#)
3. [TI Precision Labs](#)

Design Featured Op Amp

TLV170	
V_{ss}	±18 V (36 V)
V_{inCM}	(V _{ee} -0.1 V) to (V _{cc} -2 V)
V_{out}	Rail-to-rail
V_{os}	0.5 mV
I_q	125 µA
I_b	10 pA
UGBW	1.2 MHz
SR	0.4 V/µs
#Channels	1, 2, 4
www.ti.com/product/tlv170	

Design Alternate Op Amp

LMV358A	
V_{ss}	2.5 V to 5.5 V
V_{inCM}	(V _{ee} -0.1 V) to (V _{cc} -1 V)
V_{out}	Rail-to-rail
V_{os}	1 mV
I_q	70 µA
I_b	10 pA
UGBW	1 MHz
SR	1.7 V/µs
#Channels	1 (LMV321A), 2 (LMV358A), 4 (LMV324A)
www.ti.com/product/lmv358a	

Revision History

Revision	Date	Change
A	January 2019	Downscale title. Added link to circuit cookbook landing page.
B	March 2019	Changed LMV358 to LMV358A in the Design Alternate Op Amp section.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated