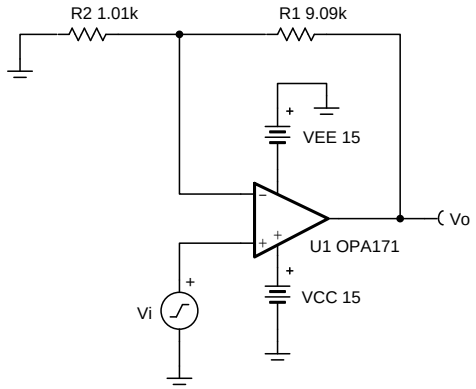
Non-inverting amplifier circuit

Design Goals

Input		Output		Supply	
ViMin	ViMax	VoMin	VoMax	Vcc	Vee
–1V	1V	–10V	10	15V	–15V

Design Description

This design amplifies the input signal, V_i, with a signal gain of 10V/V. The input signal may come from a high-impedance source (for example, MΩ) because the input impedance of this circuit is determined by the extremely high input impedance of the op amp (for example, GΩ). The common-mode voltage of a non-inverting amplifier is equal to the input signal.



Design Notes

1. Use the op amp linear output operating range, which is usually specified under the A_{OL} test conditions. The common-mode voltage is equal to the input signal.
2. The input impedance of this circuit is equal to the input impedance of the amplifier.
3. Using high-value resistors can degrade the phase margin of the circuit and introduce additional noise in the circuit.
4. Avoid placing capacitive loads directly on the output of the amplifier to minimize stability issues.
5. The small-signal bandwidth of a non-inverting amplifier depends on the gain of the circuit and the gain bandwidth product (GBP) of the amplifier. Additional filtering can be accomplished by adding a capacitor in parallel to R_1. Adding a capacitor in parallel with R_1 will also improve stability of the circuit if high-value resistors are used.
6. Large signal performance may be limited by slew rate. Therefore, check the maximum output swing versus frequency plot in the data sheet to minimize slew-induced distortion.
7. For more information on op amp linear operating region, stability, slew-induced distortion, capacitive load drive, driving ADCs, and bandwidth please see the *Design References* section.

Design Steps

The transfer function for this circuit is given below.

$$V_o = V_i \times \left(1 + \frac{R_1}{R_2}\right)$$

1. Calculate the gain.

$$G = \frac{V_{o\_max} - V_{o\_min}}{V_{i\_max} - V_{i\_min}}$$

$$G = \frac{10V - (-10V)}{1\ V - (-1\ V)} = 10V / V$$

2. Calculate values for R_1 and R_2.

$$G = 1 + \frac{R_1}{R_2}$$

Choose $R_1 = 9.09k\Omega$

$$R_2 = \frac{R_1}{G - 1} = \frac{9.09k\Omega}{10V/V - 1} = 1.01k\Omega$$

3. Calculate the minimum slew rate required to minimize slew-induced distortion.

$$SR > 2 \times \pi \times V_p \times f = 2 \times \pi \times 10V \times 20kHz = 1.257V / \mu s$$

- The slew rate of the OPA171 is 1.5V/µs, therefore it meets this requirement.

4. To maintain sufficient phase margin, ensure that the zero created by the gain setting resistors and input capacitance of the device is greater than the bandwidth of the circuit.

$$\frac{1}{2 \times \pi \times (C_{cm} + C_{diff}) \times (R_1 \parallel R_2)} > \frac{GBP}{G}$$

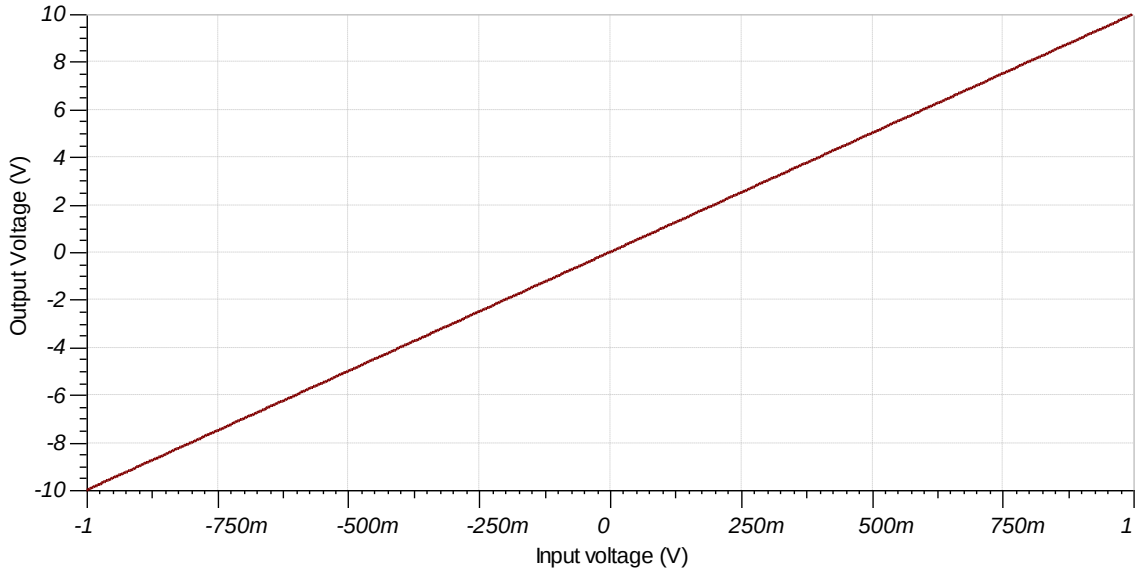
$$\frac{1}{2 \times \pi \times (3pF + 3pF) \times \frac{1.01k\Omega \times 9.09k\Omega}{1.01k\Omega + 9.09k\Omega}} > \frac{3MHz}{10V/V}$$

$$29.18MHz > 300kHz$$

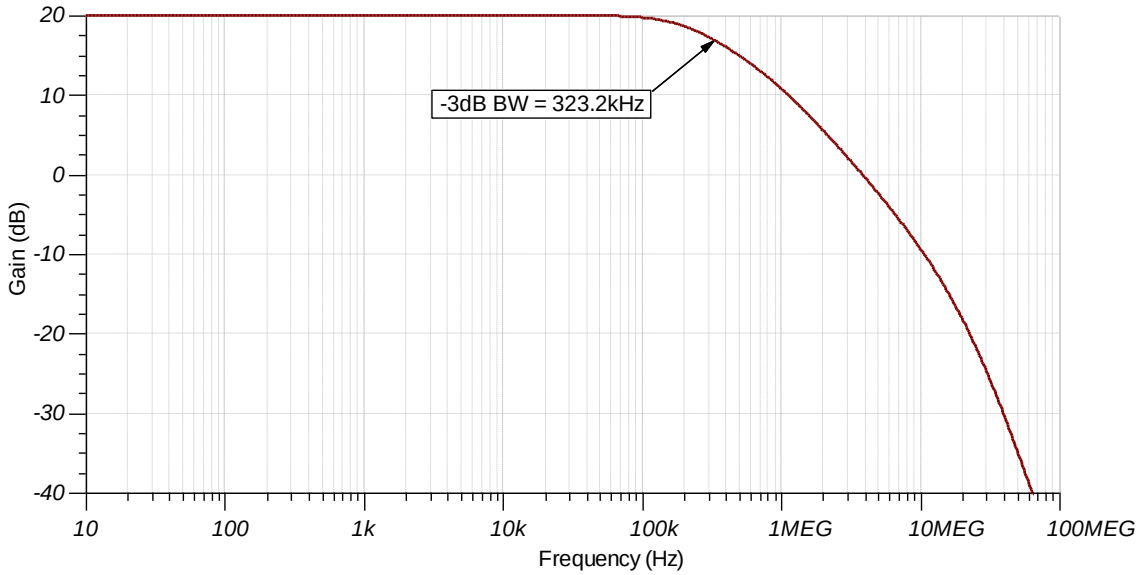
- C_{cm} and C_{diff} are the common-mode and differential input capacitances of the OPA171, respectively.
- Since the zero frequency is greater than the bandwidth of the circuit, this requirement is met.

Design Simulations

DC Simulation Results



AC Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit SPICE simulation file SBOC493.

For more information on many op amp topics including common-mode range, output swing, and bandwidth please visit TI Precision Labs.

Design Featured Op Amp

OPA171	
V_{ss}	2.7V to 36V
V_{inCM}	(V_{ee}–0.1V) to (V_{cc}–2V)
V_{out}	Rail-to-rail
V_{os}	250µV
I_q	475µA
I_b	8pA
UGBW	3MHz
SR	1.5V/µs
#Channels	1, 2, 4
www.ti.com/product/opa171	

Design Alternate Op Amp

OPA191	
V_{ss}	4.5V to 36V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	5µV
I_q	140µA
I_b	5pA
UGBW	2.5MHz
SR	7.5V/µs
#Channels	1, 2, 4
www.ti.com/product/OPA191	

Revision History

Revision	Date	Change
A	January 2019	Downscale the title and changed title role to 'Amplifiers'. Added link to circuit cookbook landing page.

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