Analog Engineer's Circuit

Signal and clock recovery comparator circuit

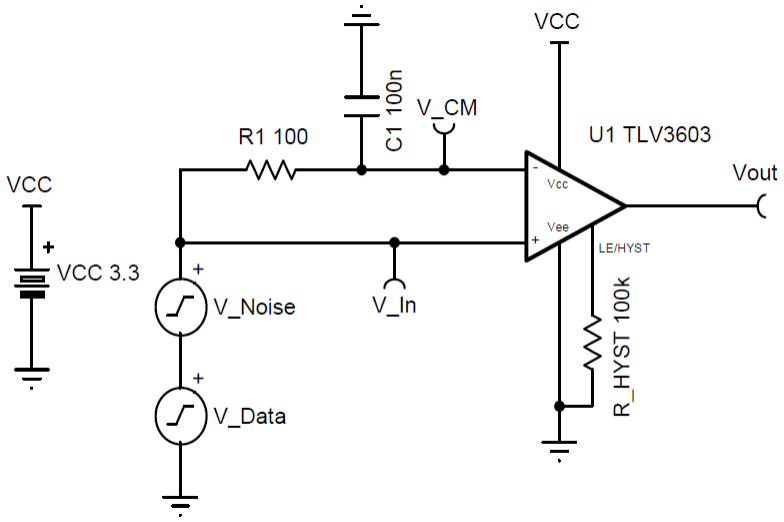
Amplifiers

Design Goals

Supply		Attenuated Input Signal		
V_{cc}	V_{ee}	V_i	V_{cm}	f
3.3V	0V	$50mV_{p-p}$	1.65V	200MHz

Design Description

The signal recovery circuit is used in digital systems to retrieve distorted clock or data waveforms. These clock and data signals can be attenuated and distorted on long traces due to stray capacitance, stray inductance, or reflections on transmission lines. The comparator is used to sense the attenuated and distorted input signal and convert it to a full scale digital output signal. A dynamic reference voltage will be connected to the inverting terminal of the comparator which is extracting the common-mode voltage from the input signal.



Design Notes

1. Select a comparator with low input offset voltage and fast propagation delay.
2. Use a comparator with a toggle frequency larger than the input signal frequency to properly process the incoming digital signal. A margin of 30% is sufficient to allow for process and temperature variations if a minimum value is not warranted in the data sheet.
3. If level translation is also required, use a comparator with separate input and output supplies.
4. If a differential output is required, use a comparator with a compatible output stage such as the LVDS compatible output on the TLV3605.
5. The signal should be symmetric around the waveform midpoint for the dynamic reference to accurately determine the common mode voltage of the input signal. For signals with duty cycles outside of 30–70%, the dynamic reference must be replaced with an external reference source.

Design Steps

1. Compare the maximum toggle frequency of the comparator to ensure it can process the input signal. This parameter is usually specified in the data sheet of the comparator. If this value is not, see the following section for guidelines on approximation. The toggle frequency of this comparator, TLV3603, is 325MHz.
2. Set the non-inverting input of the comparator to the input data signal.
3. Create a dynamic reference from a low-pass network using a capacitor, C_1, and resistor, R_1. Connect the input of the network to the non-inverting input and the output to the inverting input.
4. Size the values of the dynamic reference so that its cutoff frequency is significantly below the operating frequency of the input signal while ensuring the time constant of the network is small enough for maximum responsivity. Let C_1 = 0.1µF and designing for a time constant τ of 10µs, calculate the needed resistor value:

   $$\tau = R_1 C_1$$

   $$10\mu s = R_1(100nF) \Rightarrow R_1 = 100\Omega$$

   Using the solved-for resistor value, ensure the cutoff frequency is still significantly below the input signal frequency.

   $$f_{cutoff} = \frac{1}{2\pi R_1 C_1} = \frac{1}{2\pi(100\Omega)(100nF)} = 15.915kHz \ll 1GHz$$

   The time constant τ has an inverse relationship with f_{cutoff}. The quicker τ is, the more reactive the dynamic reference output node is to the input while pushing the cutoff frequency higher. However, if the cutoff frequency of the dynamic reference approaches the operating frequency of the input signal, the output of the network is unable to properly filter out the high-frequency component of the input signal, thereby failing to generate a stable DC reference voltage to compare the input signal against.

   A ramification to consider when balancing the accurate filtering of the signal versus τ is the start-up time. As the system starts in an uncharged state, once the system is active, there is a time period (around 5τ) until the voltage level at the inverting input is at an accurate level.
5. If the input signal is noisy in addition to being attenuated, the TLV3603 is able to handle the noise though implementation of its adjustable hysteresis feature. This pin can be driven with a voltage source or be attached to a resistor to VEE and can cause the comparator to have a hysteresis up to 65mV, as well as latching the output depending on the voltage seen at the pin. See the *TLV3601, TLV3603 325MHz High-Speed Comparator with 2.5ns Propagation Delay* data sheet for more information. For this circuit, a hysteresis of 10mV is implemented to counter the noisy input signals by connecting a 600-kΩ resistor to VEE.

Is this comparator fast enough for this input signal?

Toggle frequency, f_{Toggle}, is the metric that measures how fast a comparator can handle input signal speeds. This metric is measured as the input-signal frequency at which the output swing is a certain percentage compared to itself at low-input signal frequencies. The percentage varies by manufacturers and even by products, so it is important to check the data sheet of the part to see how this parameter is being met.

When f_{Toggle} is not included in data sheet of a part, there may be some concern as to whether that part is suitable for use in a system. In that case, here is a general approximation to gauge f_{Toggle} of the part:

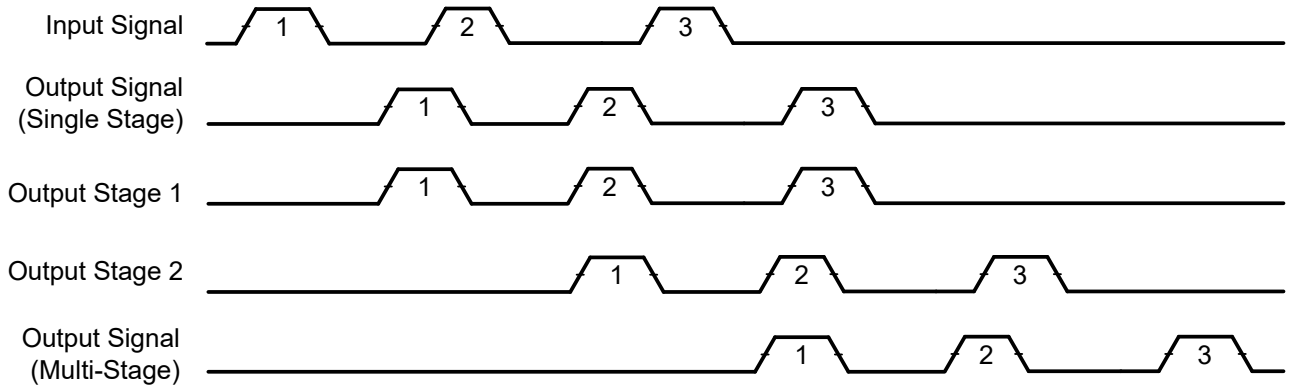
$$f_{Toggle} = (0.5t_{rise} + 0.5t_{fall} + t_{pd\_hl} + t_{pd\_lh})^{-1}$$

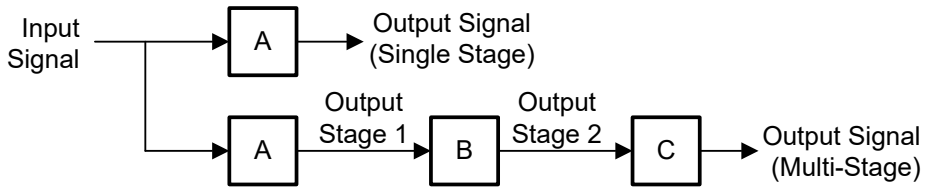
It is important to note that this approximation is conservative and may not completely match a part's f_{Toggle} inside a data sheet if specified, especially when evaluating higher speed comparators as these tend to be multi-stage comparators. Using the values included in TLV3603 data sheet:

$$f_{Toggle} = (0.375\ ns + 0.375\ ns + 2.5\ ns + 2.5\ ns)^{-1} = 173.9\ MHz$$

While the data sheet states that the toggle frequency is 325MHz, this approximation indicates that this product only handles 173.9MHz and lower signals. Why is this the case? This can be due to multiple factors, but an important consideration must be made when evaluating single (or near-single) stage products versus multi-stage products.

When using a near-single stage comparator, the input signal read by the comparator needs to pass through a low number of stages until its output transitions. f_{Toggle} is dependent on the stage with the longest propagation delay in the chain (whether that chain be one or multiple stages), rather than passing all the way through to the output before the next bit is fed in.



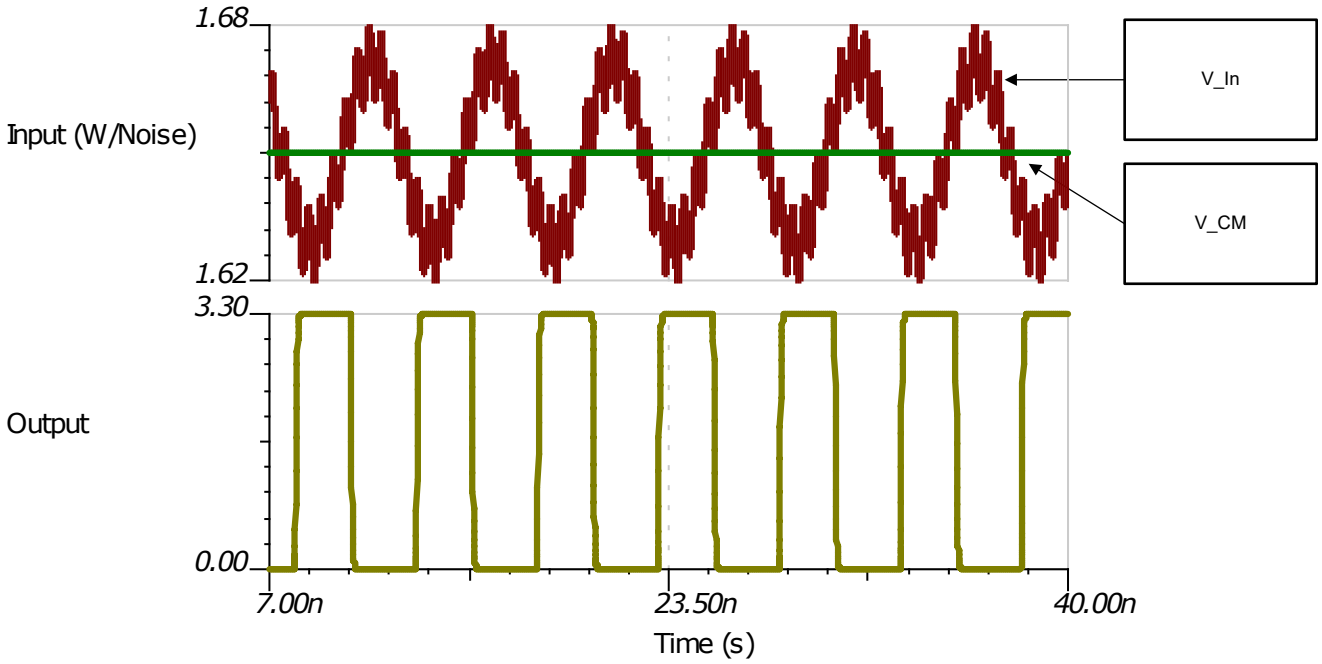


In the previous diagram, an input signal consisting of bits 1, 2, and 3 are both fed into a single stage comparator and a multi-stage comparator. The single stage comparator only has stage A, while the multi-stage comparator consists of stages A, B, and C. When bit 1 enters both comparators, it takes a period of time to get through stage A. Once it gets past stage A, on the single stage comparator, it reaches the output while on the multi-stage comparator, it enters stage B. At that point, bit 2 can begin to enter stage A. After another period of time, bit 2 reflects on the single stage output while also entering Stage B of the multi-stage comparator. Bit 1, at this point, begins to enter stage C.

This illustrates that while the propagation time may differ between a multi-stage and single stage comparator (it may be smaller, larger, or nearly the same depending on the stages), the rate at which each comparator handles these signals is dependent on when the bit clears the stage with the greatest propagation delay so that the next bit can come through the pipeline.

Design Simulations

Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See circuit spice simulation file, SNOM712.

For more information on many comparator topics including hysteresis, propagation delay and input common mode range please see, TI Precision Labs.

Design Featured Comparator

TLV3603-Q1	
V_{ss}	2.4V to 5.5V
V_{inCM}	Rail-to-rail
t_{pd}	2.5ns
V_{os}	0.5mV
V_{HYS}	0–60mV (Adjustable)
I_q	6mA
Output Type	Push-pull
#Channels	1
www.ti.com/product/tlv3603-Q1	

Design Alternate Comparator

	TLV3501	TLV3601
V_{ss}	2.7 to 5.5V	2.4 to 5.5V
V_{inCM}	Rail-to-rail	Rail-to-rail
t_{pd}	4.5ns	2.5ns
V_{os}	1mV	0.5mV
V_{HYS}	6mV	3mV
I_q	3.2mA	6mA
Output Type	Push-pull	Push-pull
#Channels	1	1
	www.ti.com/product/tlv3501	www.ti.com/product/tlv3601

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale (https:www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265