Analog Engineer's Circuit

Voltage-to-current (V-I) converter circuit with BJT

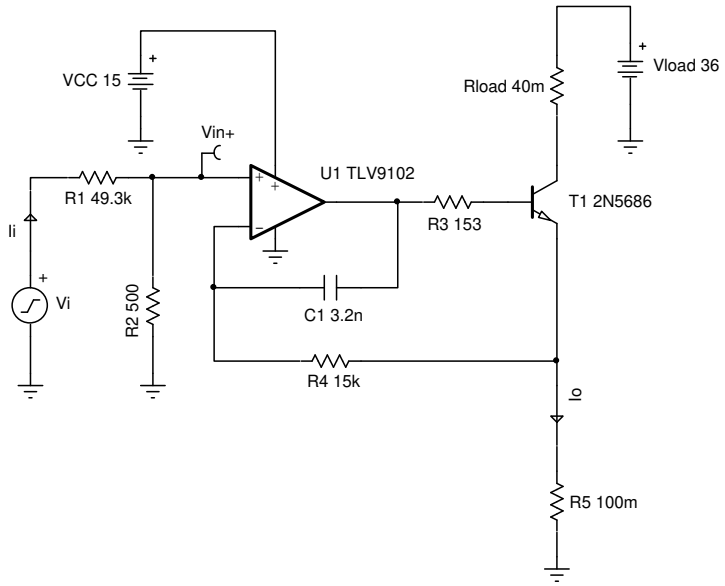
Amplifiers

Design Goals

Input			Output		Supply		
V_{iMin}	V_{iMax}	I_{iMax}	I_{oMin}	I_{oMax}	V_{cc}	V_{ee}	V_{load}
0V	10V	200µA	0A	1A	15V	0V	36V

Design Description

This low-side voltage-to-current (V-I) converter delivers a well-regulated current to a load which can be connected to a voltage greater than the op amp supply voltage. The circuit accepts an input voltage from 0V to 10V and converts it to a current from 0A and 1A. The current is accurately regulated by feeding back the voltage drop across a low-side current-sense resistor (R_5) to the op amp.



Design Notes

1. Resistor divider (R1 and R2) is implemented to limit the maximum voltage at the non-inverting input, V_{in+}, and sense resistor, R_5, at full-scale.
2. For an op amp that is not rail-to-rail input (RRI), a voltage divider may be needed to reduce the input voltage to be within the common-mode voltage of the op amp.
3. Use low resistance values for R_5 to maximize load compliance voltage and reduce the power dissipated at full-scale.
4. Using a high-gain BJT reduces the output current requirement for the op amp.
5. Feedback components R_3, R_4, and C_1 provide compensation to ensure stability. R_3 isolates the input capacitance of the bipolar junction transistor (BJT), R_4 provides a DC feedback path directly at the current-setting resistor (R_5), and C_1 provides a high-frequency feedback path that bypasses the BJT.
6. Use the op amp in a linear operating region. Linear output swing is usually specified under the A_{OL} test conditions in the device data sheet.

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Design Steps

The transfer function of the circuit is:

$$Io = \frac{R_2}{R_5 \times (R_1 + R_2)} \times Vi$$

1. Calculate the sense resistor, R_5. The sense resistor should be sized as small as possible to maximize the load compliance voltage and reduce power dissipation. Set the maximum voltage across the sense resistor to 100mV. Limiting the voltage drop to 100mV limits the power dissipated in the sense resistor to 100mW at full-scale output.

   $$\text{Let } V_{in\text{-}(max)} = 100mV \text{ at } I_{oMax} = 1A$$

   $$R_5 = \frac{V_{in\text{-}(max)}}{I_{oMax}} = \frac{100mV}{1A} = 100m\Omega$$

2. Select resistors, R_1 and R_2, for the voltage divider at the input. At the maximum input voltage, the voltage divider should reduce the input voltage to the op amp, $V_{in+(max)}$, to the maximum voltage across the sense resistor, R_5. R_1 and R_2 should be chosen such that the maximum input current is not exceeded.

   $$V_{in\text{-}(max)} = V_{in+(max)} = I_{iMax} \times R_2 = 100mV$$

   $$R_2 = \frac{V_{in+(max)}}{I_{iMax}} = \frac{100mV}{200\mu A} = 500\Omega \sim 499\Omega \text{ (Standard value)}$$

   $$V_{in+(max)} = V_{iMax} \times \left(\frac{R_2}{R_1 + R_2}\right)$$

   $$R_1 = 49.5k\Omega \sim 49.3k\Omega \text{ (Standard value)}$$

3. See the Design References section [3] for the design procedure on how to properly size the compensation components, R_3, R_4, and C_1.

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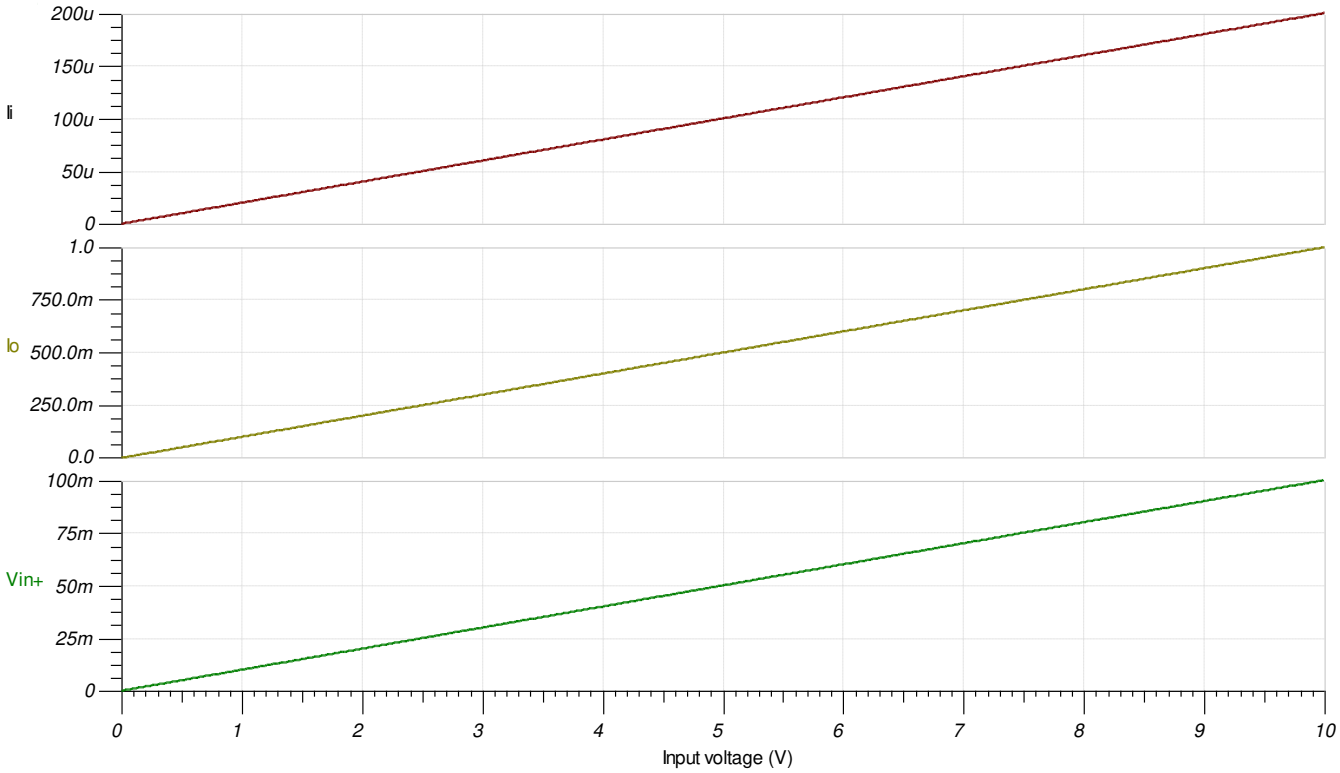
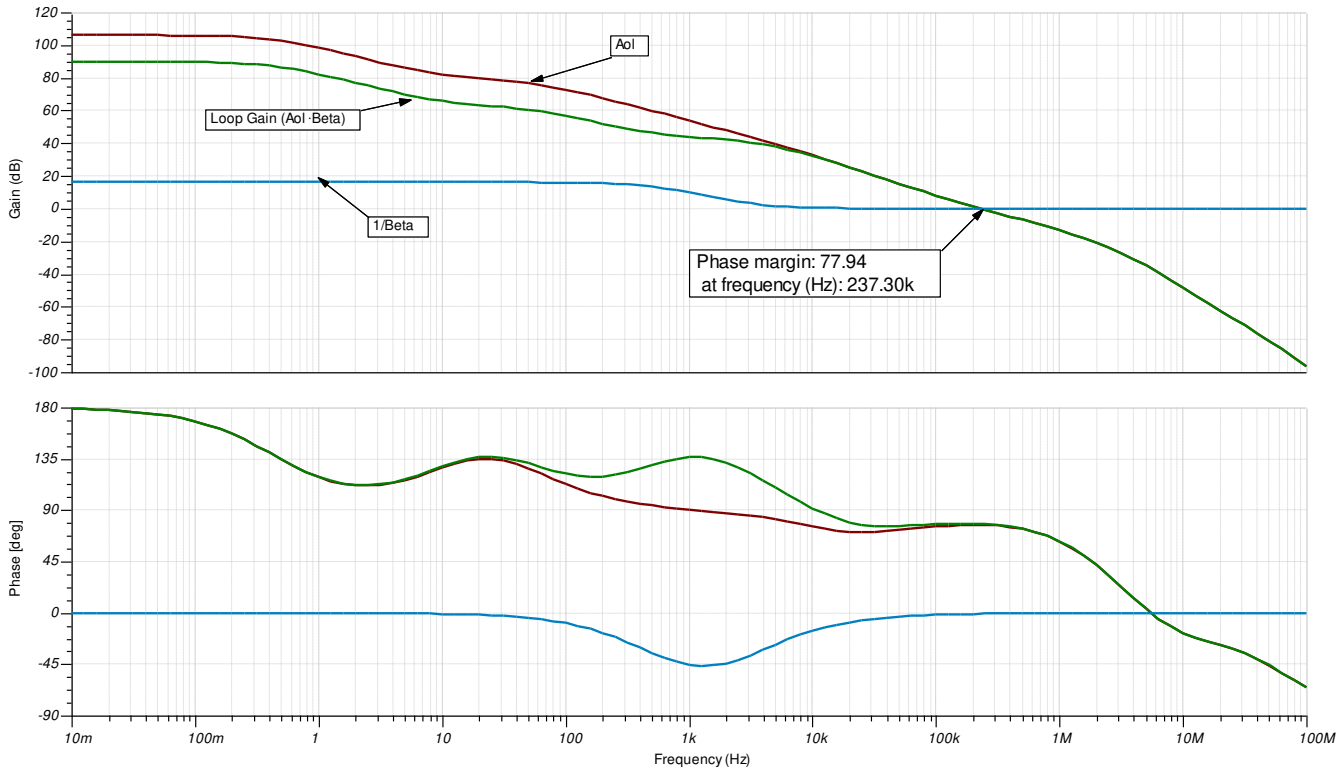
Design Simulations

DC Simulation Results



AC Simulation Results



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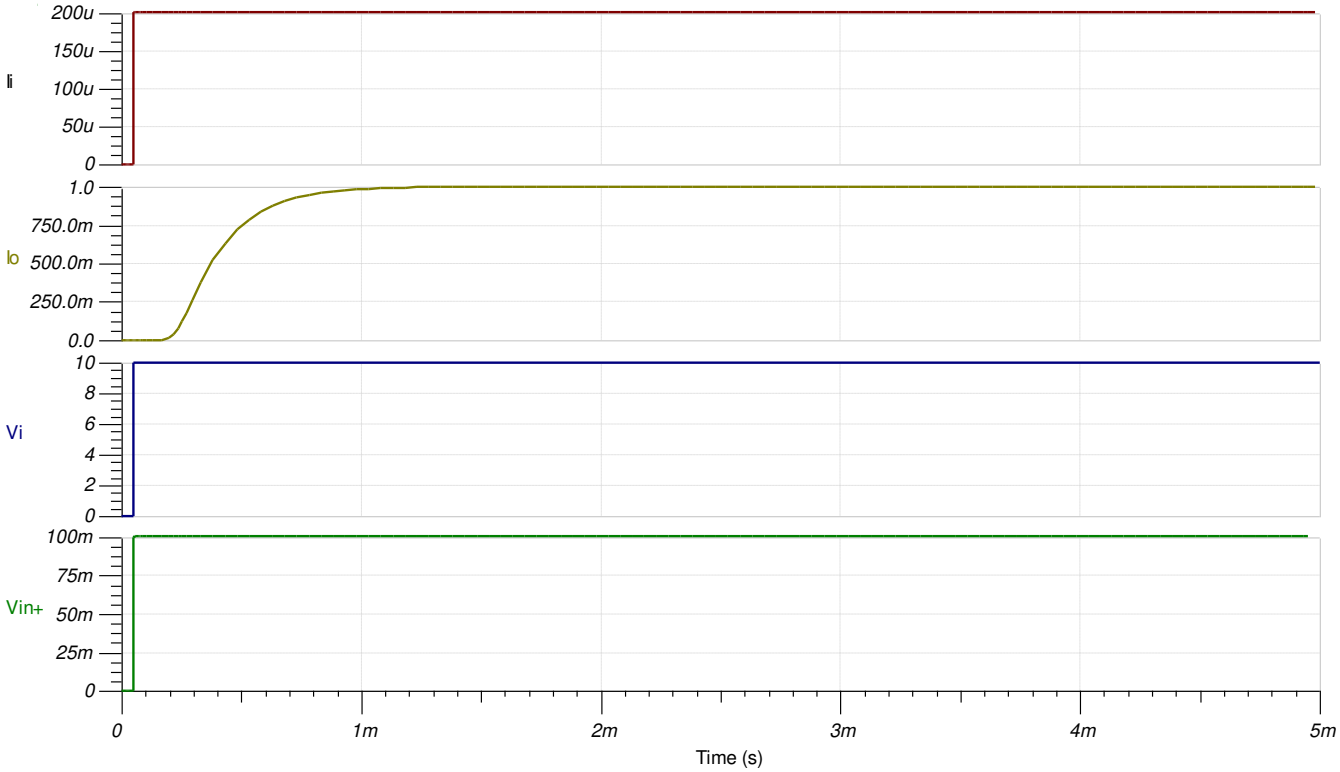
Transient Simulation Results



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Design References

1. See Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.
2. SPICE Simulation File: SBOMB58.
3. TI Precision Labs

Design Featured Op Amp

TLV9102	
V_{ss}	±1.35V to ±8V, 2.7V to 16V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.3mV
I_q	120µA
I_b	10pA
UGBW	1.1MHz
SR	4.5V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9102	

Design Alternate Op Amp

TLV9152	
V_{ss}	±1.35V to ±8V, 2.7V to 16V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	125µV
I_q	560µA
I_b	10pA
UGBW	4.5MHz
SR	20V/µs
#Channels	1, 2, 4
www.ti.com/product/TLV9152	

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