Application Report

INA293-Q1 Functional Safety FIT Rate, FMD and Pin FMA

1 Overview

This document contains information for INA293-Q1 (SOT-23-5 package) to aid in a functional safety system design. Information provided are:

- Functional Safety Failure In Time (FIT) rates of the semiconductor component estimated by the application of industry reliability standards
- Component failure modes and their distribution (FMD) based on the primary function of the device
- Pin failure mode analysis (Pin FMA)

Figure 1-1 shows the device functional block diagram for reference.

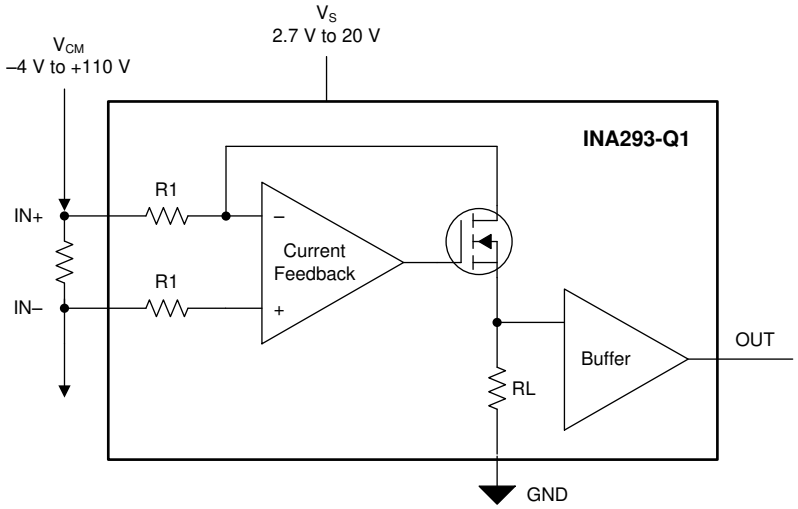

Figure 1-1. Functional Block Diagram

INA293-Q1 was developed using a quality-managed development process, but was not developed in accordance with the IEC 61508 or ISO 26262 standards.

2 Functional Safety Failure In Time (FIT) Rates

This section provides Functional Safety Failure In Time (FIT) rates for INA293-Q1 based on two different industry-wide used reliability standards:

- Table 2-1 provides FIT rates based on IEC TR 62380 / ISO 26262 part 11
- Table 2-2 provides FIT rates based on the Siemens Norm SN 29500-2

Table 2-1. Component Failure Rates per IEC TR 62380 / ISO 26262 Part 11

FIT IEC TR 62380 / ISO 26262	FIT (Failures Per 10^9 Hours)
Total Component FIT Rate	6
Die FIT Rate	4
Package FIT Rate	2

The failure rate and mission profile information in Table 2-1 comes from the Reliability data handbook IEC TR 62380 / ISO 26262 part 11:

- Mission Profile: Motor Control from Table 11
- Power dissipation: 50 mW
- Climate type: World-wide Table 8
- Package factor (lambda 3): Table 17b
- Substrate Material: FR4
- EOS FIT rate assumed: 0 FIT

Table 2-2. Component Failure Rates per Siemens Norm SN 29500-2

Table	Category	Reference FIT Rate	Reference Virtual T_J
4	BICMOS Op Amp, Comparators, Voltage Monitors	8 FIT	45°C

The Reference FIT Rate and Reference Virtual T_J (junction temperature) in Table 2-2 come from the Siemens Norm SN 29500-2 tables 1 through 5. Failure rates under operating conditions are calculated from the reference failure rate and virtual junction temperature using conversion information in SN 29500-2 section 4.

3 Failure Mode Distribution (FMD)

The failure mode distribution estimation for INA293-Q1 in Table 3-1 comes from the combination of common failure modes listed in standards such as IEC 61508 and ISO 26262, the ratio of sub-circuit function size and complexity and from best engineering judgment.

The failure modes listed in this section reflect random failure events and do not include failures due to misuse or overstress.

Table 3-1. Die Failure Modes and Distribution

Die Failure Modes	Failure Mode Distribution (%)
OUT open (Hi-Z)	20%
OUT to GND	25%
OUT to VS	25%
OUT functional, not in specification	30%

4 Pin Failure Mode Analysis (Pin FMA)

This section provides a Failure Mode Analysis (FMA) for the pins of the INA293-Q1. The failure modes covered in this document include the typical pin-by-pin failure scenarios:

- Pin short-circuited to Ground (see Table 4-2 and Table 4-6)
- Pin open-circuited (see Table 4-3 and Table 4-7)
- Pin short-circuited to an adjacent pin (see Table 4-4 and Table 4-8)
- Pin short-circuited to V_S (see Table 4-5 and Table 4-9)

Table 4-2 through Table 4-9 also indicate how these pin conditions can affect the device as per the failure effects classification in Table 4-1.

Table 4-1. TI Classification of Failure Effects

Class	Failure Effects
A	Potential device damage that affects functionality
B	No device damage, but loss of functionality
C	No device damage, but performance degradation
D	No device damage, no impact to functionality or performance

Following are the assumptions of use and the device configuration assumed for the pin FMA in this section:

- T_A = -40°C to +125°C
- V_+ = 2.7 V to 20 V
- V_{CM} = -4 V to +110 V

4.1 SOT-23-5 Package (Pinout A)

Figure 4-1 shows the INA293-Q1 pin diagram for the SOT-23-5 package (pinout A). For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA293-Q1 data sheet.

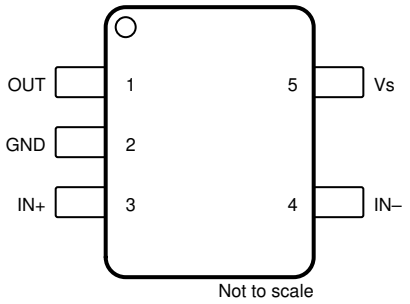

Figure 4-1. Pin Diagram (SOT-23-5 Package, Pinout A)

Table 4-2. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Normal operation.	D
IN+	3	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. In low side configuration, input pins are shorted.	B

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	4	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. In low side configuration, normal operation.	B for high-side; D for low-side
V_S	5	Power supply shorted to GND.	B

Table 4-3. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
GND	2	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
IN+	3	IN+ will be at the same potential as IN-. Differential input voltage is effectively 0 V.	B
IN-	4	IN- will be at the same potential as IN+. Differential input voltage is effectively 0 V.	B
V_S	5	No power supply to device.	B

Table 4-4. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	2 - GND	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	3 - IN+	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. In low side configuration, input pins are shorted.	B
IN+	3	4 - IN-	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-	4	5 - V_S	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}), which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
V_S	5	1 - OUT	Output will be pulled to V_S and output current will be short circuit limited. When left in this configuration for a long time, under high supplies selfheating could cause die junction temperature to exceed 150°C.	B

Table 4-5. Pin FMA for Device Pins Short-Circuited to V_S

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled to V_S and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Power supply shorted to GND.	B
IN+	3	In high-side configuration, device power supply shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
IN-	4	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}), which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
V_S	5	Normal operation.	D

4.2 SOT-23-5 Package (Pinout B)

Figure 4-2 shows the INA293-Q1 pin diagram for the SOT-23-5 package (pinout B). For a detailed description of the device pins please refer to the *Pin Configuration and Functions* section in the INA293-Q1 data sheet.

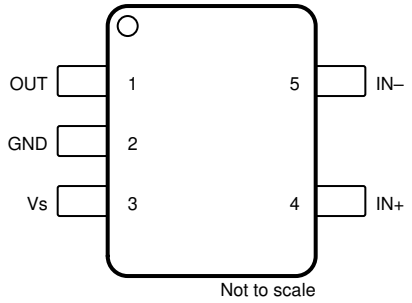

Figure 4-2. Pin Diagram (SOT-23-5 Package, Pinout B)

Table 4-6. Pin FMA for Device Pins Short-Circuited to Ground

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Normal operation.	D
V_S	3	Power supply shorted to GND.	B
IN+	4	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. In low side configuration, input pins are shorted.	B
IN-	5	In high-side configuration, a short from the bus supply to GND will occur. High current will flow from bus supply to GND. In low side configuration, normal operation.	B for high-side; D for low-side

Table 4-7. Pin FMA for Device Pins Open-Circuited

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output can be left open. There is no effect on the IC, but the output will not be measured.	C
GND	2	GND is floating. Output will be incorrect as it is no longer referenced to GND.	B
V_S	3	No power supply to device.	B
IN+	4	IN+ will be at the same potential as IN-. Differential input voltage is effectively 0 V.	B
IN-	5	IN- will be at the same potential as IN+. Differential input voltage is effectively 0 V.	B

Table 4-8. Pin FMA for Device Pins Short-Circuited to Adjacent Pin

Pin Name	Pin No.	Shorted to	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	2 - GND	Output will be pulled down to GND and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	3 - V_S	Power supply shorted to GND.	B
V_S	3	4 - IN+	In high-side configuration, device power supply shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side
IN+	4	5 - IN-	Inputs shorted together, so no sense voltage applied. Output will stay close to GND.	B
IN-	5	1 - OUT	In high-side configuration, OUT is shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, OUT is shorted to GND.	A for high-side; B for low-side

Table 4-9. Pin FMA for Device Pins Short-Circuited to V_S

Pin Name	Pin No.	Description of Potential Failure Effect(s)	Failure Effect Class
OUT	1	Output will be pulled to V_S and output current will be short circuit limited. When left in this configuration for a long time, under high supplies self-heating could cause die junction temperature to exceed 150°C.	B
GND	2	Power supply shorted to GND.	B
V_S	3	Normal operation.	D
IN+	4	In high-side configuration, device power supply shorted to bus supply, which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND (through R_{SHUNT}).	A for high-side; B for low-side
IN-	5	In high-side configuration, device power supply shorted to bus supply (through R_{SHUNT}), which may cause damage if high voltage is present. In low-side configuration, device power supply shorted to GND.	A for high-side; B for low-side

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