Application Brief

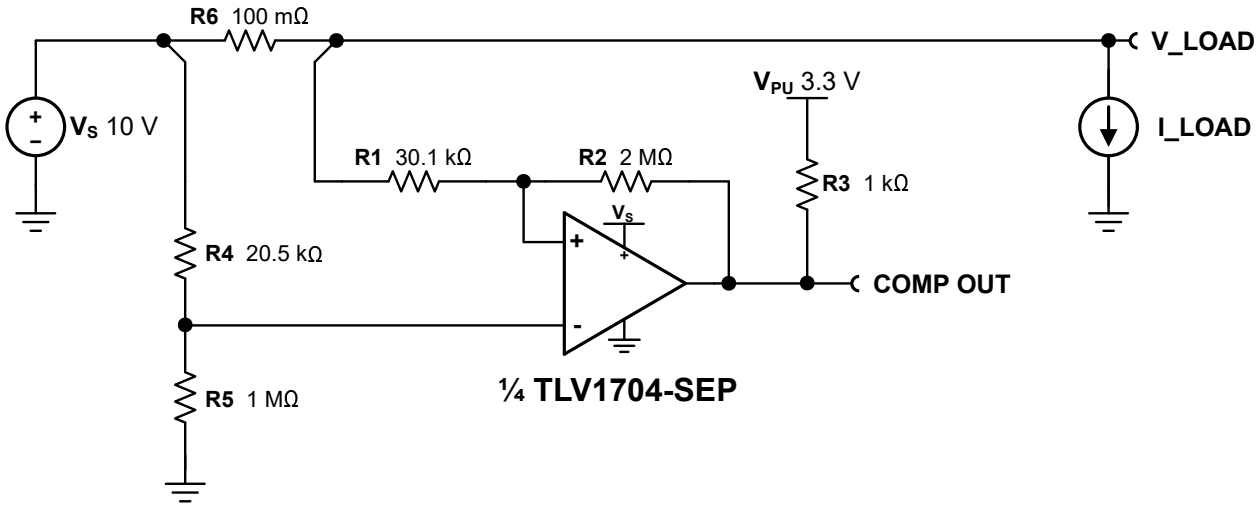
Space-Grade, 30-krad, High-Side Current Sensing Comparator Circuit

Design Goals

Load Current (I_L)		System Supply	Comparator Output Status		Radiation	
Over Current (I_{OC})	Recovery Current (I_{RC})	Typical	Over Current	Normal Operation	Total Ionizing Dose (TID)	SEL Immunity to LET
1 A	0.5 A	10 V	V_{OL} < 0.4 V	$V_{OH} = V_{PU}$ = 3.3 V	30 krad(Si)	43 MeV·cm^2/mg

Design Description

This application brief shows how to implement a simple rad-tolerant circuit that detects an over-current event caused by a single-event latch-up (SEL), in systems where not all other components SEL immune up to the target LET. This solution uses one comparator with a rail-to-rail input common mode range to create an over-current alert (OC-Alert) signal at the comparator output (COMP OUT) if the load current rises above 1A. The OC-Alert signal in this implementation is active low. So when the 1A threshold is exceeded, the comparator output goes low. Hysteresis is implemented such that OC-Alert will return to a logic high state when the load current reduces to 0.5A (a 50% reduction). This circuit uses an open-collector output comparator in order to level shift the output high logic level for controlling a digital logic input pin. For applications needing to drive the gate of a MOSFET switch, a comparator with a push-pull output is preferred.



Design Notes

1. Select a comparator with rail-to-rail input common mode range to enable high-side current sensing.
2. Select a comparator with an open-collector output stage for level-shifting.
3. Select a comparator with low input offset voltage to optimize accuracy.
4. Calculate the value for the shunt resistor (R_6) so the shunt voltage (V_{SHUNT}) is at least ten times larger than the comparator offset voltage (V_{IO}).

Design Steps

1. Select value of R_6 so V_{SHUNT} is at least 10x greater than the comparator input offset voltage (V_{IO}). Note that making R_6 very large will improve OC detection accuracy but will reduce supply headroom.

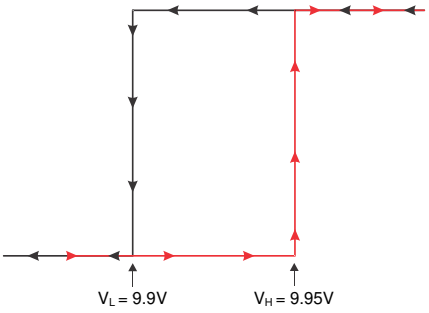
   $V_{SHUNT} = (I_{OC} R_6) \geq 10 V_{IO} = 55 \text{ mV}$

   set $R_6 = 100 \text{ m}\Omega$ for $I_{OC} = 1 \text{ A}$ & $V_{IO} = 5.5 \text{ mV}$

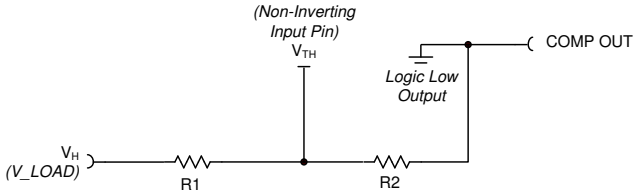
2. Determine the desired switching thresholds for when the comparator output will transition from high-to-low (V_L) and low-to-high (V_H). V_L represents the threshold when the load current crosses the OC level, while V_H represents the threshold when the load current recovers to a normal operating level.

   $V_L = V_S - (I_{OC} R_6) = 10 - (1 \times 0.1) = 9.9 \text{ V}$

   $V_H = V_S - (I_{RC} R_6) = 10 - (0.5 \times 0.1) = 9.95 \text{ V}$

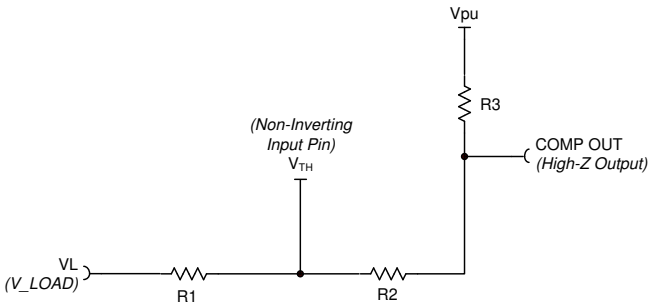


3. With the non-inverting input pin of the comparator labeled as V_{TH} and the comparator output in a logic low state (ground), derive an equation for V_{TH} where V_H represents the load voltage (V_{LOAD}) when the comparator output transitions from low to high. Note that the simplified diagram for deriving the equation shows the comparator output as ground (logic low).



$$V_{TH} = V_H \left(\frac{R_2}{R_1 + R_2} \right)$$

4. With the non-inverting input pin of the comparator labeled as V_{TH} and the comparator output in a high-impedance state, derive an equation for V_{TH} where V_L represents the load voltage (V_{LOAD}) when the comparator output transitions from high to low. Applying "superposition" theory to solve for V_{TH} is recommended.



$$V_{TH} = V_L \left(\frac{R_2 + R_3}{R_1 + R_2 + R_3} \right) + V_{PU} \left(\frac{R_1}{R_1 + R_2 + R_3} \right)$$

5. Eliminate variable V_{TH} by setting the two equations equal to each other and solve for R_1. The result is the following quadratic equation. Solving for R_2 is less desirable since there are more standard values for small resistor values than the larger ones.

   $$0 = V_{PU} R_1^2 + [V_{PU} R_2 + V_L (R_3 + R_2) - V_H R_2] R_1 + (V_L - V_H) [R_2^2 + (R_2 R_3)]$$

6. Select values for R3 and R2. Please note that R_3 is significantly smaller than R_2 ($R_3 << R_2$). Increasing R_3 will cause the comparator logic high output level to increase beyond V_{PU} and should be avoided. For example, increasing R_3 to a value of 100k can cause the logic high output to be 3.6 V. In this case, we can select R_2 = 2M and R_3 = 1k.

   $$R_2 = 2\ M\Omega$$

   $$R_3 = 1\ k\Omega$$

7. Calculate R_1 after substituting in numeric values for V_{PU}, R_2, V_L, V_H, and R_3. For this design, set V_{PU} = 3.3, R_2 = 2M, V_L = 9.9, V_H = 9.95, and R_3 = 1k.

   $$0 = 3.3\ R_1^2 + (6.591\ M)\ R_1 - (200.1\ G)$$

   $$\text{the positive root for } R_1 = 29.9\ k\Omega$$

   $$\text{using standard 1\% resistor values, } R_1 = 30.1\ k\Omega$$

8. Calculate V_{TH} using the equation derived in Design Step 3; use the calculated value for R_1. Note that V_{TH} is less than V_L since V_{PU} is less that V_L.

   $$V_{TH} = V_H \left(\frac{R_2}{R_1 + R_2} \right) = 9.802\ V$$

9. With the inverting terminal labeled as V_{TH}, derive an equation for V_{TH} in terms of R_4, R_5, and V_S.

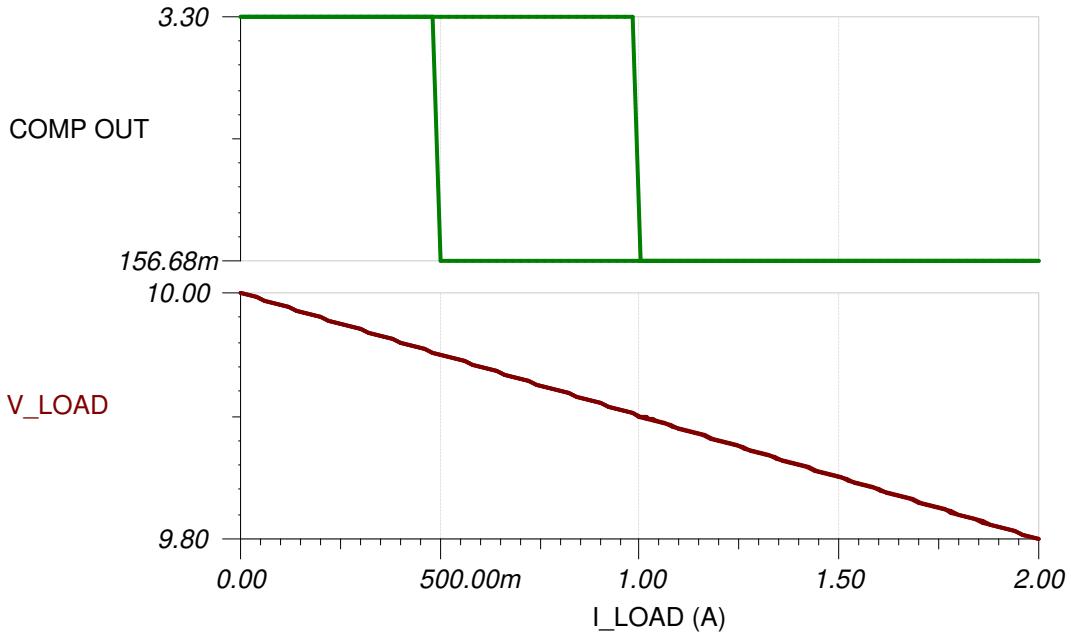
   $$V_{TH} = V_S \left(\frac{R_5}{R_4 + R_5} \right)$$

10. Calculate R_4 after substituting in numeric values R_5=1M, V_S=10, and the calculated value for V_{TH}.

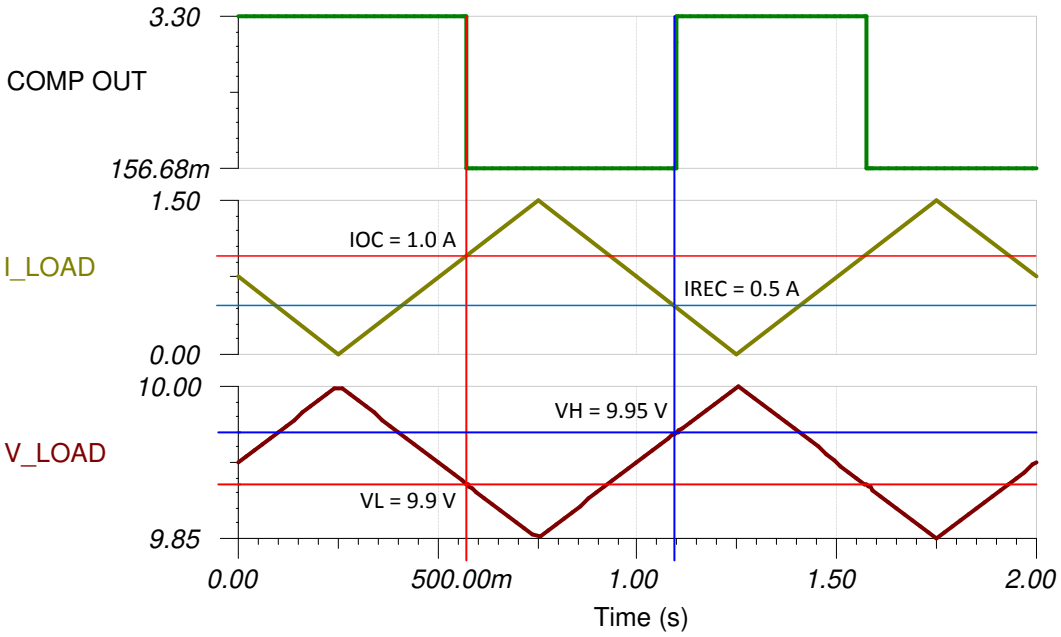
$$R_4 = \left(\frac{R_5 \left(V_S - V_{TH} \right)}{V_{TH}} \right) = 20.15\ k\Omega$$

using standard 1 % resistor values , $R_4 = 20.5\ k\Omega$

Design Simulations



Transient Simulation Results



Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

See Circuit SPICE Simulation File SBOMBL5, http://www.ti.com/lit/zip/sbombl5.

Design Featured Comparator

TLV1704-SEP	
V_S	2.2 V to 36 V
V_{inCM}	Rail-to-rail
V_{OUT}	Open-Collector, Rail-to-rail
V_{OS}	500 µV
I_Q	55 µA/channel
$t_{PD(HL)}$	460 ns
#Channels	4
TID Characterization (ELDRS-Free)	30 krad(Si)
TID Radiation Lot Acceptance Test (RLAT) / RHA	20 krad(Si)
SEL Immune to LET	43 MeV·cm^2/mg
https://www.ti.com/product/TLV1704-SEP	

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