

Under the Hood: Output Swing Limitations of Current Sense Amplifiers



ABSTRACT

Current shunt amplifiers, like traditional operational amplifiers, have output stage limitations. This paper provides an in depth look at these limitations of output voltage and output current, and how these parameters work together in current sense amplifiers. Claw curves are discussed from the perspective of a high level output stage, including why such stages result in output voltage limitations.

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1 Introduction

Unlike the ideal operational amplifier, real operational amplifiers have input and output limitations that dictate a realistic range of values of where they can operate and remain working in a linear state.

In the case of current sensing amplifiers, the typical input restriction of the standard operational amplifier is removed. This is due to an internal topology of input stage transistors that allows for common mode voltages far in excess of the supply voltage(s). This common mode voltage is rejected, the differential voltage is level shifted down, and is then processed by the output stage. The ability of such a front end is useful in various scenarios, from the avoidance of additional components for level shifting data for operation by an analog to digital converter, avoiding additional supply voltages simply for biasing operational amplifiers, and many more.

However, when discussing the output structure of a current sense amplifier, the output stage typically contains design constraints that must be taken into account for the device to operate linearly. Typically, current sense amplifiers employ CMOS type output stages, which display a small amount of swing loss as the demand for load current increases. These restrictions are made apparent in the datasheet, and reside in a graph commonly referred to as a "claw" curve.

2 Output Swing in Current Sense Amplifiers

A mistake that is often made with regard to swing limitations is that they are treated as a static condition, if considered at all. Commonly, swing test conditions can often be found in the *Electrical Characteristics* table of a current sense amplifier data sheet, such is in [Figure 2-1](#).

at $T_A = 25^\circ\text{C}$, $V_S = 5\text{ V}$, $V_{\text{SENSE}} = V_{\text{IN}+} - V_{\text{IN}-}$, $V_{\text{CM}} = 12\text{ V}$, and $V_{\text{REF}1} = V_{\text{REF}2} = V_S / 2$ (unless otherwise noted)

VOLTAGE OUTPUT ⁽¹⁾				
Swing to V_S power-supply rail	$R_L = 10\text{ k}\Omega$ to GND $T_A = -40^\circ\text{C}$ to 125°C	$V_S - 0.05$	$V_S - 0.2$	V
Swing to GND	$R_L = 10\text{ k}\Omega$ to GND, $V_{\text{SENSE}} = 0\text{ mV}$ $V_{\text{REF}1} = V_{\text{REF}2} = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to 125°C	$V_{\text{GND}} + 1$	$V_{\text{GND}} + 10$	mV

Figure 2-1. INA240 Output Swing Limitations

Examining this information from the *INA240 High- and Low-Side, Bidirectional, Zero-Drift, Current-Sense Amplifier With Enhanced PWM Rejection Data Sheet*, several observations are obtained. First, the output of the amplifier is not ideal to the supply, but rather is only capable of swinging to 4.8 V in the worst case (4.95 V typical) condition for a supply of 5 V. The same observation is also made regarding the device's ability to swing to GND. This information demonstrates that, should the device be operated in a unidirectional manner, that is, the REF pins of the INA240 both set to GND, that the output is not capable of truly measuring 0 A. (A true drive to 0 A is possible in a unidirectional setup, however, if the reference is used to pedestal above the swing condition. This comes at the loss of a small amount of dynamic range.)

These conditions do not hold true for the entirety of the potential load range, however. As required load current increases, this often comes at the expense of output swing head room of the device. The conditions above only examine swing on the output of the device in a single location for potential loading, in this case 10k Ω to GND. Should the loading of the output change, and more current is demanded, this can potentially alter the output stage's swing characteristics, and lead to saturation against the rail if not properly designed for. A good example to imagine here is a step in load current at the output of the current sense amplifier. The designer needs to ensure that the largest load current is taken into account with respect to desired full scale range to ensure that the output of the device is capable of handling this change.

Load resistance and the maximum desired output voltage for the output stage allow the engineer to calculate the maximum current required by the load. For example, in the data sheet test condition discussed above, the maximum output capable is 4.8 V, and the load resistance is 10 k Ω . If a design were in motion with these desired parameters, then maximum current sourced by the output can be calculated as:

$$I_{\text{LOAD, max}} = \frac{V_{\text{OUT, max}}}{R_{\text{LOAD}}} = \frac{4.8\text{ V}}{10\text{ k}\Omega} = 480\ \mu\text{A} \quad (1)$$

For the Texas Instruments' amplifier portfolio, this information across the load current range is typically conveyed in a common figure referred to as the "claw" curve, as they somewhat resemble animal claws. Figure 2-2 shows the claw curve of the INA240.

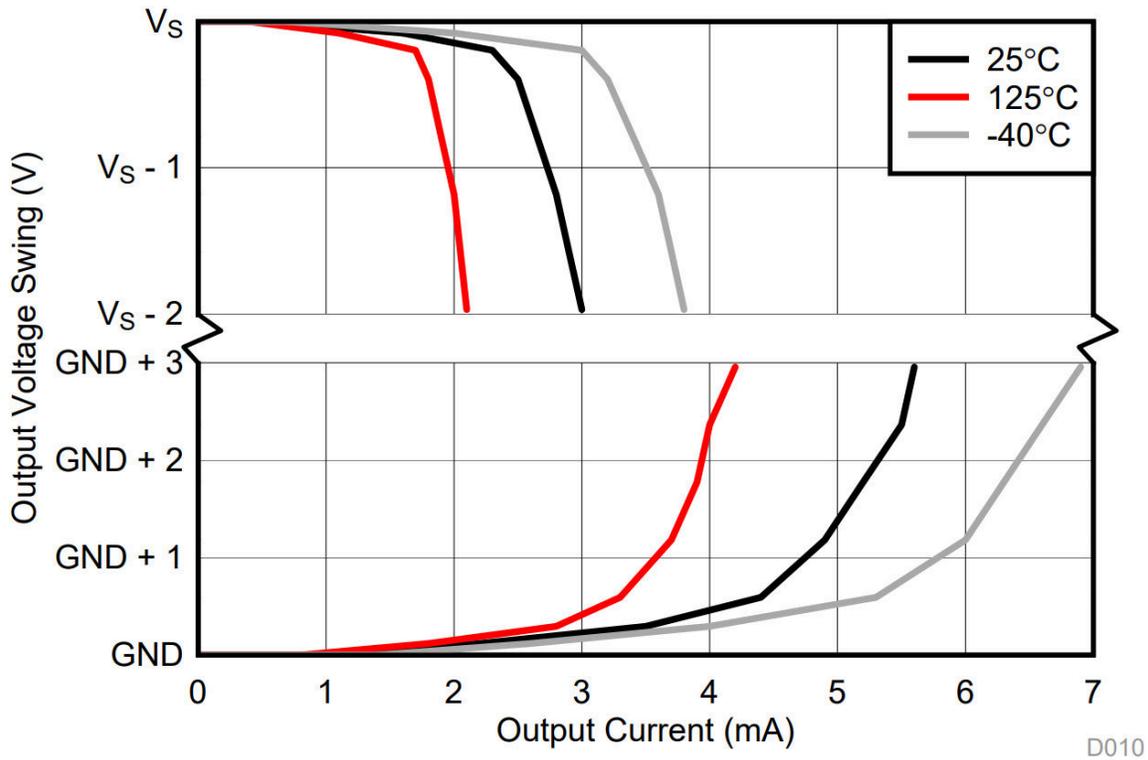


Figure 2-2. INA240 Output Voltage Swing vs Output Current Capability

These curves are normally divided into a top and bottom section, and the above curve is no different. The upper family of curves demonstrates the device's ability to source current, while the lower family of curves gives the device's ability to sink current. Information is also provided at the ambient temperature point, and the extremes of the device's temperature range. Some devices may include additional temperature curves, but these three datasets will normally be provided at a minimum.

Breaking down the curves, you can again make several observations. First, it can be seen that as the desired load current grows, the ability of the device to swing completely to the rail diminishes. This is due to the fact that, for CMOS output stages, as load current increases through the FET, and a drop is created over the $R_{DS(ON)}$ of the FET that will scale with the output current of the device. This is visualized in a high level diagram in Figure 2-3.

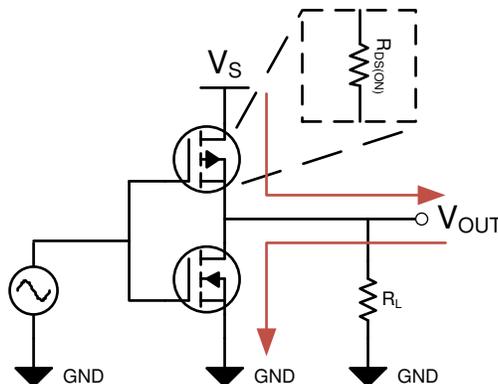


Figure 2-3. CMOS Output Stage and Load Current Flow

Next, this relationship is not linear across the entire range, and a portion of the curve is reached where significant falloff is observed. This is due to the fact that the $R_{DS(ON)}$ of the FETs is not a linear process, and increases with increasing current from drain to source.

Finally, an important aspect of these curves to understand is that these curves are not meant to be interpreted as a simple "translational" relationship as the claw curve limit is reached. Typically, a good design rule is to provide some amount of headroom away from the hard limit of the claw curve. While amplifier output stages are relatively linear to a point, there are diminishing returns as the rail is approached, and components of both the linear area and saturation area will be present in the output. Figure 2-4 shows a typical FET curve is demonstrated to help visualize this in .

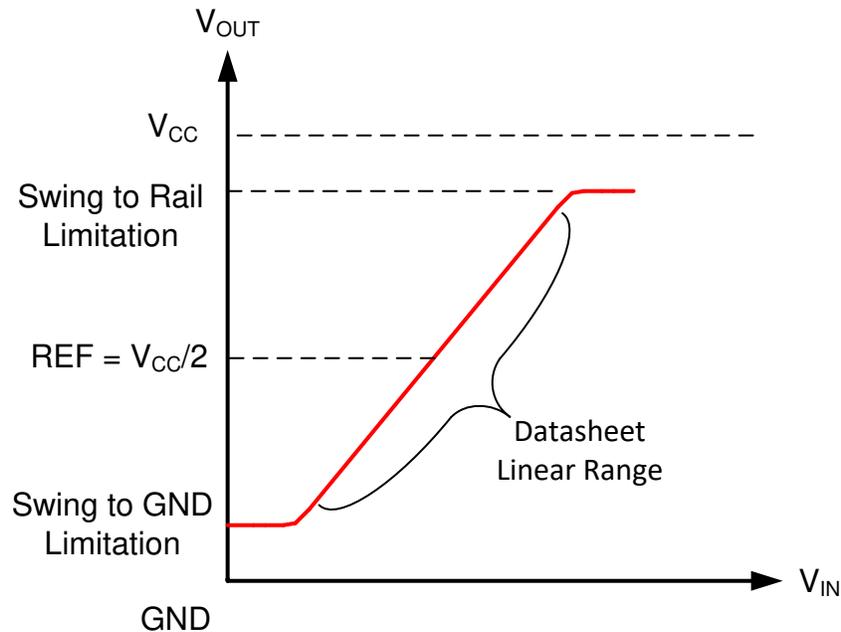


Figure 2-4. Typical Current Sense Amplifier Output Curve

For this reason, it is typically recommended that a small amount of margin be built into the design to work away from the hard value shown in the claw curve, nominally a few tens to hundreds of millivolts.

3 References

- Texas Instruments: [INA240 High- and Low-Side, Bidirectional, Zero-Drift, Current-Sense Amplifier With Enhanced PWM Rejection Data Sheet](#)

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