Analog Engineer's Circuit

Op Amp LDO Circuit

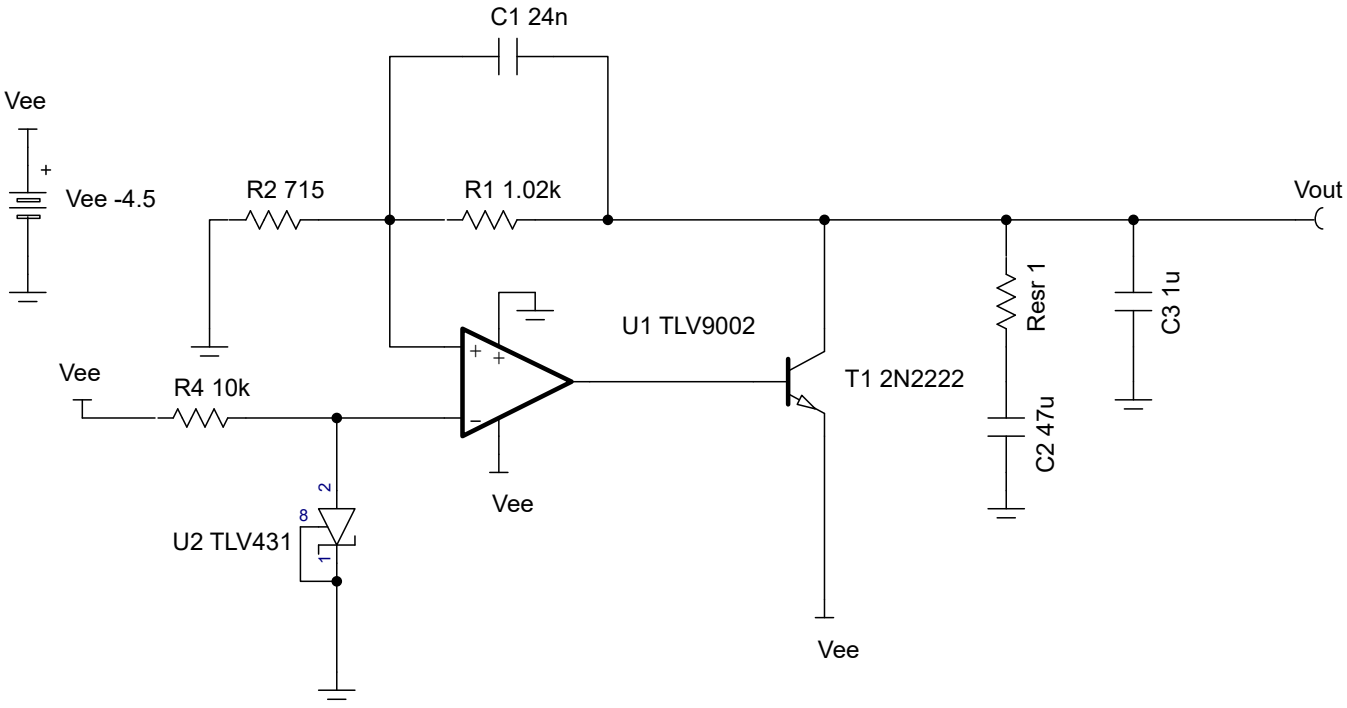
Amplifiers

Design Goals

Input	Output		Supply		
V_I	V_o	I_{out}	V_{cc}	V_{eemax}	V_{eemin}
–5.5 V < V_{ee} < –4.5 V	–3 V	600 mA	0 V	–4.5 V	–5.5 V

Design Description

This design accurately steps down a voltage level and holds it stable at a fixed output voltage (low dropout regulator). The regulator takes a –4.5-V to –5.5-V input voltage and steps it down to a –3-V rail that supplies current up to 600 mA.



Design Notes

1. Use the op amp in a linear operating region. Ensure that the inputs of the op amp do not exceed the common-mode range of the device. Linear output swing is usually specified under the A_{OL} test conditions.
2. The common-mode voltage is equal to the inverting input voltage, set by the TLV431 reference of –1.24 V.
3. Using a high-gain BJT reduces the output current requirement for the op amp.
4. The majority of the power loss is $|V_{ee} – V_{out}| \times I_{out}$ and will be dissipated in transistor T_1. A larger V_{ee} will increase power loss and the temperature of T_1.
5. Other op amps may be used in place of the TLV9002, but may require adjustment of the feedback stabilization.
6. Positive feedback to the amplifier is used, because an inversion is performed by T_1.

Design Steps

The transfer function of the circuit is:

$$V_{out} = -1.24\ \text{V} \times \frac{R_1 + R_2}{R_2}$$

1. Based on the desired output voltage, in this case -3V, select a ratio of R_1 and R_2 that satisfies the above equation.

$$-3\ \text{V} = -1.24\ \text{V} \times \frac{R_1 + R_2}{R_2}$$

$$1.419 \times R_2 = R_1$$

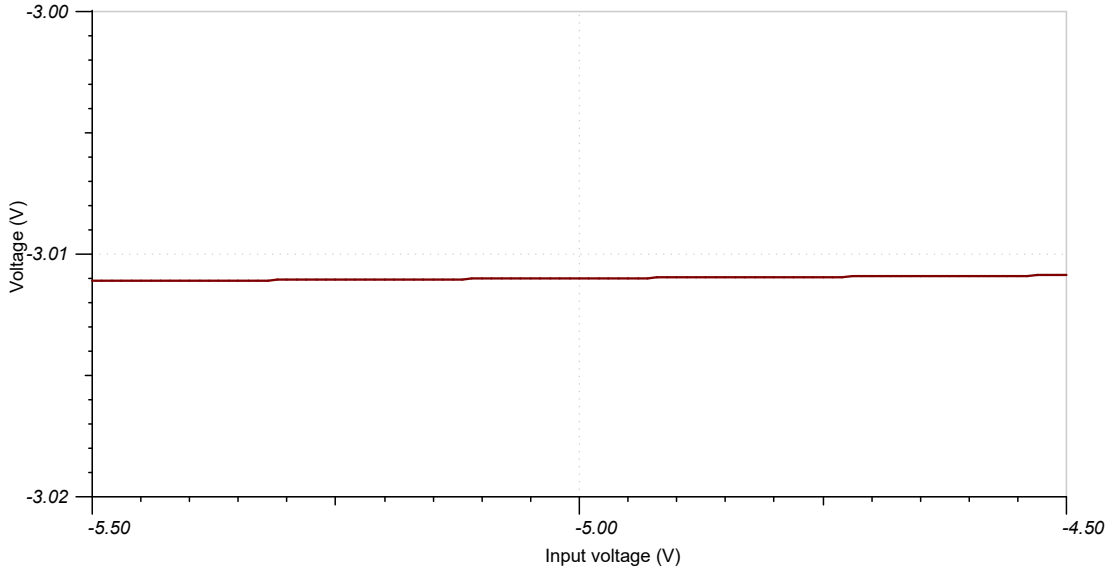
Selecting standard resistors, choose 1.02 kΩ and 715 Ω.

2. For sizing the output capacitance, the product of C_2 and R_{esr} should generate a zero below 10 kHz to ensure stability. The ESR zero is located at:

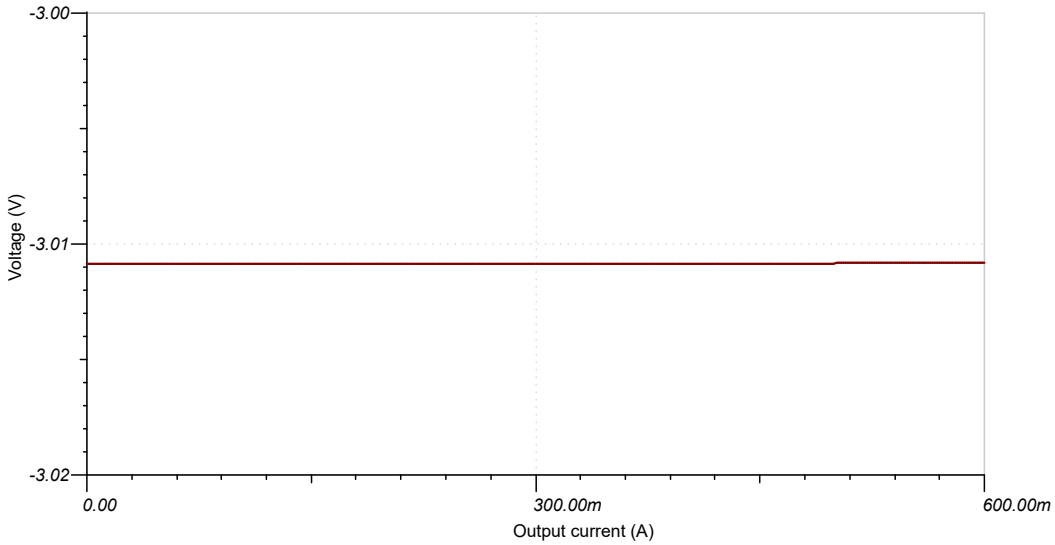
$$F_{z(ESR)} = \frac{1}{2\pi R_{esr} C_2} = \frac{1}{2\pi\left(1\ \Omega\right)\left(47 \times 10^{-6} F\right)} = 3.38\ \text{kHz}$$

Design Results

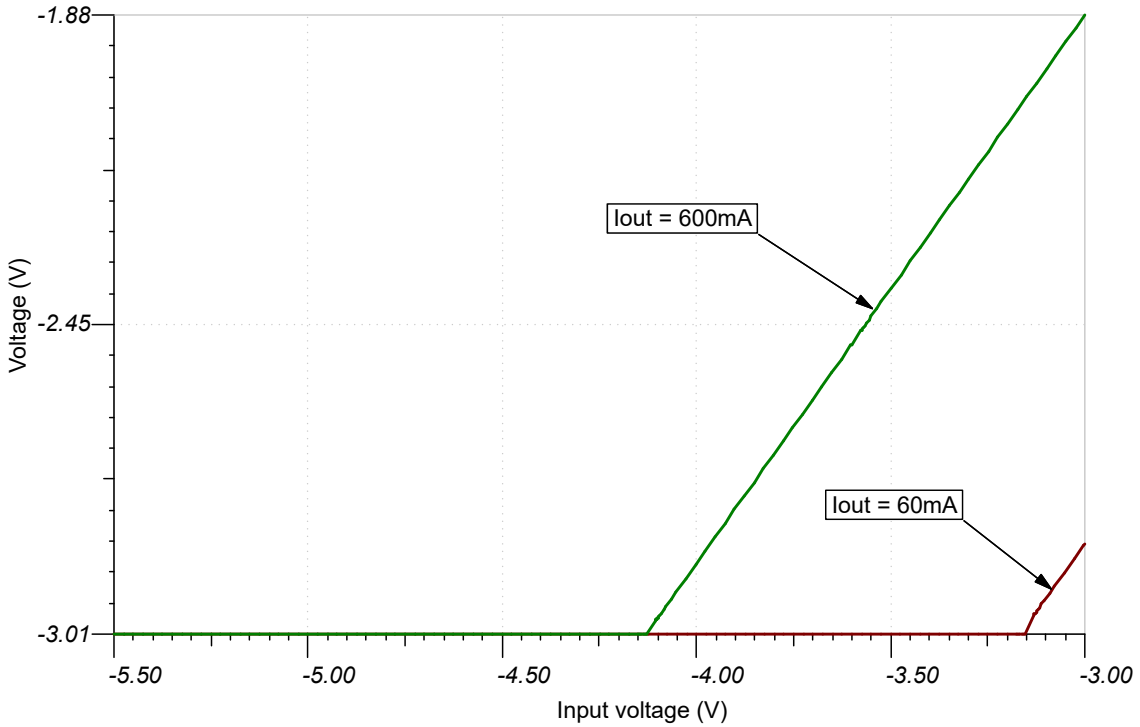
DC Analysis Results



Vee Sweep

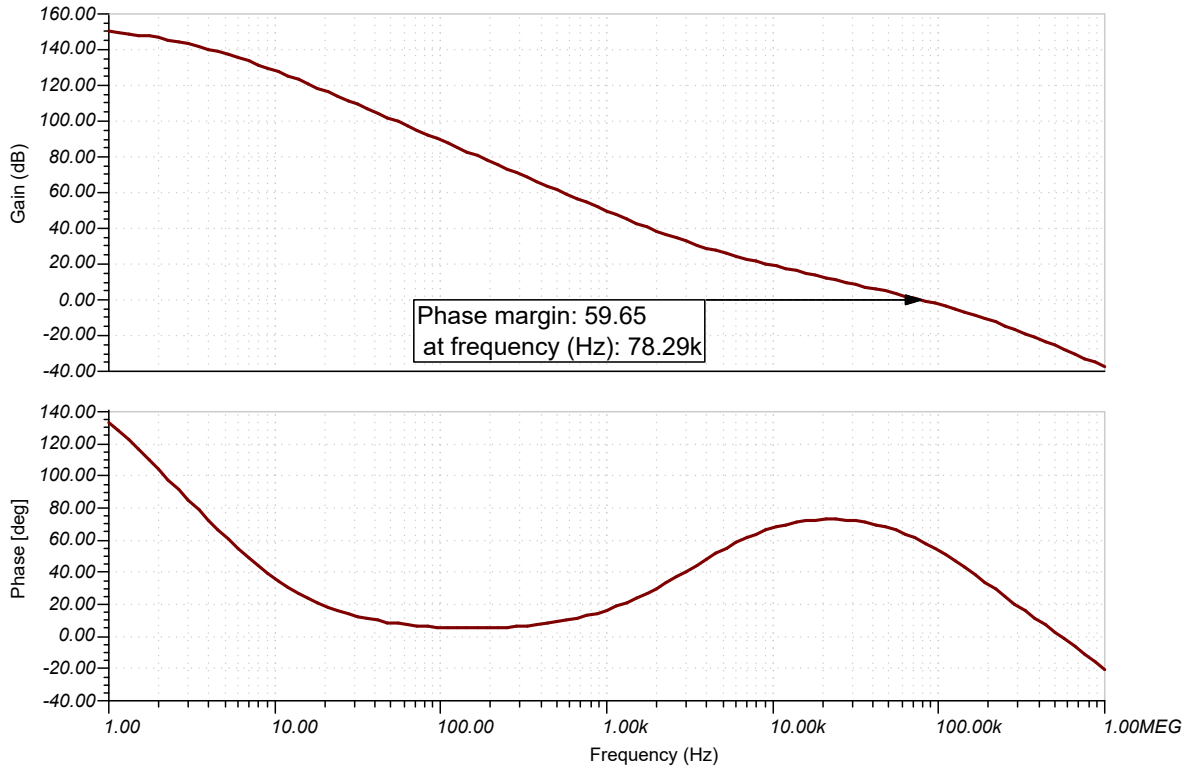


Output Current Sweep

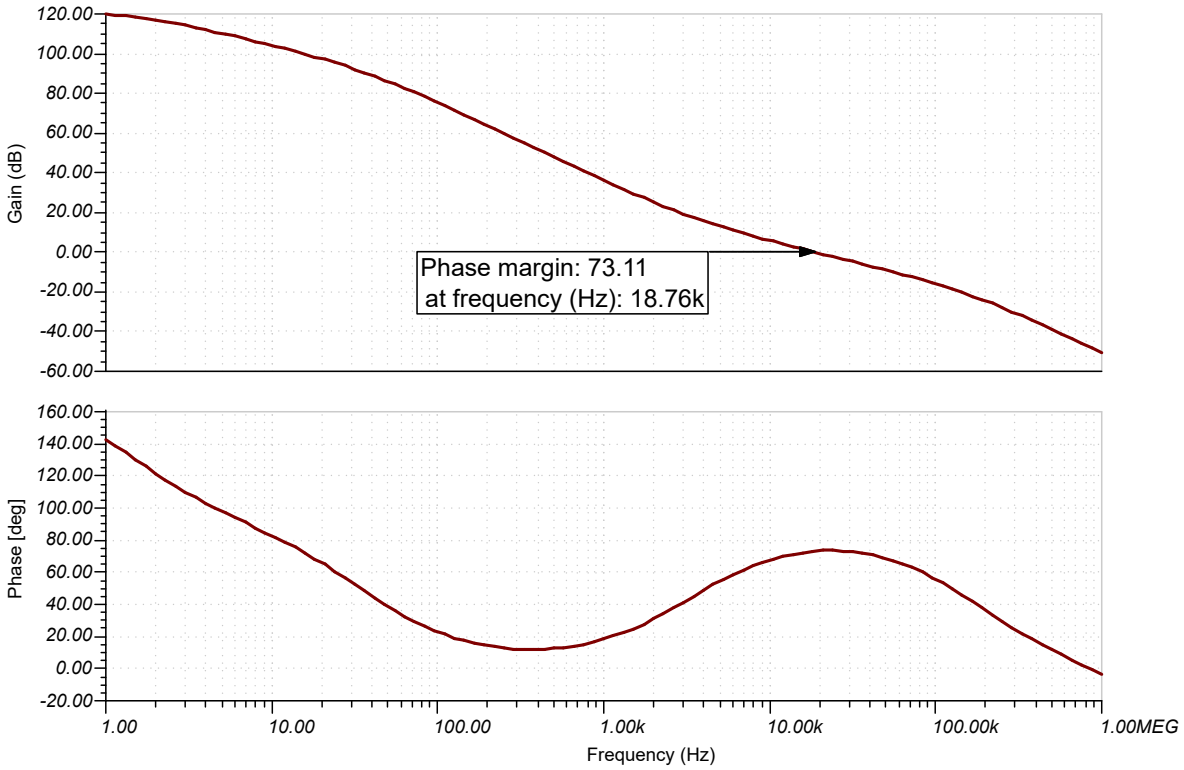


Dropout Voltage

AC Analysis Results

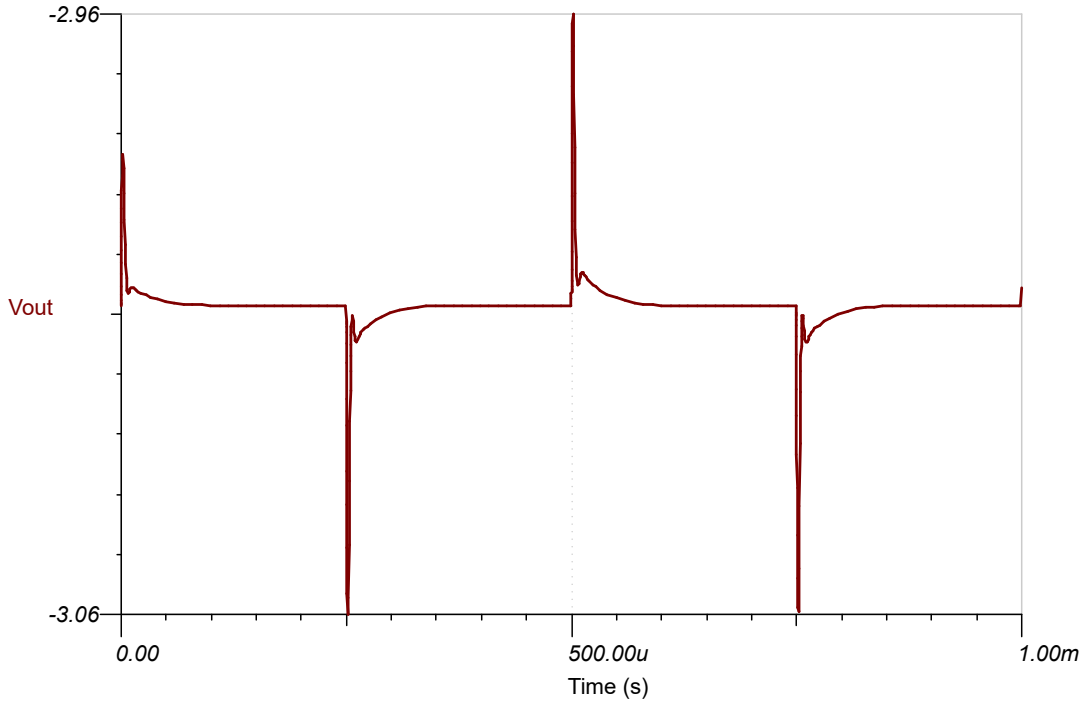


Bode 60 mA



Bode 600 mA

Transient Analysis Results



Transient Response (100-mA Step)

Design References

See the Analog Engineer's Circuit Cookbooks for TI's comprehensive circuit library.

AN-1482 LDO Regulator Stability Using Ceramic Output Capacitors

Space-Grade, 100-krad, –2.5-V, Discrete Negative LDO Linear Regulator Circuit

For more information on many op amp topics including common-mode range, output swing, and bandwidth, please visit TI Precision Labs.

Design Featured Devices

TLV9001	
V_{ss}	1.8 V–5.5 V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	0.4 mV
I_q	0.06 mA
I_b	5 pA
UGBW	1 MHz
SR	2 V/µs
#Channels	1
TLV9001	

Design Alternative Devices

OPA392	
V_{ss}	1.7V–5.5V
V_{inCM}	Rail-to-rail
V_{out}	Rail-to-rail
V_{os}	1 µV
I_q	1.22 mA
I_b	0.01 pA
UGBW	13 MHz
SR	4.5 V/µs
#Channels	1
OPA392	

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