

Application Note

JFE2140 Ultra-Low-Noise Preamplifier



Chris Featherstone

Precision Amplifiers

ABSTRACT

Many engineers face the challenge of amplifying small signals produced by sensors with high source impedance in a low-noise circuit. Amplifier circuit design for sensor applications such as hydrophones, guitar pickups, high source impedance microphones, and turntables can benefit from a combination of discrete components and operational amplifiers. This application note discusses the use of JFET and Operational Amplifiers (op amps) in a composite amplifier configuration to accomplish this design challenge.

Table of Contents

1 Introduction.....	2
2 Theory of Operation.....	3
3 Stability.....	7
4 Summary.....	9

List of Figures

Figure 1-1. Preamplifier With JFE2140 Front End in a Closed-Loop Circuit.....	2
Figure 2-1. Preamp With JFE2140 Front End Small Signal T-Model.....	3
Figure 2-2. Transconductance vs Drain-To-Source Current.....	4
Figure 2-3. Loop Parameters (dB) vs Frequency (Hz).....	4
Figure 2-4. A_{cl} (dB) vs Frequency (Hz).....	5
Figure 2-5. Gain Bandwidth Comparison.....	6
Figure 3-1. Loop Analysis for Preamp With JFE2140 Front End Using the Small-Signal T-Model.....	7
Figure 3-2. Stability Analysis.....	8

List of Tables

Table 2-1. Circuit Topology Comparison	6
--	---

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

Amplifying the small signals produced by sensors in a low-noise circuit is a very common but difficult problem. This was outlined in the [JFE150 Ultra-Low-Noise Pre-Amp](#) application note. High source impedance sensors such as a microphone, that produce signals on the order of a few thousandths of a volt, are loaded by low noise and low input impedance bipolar junction transistor (BJT) stages. Using a complementary metal-oxide semiconductor (CMOS) device is a good choice for a high input impedance; however, the noise performance is worse than that of a bipolar input. The discrete junction field-effect transistor (JFET) has better noise performance than the CMOS device and also has high input impedance. More details are found in the [Trade-offs Between CMOS, JFET, and Bipolar Input Stage Technology](#) application report. A discrete JFET such as TI's [JFE2140](#), when followed by a bipolar op amp such as the [OPA202](#), offers a way to achieve high input impedance and low noise with flexible biasing, see [Figure 1-1](#).

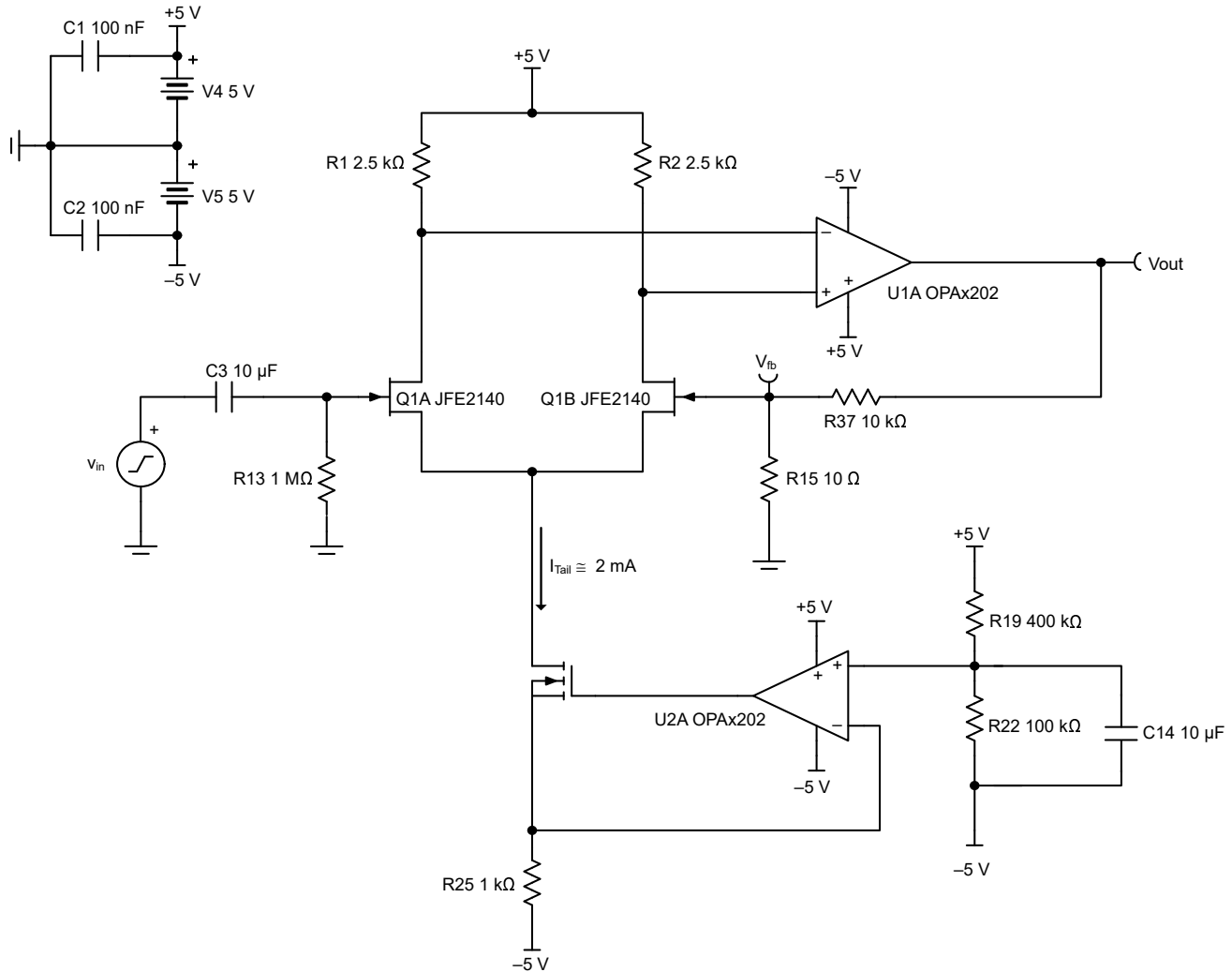


Figure 1-1. Preamplifier With JFE2140 Front End in a Closed-Loop Circuit

2 Theory of Operation

The JFET preamplifier (preamp) circuit is easiest to analyze using the small-signal T-model as shown in Figure 2-1. To understand the operation of this circuit, begin by examining the preamp at the input. A sensor generates a small-signal input voltage (v_{in}), which modulates the gate-to-source voltage (v_{gs}) of the JFET. The JFE2140 is the first gain stage in the preamp circuit and conducts a small-signal drain-to-source current $i_{ds1} = g_{m1} \times v_{gs1}$ that fluctuates with v_{in} . The transconductance gain parameter (g_m), is expressed in Siemens and v_{gs} is expressed in volts.

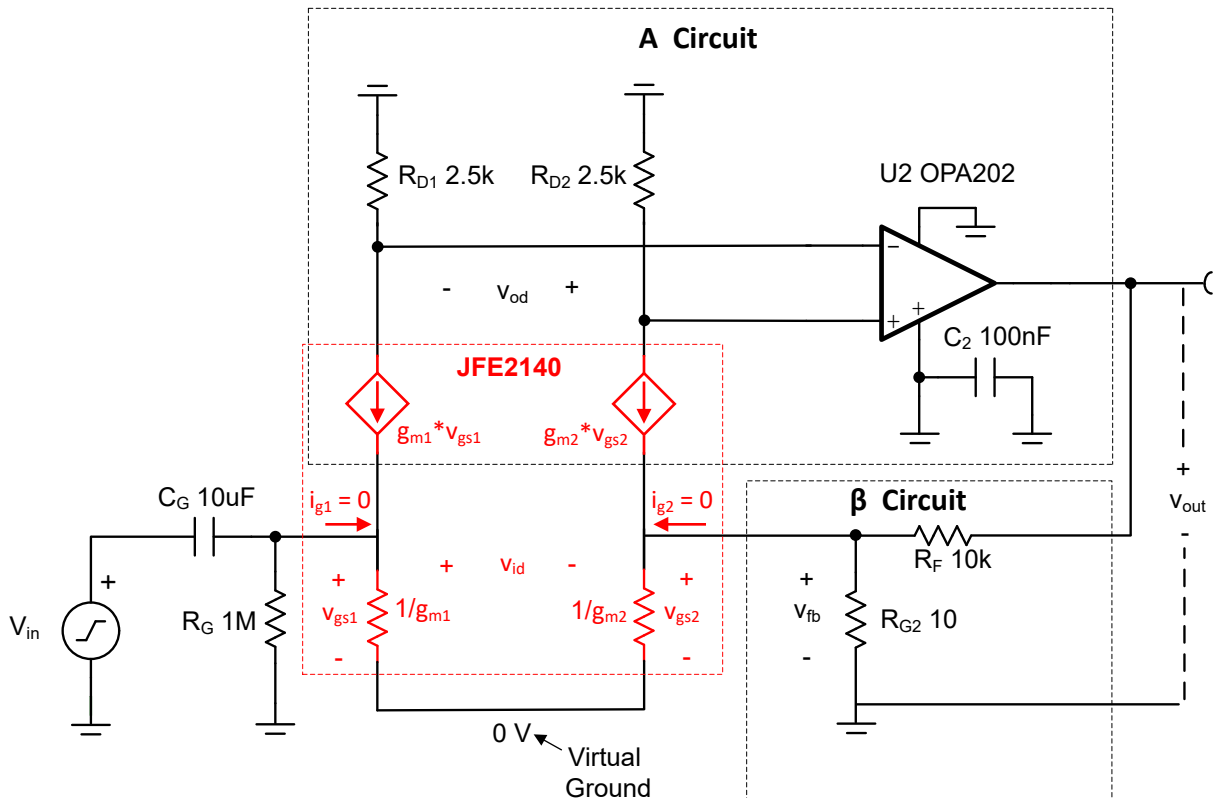


Figure 2-1. Preamp With JFE2140 Front End Small Signal T-Model

The small-signal current i_{ds1} flows through resistors R_{D1} and R_{D2} forming a differential voltage v_{od} between the drains of the JFE2140. The OPA202 monitors v_{od} and drives the loop with voltage v_{out} such that the inputs of the OPA202 are approximately equal. The JFE2140 combined with the OPA202 form the feedforward gain stage A shown in Figure 2-1. Assuming symmetry and $i_{ds1} = i_{ds2}$, the gain of the JFE2140 is $g_m \times R_D$. The transconductance parameter g_m can be approximated from Figure 2-2. At a drain-to-source current of 1 mA, the measured g_m is approximately 7.5 mS.

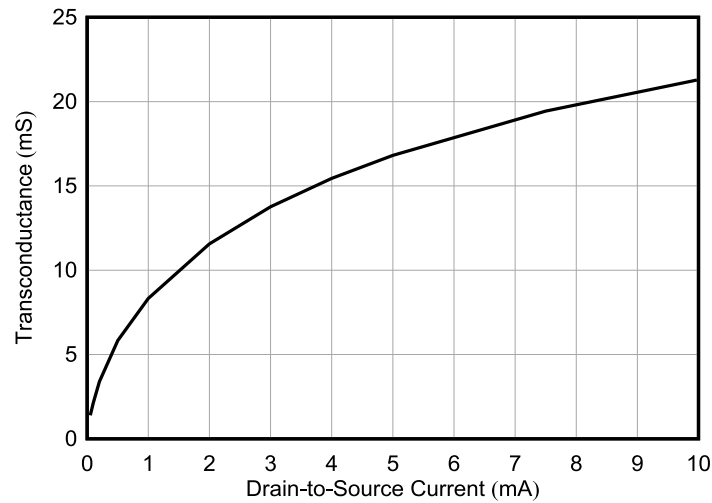


Figure 2-2. Transconductance vs Drain-To-Source Current

The DC A_{ol} of the OPA202 is 150 dB. Combined with the JFET gain, the resulting feedforward gain A is calculated as shown in Equation 1. The simulated feed forward gain is shown in Figure 2-3 and is $A = 175$ dB. This closely matches the calculated result.

$$A_{dB} = 20 \times \log(7.5 \text{ mS} \times 2.5 \text{ k}\Omega) + 150 \text{ dB} = 175.46 \text{ dB} \quad (1)$$

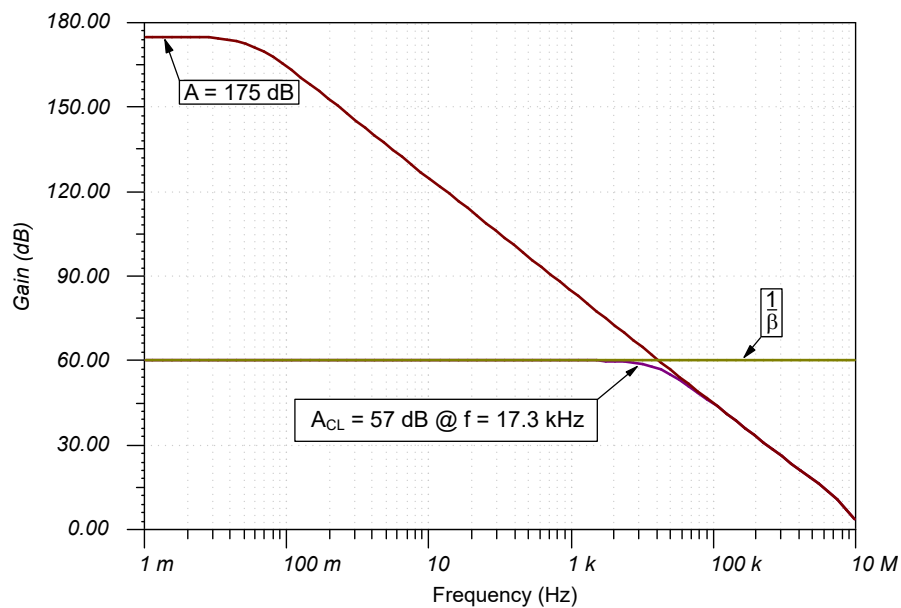


Figure 2-3. Loop Parameters (dB) vs Frequency (Hz)

Because wafer process variations can yield up to 30% variations in g_m , adding a feedback network (β) maintains a predictable closed-loop gain. The β feedback network consists of resistors R_F , and R_{G2} and is a series-shunt feedback network. The β network samples v_{out} by shunting the output of the OPA202 and feeds back a proportional voltage v_{fb} . The voltage $v_{fb} = v_{gs2}$. The gate is the feedback-summing node of the circuit. In this configuration, the loop is closed. An increase of the input differential voltage v_{id} results in a rise of v_{od} and therefore v_{out} . If v_{out} rises, then v_{gs2} rises. An increase of v_{gs2} lowers v_{id} . A decrease of the differential voltage between the JFET drains is observed. The final outcome is a reduction of v_{out} which completes the negative feedback loop of the preamplifier.

The standard closed-loop gain (A_{cl}) Equation 2 applies.

$$A_{cl} = \frac{A}{1 + A\beta} \tag{2}$$

Assuming the feedforward gain A is much greater than β , A_{cl} is approximately determined by resistors R_F and R_{G2} in the mid-band frequencies. A_{cl} can be approximately calculated using Equation 3 .

$$A_{cl} \approx \frac{1}{\beta} \approx \frac{R_F}{R_{G2}} + 1 \tag{3}$$

$$A_{cl} \approx 1001 \frac{V}{V} \text{ or } 60 \text{ dB} \tag{4}$$

Figure 2-4 shows the closed-loop gain vs frequency response of the JFET preamplifier circuit.

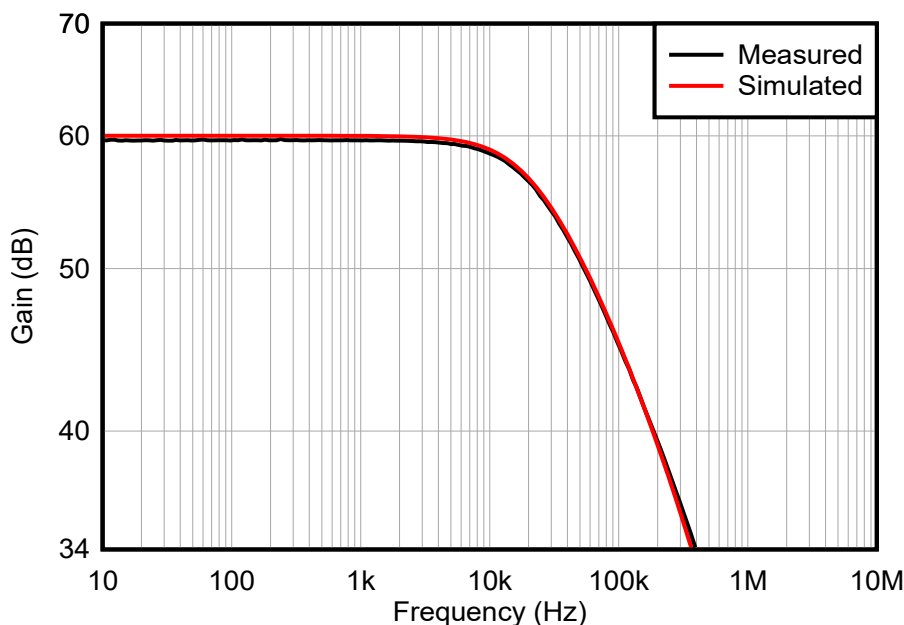


Figure 2-4. A_{cl} (dB) vs Frequency (Hz)

Figure 2-5 compares the gain bandwidth of the JFE2140 composite preamp circuit to the OPA202 and the OPA145. Each configuration is in a gain of 60 dB. Table 2-1 shows that the JFE2140 composite preamp circuit achieves the highest bandwidth of the 3 circuits. This is made possible by the additional feedforward gain that the discrete JFET front end contributes. Table 2-1 also shows the ultra-low-noise performance that the JFE2140 composite circuit achieves.

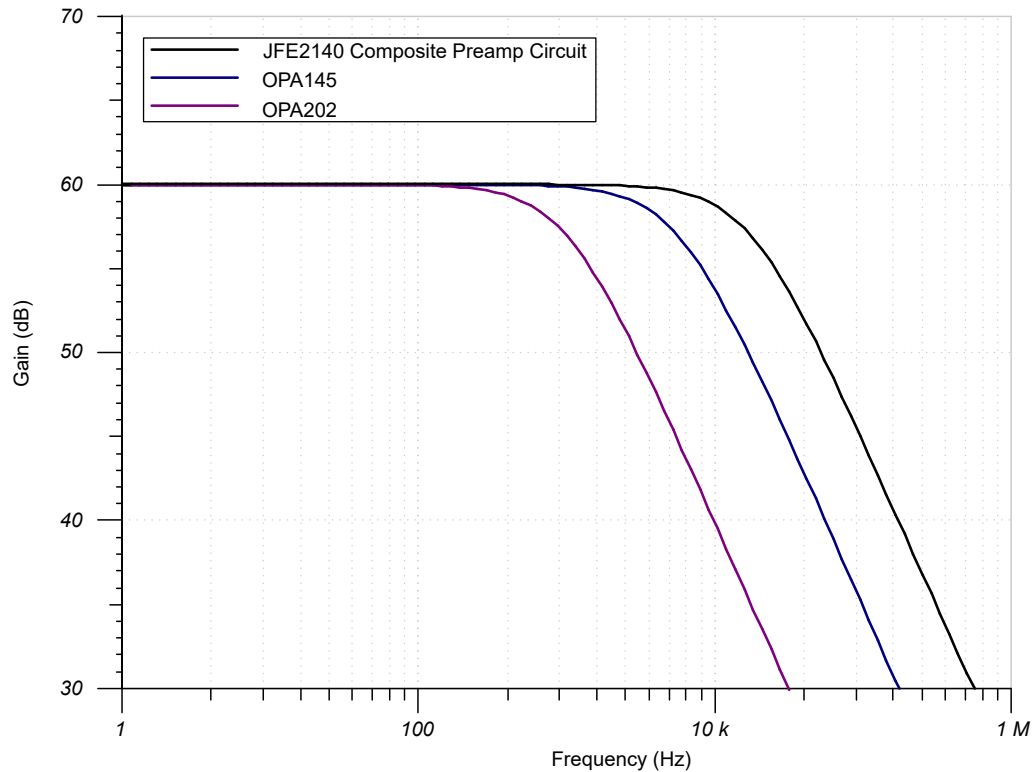


Figure 2-5. Gain Bandwidth Comparison

Table 2-1. Circuit Topology Comparison

Amplifier	-3 dB Point	Voltage Noise Input-Referred f = 1 kHz	Total Iq
JFE2140 Composite Preamp Circuit	17.3 kHz	$1.96 \frac{nV}{\sqrt{Hz}}$	3.6 mA
OPA145	5.56 kHz	$7.1 \frac{nV}{\sqrt{Hz}}$	449 μ A
OPA202	988 Hz	$8.9 \frac{nV}{\sqrt{Hz}}$	582 μ A

3 Stability

The loop parameters A , and $1/\beta$ can be determined in simulation by breaking the loop. This is accomplished in a SPICE simulator by driving the loop with V_{Loop} as shown in Figure 3-1.

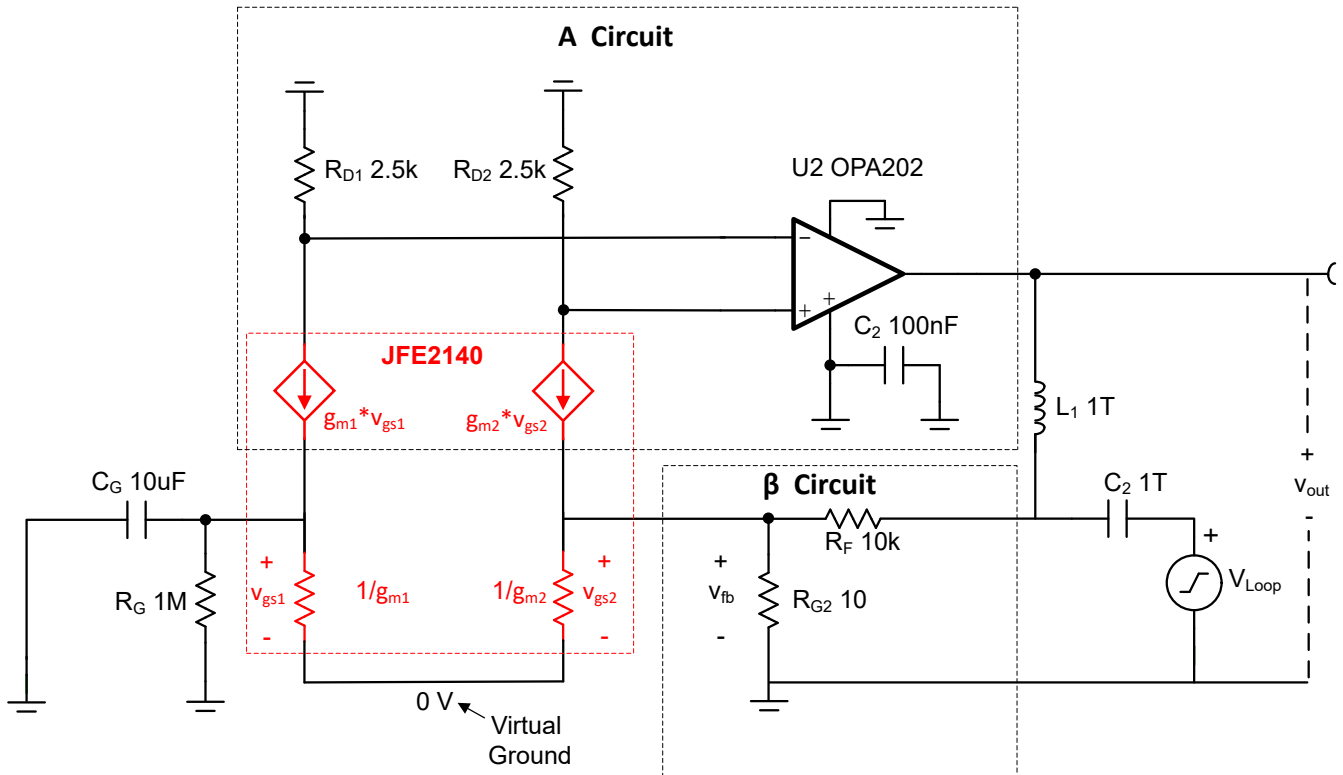


Figure 3-1. Loop Analysis for Preamp With JFE2140 Front End Using the Small-Signal T-Model

At high frequencies the inductor L_1 is an open and the capacitor C_2 is a short. This method isolates the circuits A and β , to plot the frequency response of each, as shown in Figure 3-2.

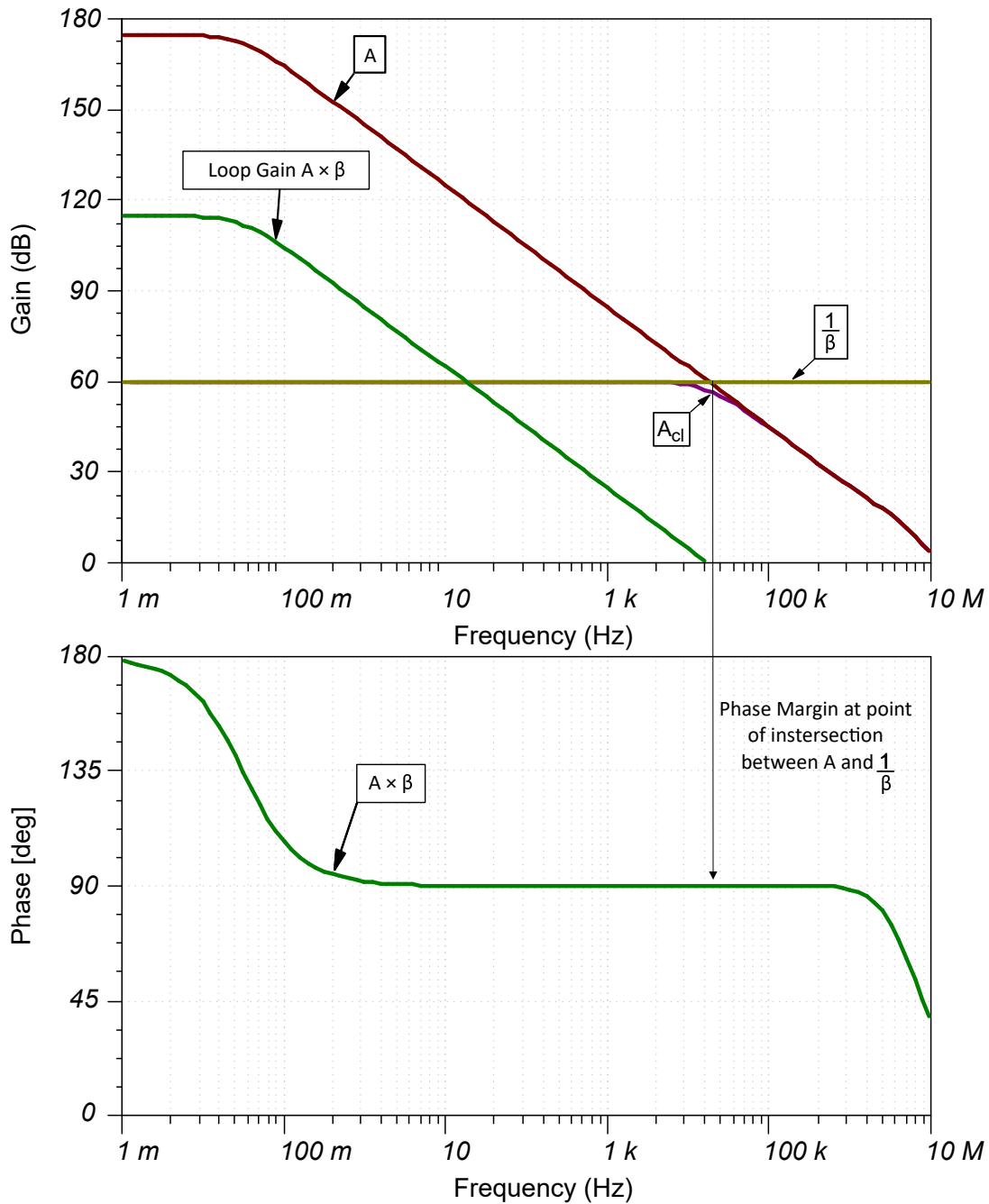


Figure 3-2. Stability Analysis

The upper -3 dB point of A_{cl} occurs when A and $1/\beta$ meet. Breaking the loop also allows the designer to check for circuit stability as shown with the loop gain ($A \times \beta$) phase plot in [Figure 3-2](#). At the point of intersection of A and $1/\beta$, the phase margin = $180^\circ - 90^\circ = 90^\circ$. A capacitor placed across resistor R_F in the β circuit can improve stability in applications that are susceptible to instability. Applications that drive heavy capacitive loads can benefit from an isolation resistor placed outside the loop on v_{out} .

4 Summary

Amplification of small signals in applications such as professional microphones, audio interfaces, mixers, turntables, and guitar amplifiers is very challenging. These types of applications benefit from the bias flexibility, high-input impedance, and low noise that a discrete JFET offers.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2023, Texas Instruments Incorporated