

Inrush Current Limit in the TPS720xx

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ABSTRACT

When not properly limited, the inrush current in low-dropout regulators (LDOs) can cause system level failures. The [TPS720xx series of LDOs](#) have a unique inrush current limit feature and a monotonic output voltage ramp, which significantly eases the system level power-supply design. This application report explains how the TPS720xx inrush current limit is different from other inrush limit schemes in that it is always limited to a fixed value in addition to the load current demand. The fixed value of the inrush current limit is determined by the combination of capacitance and the system load current at the output of the LDO (for example, capacitor scaling downstream).

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1 Introduction

The power source of a system is under great stress when the system powers on. It is expected to have a low impedance to charge all the capacitive loads during the transient phase of the start-up process until the system reaches a steady state. System designers must consider the finite source impedances and design their power systems accordingly to avoid significant application redesign time and effort.

The power source for an LDO included in a system can have variable characteristics and constraints. Because of the finite impedance of the sources, these types of LDOs are expected to limit the initial charging current; a large inrush current can cause the power source to dip dangerously low, at times even low enough to cause system-level problems.

[Figure 1](#) shows an example system implementation, where a dc-to-dc step-down converter is followed by an LDO for efficiency and better noise performance.

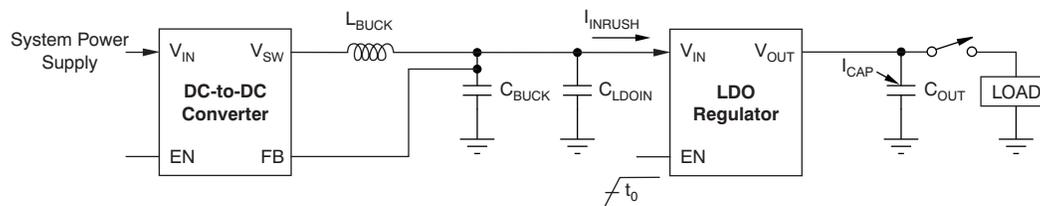


Figure 1. Typical Power System Implementation

Inrush current is a measure of the transient current taken from the supply pin during the initial startup sequence. Typically, when the part is enabled, a great deal of current is drawn from the supply to charge C_{OUT} to the final steady state value.

Many LDOs do not support an inrush current limit feature. This absence of a key feature creates problems that become especially severe if the LDO is capable of high load current and the input source is a switching converter. The output of the switching converter can be pulled down by a large inrush current that flows into charge C_{OUT} , triggering the step-down regulator PowerGood circuit, and in some cases forcing the circuit to reset. The step-down regulator may then cycle between charging and reset states. This cycling appears as low-frequency power-supply oscillations.

A typical inrush current value, assuming that very low impedance is charging the capacitance, can be found from [Equation 1](#):

$$I_{INRUSH} = C_{TOTAL} \times \frac{dV}{dT} \quad (1)$$

where V is the final voltage to which the output of the LDO regulates. If we know the total capacitance, C_{TOTAL} , at the LDO output, we can then compute the current that is drawn from the supply. Consider this example:

- Total capacitance on the LDO output is 2.2 μ F
- Final output voltage is 1.3V
- The circuit is capable of supplying current such that the output charges in 1 μ s

Using [Equation 1](#), the current drawn from the source is calculated to be 2.86A.

The reason for this behavior can also be explained using the impedance of the components connected to any node. A capacitor behaves much like a short-circuit during initial and high-frequency ramp-up periods. This behavior causes a high current to flow into the capacitor, such that the terminal connected to the output charges and rises towards its final steady state value.

Because of the above charging current into the LDO output, the LDO power source (that is, a dc-to-dc step-down regulator) will not have enough bandwidth to supply the inrush current demand of the LDO. Moreover, if we assume that the dc-dc converter uses a 1 μ H inductor, a voltage as high as 2.86V must develop across this inductor in 1 μ s. The input to output differential may not be available to give this current and therefore the output of the dc-dc converter will dip. The inrush current must therefore be supplied by the output capacitor of the step-down regulator. If we assume that this capacitor is 10 μ F, then the inrush current that will cause a voltage dip on the output of the step-down converter can be calculated from [Equation 2](#):

$$dV_{BUCK} = \frac{I_{INRUSH} \times dt}{C_{BUCK}} \quad (2)$$

From the [earlier inrush current calculation](#) of 2.86A in 1 μ s, the voltage dip at the output of the step-down converter is 286mV. For a 1.8V, 5% output step-down regulator, this voltage dip is 22% from the nominal value. The step-down regulator is grossly out of regulation.

If the step-down regulator has a very large output capacitor and is capable of supplying this inrush current, however, a second problem arises. The LDO charges the output capacitor C_{OUT} to its final regulation voltage. If the LDO is capable of supplying any amount of current, the output would jump up to its final value in very little time. Depending on the feedback loop response time of the LDO, the output would overshoot. This overshoot can sometimes be very large, and is capable of causing damage to sensitive load circuitry.

Another application example is an LDO used in a USB V_{BUS} -powered application. To prevent the possibility of damage to an upstream device, USB devices that are bus powered must implement inrush current limiting as defined in the [USB 2.0 specification](#). The profile of the inrush current spike is restricted so that the transient response of the input V_{BUS} power supply is not overwhelmed.

According to the USB 2.0 specification, the rising edge of the current spike must be no more than 100mA/ μ s. Designers must verify inrush current when devices wake up, either by themselves in a remote wakeup event or when the device is signaled to resume operation. The device must limit the inrush current on V_{BUS} . The maximum droop on V_{BUS} through the hub is 330mV. Additionally, the device must have sufficient onboard bypass capacitance, or a controlled power-on sequence such that the current drawn from the hub does not exceed the maximum current capability of the port at any time. Bus-powered hubs must have a V_{Drop} of < 100 mV between upstream and downstream ports when 100mA loads are present on all downstream ports. Bus-powered hubs with captive cables must have a V_{Drop} of < 350 mV between upstream and all downstream ports, including the cable. This constraint leaves very little voltage droop margin for the implementation of inrush current limit on an LDO.

A typical application where a monotonic output voltage ramp of the LDO is important is one in which an LDO powers a resistive type of load. The current transient on the input source depends on the LDO output voltage ramp rate. If the LDO does not implement an inrush current limit, the output voltage jumps up or overshoots the target output voltage and causes a large current draw from the input source. A controlled output voltage ramp rate is desirable because this limit controls the current flow to the resistive load. A field-programmable gate array (FPGA) is a typical example of a resistive load.

2 Current Controlled Charging

In this discussion thus far, it is assumed that the LDO has very low impedance between V_{IN} and V_{OUT} while charging the capacitances. If the impedance of the LDO is made high enough, however, then the current that is drawn through V_{IN} can be controlled. A better method of controlling the charging currents is to use an ideal current source. Because the current source impedance is very high, it cannot supply arbitrary amounts of high currents demanded by the low-impedance capacitor. This technique ensures controlled current charging or inrush current limit.

If the controlled charging current has a fixed value, $I_{INRUSHLIMIT}$, then this solution has the following drawback, however. If I_{LOAD} is greater than $I_{INRUSHLIMIT}$, then C_{OUT} does not charge at all; the total amount of charging current is diverted into the load. If I_{LOAD} is lesser than $I_{INRUSHLIMIT}$, then the difference current (or $I_{INRUSHLIMIT} - I_{LOAD}$) charges the LDO output capacitor C_{OUT} . If the difference current is very small, then it produces slow charging and a very slow startup.

3 TPS720xx Inrush Current Limit

The TPS720xx series of LDO regulators have a unique onboard inrush current limit circuit architecture: the current drawn through the V_{IN} pin is limited to a finite value. This $I_{INRUSHLIMIT}$ charges the output to its final voltage. All the current drawn through V_{IN} goes to charge the output capacitance when the load is disconnected. Equation 3 shows the inrush current limit performed by the circuit:

$$I_{INRUSHLIMIT} (A) = C_{OUT} (\mu F) \times 0.0454545 (V/\mu s) + I_{LOAD} (A) \quad (3)$$

Assuming a C_{OUT} of 2.2 μ F with the load disconnected (that is, $I_{LOAD} = 0$), the $I_{INRUSHLIMIT}$ is calculated to be 100mA. The inrush current charges the LDO output capacitor. If the output of the LDO regulates to 1.3V, then the LDO charges the capacitor to the final value in 28.6 μ s. This time period is large enough for the step-down regulator feedback loop to bring the output back into regulation and thus reduce the transient glitch at the output of the step-down converter.

Another consideration is when a load is connected to the output of an LDO. This connected load tries to steer a portion of the current away from C_{OUT} . The output in this case will not ramp up in the same way as before. For example, if the load connected at the output demands more than $I_{INRUSHLIMIT}$, before the output reaches the final value, the output will hold at the $I_{INRUSHLIMIT}$ value, and not charge any further. To accommodate such conditions, the TPS720xx inrush current limit circuit employs a new technique that supplies not only the $I_{INRUSHLIMIT}$ but also the additional current needed by the load.

As Figure 2 shows, if the load is continually connected, upon enabling, part of the load will also demand current when V_{OUT} begins to charge. Therefore, the current that is drawn from the supply through the V_{IN} pin not only must provide the current to charge the capacitor; is also must provide the current demanded by the load. In the case of the TPS720xx, the current that is provided by the step-down regulator would be ($I_{CAP} + I_{LOAD}$). As a result, with an output capacitor of 2.2 μ F under no-load conditions, I_{SUPPLY} is 100mA; with a full load of 350mA, $I_{SUPPLY} = 450$ mA.

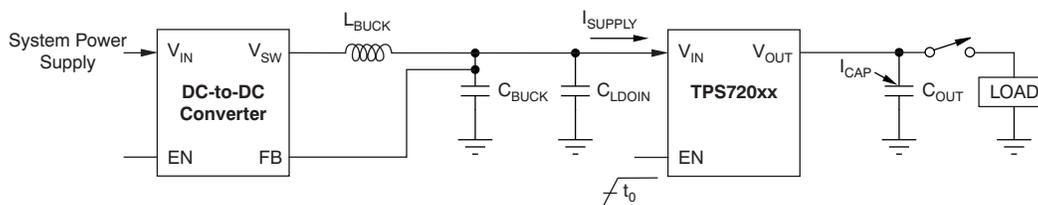


Figure 2. TPS720xx with Load Switched On

An important note is that if the total current taken from the supply exceeds the current limit that is set at 525mA, the current limit would activate. In this case, the current demand by the load is met, and the current that flows through the capacitor would diminish, thereby slowing the overall charge time. When the LDO output capacitor is completely charged and stops demanding current, $I_{\text{SUPPLY}} = I_{\text{LOAD}}$ and no additional current flows into the capacitor.

From Equation 3, we can observe that the slew rate at the output of the LDO is fixed at a constant value of $0.0454545\text{V}/\mu\text{s}$. The output voltage ramp rate is fixed regardless of the load capacitance, and the inrush current is directly proportional to the load capacitance. The fixed ramp rate limits the current into a resistive load typical in an FPGA application.

Figure 3 and Figure 4 show oscilloscope screen captures of the inrush currents on V_{IN} of the TPS720xx with C_{OUT} of $2.2\mu\text{F}$, at $I_{\text{LOAD}} = 0\text{mA}$ and $I_{\text{LOAD}} = 350\text{mA}$, respectively.

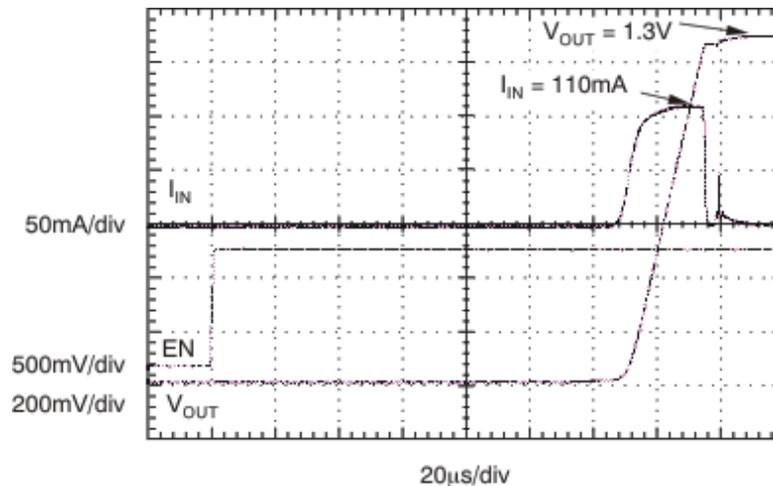


Figure 3. TPS720xx Inrush Current Limit with $V_{\text{BIAS}} = 2.7\text{V}$, $V_{\text{IN}} = 1.8\text{V}$, $V_{\text{OUT}} = 1.3\text{V}$, $C_{\text{OUT}} = 2.2\mu\text{F}$, and $I_{\text{LOAD}} = 0\text{mA}$

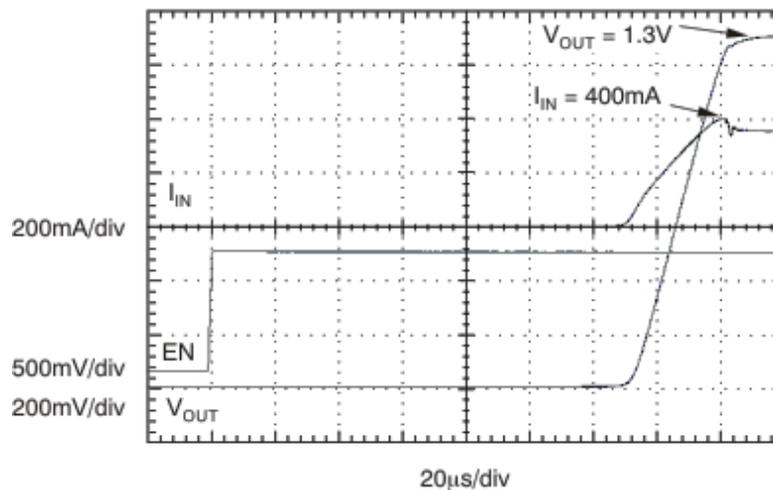


Figure 4. TPS720xx Inrush Current Limit with $V_{\text{BIAS}} = 2.7\text{V}$, $V_{\text{IN}} = 1.8\text{V}$, $V_{\text{OUT}} = 1.3\text{V}$, $C_{\text{OUT}} = 2.2\mu\text{F}$, and $I_{\text{LOAD}} = 350\text{mA}$

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