Texas Instruments

Application Report
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Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator

ABSTRACT

In low-dropout regulator (LDO) applications, a feedforward capacitor (C_{FF}) improves the stability, output noise, load transient response, and power-supply rejection ratio (PSRR) of the LDO. These advantages justify using C_{FF} in most applications; however, there are several issues that must be addressed. The power-good (PG) function may not be valid with a large C_{FF} during start-up. Also, C_{FF} can cause spurious triggering of the PG pin during a large-load transient. Lastly, the FB pin can go to a negative voltage, which may exceed the absolute maximum value when the LDO is shutting down with C_{FF}.

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1 Advantages of a Feedforward Capacitor

Figure 1 shows an application circuit of an LDO with a C_{FF} that is in parallel with R1. There are several advantages to using an LDO with a C_{FF}. Section 1.1 explains the stability of the LDO and how to use C_{FF} to improve LDO stability. Section 1.2 describes a C_{FF} that reduces the output noise and improves the PSRR. Section 1.3 shows that C_{FF} improves the load transient.

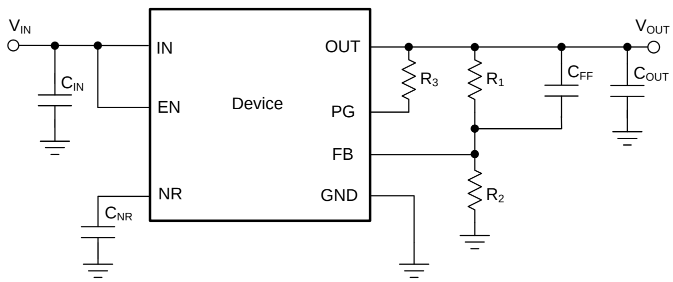

Figure 1. LDO with C_{FF}

1.1 *A Feedforward Capacitor Improves the Stability of the LDO*

Figure 2 shows a small-signal model of the LDO. The voltage on the FB pin is shown as V_{FB}. The voltage on the OUT pin is shown as V_{OUT}. The voltage of the LDO reference is shown as V_{ref}.

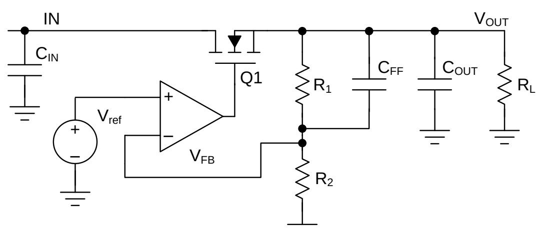

Figure 2. Small-Signal Model of the LDO

While most LDOs have internal compensation, using C_{FF} improves the stabillity of the LDO by adding a zero (Z_{FF}) and a pole (P_{FF})to the LDO feedback loop. From the small-signal analysis of the LDO shown in Figure 3, we see that the LDO has two low-frequency poles, P_{COMP} and P_{LOAD}. The frequency of P_{FF} is R1 / R2 times higher than the frequency of the Z_{FF}. As Figure 3 shows, the Z_{FF} that is generated by C_{FF} improves the phase margin of the LDO if Z_{FF} is close to the open-loop, unity-gain frequency. In addition, the zero increases the bandwidth of the LDO feedback loop and improves the load transient response of LDO. For more information about LDO stability, see Application Report SNVA167, *AN-1482 LDO Regulator Stability Using Ceramic Output Capacitors*.

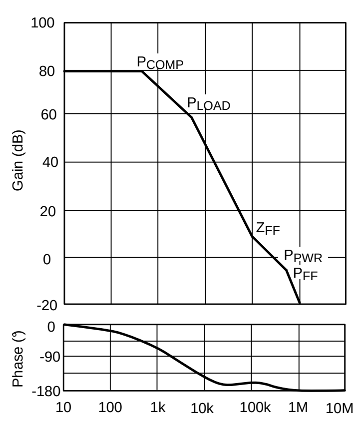

Figure 3. Bode Plot of the LDO Using C_{FF}

1.2 A Feedforward Capacitor Reduces the Output Noise and Improves PSRR

Noise is generated by the transistors and resistors in the LDO internal circuitry and by the external components. For more information about LDO noise, see Application Report SLYT489, *LDO Noise Examined in Detail*.

At higher frequencies, V_{FB} and V_{OUT} are effectively shorted by C_{FF}, which prevents the reference noise from being increased by the gain of the error amplifier. Figure 4 shows that using a larger C_{FF} results in lower LDO noise. Table 1 shows the RMS noise of the LDO. These noise measurements are based on the TPS7A8300 with the following values for C_{FF}: open, 10 nF, 100 nF, and 10 µF.

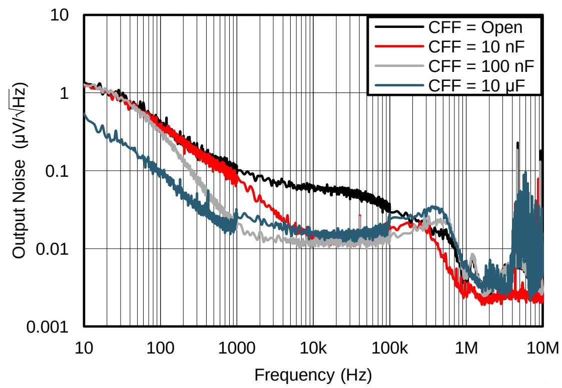

Figure 4. Output Spectral Noise Density for Various C_{FF} Values

Table 1. RMS Noise from 10 Hz to 100 kHz

C_{FF} Value	RMS Noise
Open	17.47 μV_{RMS}
10 nF	9.59 μV_{RMS}
100 nF	8.14 μV_{RMS}
10 µF	5.68 μV_{RMS}

C_{FF} also improves the PSRR of the LDO. The PSRR is a measurement of how well a circuit rejects ripple coming from the input power supply at various frequencies. This PSRR is very critical in many RF and wireless applications. The PSRR is determined primarily by the open-loop gain of the LDO. For more inforamtion, see Application Report SLYT202, *Understanding Power Supply Ripple Rejection in Linear Regulators*.

As mentioned in Section 1.1, C_{FF} improves the open-loop gain of the LDO; therefore, C_{FF} improves the PSRR of the LDO. This improvement can be seen in Figure 5. These PSRR measurements are based on the TPS7A8300 with the following values for C_{FF}: open, 10 nF, and 10 µF.

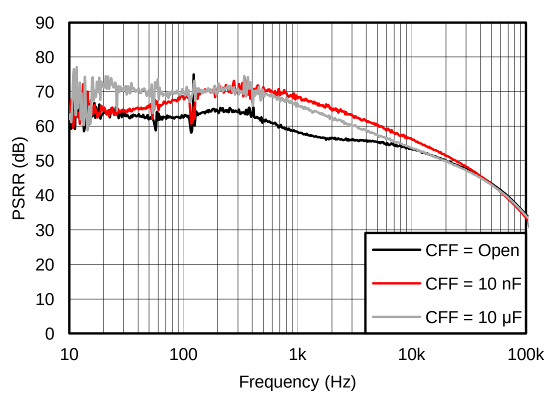

Figure 5. PSRR for Various C_{FF} Values

1.3 A Feedforward Capacitor Improves the Load Transient

As mentioned in Section 1.1, a C_{FF} improves the bandwidth of the LDO feedback loop. Accordingly, the load transient that is influenced by the bandwidth is improved by using a C_{FF}. In other words, an ac signal on V_{OUT} directly passes through the C_{FF} to the V_{FB}. Comparing to the normal transient response without a C_{FF} to the transient response with a C_{FF} shows that the increased ac signal on V_{FB} lowers the peak-to-peak output voltage. Figure 6 shows the output voltage amplitude of the TPS7A8300 without C_{FF} during a load transient. Figure 7 shows the output voltage amplitude of the TPS7A8300 with a 10 nF C_{FF} during a load transient.

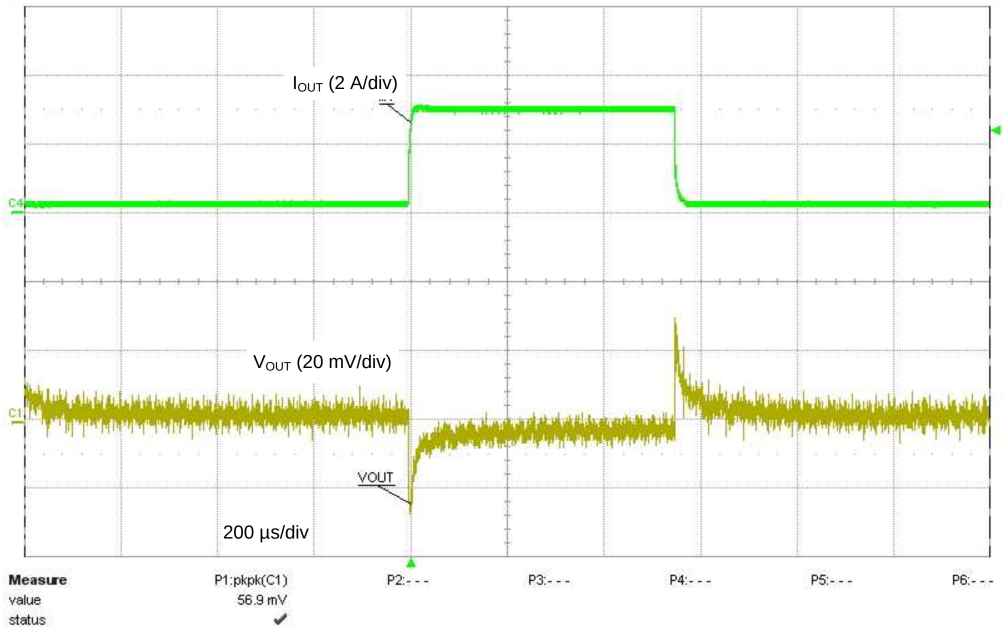

Figure 6. LDO without C_{FF} During a Load Transient

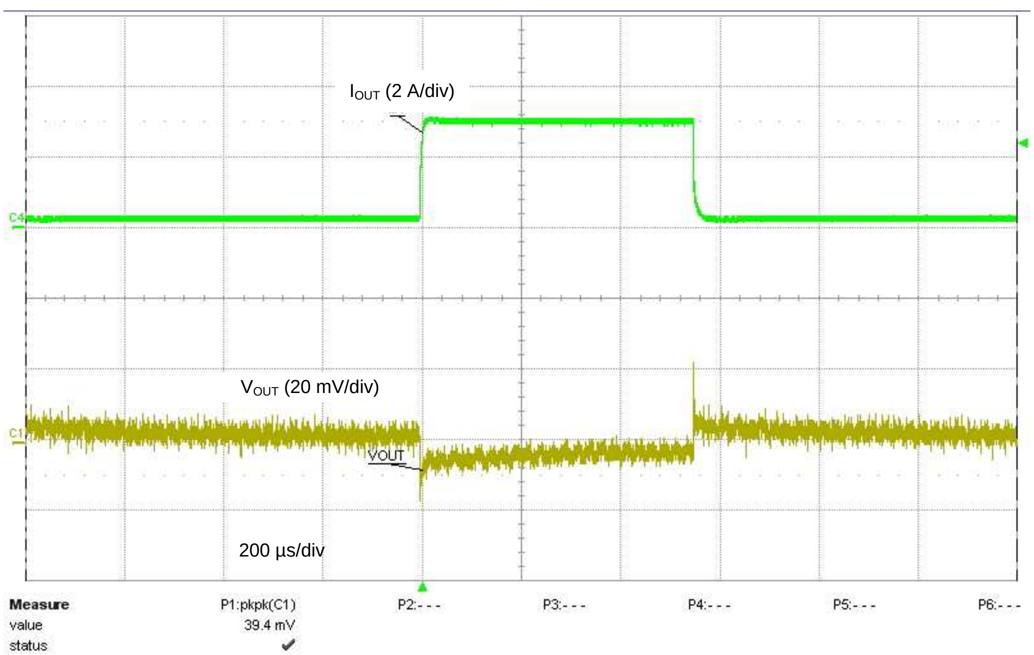

Figure 7. LDO with 10-nF C_{FF} During a Load Transient

2 Disadvantages of the Feedforward Capacitor

As mentioned in Section 1, there are many advantages to use a C_{FF} in an LDO. However, there are also some disadvantages to using a C_{FF} in an LDO. Section 2.1 explains a slow-start issue in an LDO with a C_{FF} during start-up. Section 2.2 describes the effects of C_{FF} on PG during load-transient. Section 2.3 shows how C_{FF} affects the FB pin during shutdown.

2.1 Start-Up Issue

Many LDOs have a power-good comparator that asserts when the regulated output voltage is less than the PG threshold, as shown Figure 8. The TPS7A8300 (SBVS197) is used in this example. When the output voltage, V_{OUT}, falls below the PG threshold voltage (V_{ITPG} = 0.9V_{OUT}), the PG pin open-drain output engages (low impedance to GND). When the output voltage (V_{OUT}) exceeds the V_{ITPG} threshold by an amount greater than 0.02V_{OUT}, the PG pin becomes high-impedance. The power-good comparator compares V_{FB} to V_{ref}. As Figure 9(a) shows during the start-up time, V_{FB} is equal to V_{ref}, which is proportional to V_{OUT} without a feedforward capacitor. Figure 9(a) also shows that the PG pin goes high when V_{FB} is greater than the threshold.

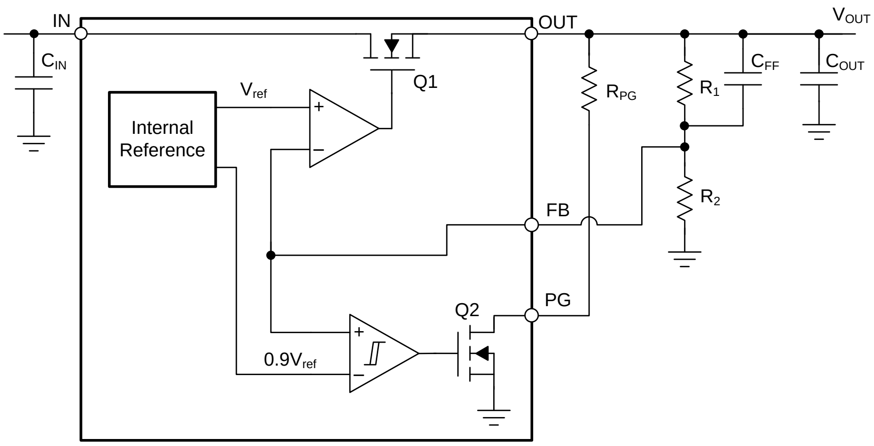

Figure 8. LDO Internal Structure with Power-Good Comparator

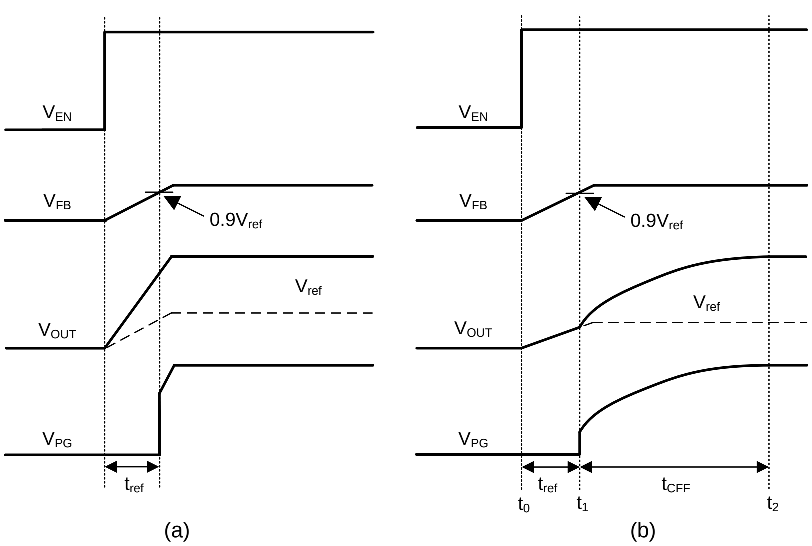

Figure 9. Start-up (a) without C_{FF} and (b) with Large 10-µF Capacitor

With C_{FF}, the start-up time is divided into two stages, as shown in Equation 1:

$$t_{start\text{-}up} = t_{ref} + t_{CFF} \quad (1)$$

During the t_{ref} time, V_{OUT} tracks V_{FB}. V_{FB} is controlled by the LDO feedback loop and is forced to match V_{ref}. The t_{ref} is determined by the internal soft-start charging circuit. The t_{ref} soft-start ramp time depends on the soft-start current (I_{SS}), the soft-start capacitance (C_{SS}), and the internal reference (V_{SS}). After the t_{ref} period expires, both V_{OUT} and V_{FB} are equal to the reference voltage, as shown in Equation 2:

$$t_{ref} = \frac{V_{SS} \bullet C_{SS}}{I_{SS}} \quad (2)$$

At t_1, the PG pin is asserted (pulled up to V_{OUT}) when V_{FB} reaches the reference voltage because the internal power-good comparator monitors the V_{FB} voltage and V_{FB} increases above the PG threshold ($0.9V_{ref}$). However, it takes t_{CFF} time for V_{OUT} to reach the regulated voltage. t_{CFF} is the feedforward capacitor charging time. The t_{CFF} charging time is determined by the resistance of R1 and the capacitance of C_{FF}. If the capacitance is small, then t_{CFF} is shorter than t_{ref}, and there is no issue with PG. However, if the capacitance of C_{FF} is very large, then t_{CFF} is much longer than t_{ref}. The zero state response approximation formula of t_{CFF} is shown in Equation 3:

$$t_{CFF} = 3R_1 \bullet C_{FF} \quad (3)$$

Figure 9(b) shows that V_{OUT} rises to the regulated voltage very slowly. At t_1, the PG pin asserts and follows the slowly-rising V_{OUT}. Downstream components see this as a logical high, even though V_{OUT} has not settled to the regulated voltage.

Figure 10 shows the start-up of TPS7A8300 with s 10-nF C_{FF}. Figure 11 shows the start-up of TPS7A8300 with a 10-µF capacitor. The test results show that the 10-µF C_{FF} increases the start-up time significantly, and PG is not valid in this condition. If a large feedforward capacitor is necessary in an application, take this issue into consideration.

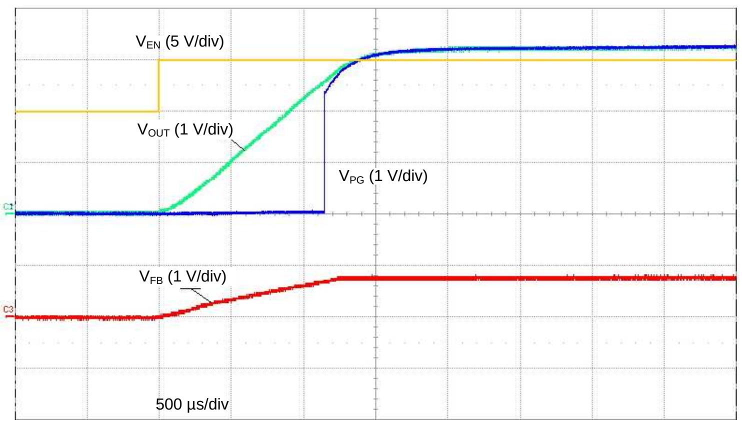

Figure 10. Start-Up Plot of the TPS7A8300 with 10-nF C_{FF}

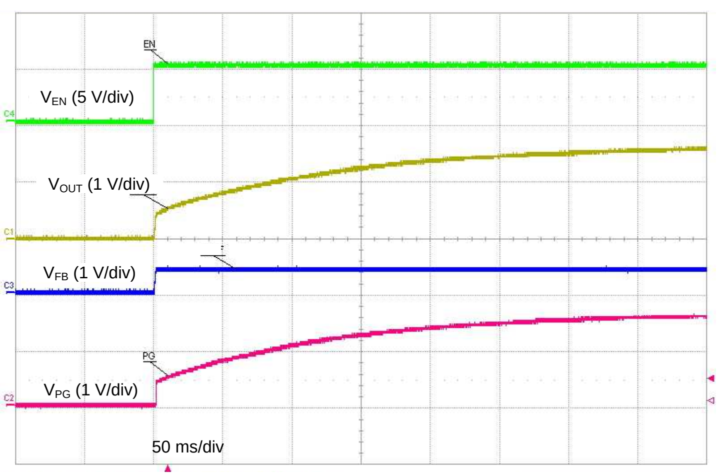

Figure 11. Start-Up Plot of the TPS7A8300 with 10-µF C_{FF}

2.2 C_{FF} Effect on a Large-Load Transient

Another potential issue regards the PG function when using C_{FF} during a large load transient. For example, during a load transient, the undershoot on V_{OUT} directly couples through C_{FF}, and the same undershoot amplitude is forced onto V_{FB}. Because of the power-good comparator monitoring V_{FB}, if the under-shoot amplitude on V_{FB} is large enough, V_{FB} falls below the V_{ITPG} threshold and results in PG deasserting (low impedance to GND). Figure 12 shows the TPS7A8300 with a 10-µF C_{FF} during a large load transient (from 0.1 A to 3 A); the PG pin generates the false signal.

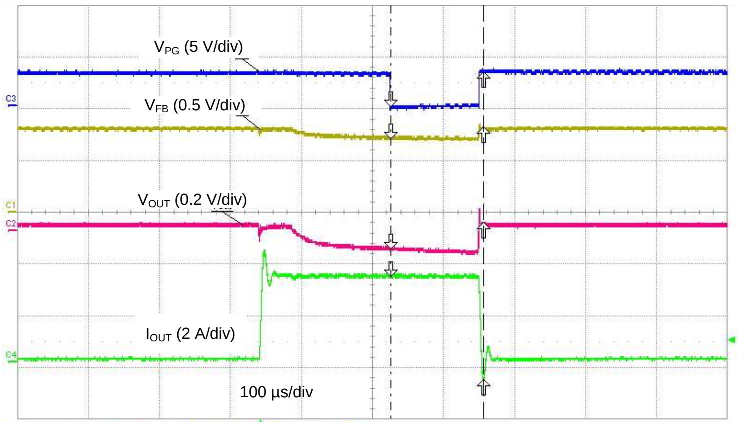

Figure 12. TPS7A8300 with 10-µF C_{FF} During a Load Transient

2.3 C_{FF} Effect on V_{FB} During Shutdown

The final disadvantage is similar to the issue discussed in Section 2.2. When the LDO is shut down by disabling EN or by the V_{IN} rail collapsing, C_{FF} causes negative voltage on the FB pin. The reason is that when the LDO is shut down, the charge stored in C_{FF} discharges through the internal electrostatic discharge (ESD) diode connected between the FB pin and the GND pin, as shown in Figure 13. This discharge may result in exceeding the negative absolute maximum value of the FB pin. The example in Figure 14 shows that the FB pin goes negative when the LDO shuts down. This issue can be avoided by adding a Schottky diode between the FB pin and the GND pin.

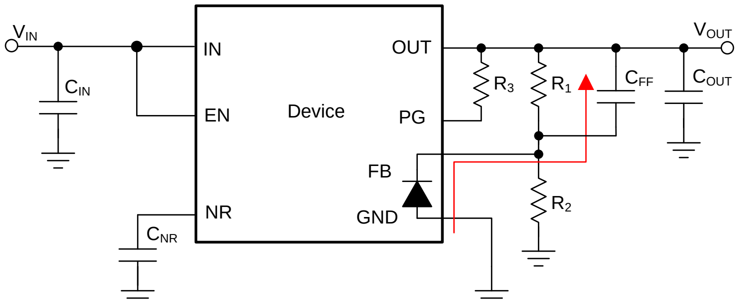

Figure 13. LDO with Internal ESD Model

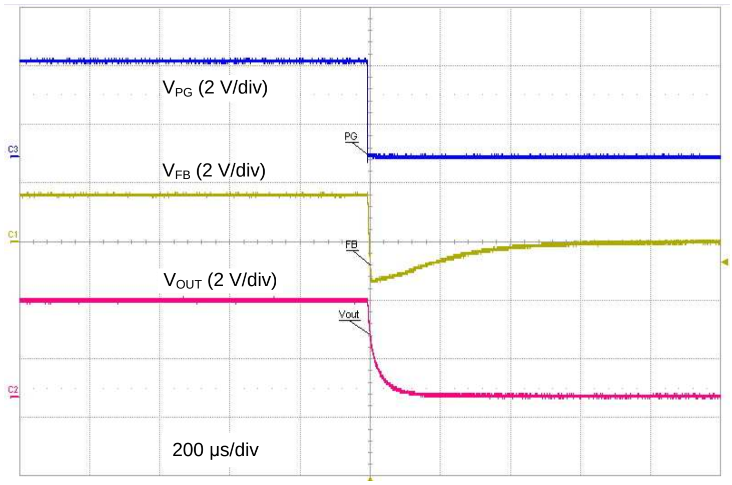

Figure 14. TPS7A8300 Shutdown Plot with 10-µF C_{FF}

3 Summary

In conclusion, using C_{FF} with an LDO improves the noise, PSRR, load transient response, and stability. These advantages make C_{FF} useful to power noise-sensitive applications, such as RF components, wireless infrastructure, and test and measurement applications. On the other hand, C_{FF} can cause slow start-up. C_{FF} can also cause the PG function to be invalid at start-up and during a transient. Lastly, during LDO shut-down, C_{FF} may result in exceeding the negative absolute maximum value of the FB pin. Make sure to take these C_{FF} drawbacks into consideration when designing a circuit.

4 References

1. SNVA167 — *LDO Regulator Stability Using Ceramic Output Capacitors*
2. SLYT489 — *LDO Noise Examined In Detail*
3. SLYT202 — *Understanding Power Supply Ripple Rejection in Linear Regulators*
4. SBVS197 — TPS7A8300 2-A, 6-µV_{RMS}, RF, LDO Voltage Regulator

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