Power-Dissipation Calculations for TI FIFO Products

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TEXAS INSTRUMENTS

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Abstract

Power consumption has become a major consideration in today's circuit design. Low power consumption is one of the major advantages of Texas Instruments (TI) FIFO products. Power calculations are required to meet the design requirements relating to the chip temperature and system power. The only way that a designer can minimize the power requirements of a board or a system is to understand and control the causes. This application report assists the component and system design engineer to evaluate the power consumption of TI ACT and ABT FIFO products.

Introduction

A simple method of calculating power dissipation for FIFO products under varying conditions is presented in this application report. Power calculations include the power dissipation when a FIFO is transferring data as well as when only clocks are running and no data is being transferred. Power consumption in a FIFO product is dependent on clock switching frequency, data-input switching frequency, data-output switching frequency, and data-output capacitive loading.

In this report, a simplified introduction to the physics of CMOS devices regarding power consumption is presented. In the second part of this application report, power-calculation examples for FIFO products are presented in two subsections. The first subsection includes power-dissipation calculations for advanced CMOS (ACT) FIFO products, including an example using the SN74ACT3632. The second subsection includes power-dissipation calculations for advanced BiCMOS (ABT) FIFO products, including an example using the SN74ABT3614. Appendix A includes several graphs of I_{CC} versus frequency to assist the design engineer with the information required for calculating power consumption. In addition, the graphs of I_{CC} versus frequency assist the designer in selecting a device with the lowest power consumption. Appendix B presents reliability information and a table of maximum power versus ambient temperature for different package types. Finally, the goals, achievements, and results of this application report are included in the summary.

CMOS and BiCMOS Power Basics

Power dissipation is dependent on supply voltage (V_{CC}) and supply current (I_{CC}). It is calculated using the formula:

$$P = V_{CC} \times I_{CC}$$

Any CMOS function can be broken down to a gate-level model. The simplest CMOS circuit is an inverter as shown in Figure 1. When the input voltage is at ground or V_{CC} level, one transistor is fully on and the other transistor is fully off. This results in a negligible I_{CC} that is simply the reverse-leakage current flowing through the nonconducting transistor. Quiescent power is due to this current (referred to as idle I_{CC} in this application report).

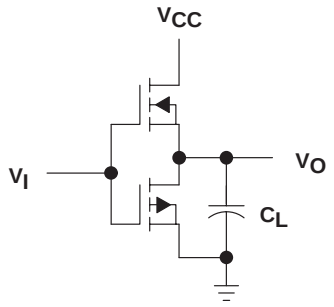

Figure 1. Gate Model of a CMOS Inverter

When the input switches from V_{CC} to ground or vice versa during the transition period, both transistors are on, resulting in current flow from V_{CC} to ground. This current is called through current (referred to as active current in this application report). For many applications using CMOS and BiCMOS devices, switching power accounts for most of the power consumption.

The through-current waveform supplied by V_{CC} to a CMOS gate is shown in Figure 2. As the switching frequency increases, the number of current spikes also increases. For instance, if the switching frequency is doubled, the number of current spikes double. Figure 3 shows the current spikes for the same device at twice the frequency of the signal shown in Figure 2. Since power is directly proportional to the RMS current, the increase in frequency results in increased power dissipation. Power consumption due to the load should also be considered. For a CMOS device with an entirely capacitive load, the transient power due to the load is calculated using the formula:

$$P = C_L \times V_{CC}^2 \times f_o$$

Where:

C_L = load capacitance
V_{CC} = supply voltage
f_o = output switching frequency

Power calculations are presented in more detail in the following sections of this application report.

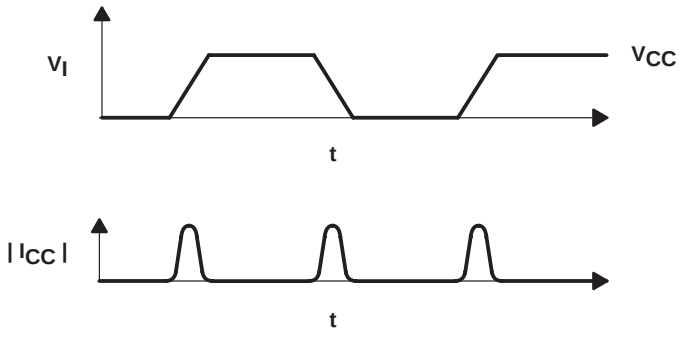

Figure 2. Current Waveform Supplied by V_{CC} to a CMOS Gate

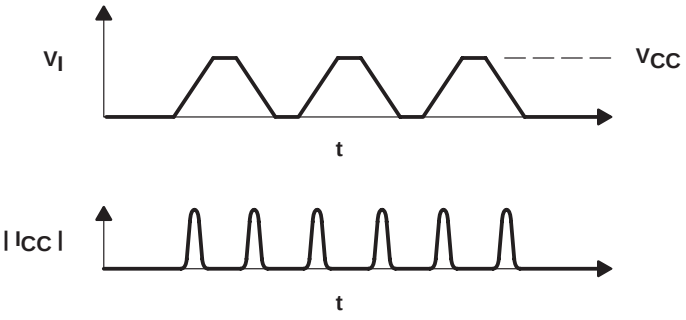

Figure 3. Current Waveform When Switching Frequency Is Doubled

Power Calculation

The total power consumption in the ACT and ABT FIFOs is the sum of the quiescent or nonswitching power (P_q) and dynamic or switching power (P_d):

$$P_T = P_d\,(DC_d) + P_q\,(1 - DC_d)$$

Where:

P_T	=	total power
P_d	=	dynamic or switching power
P_q	=	quiescent or nonswitching power
DC_d	=	% time FIFO is switching
$1 - DC_d$	=	% time FIFO is not switching

Quiescent or Nonswitching Power Dissipation in ACT FIFO Devices (CMOS FIFO products)

The quiescent power consumed by a CMOS device is given by the formula:

$$P_q = V_{CC} \times I_{CC}\,(\text{total})$$

Where V_{CC} is the supply voltage and I_{CC} (total) includes the increase in I_{CC} due to inputs being driven by TTL devices. This is calculated as:

$$I_{CC}\,(\text{total}) = [N_{TTL} \times \Delta I_{CC} \times DC_{VIH}] + I_{CCI}$$

Where:

I_{CCI}	=	$f_{clock} \times pF_{(clock)}$ = supply current when FIFO is idle (the clocks are running but no data is written to or read from the FIFO)
f_{clock}	=	clock switching frequency
$pF_{(clock)}$	=	clock switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet)
N_{TTL}	=	number of inputs driven by TTL levels
ΔI_{CC}	=	increase in supply current for each input at a TTL high level (see data sheet)
DC_{VIH}	=	% of TTL signals at a high level of 3.4 V

Therefore, the quiescent power is calculated by:

$$P_q = V_{CC} \times [I_{CCI} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})]$$

Dynamic or Switching Power Dissipation in ACT FIFO Devices (CMOS FIFO products)

For most applications, dynamic power accounts for most of the total power dissipation of a CMOS device. Dynamic power is dependent on the load capacitance, output switching frequency, input switching frequency, and the power-dissipation capacitance of the device. The following equation is typically used to calculate power consumption in a CMOS device (refer to *Texas Instruments Advanced CMOS Logic Designer's Handbook*, literature number SCAA001A).

$$P_d = (C_{pd} \times V_{CC}^2 \times f_i) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

The value C_{pd} is not provided for most FIFO devices. It is more accurate to calculate power of a FIFO device by obtaining active I_{CC} versus frequency curves, I_{CCf} (supply current when the FIFO is transferring data) and the slope of the I_{CC} versus frequency curve (which essentially display the same information). Consequently, dynamic power includes the power dissipation due to active I_{CC} without the output load and power dissipation due to the output load current.

$$P_d = V_{CC} \times I_{CC}\,(\text{total}) + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

Where:

$V_{CC} \times I_{CC}$ (total)	=	device switching power without load
I_{CC} (total)	=	$[I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})]$
$\Sigma(C_L \times V_{CC}^2 \times f_o)$	=	power due to output switching frequency and load capacitance

Therefore, dynamic power consumption is calculated by:

$$P_d = V_{CC} \times [I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] + \Sigma(C_L \times V_{CC}^2 \times f_o)$$

Where:

V_{CC} = supply voltage
I_{CCf} = supply current when the FIFO is transferring data (see active I_{CC} versus frequency plot in data sheet)
N_{TTL} = number of inputs driven by TTL levels
ΔI_{CC} = increase in supply current for each input at a TTL high level (see data sheet)
DC_{VIH} = % of inputs at a TTL high level
C_L = load capacitance
f_o = output switching frequency

Example 1

This example shows how to calculate the power dissipation for an SN74ACT3632 bidirectional FIFO used in a system under the following conditions:

- Data input lines (A0–A35) are driven by a TTL device.
- Control signals (CLKA, CLKB, $\overline{CSA}$, $\overline{CSB}$, W/$\overline{RA}$, $\overline{W}$/RB, $\overline{RST1}$, $\overline{RST2}$, ENA, ENB, MBA, MBB, FSO, FS1) are driven by a CMOS device.
- The output of the FIFO is fed to a memory device.
- Only 3/4 of the inputs (or outputs) are switching at a given time.
- The port-B clock rate is 33.3 MHz and the port-A clock rate is 40 MHz.
- The SN74ACT3632 is only used about 1/3 of the time by the system.
- The load capacitance on each output is about 30 pF, and the supply voltage is set at 5 V.
- The SN74ACT3632 is used equally in both directions.

The following parametric values are needed to calculate power dissipation:

Where:

V_{CC} = supply voltage = 5 V
DC_d = % time FIFO is switching = 1/3
$1 - DC_d$ = % time FIFO is not switching = 2/3
f_{clockA} = clock switching frequency of port A = 40 MHz
f_{clockB} = clock switching frequency of port B = 33.3 MHz
pF = clock switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet) = 0.184 mA/MHz
I_{CCI} = $I_{CLKA} + I_{CLKB} = (f_{clockA} \times pF) + (f_{clockB} \times pF)$ = (40 MHz + 33.3 MHz) × 0.184 mA/MHz = 13.4872 mA
N_{TTL} = number of inputs driven by TTL levels = 36
I_{CCf} = active supply current when FIFO is transferring data from the curve if I_{CC} versus frequency = 115 mA @ 33.3 MHz
ΔI_{CC} = increase in supply current for each input at a TTL high level (see data sheet)
= 0 mA if $\overline{CSA} = V_{IH}$ or $\overline{CSB} = V_{IH}$
= 1 mA if $\overline{CSA} = V_{IL}$ or $\overline{CSB} = V_{IL}$
= 1 mA for all other inputs (see data sheet)

In this example (ΔI_{CC} = 1 mA is assumed):

DC_{VIH} = 3/4
C_L = load capacitance = 30 pF
f_o = output switching frequency = 1/2 (since maximum data rate is 1/2 clock frequency) × 3/4 (since 3/4 of the outputs are switching at a given time) × 33.3 (slowest of the two clock frequencies, f_{clockA} or f_{clockB}) = 12.4875 MHz

I_{CCf} and I_{CCI} are taken from graphs of I_{CC} versus clock frequency. In the case of SN74ACT3632, I_{CCI} is taken for either of the two clocks while only one clock is switching. All other inputs are tied to 0 or to $V_{CC} - 0.2$ V and all the outputs are disconnected. Later, I_{CCf} is measured while simultaneously reading and writing a FIFO with both CLKA and CLKB set to f_{clock}.

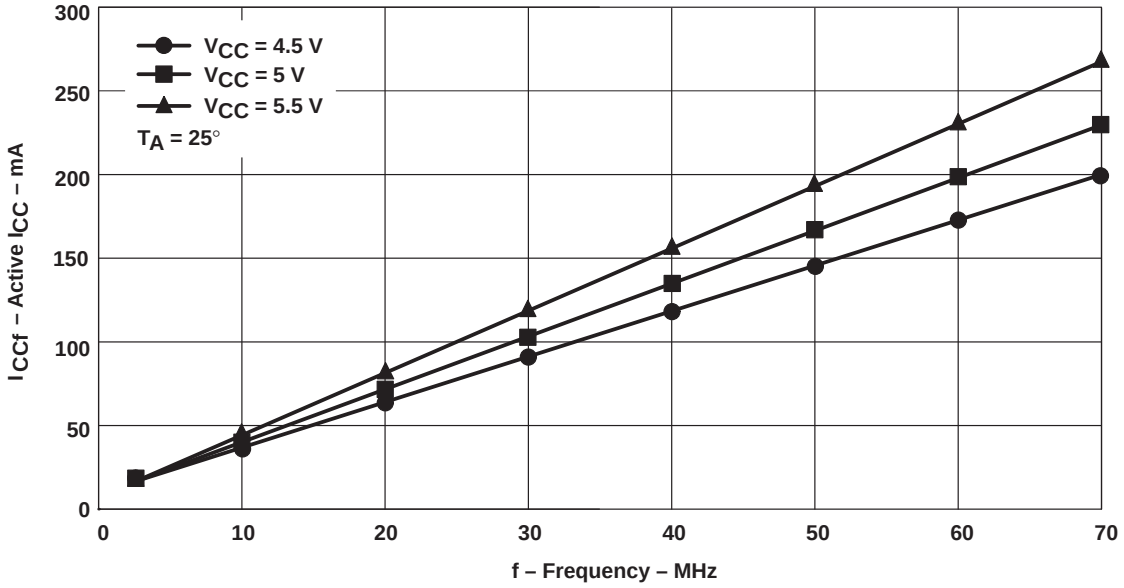

Figure 4. SN74ACT3632 Active I_{CC} Versus Frequency

Solution

$$\begin{aligned} P_T &= P_T \text{ (from A to B)} + P_T \text{ (from B to A)} \\ &= P_q \text{ (from A to B)} + P_q \text{ (from B to A)} + P_d \text{ (from A to B)} + P_d \text{ (from B to A)} \\ &= P_q + P_d \end{aligned}$$

Where P_q and P_d include power from A to B and from B to A directions.

Quiescent Power

$$\begin{aligned} P_q &= V_{CC} \times [I_{CCI} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] \\ &= 5 \times [13.4872 \text{ mA} + (36 \times 1 \text{ mA} \times 3/4)] = 202.436 \text{ mW} \end{aligned}$$

Dynamic Power

$$\begin{aligned} P_d &= V_{CC} \times [I_{CCf} + (N_{TTL} \times \Delta I_{CC} \times DC_{VIH})] + \Sigma(C_L \times V_{CC}^2 \times f_o) \\ &= 5 \times [115 \text{ mA} + (36 \times 1 \text{ mA} \times 3/4)] + [36 \times 30 \text{ pF} \times (5 \text{ V})^2 \times 12.4875 \text{ MHz}] \\ &= 710 \text{ mW} + 337.1625 \text{ mW} = 1047.1625 \text{ mW} \end{aligned}$$

Total Power

$$\begin{aligned} P_T &= P_d (DC_d) + P_q (1 - DC_d) \\ &= 1047.1625 \text{ mW} \times 1/3 + 202.436 \text{ mW} \times 2/3 = 484.0115 \text{ mW} \end{aligned}$$

Therefore, total power is approximately:

$$P_T = 484 \text{ mW}$$

The SN74ACT3632 is available in 120-pin TQFP and 132-pin PQFP packages (refer to Appendix B for the maximum power curve calculated for reliability purposes). At maximum ambient temperature (70°C) and no air flow for 132-pin PQFP and 120-pin TQFP packages, the maximum power that the packages can dissipate to free air is 1610 mW and 1606 mW, respectively. The SN74ACT3632, in this example, meets the reliability requirement since 484 mW is much less than 1610 mW or 1606 mW.

Quiescent or Nonswitching Power Dissipation in ABT FIFO Devices (BiCMOS FIFO products)

Unlike CMOS devices that have a single value for I_{CC}, BiCMOS devices have varying static current levels depending on the state of the output (I_{CCL}, I_{CCH}, I_{CCZ}). Quiescent power includes the power consumed while outputs are active, the power consumed when outputs are disabled, and the power consumed by the switching clocks. The design of the BiCMOS inputs is such that when a TTL high level is applied at the input, it does not increase the current; therefore, the ΔI_{CC} term ($N_{TTL} \times \Delta I_{CC} \times DC_d$) is excluded from the following equation (from *Texas Instruments ABT Advanced BiCMOS Technology Data Book, 1993,* literature # SCBD002A) in calculating power for ABT FIFO products.

$$P_q = V_{CC} \times [\, DC_{EN} \times (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1 - DC_{EN})I_{CCZ} + I_{CCI}\,]$$

Where:

$V_{CC} \times [\, DC_{EN} \times (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T)]$ = power consumed while outputs are active
$V_{CC} \times (1 - DC_{EN})I_{CCZ}$ = power consumed when outputs are disabled
$V_{CC} \times I_{CCI}$ = power consumed by switching clocks
V_{CC} = supply voltage
I_{CCI} = $f_{clock} \times pF$ = supply current when FIFO is idle (the clocks are running but no data is written to or read from the FIFO) (not in the data sheet)
f_{clock} = clock switching frequency
pF = clock switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet)
DC_{EN} = % duty cycle enabled
I_{CCH} = power-supply current when outputs are in high state (see data sheet)
I_{CCL} = power-supply current when outputs are in low state (see data sheet)
I_{CCZ} = power-supply current when outputs are in high-impedance state (see data sheet)
N_L = number of outputs in low state
N_H = number of outputs in high state
N_T = total number of outputs

Dynamic or Switching Power Dissipation in ABT FIFO Devices (BiCMOS FIFO products)

For most applications, dynamic power accounts for most of the total power consumption of a BiCMOS device. Dynamic power consumption includes the device switching power consumed without the load, as well as the power consumed due to the capacitive load.

$$P_d = V_{CC} \times I_{CCf} + \Sigma[\, V_{CC} \times C_L \times (V_{OH} - V_{OL}) \times f_o\,]$$

Where:

$V_{CC} \times I_{CCf}$ = device switching power without the load
$\Sigma[\, V_{CC} \times C_L \times (V_{OH} - V_{OL}) \times f_o\,]$ = power consumed due to the output switching frequency and the load capacitance
V_{CC} = supply voltage
I_{CCf} = supply current when FIFO is transferring data, active current (see active I_{CC} versus frequency plot in data sheet)
f_o = output switching frequency
V_{OH} = output voltage in high state
V_{OL} = output voltage in low state
C_L = load capacitance

Example 2

This example shows how to calculate the power dissipation for an SN74ABT3614 bidirectional FIFO used in a system under the following conditions:

- Data input lines (A0–A35) and the control signals (CLKA, CLKB, $\overline{\text{CSA}}$, $\overline{\text{CSB}}$, W/$\overline{\text{R}}$A, W/$\overline{\text{R}}$B, ENA, ENB, MBA, $\overline{\text{BE}}$, $\overline{\text{RST}}$, SIZ0, SIZ1, ODD/$\overline{\text{EVEN}}$, SW0, SW1, PGA, PGB) are driven by a CMOS device.
- Only 2/3 of the inputs (or outputs) are switching at a given time.
- The output of the FIFO is fed to a memory device.
- The port-B clock rate is 33.3 MHz and the port-A clock rate is 40 MHz.
- The SN74ABT3614 is only used 60% of the time by the system.
- The load capacitance of each output is about 50 pF, and the supply voltage is set to 5 V.
- During the FIFO active period, the bus is enabled 75% of the time.
- When the bus is enabled, the output is in the high state 80% of the time.
- The SN74ABT3614 is used equally in both directions.

Figures 5 through 7 and included information are needed to calculate power dissipation:

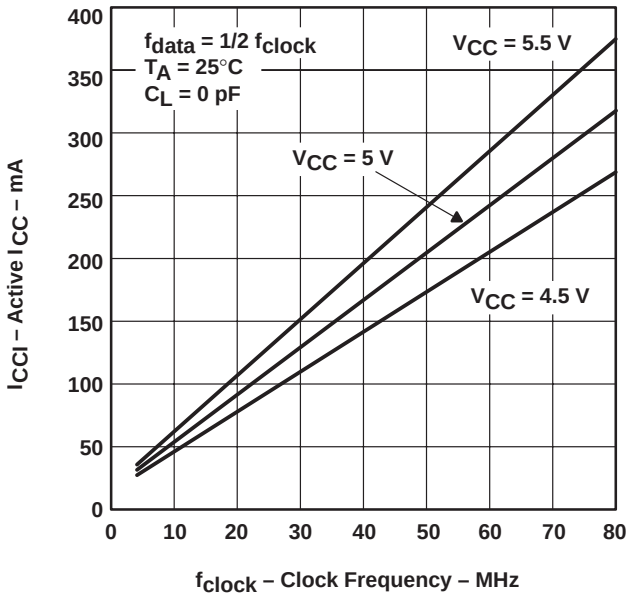

Figure 5. SN74ABT3614 Active I_{CC} With CLKA and CLKB Switching, Simultaneous Read/Write and CLKB as Data Output

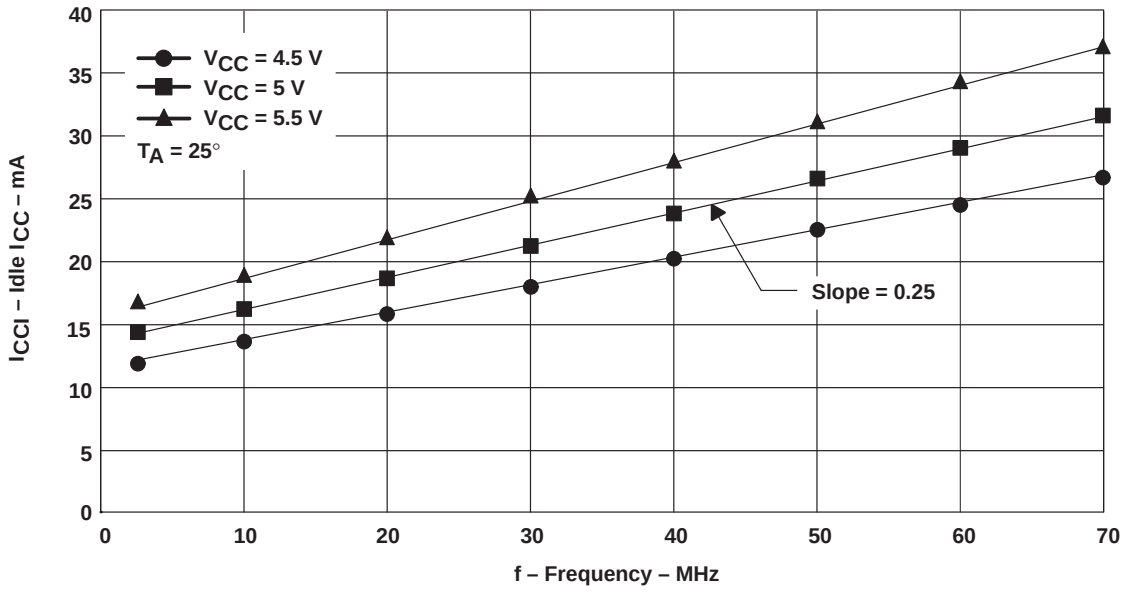

Figure 6. SN74ABT3614 Idle I_{CC} With CLKA Switching, Other Inputs at 0 or V_{CC} − 0.2 V and Outputs Disconnected

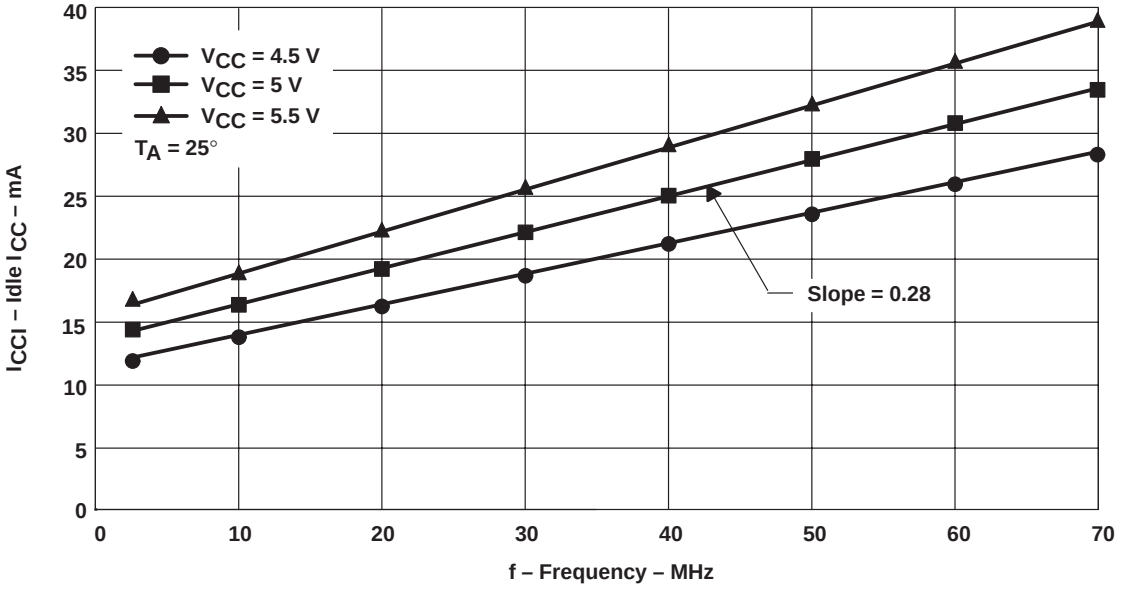

Figure 7. SN74ABT3614 Idle I_{CC} With CLKB Switching, Other Inputs at 0 or V_{CC} − 0.2 V and Outputs Disconnected

The following parametric values are needed to calculate power dissipation:

V_{CC} = supply voltage = 5 V
V_{OH} = V_{CC} – 1.3 V
V_{OL} = 0.3 V
DC_d = % time FIFO is switching = 0.6
$1 – DC_d$ = % time FIFO is not switching = 0.4
f_{clockA} = clock switching frequency of port A = 40 MHz
f_{clockB} = clock switching frequency of port B = 33.3 MHz
pF(A) = clock-A switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet) = 0.25
pF(B) = clock-B switching power factor, the slope of I_{CC} versus f_{clock} curve (see data sheet) = 0.28
DC_{EN} = % duty cycle enabled = 0.75
I_{CCI} = $[f_{clockA} \times pF(A] + [f_{clockB} \times pF(B) = (40 \times 0.25) + (33.3 \times 0.28) = 19.32$ mA
I_{CCf} = idle supply current when FIFO is transferring data = 136.26 mA
I_{CCH} = active supply current when outputs are in high state (see data sheet) = 30 mA
I_{CCL} = power supply current when outputs are in low state (see data sheet) = 130 mA
I_{CCZ} = power supply current when outputs are in high-impedance state (see data sheet) = 30 mA
N_L/N_T = ratio of number of outputs in low state to total number of outputs = 0.2
N_H/N_T = ratio of number of outputs in high state to total number of outputs = 0.8
C_L = load capacitance = 50 pF
f_o = 1/2 (since maximum data rate is 1/2 clock frequency) × 2/3
(since 2/3 of the outputs are switching at a given time) × 33.3 MHz
(slowest of the the two clock frequencies, f_{clockA} or f_{clockB}) = 11.1 MHz

Solution

$$\begin{aligned} P_T &= P_T \text{ (from A to B)} + P_T \text{ (from B to A)} \\ &= P_q \text{ (from A to B)} + P_q \text{ (from B to A)} + P_d \text{ (from A to B)} + P_d \text{ (from B to A)} \\ &= P_q + P_d \end{aligned}$$

Where P_q and P_d include power from A to B and from B to A directions.

Quiescent Power

$$\begin{aligned} P_q &= V_{CC} \times [DC_{EN} \times (N_H \times I_{CCH}/N_T + N_L \times I_{CCL}/N_T) + (1 – DC_{EN})I_{CCZ} + I_{CCI}] \\ &= 5 \text{ V} \times [0.75 \times (0.8 \times 30 \text{ mA} + 0.2 \times 130 \text{ mA}) + (1 – 0.75)\ 30 \text{ mA} + 19.32 \text{ mA}] \\ &= 5 \text{ V} \times [37.5 \text{ mA} + 7.5 \text{ mA} + 19.32 \text{ mA}] = 321.6 \text{ mW} \end{aligned}$$

Dynamic Power

$$\begin{aligned} P_d &= V_{CC} \times I_{CCf} + \Sigma[V_{CC} \times C_L \times (V_{OH} – V_{OL}) \times f_o] \\ &= 5 \text{ V} \times 136.25 \text{ mA} + \Sigma[5 \times 50 \text{ pF} \times (5 \text{ V} – 1.3 – 0.3 \text{ V}) \times (11.1 \text{ MHz})] \\ &= 681.25 \text{ mW} + (36 \times 9.44 \text{ mW}) = 681.25 \text{ mW} + 339.66 \text{ mW} = 1020.91 \text{ mW} \end{aligned}$$

Total Power

$$\begin{aligned} P_T &= P_d\ (DC_d) + P_q\ (1 – DC_d) \\ &= 1020.91 \text{ mW} \times 0.6 + 321.6 \times 0.4 = 741.19 \text{ mW} \end{aligned}$$

Therefore, total power is approximately:

$$P_T = 741.19 \text{ mW}$$

The SN74ABT3614 is available in 120-pin TQFP and 132-pin PQFP packages (refer to Appendix B for the maximum power curve calculated for reliability purposes). At maximum ambient temperature (70°C) and no air flow for the 132-pin PQFP and 120-pin TQFP packages, the maximum power that the package can dissipate to free air is 1610 mW and 1606 mW,

respectively. The SN74ABT3614, in this example, meets the reliability requirement since 741.19 mW is much less than 1610 mW or 1606 mW.

Summary

Power-dissipation calculations are essential to meet the design requirements related to the chip temperature and the system power. In this application report, a simple method of calculating power is provided to assist the design engineer with power-dissipation calculations for TI CMOS and BiCMOS FIFO products. Total power includes quiescent power and dynamic power. For most applications using CMOS and BiCMOS FIFOs, dynamic power accounts for most of the power requirement. Examples of power-dissipation calculations are provided to show the practical use of this application report. In each example, the reliability of the chip was tested against the absolute maximum power dissipation in free air. For example, the total calculated power consumption for the SN74ACT3632 and SN74ABT3614 examples resulted in 484 mW and 741 mW, respectively. These values are much less than the maximum power dissipation of the 120-pin TQFP (1606 mW) or 132-pin PQFP (1610 mW) packages in still air. I_{CC} versus frequency curves are provided in Appendix A. These graphs assist the design engineer in the search for the FIFO device with the minimum power consumption. After total power is calculated for a system, the design engineer can ensure that this value does not exceed the maximum power capability of the package type. The table of maximum power versus ambient temperature for different package options are included in Appendix B.

Acknowledgements

The author would like to express her appreciation to Kam Kittrell for his editorial comments and Al Sawyer for his assistance in providing the I_{CC} versus frequency curves in Appendix A.

Appendix A
Graphs of I_{CC} Versus Frequency

The following information is provided to assist the designer with the power-consumption calculations. Graphs of I_{CC} versus frequency are shown for the SN74ACT7803, SN74ACT7811, SN74ACT3641, SN74ACT7807, and SN74ABT7819. While the FIFOs were idle, data was taken on five units on an automatic test machine (HP 82000). Five readings were taken for each frequency and the average was used to plot the graphs. The tests were done by setting V_{IL} and V_{IH} as shown below:

V_{IL} = 0 V
V_{IH} = V_{CC} – 0.2 V

For each of the FIFOs, two graphs are provided for idle I_{CC}. One graph shows the I_{CC} versus frequency when WRTCLK is running, whereas the other graph shows the I_{CC} versus frequency when RDCLK is running. The slope of the 5-V supply voltage curve is calculated for both graphs and the largest of the two slopes is used as the power factor for power calculations.

The slopes of the I_{CCI} versus frequency graphs in the tests performed were 0.09 (SN74ACT7807), 0.12 (SN74ACT7803, SN74ACT7811), 0.2 (SN74ACT3641), and 0.28 (SN74ABT3614); therefore, if the slope of the I_{CCI} versus frequency plot is not readily available, it is appropriate to estimate the slope as 0.2.

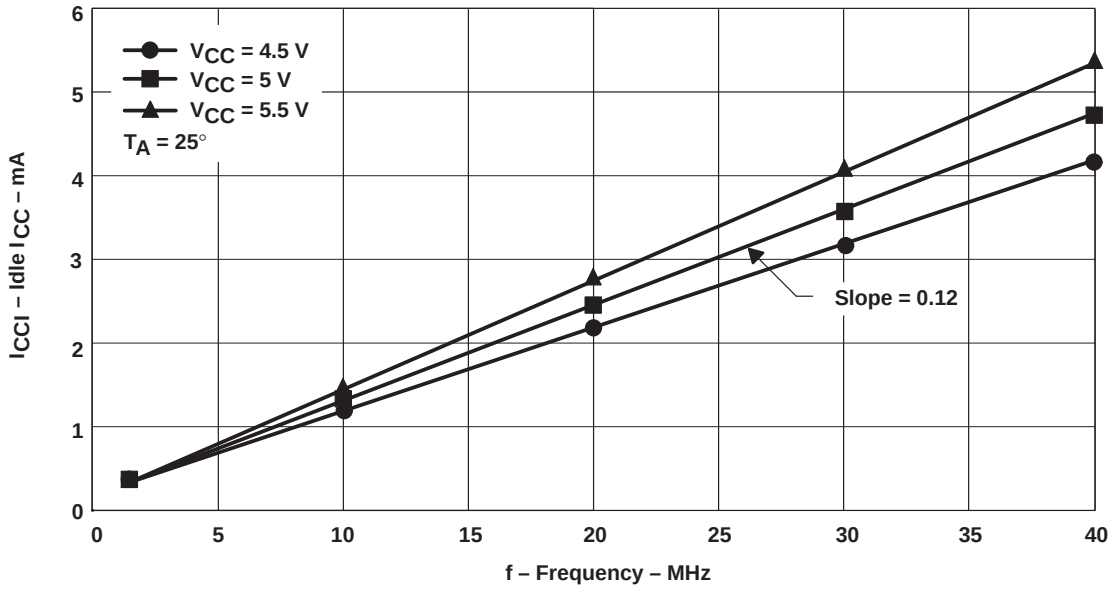

Figure A–1. SN74ACT7811 Idle I_{CC} With RDCLK or WRTCLK Switching

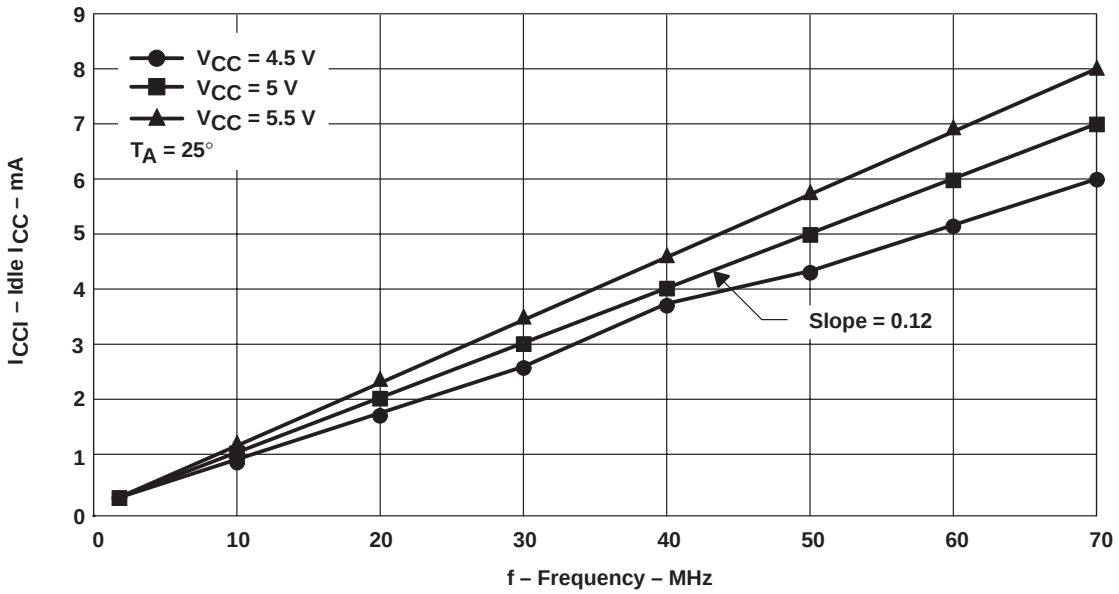

Figure A–2. SN74ACT7803 Idle I_{CC} With RDCLK or WRTCLK Switching

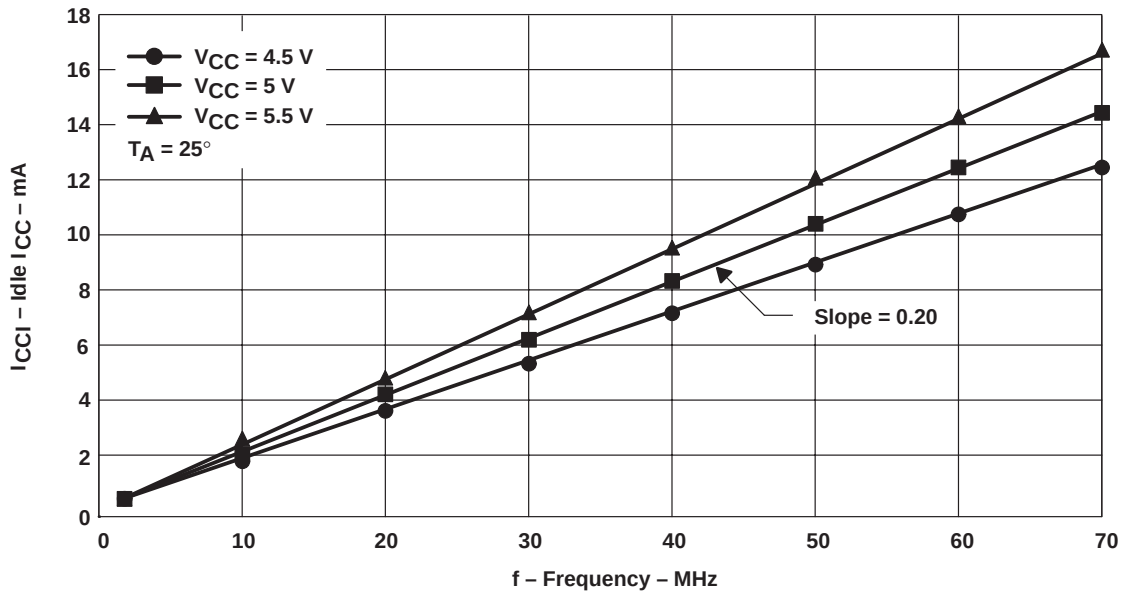

Figure A–3. SN74ACT3641 Idle I_{CC} With CLKA Switching

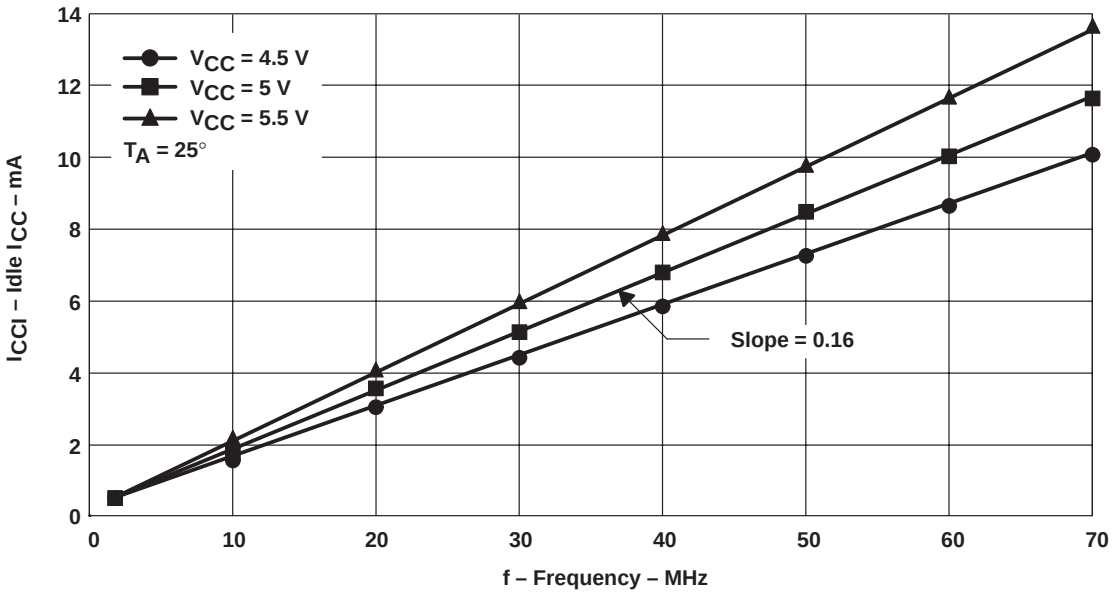

Figure A–4. SN74ACT3641 Idle I_{CC} With CLKB Switching

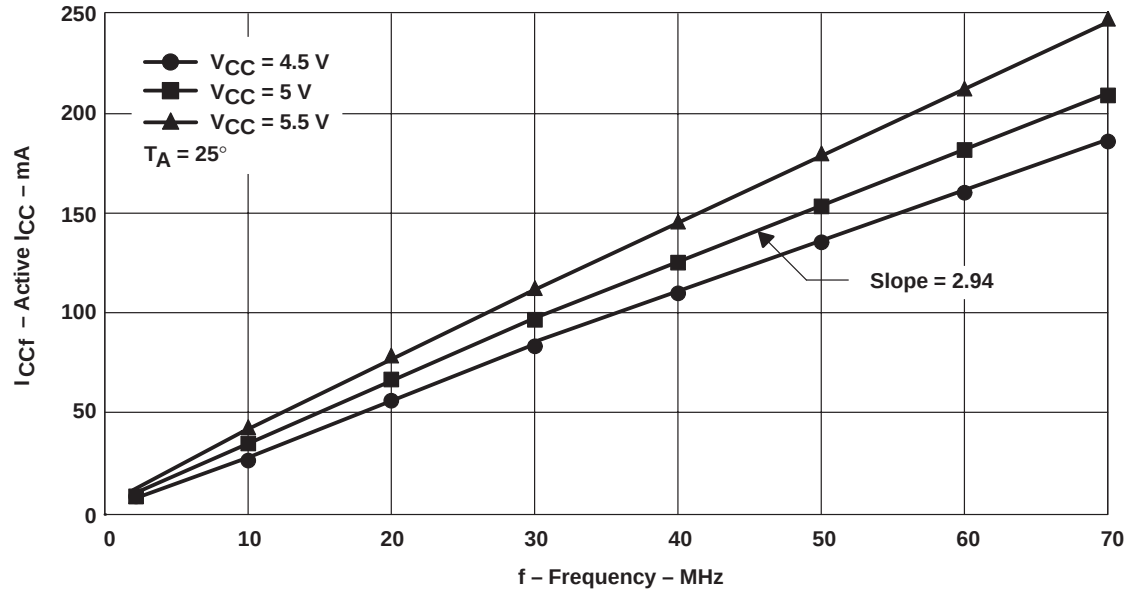

Figure A–5. SN74ACT3641 Active I_{CC} With CLKA and CLKB Switching, Simultaneous Read/Write and CLKB as Data Output

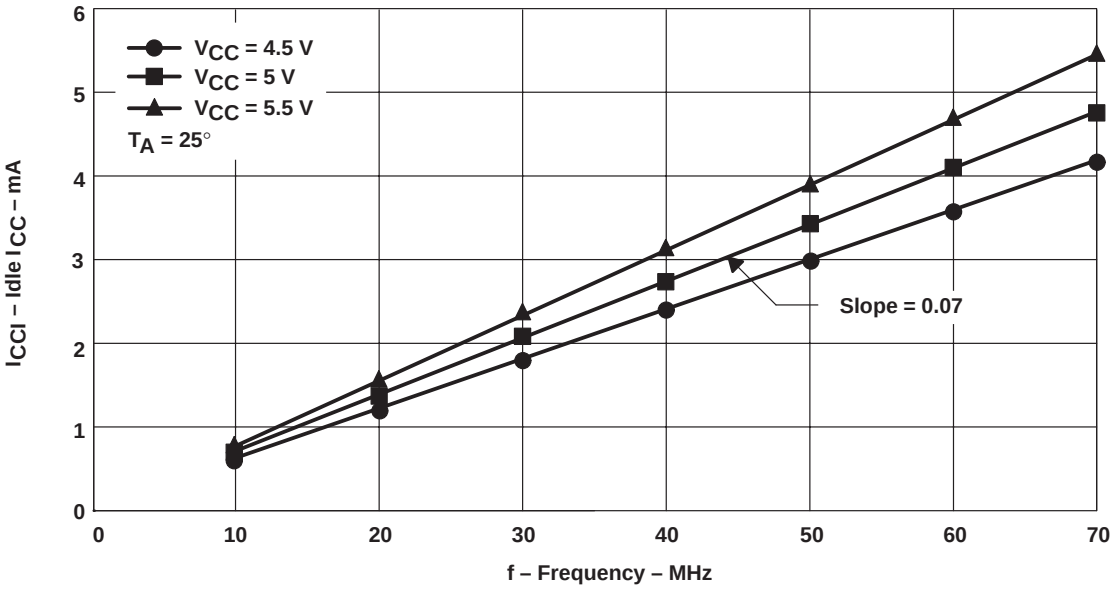

Figure A–6. SN74ACT7807 Idle I_{CC} With WRTCLK Switching, Other Inputs at 0 or V_{CC} − 0.2 V and Outputs Disconnected

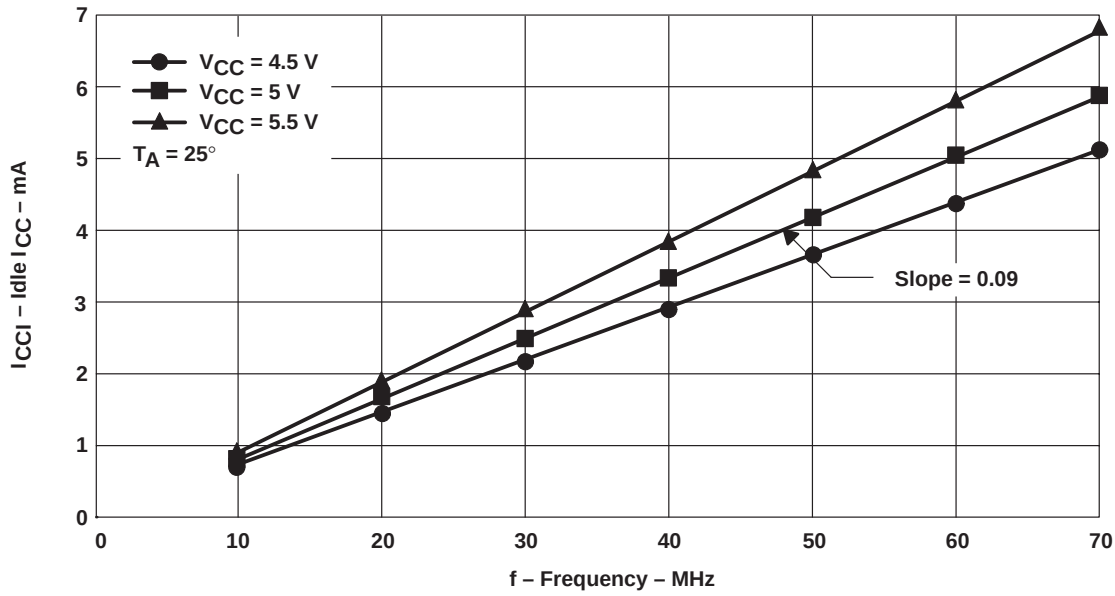

Figure A–7. SN74ACT7807 Idle I_{CC} With RDCLK Switching, Other Inputs at 0 or V_{CC} − 0.2 V and Outputs Disconnected

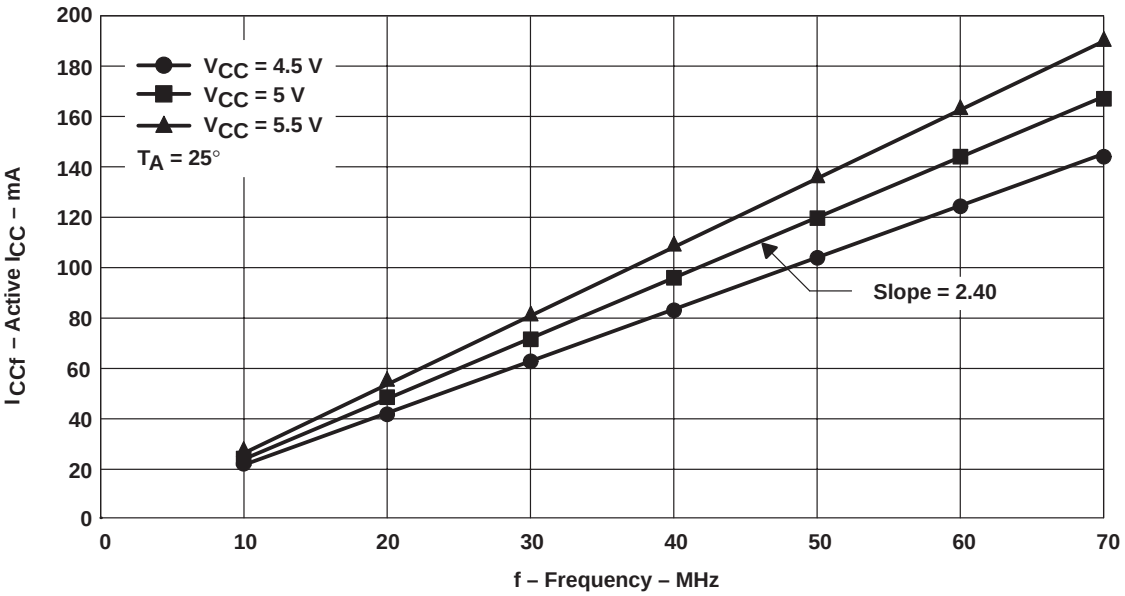

Figure A–8. SN74ACT7807 Active I_{CC} With Simultaneous Read/Write

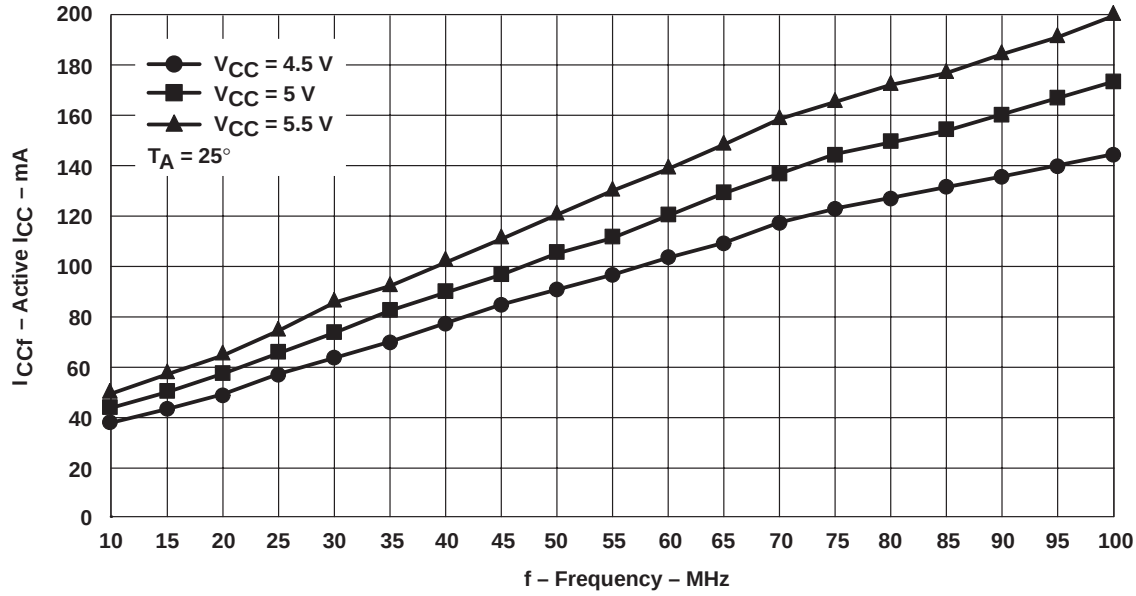

Figure A–9. SN74ABT7819 Active I_{CC} Versus Frequency

Appendix B
Maximum Power Dissipation for Different Package Types

For reliability purposes, maximum power is calculated for each package option using the following equation:

$$\text{Chip temperature} = \text{Power} \times \Theta_{JA} + T_A$$

Where:

Chip temperature = 150°C (absolute maximum chip temperature)
Θ_{JA} = thermal characteristics of a package (known)
T_A = ambient temperature (known)

Table 1 lists maximum power dissipation by package type for ambient temperature from 25°C to 90°C.

Table B–1. Maximum Power Dissipation (mW) for Packaged FIFOs

AMBIENT TEMPERATURE (°C)	25	30	35	40	45	50	55	60	65	70	75	80	85	90
PQ132 PQFP	2,515	2,414	2,314	2,213	2,113	2,012	1,911	1,811	1,710	1,509	1,509	1,408	1,308	1,207
PCB120 TQFP	2,510	2,410	2,309	2,209	2,108	2,008	1,908	1,807	1,707	1,505	1,505	1,406	1,305	1,205
PN80 TQFP	1,424	1,367	1,310	1,253	1,196	1,139	1,082	1,025	968	854	854	797	740	683
PM64 TQFP	1,351	1,297	1,243	1,189	1,135	1,081	1,027	973	919	811	811	757	703	649
PH80 PQFP	1,490	1,430	1,371	1,311	1,251	1,192	1,132	1,073	1,013	894	894	834	775	715
DL56 SSOP	1,330	1,277	1,223	1,170	1,117	1,064	1,011	957	904	798	798	745	691	638
DW28 SOIC	1,528	1,467	1,406	1,345	1,284	1,222	1,161	1,100	1,039	917	917	856	795	733
DW24 SOIC	1,420	1,364	1,307	1,250	1,193	1,136	1,080	1,023	966	852	852	795	739	682