High-Speed, High-Drive SN74ABT7819 FIFO

Teruo Ishii and Navid Madani
Advanced System Logic – Semiconductor Group

SCAA016A
March 1996

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Certain applications using semiconductor products may involve potential risks of death, personal injury, or severe property or environmental damage ("Critical Applications").

TI SEMICONDUCTOR PRODUCTS ARE NOT DESIGNED, INTENDED, AUTHORIZED, OR WARRANTED TO BE SUITABLE FOR USE IN LIFE-SUPPORT APPLICATIONS, DEVICES OR SYSTEMS OR OTHER CRITICAL APPLICATIONS.

Inclusion of TI products in such applications is understood to be fully at the risk of the customer. Use of TI products in such applications requires the written approval of an appropriate TI officer. Questions concerning potential risk applications should be directed to TI through a local SC sales office.

In order to minimize risks associated with the customer's applications, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Contents

List of Illustrations

Introduction

First-in, first-out (FIFO) memories are used as high-speed data-stream buffers for maximizing throughput between buses having different data-transfer speeds, for example, between multiprocessors or a microprocessor and peripheral circuits. Recently, the processing speed of microprocessors has become so fast that the gap between the speed of the microprocessor and peripheral circuits has widened. As a result, the demand for faster FIFOs that can maximize the use of the microprocessor capabilities has increased. Usually, when a memory integrated circuit drives a heavy-load bus line, external bus buffers are required. FIFO memories, however, help to minimize the design complexity and cycle time by providing the capability to buffer data while at the same time directly driving the bus line.

The Texas Instruments SN74ABT7819 is a high-speed, high-drive, advanced BiCMOS FIFO with operating frequencies up to 80 MHz and a drive capability of I_{OH}/I_{OL} = –12/24 mA (see Figure 1).

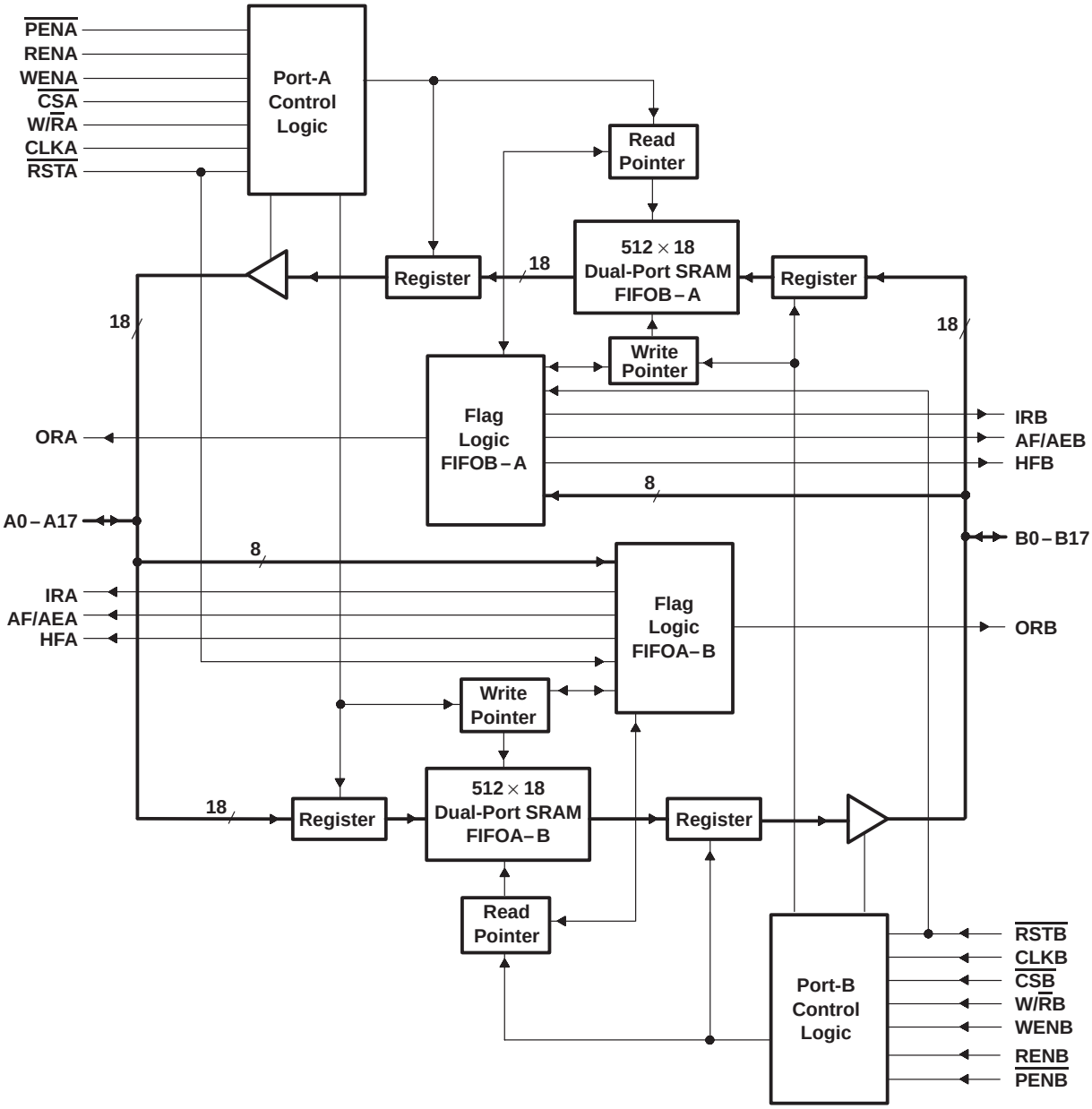


Figure 1. SN74ABT7819 Block Diagram

Structure

The SN74ABT7819 is a 512 × 18 dual-port bidirectional clocked FIFO (see Figure 1). It comprises two SRAMs (FIFOA, FIFOB), specific circuits for controlling these two SRAMs, and I/O registers. Read/write operations are carried out on the SRAMs at the low-to-high transition of their respective free-running clocks, CLKB and CLKA. Read/write operations are synchronized by independent clocks from the system. Likewise, EMPTY and FULL flags are synchronized with independent clocks from the system. Neither an external clock-enable circuit nor an external circuit for synchronizing output flags to the clocks are required. Output data is buffered by output registers and can be enabled at all times. These features facilitate design by eliminating the need for detailed timing considerations, especially in applications requiring high-speed operation.

High-Speed Performance

The SN74ABT7819-12 is a high-speed FIFO memory with an access time of 9 ns (at C_L = 50 pF). Operation is specified for free-running clock (CLKA, CLKB) inputs of up to 80 MHz. These high-speed characteristics allow microprocessor time management to be reduced and allow an efficient system to be configured. Figure 2 shows the waveform of output data read by an 80-MHz clock.

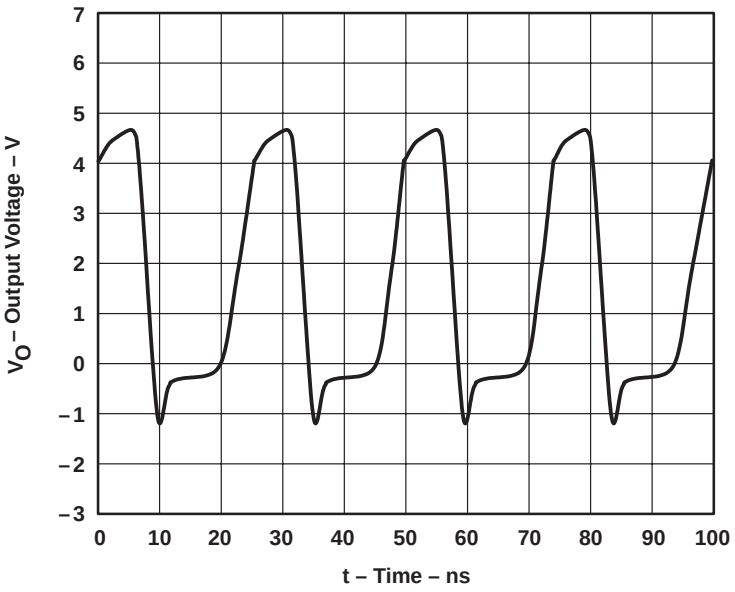


Figure 2. Output Waveform at 80-MHz Clock (C_L = 50 pF)

High-Drive Capability

The advanced BiCMOS SN74ABT7819 comprises a bipolar-output circuit that achieves a high-drive capability. Figure 3 shows the output characteristics for the SN74ABT7819. Output impedance is equivalent to about 30 Ω at high output and 50 Ω at low output. Output impedance values for the SN74ABT7819 are equivalent to the output impedance for FAST and BCT bus-interface logic; therefore, a designer can effectively implement the SN74ABT7819 as an interface to a bus line.

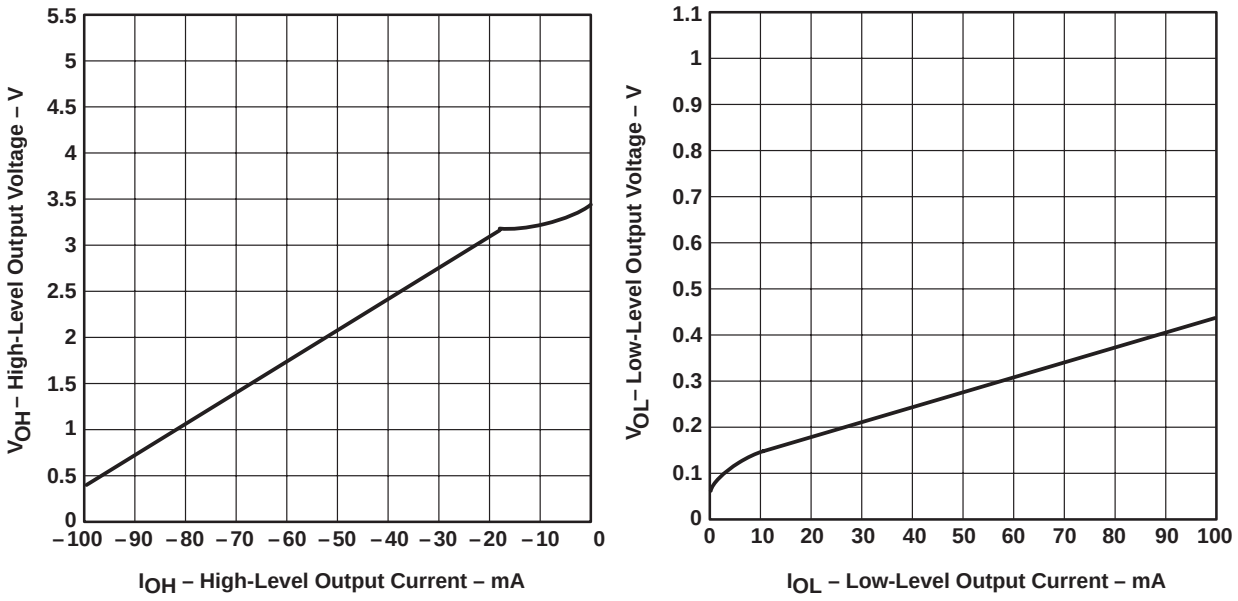


Figure 3. Output Characteristics of the SN74ABT7819 (V_{CC} = 5 V, T_A = 25°C)

Incident-Wave Switching Capability

When specific data (rectangular wave) is carried over the transmission line, data is influenced by the impedance of the transmission line, introducing distortion in the data waveforms. This distortion can cause a mismatch in required data-transfer speed; therefore, the characteristic impedance of the transmission line must be considered in the system design. The following describes the relationship between the output characteristics of the SN74ABT7819 and the transmission line.

The impedance of the transmission line and the drive capability of the device can introduce distortion in the waveforms at the low-to-high and high-to-low transition referred to as shelf voltage. The shelf voltage lowers as the impedance of the transmission line and the drive capability of the device decrease. The shelf voltage is expressed by the following equations and is shown in Figure 4.

$$V_{OHS} = \frac{Z_O}{Z_{ONH} \times Z_O} \times V_{OH} \quad \text{(a low-to-high transition)} \tag{1}$$

$$V_{OLS} = \frac{Z_{ONL}}{Z_O \times Z_{ONL}} \times V_{OH} \quad \text{(a high-to-low transition)} \tag{2}$$

Where:

V_{OHS} = Shelf voltage at the low-to-high transition (V)
V_{OLS} = Shelf voltage at the high-to-low transition (V)
V_{OH} = High output voltage of device (V)
Z_{ONH} = High output on resistance of device (Ω)
Z_{ONL} = Low output on resistance of device (Ω)
Z_O = Impedance of transmission line (Ω)

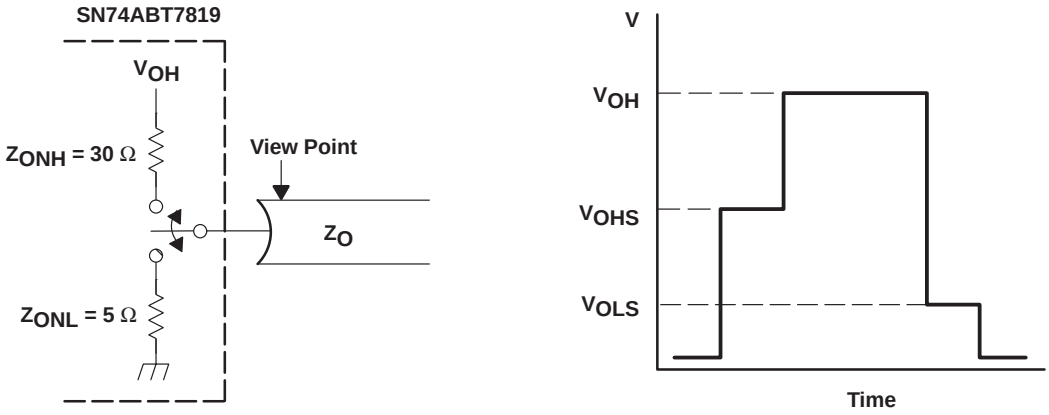


Figure 4. Shelf Voltage When Switching a Transmission Line

When a low-impedance line is driven by a device with high output resistance, the shelf voltage occurs in the threshold region, causing delay in establishing the transmitted logic. In order to drive a low-impedance transmission line without any performance degradation, a high-drive capability is required.

On the bus lines of backplanes or memories, the impedance of the transmission line drops as load capacitance is distributed over the transmission line. Generally, the characteristic impedance and the propagation delay time of the transmission line are shown by the following equations:

$$Z_O = \sqrt{\frac{L_O}{C_O}} \quad \textbf{(3)}$$

$$t_{pd} = \sqrt{C_O \times L_O} \quad \textbf{(4)}$$

Where:

Z_O = Impedance of transmission line (Ω)
L_O = Impedance per unit length (H)
C_O = Capacitance per unit length (F)
t_{pd} = Propagation delay time of transmission line (s/m)

When the load capacitance is applied on the transmission line, the characteristic impedance and the propagation delay time of the transmission line are changed as follows:

$$Z' = \sqrt{\frac{L_O}{C_O + C_l}} + \frac{Z_O}{\sqrt{1 + \frac{C_l}{C_O}}} \quad \textbf{(5)}$$

$$t_{pd}' = \sqrt{L_O \times (C_O + C_l)} = t_{pd}\sqrt{1 + \frac{C_l}{C_O}} \quad \textbf{(6)}$$

Where:

Z' = Impedance after application of capacitance (Ω)
t_{pd}' = Propagation delay time after application of capacitance (s/m)
C_l = Applied capacitance (F)

Example

The effect of loading a $Z_O = 100\ \Omega$ and $t_{pd} = 7$ ns transmission line with 8-pf loads equally spaced at 3-cm intervals is calculated in equations 7 and 8. The high- and low-output impedance necessary to drive the loaded transmission line with no settling time delay is calculated in equations 9 and 10.

From equations 3 and 4:

$$L_O = Z_O \times t_{pd} = 100 \times 7 \times 10^{-9} = 700\ \text{nH/m} = 21\ \text{nH/3cm}$$

$$C_O = t_{pd}/Z_O = 7 \times 10^{-9}/100 = 70\ \text{pF/m} = 2.1\ \text{pF/3cm}$$

Substituting for C_O in equations 5 and 6:

$$Z_O' = \frac{Z_O}{\sqrt{1 + \frac{C_l}{C_O}}} = \frac{100}{\sqrt{1 + \frac{8 \times 10^{-12}}{2.1 \times 10^{-12}}}} = 45.6\ \Omega \quad \textbf{(7)}$$

$$t_{pd}' = t_{pd}\sqrt{1 + \frac{C_l}{C_O}} = 7 \times 10^{-9}\sqrt{1 + \frac{8 \times 10^{-12}}{2.1 \times 10^{-12}}} = 15.4\ \text{ns/m} \quad \textbf{(8)}$$

The values calculated by equations 7 and 8 are $Z_O' = 45.6\ \Omega$ and $t_{pd}' = 15.4$ ns/m, respectively. The propagation delay time of the transmission line is about doubled, and the impedance of the transmission line is about halved. The output impedance required of a device to drive this transmission line without a settling time delay is calculated by the following equations:

(high-output impedance)

$$2 \le \frac{Z_O'}{Z_{ONH} + Z_O} \times V_{OH} \quad \textbf{(9)}$$

$$2 \le \frac{45.6}{Z_{ONH} + 45.6} \times 3.5$$

$$Z_{ONH} \le 34.2\ \Omega$$

(low-output impedance)

$$0.8 \ge \frac{Z_{ONL}}{Z_O' + Z_{ONL}} \times V_{OH} \quad \textbf{(10)}$$

$$0.8 \ge \frac{Z_{ONL}}{45.6 + Z_{ONL}} \times 3.5$$

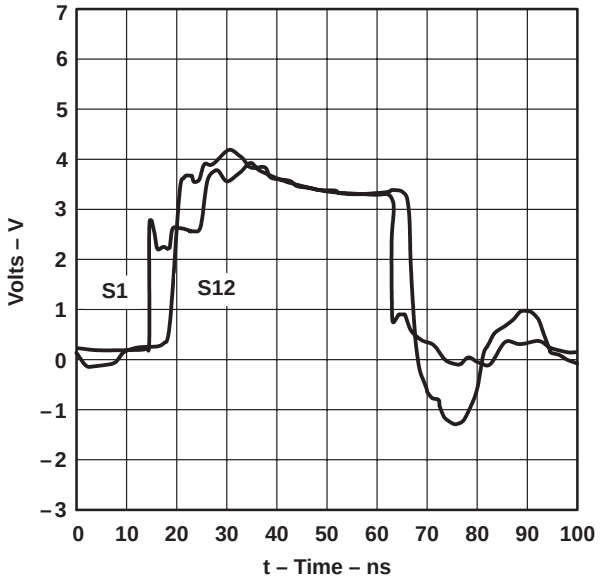
$$Z_{ONL} \le 13.5\ \Omega$$

The transmission line must be driven by a device having an output impedance of 34 Ω or less at high output and 13 Ω at low output; therefore, this transmission line can be driven with the SN74ABT7819.

VME Backplane Drive

Since the drive performance of almost all memory integrated circuits is low, it has been difficult to drive memory lines or backplane buses directly; therefore, external bus buffers have been required to interface a memory to a bus driver. Now the SN74ABT7819 allows direct driving of medium-scale bus lines.

Figure 5 shows the waveform of a 12-slot VME backplane driven by an SN74ABT7819 FIFO from the line end. Although waveform distortion caused by multiple reflection due to the 3-cm stub length and DIN connector occurs, there is no influence of reflection in the threshold region; therefore, when the SN74ABT7819 drives the VME backplane from the end, direct driving is possible. However, when the 12-slot VME bus is driven from the center, the backplane line is regarded as a branch pattern and the impedance becomes one-half the impedance at that point, resulting in generation of a step in the threshold region (see Figure 6). For this reason, a bus buffer having a higher drive capability is required.



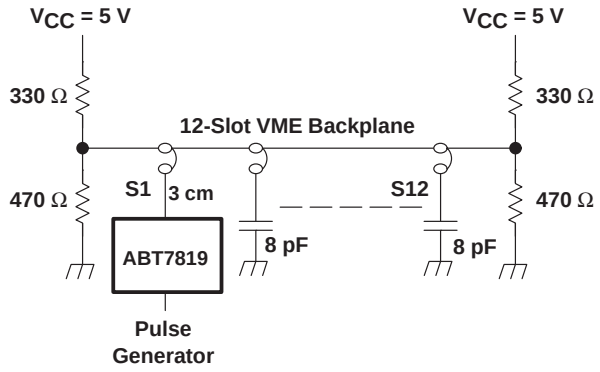
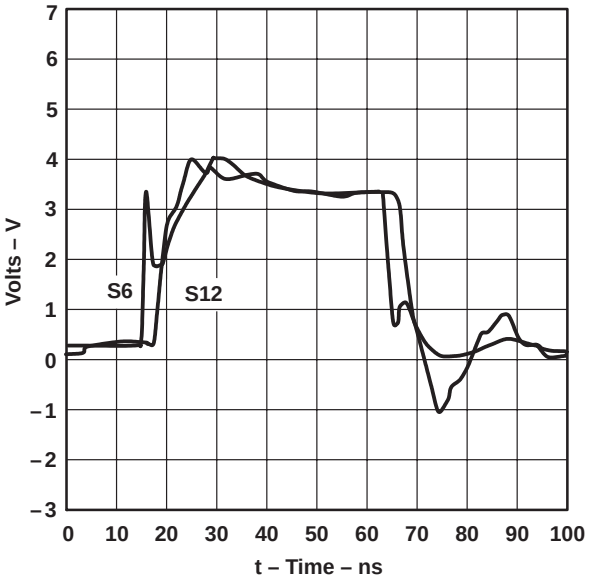


Figure 5. Backplane Driven From End



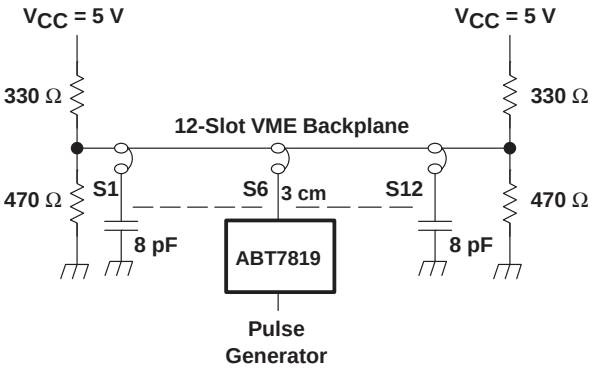


Figure 6. Backplane Driven From Center

Figure 7 shows the stepped levels when the VME bus is driven from the center slot by the SN74ABT7819. The influence of multiple reflections increases and the level of the shelf approaches the threshold region as the number of slots increases (the transmission line of the backplane is optimized corresponding to the number of slots). Based on these results, a design of five or fewer slots is preferable for driving with sufficient margin to preclude unwanted delay and possible data errors.

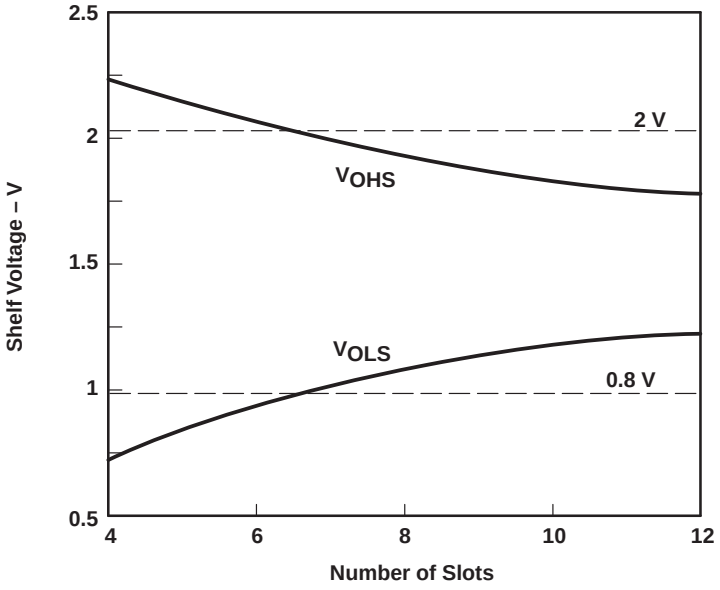


Figure 7. Number of Slots Versus Shelf Voltage (Center Drive)

Summary

The SN74ABT7819 is a high-speed, high-drive capability FIFO memory that meets the high-speed data-transfer rate requirements and drives the bus lines directly. This application report presents the essential points that a designer should consider in using a SN74ABT7819 for high-speed data transfer. The importance of drive capability and the influence of distortion is explained. Comprehending the relationship between drive capability and transmission line characteristics is essential to obtain the best performance of the SN74ABT7819.

Reference

Bus-Interface Circuits Application and Data Book, Texas Instruments Incorporated, 1990