General Application Setup for CDCFR83/CDCR83

Dung Nguyen *High-Speed Communication Control Products*

ABSTRACT

This application note describes the Texas Instruments CDCR83 and CDCFR83 clocks for Direct Rambus™ system design. The document provides general guidance on power supply, system board layout to achieve a high level of signal integrity and low clock jitter, and translating switching level for various applications. This guide is not totally exclusive to the Rambus™ application and some of the information can be applied to other PLL based clock devices.

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Introduction

The goal of this document is to give the system designer general information that can be used to meet the needs of their specific application. This document, uses schematics and simple layout drawings to demonstrate power supply decoupling and filtering. In addition, this document shows some useful techniques to improve signal quality and to reduce PLL induced jitter.

Power Supply Considerations

The CDCFR83, CDCR83 are high performance devices that operate at frequencies high enough to warrant additional attention to power supply filtering and decoupling. Certain power signals are listed below to help the designer understand their significance.

Table 1. CDCFR83, CDCR83 V_{DD} Power Supply Ranking

Reference Designator	Design Blocks of FR83, R83 Supplied by This Pin	Special Requirements	Noise Sensitivity (see Note 1)
$V_{DD}P$	Phase lock loop	The most sensitive to noise. Requires a filter network	1
$V_{DD}IR$	Voltage reference for REFCLK	Recommend a filter network.	2
$V_{DD}C$	Phase aligner	Decoupling capacitor needed.	3
$V_{DD}O$	Clock outputs	Decoupling capacitor needed. This is a very noisy signal	4
$V_{DD}IPD$	Voltage reference for phase detector and STOPB	Decoupling capacitor	4

Note 1: Noise sensitivity of 1 is most critical and of 4 is least critical.

A sample schematic that can be used as general guidance in designing a system is shown in Figure 1. The designer's physical layout depends on the noise levels on the system power bus and noise generated by adjacent components. Thus, the designer may need to take additional noise abatement actions in order to meet the system requirements.

The most critical power source is the PLL input voltage, $V_{DD}P$. This power supply must be filtered using a ferrite filter network. Low frequency noise, which is less than 2 MHz, is easily coupled into the PLL and can result in excessive jitter or false lock of the PLL. In most cases, peak-peak ripple voltage should be less than 50 mV.

The next critical source is the power supply for the reference clock, $V_{DD}IR$. This also has a great affect on the induced jitter. The reference voltage is divided by two through an internal voltage divider and then compared to the incoming clock's rising edge. If the reference voltage varies due to noise, then the reference level of comparator circuitry that looks at the clock edge clock varies, thus creating a phase distortion or jitter event.

The phase aligner circuitry is less sensitive to noise due to the slower time response of this circuitry and greater noise immunity. Therefore, the designer can use decoupling capacitors as a filtering element and to meet the power needs for these pins.

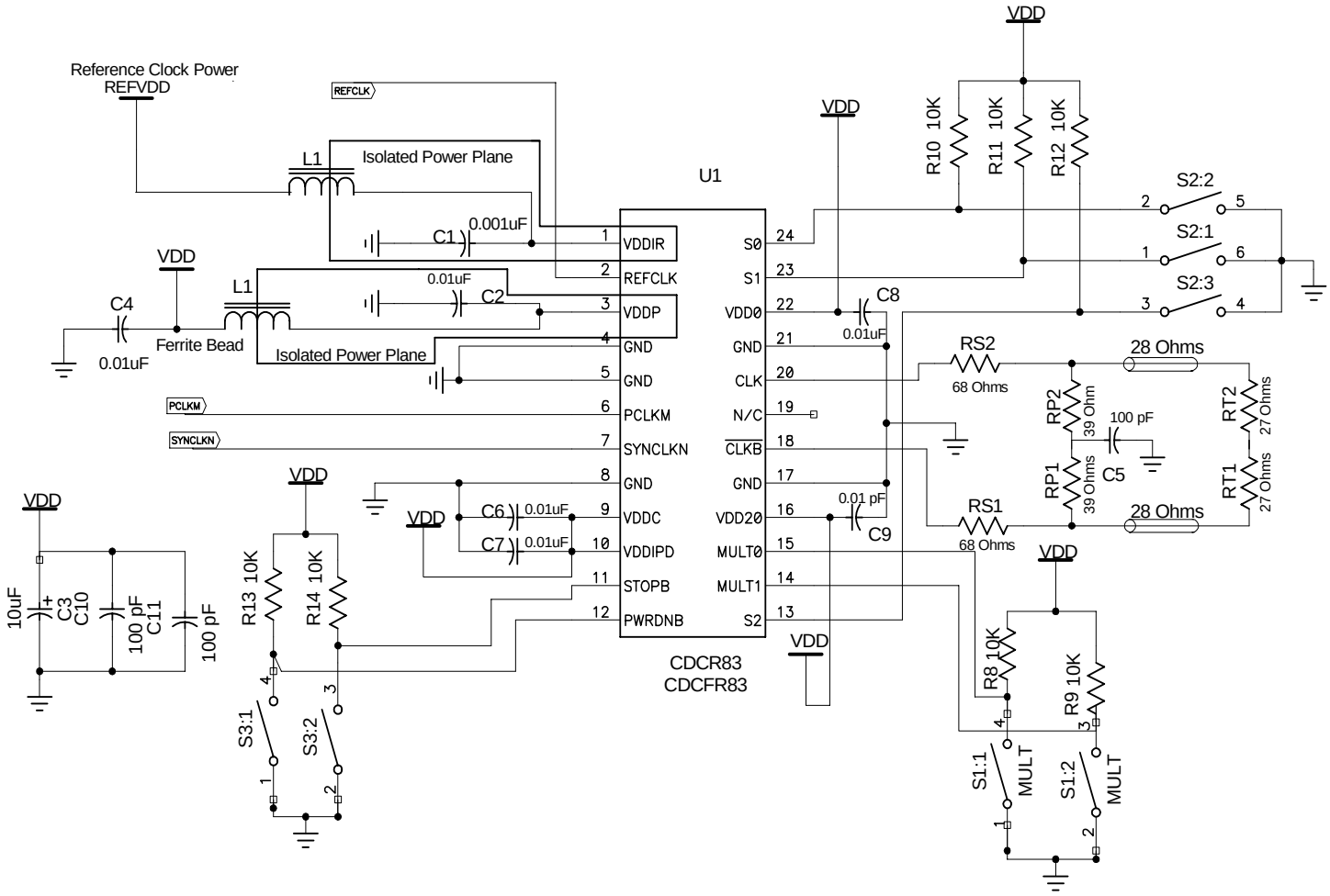

Figure 1. Example CDCR83/FR83 Schematic

In the above schematic, there is a ferrite bead on each power pin that is highly sensitive to noise according to Table 1. The purpose of this ferrite bead is to prevent translating noise from the system power supply. There are many kinds of ferrite bead from different manufacturers. We have designed several different EVM boards using a ferrite bead that has an impedance of 6 Ω at 100 MHz and they work well. The part number of the ferrite from Murate Erie that we used is BLM21B03-PT. These sensitive-to-noise power pins should have power planes that are separate from the system power plane. On each power pin, there is a 0.01-µF bypass capacitor that is used to bypass noise to GND. The capacitor should have minimum parasitic inductance and resistance. Surface mount of package size 0603 ceramic capacitor is recommended. The switch and 10-kΩ resistor on pins S0, S1, S2, STOPB, PWRDNB, MULT0, and MULT1 give the system designer an option of selecting operating frequency, power down and disable output. When the switch is turned on, the signal is pulled down to a low state. When the switch is turned off, the signal is pulled to high state via the 10-kΩ pullup resistor.

Board Layout Recommendations

The general board layout guidance below aids designers and answers questions that normally occur during the layout phase of the design. Here we address issues that are useful in preserving signal integrity and optimizing device performance.

The first layout consideration is decoupling capacitors, how to select and place them. Decoupling capacitors serve the purpose of supplying charge and filtering lower frequency harmonics. For the higher frequency harmonics, designers may wish to take advantage of the capacitance of the power to ground spacing. In general, if the power to ground spacing is 10 mils or less, the planes can be used effectively to bypass the higher frequency components of this device. In all cases, discrete bypass capacitors should be used and should be placed as close as possible to the pin they are bypassing.

The second layout consideration is noise isolation of critical parts of the device. As can be seen in Figure 1, the phase locked loop power supply (VDDP) and the supply for the reference clock (VDDIR) are critical and require special filtering. This filtering and isolation are best achieved by splitting the power planes in order to filter noise between VDD plane and VDDP plane and between VDDIR plane and REFVDD plane. The ferrite bead can be used to bridge the split planes as shown in Figure 1. Low impedance capacitors are also placed in each of the split power planes to GND to lower impedance of the return-current path from power plane to GND in order to maintain the plane for the PLL power supply and the reference clock power supply as quietly as possible.

The last layout consideration is simply maintaining the signal integrity of the clock signal as it is transmitted across the circuit board. The goal is for the clock signal that arrives at the receivers (RAM and RAC) to be essentially the same as the clock generated by the CDCR83/CDCFR83 differential drivers. The next paragraph explains the effects of reflection and methods of reducing reflections.

Vias are often necessary for connecting signals from one plane to another. If vias are necessary in a design, place them as close as possible to the driver to minimize their effects. Both vias and connectors can attenuate the higher frequency harmonics and result in rounding of the clock edges indicated by sinusoidal waveforms. Choose connectors with low inductance and adjust pad size to minimize the low pass filtering created by a pad-connector pad interface.

In addition, if a component is placed in series with a transmission line, match the component-pad width to the transmission line width to prevent impedance mismatch. Differential signals can be routed close together. Interference can occur as a result of difference in trace length or capacitance. This interference contributes to increasing clock jitter and degrading the system performance. Therefore, matching trace length and controlling spacing between differential traces are very important for signal integrity.

Finally, isolate the differential clock lines from other single-ended signals on the application board such as TTL and noisy power supply lines.

Overall, the CDCFR83/CDCR83 are high performance low jitter devices that provide optimal performance in the designer’s system.

Translating the Switching Level for Other Applications

The loading for CLK and CLKB shown in Figure 1 is typically used for Rambus applications. However, CDCR83 and CDCFR83 can also be used for other applications such as a SerDes application that requires different swing level of clock signal. Figure 2 illustrates the external circuitry needed.

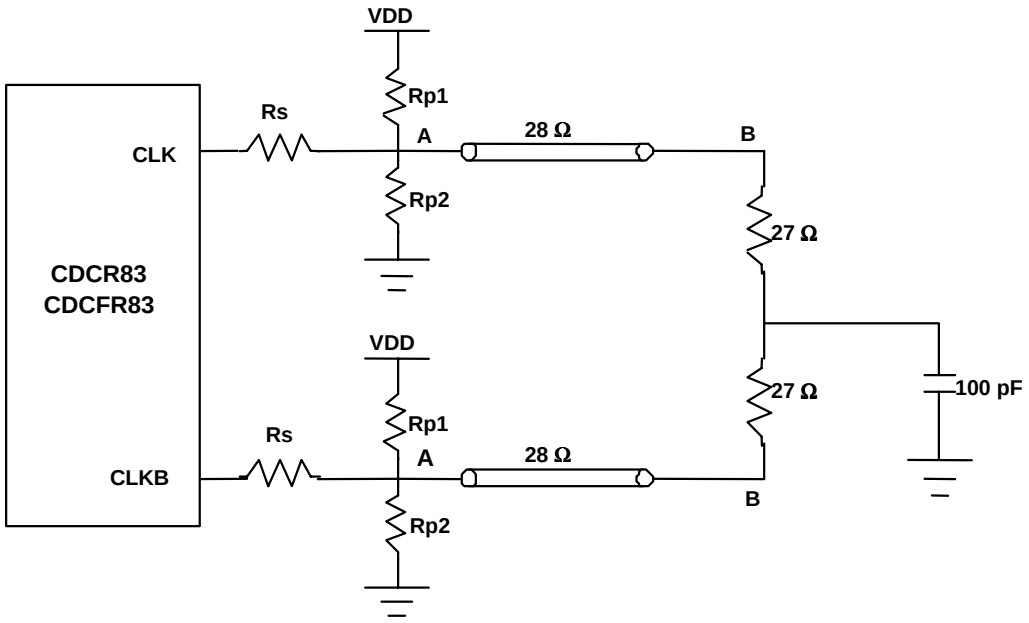

Figure 2. Example Schematic for SerDes Applications

Rs, Rp1, and Rp2 are chosen so that the parallel combination Rp1||Rp2||(Rs+Rout) is equal to the impedance of the transmission line that is 28 Ω. Rout is the output impedance of CDCR83 or CDCFR83. The parallel combination Rp1||Rp2 forms with (Rs + Rout) a voltage divider that cut the signal to a ratio of:

$$V_A = V_{CLK,CLKB} \times \frac{Rp1 \,||\, Rp2}{Rp1 \,||\, Rp2 + (Rs + Rout)} \quad (1)$$

The 27-Ω resistor at the receiver forms another voltage divider and cut the signal in half compared to the signal at node A.

$$V_B = \frac{1}{2} \times V_A \quad (2)$$

The ratio of Rp1/Rp2 is used to set the dc bias point of the clock signal. For example, in some applications of SerDes, clock signals are required to have a swing of 800 mV with Voh max of 1.8 V. However, typical swing and V_{OH} for CDCR83, CDCFR83 in Figure 1 are 500 mV and 1.75 V respectively. With Rp1 = 180 Ω, Rp2 = 91 Ω, and Rs = 33 Ω, the requirement is satisfied assuming Rout = 20 Ω. Figure 3 below is the simulation waveform probed at the 27-Ω resistor in Figure 2 when Rp1 = 180 Ω, Rp2 = 91 Ω and Rs = 33 Ω.

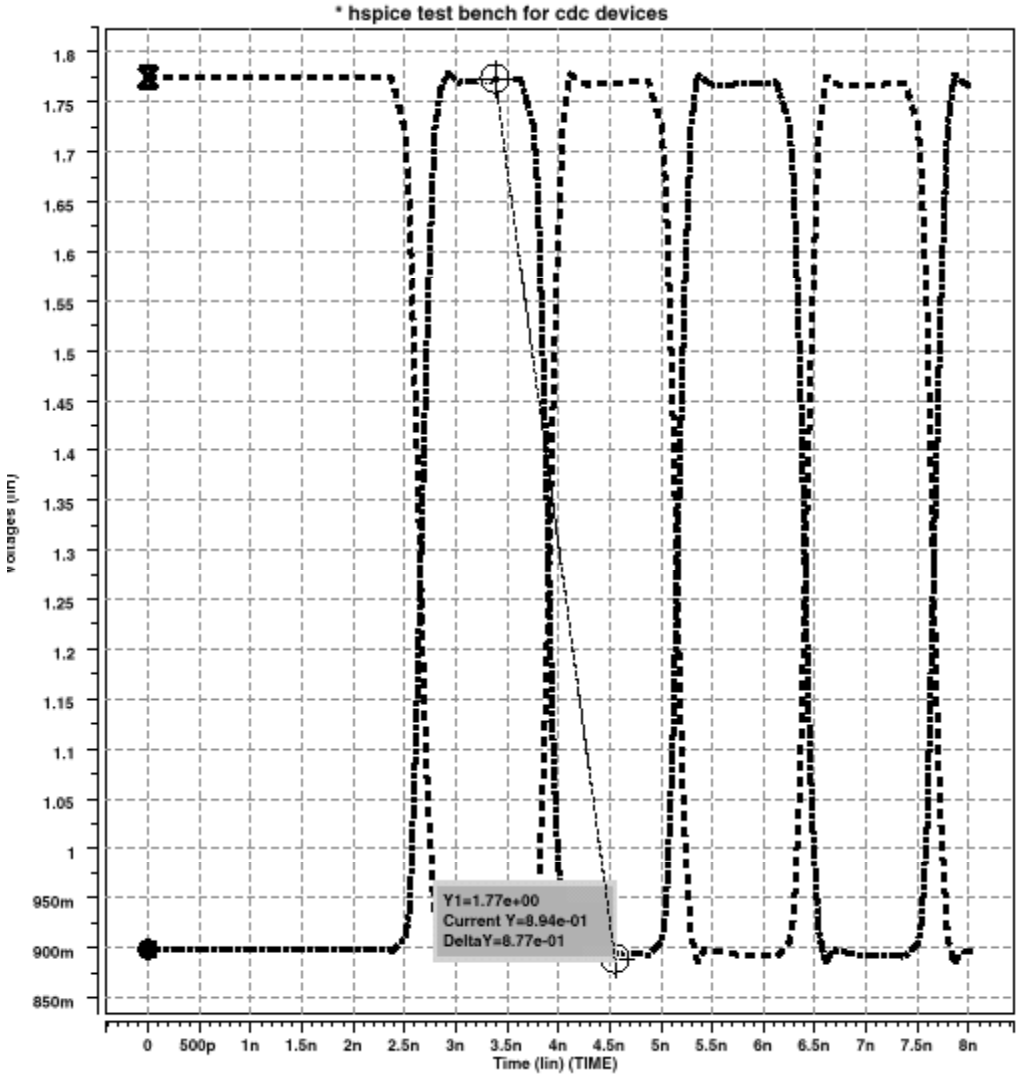

Figure 3. Hspice Waveform of Figure 2

Using CDCR83, CDCFR83 in Reduced Jitter Mode

In some applications where the phase aligner (PA) is not needed, SYNCLKN and PCLKM should be connected to GND to reduce jitter. In this case, about 15-ps jitter will be improved compared to the case of using PA. PA is usually needed in PC applications. In SerDes or consumer applications, PA is usually not needed.

References

1. *Direct Rambus™ System and Board Design Considerations*
2. This application note gives general board layout guidance and EMI considerations. http://www.rambus.com/docs/Crctdsgn.pdf
3. *Base/Concurrent Rambus™ Layout Guide*
4. This application note provides board layout details. A layout helper spreadsheet is also available which calculates PCB board parameters that meets Rambus requirements.
5. Johnson, H.W., and Gram, M. *High-Speed Digital Design*. Prentice Hall, 1993

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265