Benefits of Using TI's Non-PLL Clock Buffer: Best in Class Phase Noise/Phase Jitter and Crosstalk Performance

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ABSTRACT

This application report presents various jitter and phase noise measurements of three differential clock drivers. A Texas Instruments device was compared to two independent competitor devices. This report proves that clock buffer selection does have an impact on the total system timing budget, particularly when the system has two different input signals connected. Buffers must be able to resist the effect of crosstalk in order to stay within the timing budget. In addition, the report explains the types of jitter, their causes and recommendations on lessening their effect on timing budget.

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1 Introduction

This report presents data proving that clock buffer selection is important when designing a system with critical timing budget requirements. When working with a system that has two different input clock sources, crosstalk amplifies the need to carefully select a buffer. The test results in this report were obtained under almost ideal conditions (clean power supply, no other noise source (such as close-by ICs) near the device under test (DUT), room temperature). Note that in an actual system, jitter results would likely be higher and therefore using devices with the highest noise margin is the best choice.

The CDCLVD110 is a programmable 2.5 V, 1:10 LVDS (low voltage differential signaling) clock driver. It features dual selectable inputs through and internal MUX. The input is selected through an external pin (CLK_SEL). All measurements contained in this report were taken at room temperature. The CDCLVD110 clock buffer is characterized for industrial temperature (-40°C to 85°C) has a maximum operating frequency of 1.1 GHz.

Amongst the many applications, SONET and RF have the most stringent jitter and skew requirements and system-timing budgets are normally tight. The need for differential signaling is critical in reducing various noise components. These issues include EMI (electromagnetic interference), signal reflection, power consumption, capacitive and inductive crosstalk, and transient switching noise.

1.1 Definitions

Crosstalk, another name for parasitic coupling between signals, is the effect of capacitive coupling to cause a logic transition. Capacitive coupling is the transfer of energy between nearby switching integrated circuits. The coupling depends on factors such as the distance between the traces, the signal swing, the operating frequency, and the permittivity of the silicon dioxide. Coupling can be improved by physically increasing the distance between the traces. Power and ground planes can also act as shields to minimize crosstalk.

The timing budget is defined by dynamic (jitter) and static errors (skew). Depending on the system architecture, a sub-set of parameters out of the data sheet is only affecting the timing budget. Jitter is a timing distribution of the clock signal and expresses the edge deviation from ideal. Jitter is composed of both deterministic and random (Gaussian) content.

Jitter is any edge deviation from the ideal. The causes of jitter include: power supply noise, thermal and mechanical noise from the input signal, reflection, EMI, and random noise. A few suggestions for reducing jitter include: power supply bypassing (10 µF – 47 µF) to prevent voltage droop and ripple due to current surges, filtering each VCC pin (with 0.1 µF) low-effective series resistance capacitor, using proper termination, using differential signaling as opposed to single-ended signaling, and minimizing noise coupling by isolating other high frequency signals from the clock driver.

Period jitter is the deviation in cycle time of a signal with respect to an ideal period over a random sample of cycles. Period jitter is important since it includes the max/min frequency and it specifics the shortest clock period. It is important for the set-up and hold-time budget. Calculation with period jitter is sufficient for subsystems using clock and data signals derived by the same clock source. Use phase jitter to calculate your jitter budget in case a signal comes into such subsystem from an external clock source (e.g. use of ADC, SerDes) or is generated from the clock source that feeds the clock buffer of interest. Period jitter can be measured with any oscilloscope. The trigger input and signal input both must be driven from the output of the clock driver.

Peak-to-peak (PP) period jitter is the total jitter range from minimum to maximum values of a clock signal. PP jitter increases indefinite with recording time. Thus, PP jitter values are only meaningful if either the recording length or the relative bit error rate is known.

RMS period jitter is one standard deviation (1σ) of the PP jitter of a clock signal. RMS jitter is only valid for Gaussian (Normal) distribution. RMS jitter is independent of the sampling window, and thus, better suited to compare performance of two or more devices where sampling time window differs or is unknown.

Cycle-to-cycle (CC) period jitter (e.g., adjacent cycle jitter) is the variation in cycle time of a signal between consecutive cycles, over a random sample of successive cycle pairs. CC jitter is also a good value to calculate the setup and hold-time budget since it defines the min/max variation of the timing variation from ideal for the next clock edge.

Phase jitter or accumulated jitter is the absolute deviation of a clock edge from its ideal position in timing. While Period jitter only accounts the variation between clock periods, Phase jitter accumulates the error of each period and therefore is always bigger. The wider the recording time window is, the more frequency bandwidth becomes integrated into the total phase jitter. Phase jitter can also be measured by integrating phase noise over the frequency band of interest. Either way, the system designer must specify the minimum and maximum frequency for the integration.

For setup and hold-time budget calculation, the PP value of the phase jitter is important. Note that only the added phase noise by the clock driver is of interest to find the worse edge position between the master clock in the system and the subsystem. The absolute phase jitter of the master clock itself adds to all clock signals in the system, thus canceling its effect.

1.1.1 ADC and SerDes System

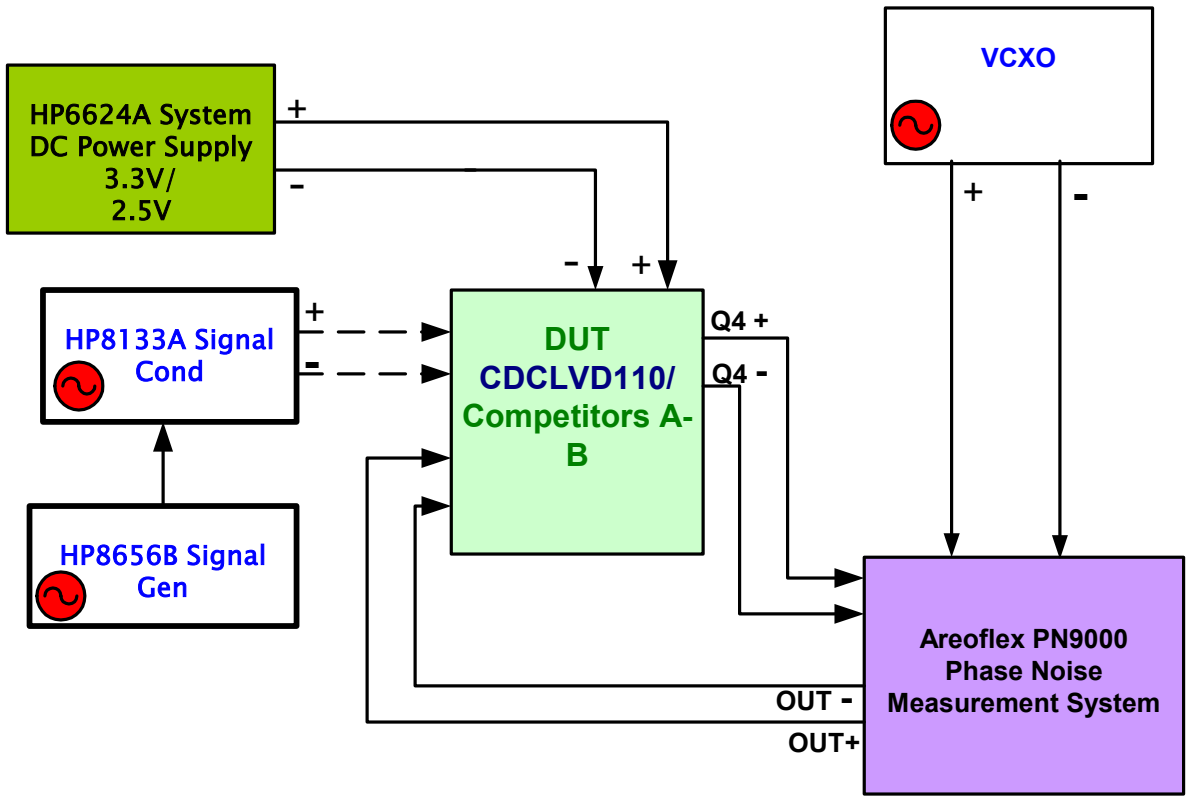
When using an AD converter and SerDes transceiver, the incoming data are often sourced by a completely independent clock source and not synchronized to the main system clock (at least no short-term synchronization). Thus, the absolute phase jitter becomes important. A lower frequency band limit must be established (e.g., 12 kHz to full range). For AD converter, the limit on the low side relates to the sampling window of the ADC that becomes further processed by digital algorithms (e.g. DSP tap size for a FFT). For a SerDes PLL, low Phase jitter is critical around the PLL's bandwidth. Thus jitter frequency has an upper and low limit (e.g., 12 kHz - 20 MHz for OC48).

Phase jitter can be measured with any oscilloscope. The trigger input must be fed by the clock signal driving the clock buffer under test, while the scope signal input must be driven from the output of the clock buffer under test.

Phase Noise (PN) is the short-term instability caused by variation of frequency (phase) of a signal referenced to the carrier level and a function of the carrier offset (i.e., relative noise level within a 1-Hz bandwidth). Integration of PN over a given frequency band yields phase jitter RMS.

1.2 Test Setup

The block diagrams of the test setup are shown in Figure 1 and Figure 2. At frequencies between 50 MHz and 622.08 MHz he clock source for the Tektronix 694C real time oscilloscope and the Tektronix 11801C digital sampling scope was provided by HP8696B, conditioned by HP8133A. At frequencies of 1GHz or above the HP8133A provided the signal. A VCXO served as the clock source for the AeroFlex PN9000.



Note: Dotted line indicates additional setup for crosstalk measurements.

Figure 1. Test Setup for Phase Jitter Measurements Taken From AeroFlex PN9000

The phase noise measurements were taken by the AeroFlex PN9000 phase noise measurement system using the added phase noise measurement technique. A 622.08-MHz VCXO was used as the low-noise floor frequency source. The PN9000 equipment noise floor allows for measurements as sensitive as -160 dBc and is capable of measuring -60 dBc below the VCXO, enabling it to accurately measure the noise contributed by the buffer.

The crosstalk measurements were taken with a second input signal in addition to the previous setup. The second input signal was provided by the HP8656B at 622.18 MHz. The input pair fed by the VCXO was selected through the clock select pin CLK_SEL on each device.

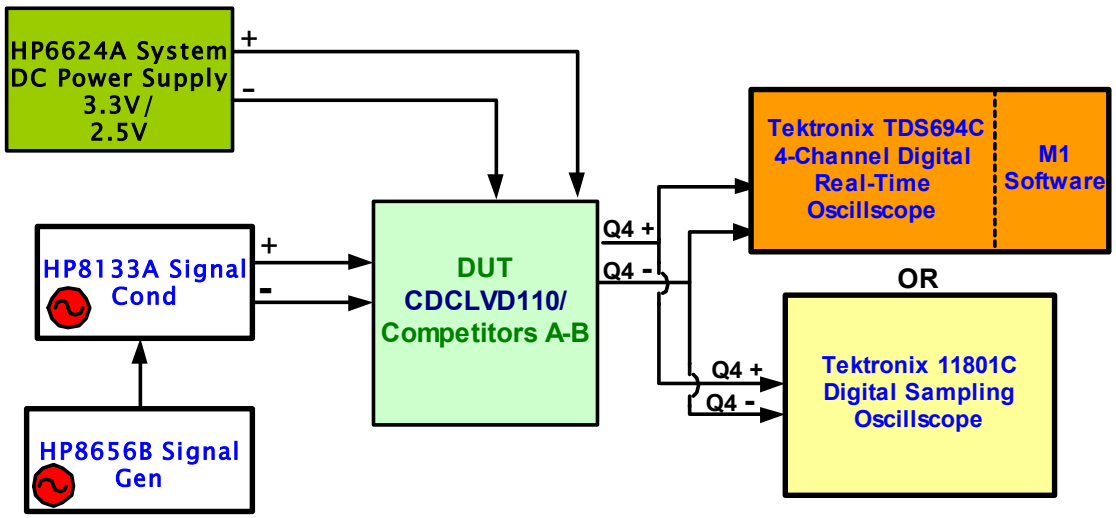


Figure 2. Test Setup for Jitter Measurements Taken From Tektronix TDS694C and 11801C

For both oscilloscope setups, the frequency source was the HP8656B signal generator via the HP8133A for frequencies below 1 GHz. Above 1 GHz, the HP8133A alone served as the signal source. Thus, the signal input into each oscilloscope is a combination of source noise and added clock buffer noise.

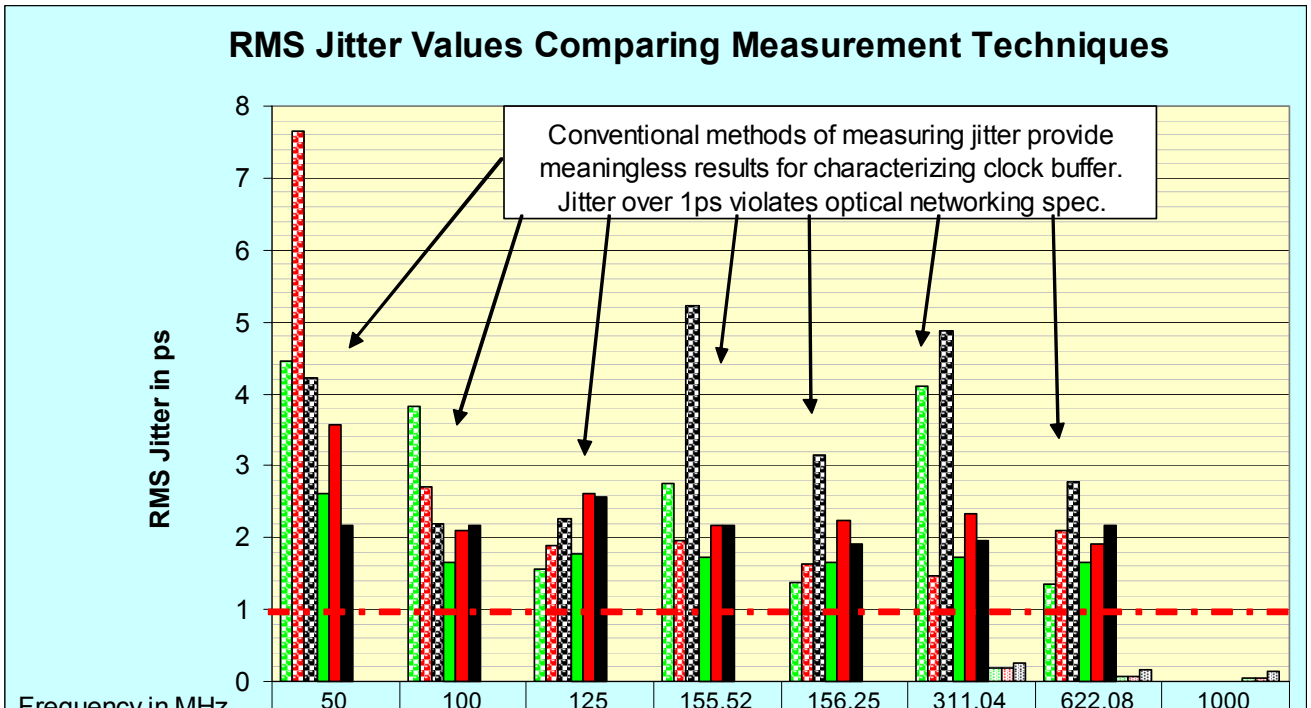
The Tektronix 11801C digital sampling oscilloscope was used to take both PP period jitter and RMS jitter measurements. The peak-to-peak measurements were obtained from a 700,000 hit plot. The RMS measurements were taken from a 0.4-mV section of a 20,000 hit plot.

The Tektronix 694C was used to measure PP, CC, and RMS jitter of the devices. It was connected through GPIB to a PC with Amhorst M1™ software, which gave the jitter measurements.

2 Measurement Data

2.1 Measurement Systems Compared

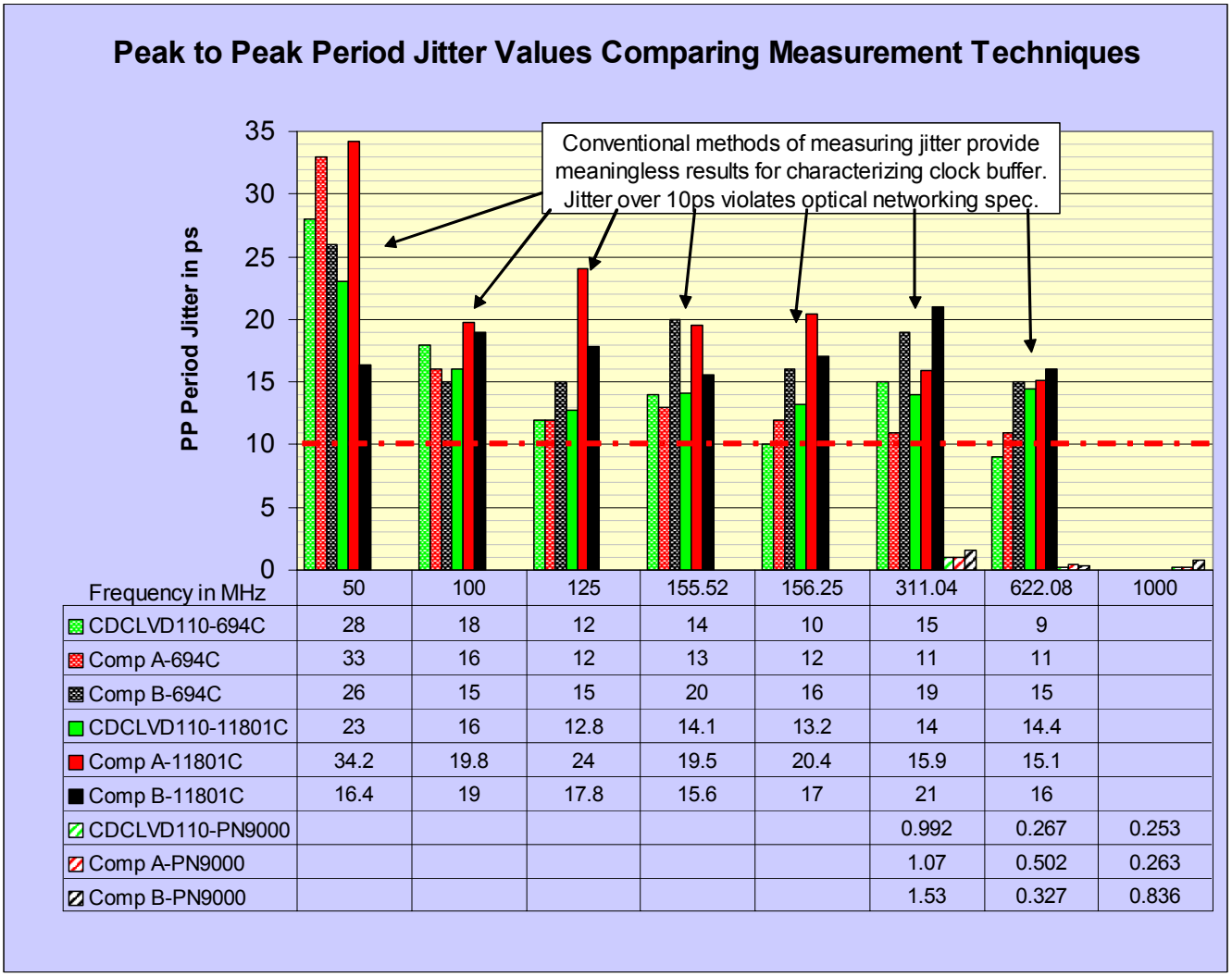
Most existing measurement methods of quantitatively measuring RMS jitter do not have the ability to exclude the noise given by the source. Furthermore, most test equipment has an equipment noise floor higher than the noise created within a clock buffer and therefore is not sufficient to measure noise created by a clock. The varying results shown in Figure 3 indicate that the measurement systems used for the testing are not all of equal reliability. Only the PN9000 is capable of differentiating between the buffer and the noise floor, while the other measurement systems have noise floors that exceed that of the buffer. The results from the PN9000 show that CDCLVD110 has consistently the lowest noise floor at the tested frequencies. The CDCLVD110 causes the least amount of jitter from input to output and therefore is the best choice to meet the total timing budget requirements. Note that the PN9000 is calibrated to measure at frequencies only above 250 MHz.



Frequency in MHz	50	100	125	155.52	156.25	311.04	622.08	1000
CDCLVD110-694C	4.457	3.823	1.557	2.747	1.373	4.11	1.343	
Comp A-694C	7.643	2.71	1.89	1.953	1.64	1.477	2.093	
Comp B-694C	4.21	2.193	2.257	5.22	3.14	4.87	2.777	
CDCLVD110-11801C	2.62	1.66	1.77	1.72	1.66	1.72	1.65	
Comp A-11801C	3.58	2.09	2.61	2.16	2.23	2.34	1.92	
Comp B-11801C	2.17	2.18	2.56	2.18	1.92	1.95	2.16	
CDCLVD110-PN9000						0.177	0.062	0.055
Comp A-PN9000						0.188	0.064	0.055
Comp B-PN9000						0.267	0.165	0.149

Figure 3. RMS Jitter Values Compared Among Three Different Test Setups

The only trustworthy results in Figure 4 are taken by the PN9000, as it is capable of excluding the source noise from the noise measurement of the DUT. The data shows that the CDCLVD110 also has the lowest PP period jitter, contributing an amount insignificant to the timing budget. Note that the PN9000 is calibrated to measure at frequencies only above 250 MHz.

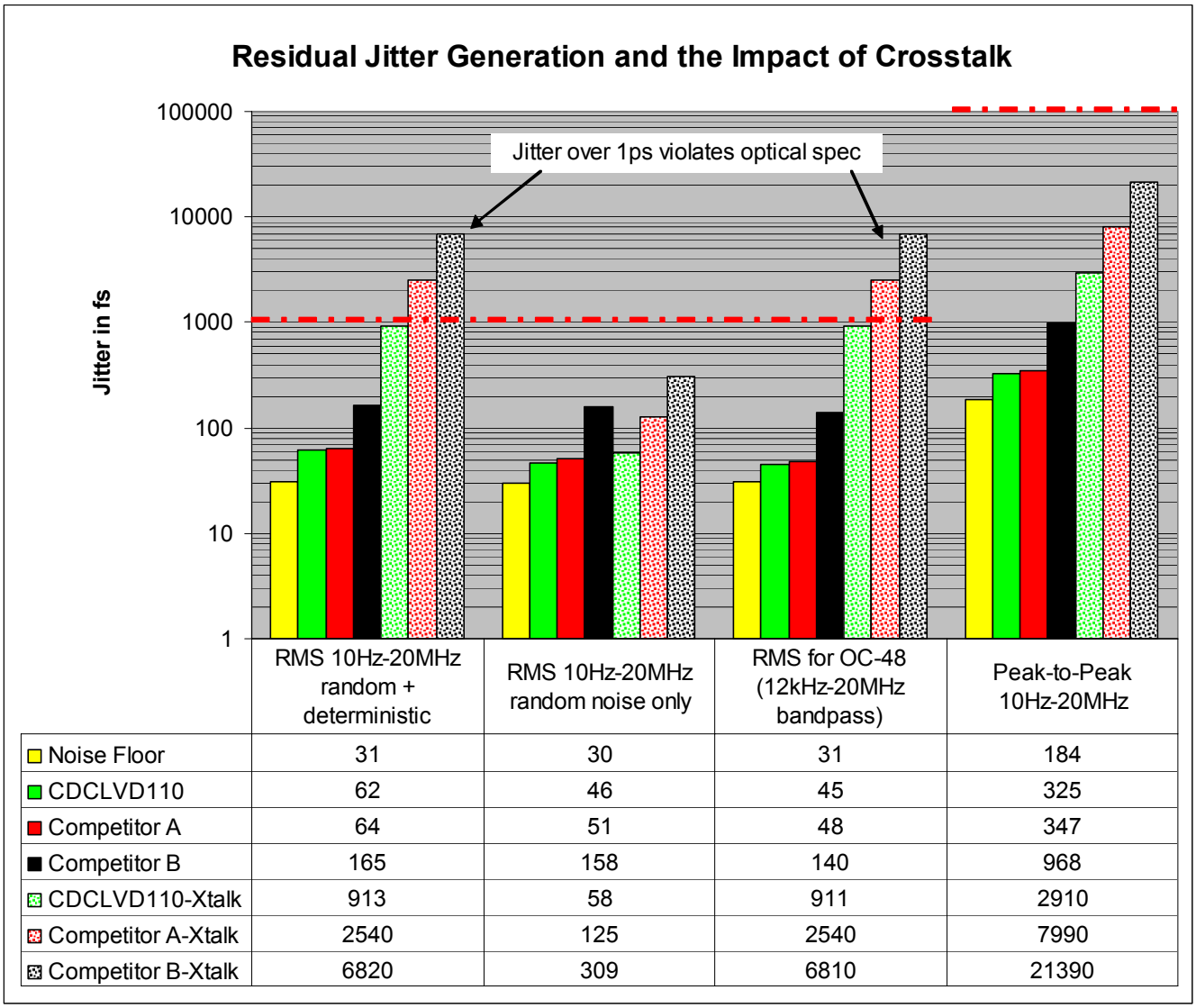


Frequency in MHz	50	100	125	155.52	156.25	311.04	622.08	1000
CDCLVD110-694C	28	18	12	14	10	15	9	
Comp A-694C	33	16	12	13	12	11	11	
Comp B-694C	26	15	15	20	16	19	15	
CDCLVD110-11801C	23	16	12.8	14.1	13.2	14	14.4	
Comp A-11801C	34.2	19.8	24	19.5	20.4	15.9	15.1	
Comp B-11801C	16.4	19	17.8	15.6	17	21	16	
CDCLVD110-PN9000						0.992	0.267	0.253
Comp A-PN9000						1.07	0.502	0.263
Comp B-PN9000						1.53	0.327	0.836

Figure 4. Peak-to-Peak Period Jitter Compared Among Three Different Test Setups

2.2 PN9000 Results

The measurements displayed in Figure 5 were taken using the PN9000 with a 622.08-MHz VCXO as the signal source. Although all three devices meet the < 1ps RMS jitter required by optical specifications, when a second input frequency is introduced the results change. As shown in Figure 5, the CDCLVD110 is the least susceptible to crosstalk and therefore the only one of the three devices tested that does not violate the 1-ps RMS jitter spec for total RMS jitter and RMS for OC-48.



	RMS 10Hz-20MHz random + deterministic	RMS 10Hz-20MHz random noise only	RMS for OC-48 (12kHz-20MHz bandpass)	Peak-to-Peak 10Hz-20MHz
Noise Floor	31	30	31	184
CDCLVD110	62	46	45	325
Competitor A	64	51	48	347
Competitor B	165	158	140	968
CDCLVD110-Xtalk	913	58	911	2910
Competitor A-Xtalk	2540	125	2540	7990
Competitor B-Xtalk	6820	309	6810	21390

Figure 5. PN9000 Phase Jitter Measurements

Figure 6 presents the PN plots of the three devices tested and the noise floor. The plots were taken by the PN9000 using a 622.08-MHz VCXO as the signal source. As can be seen from Figure 6, the CDCLVD110 has the lowest PN plot of all three devices and is limited at higher frequencies by the noise floor of the measurement system.

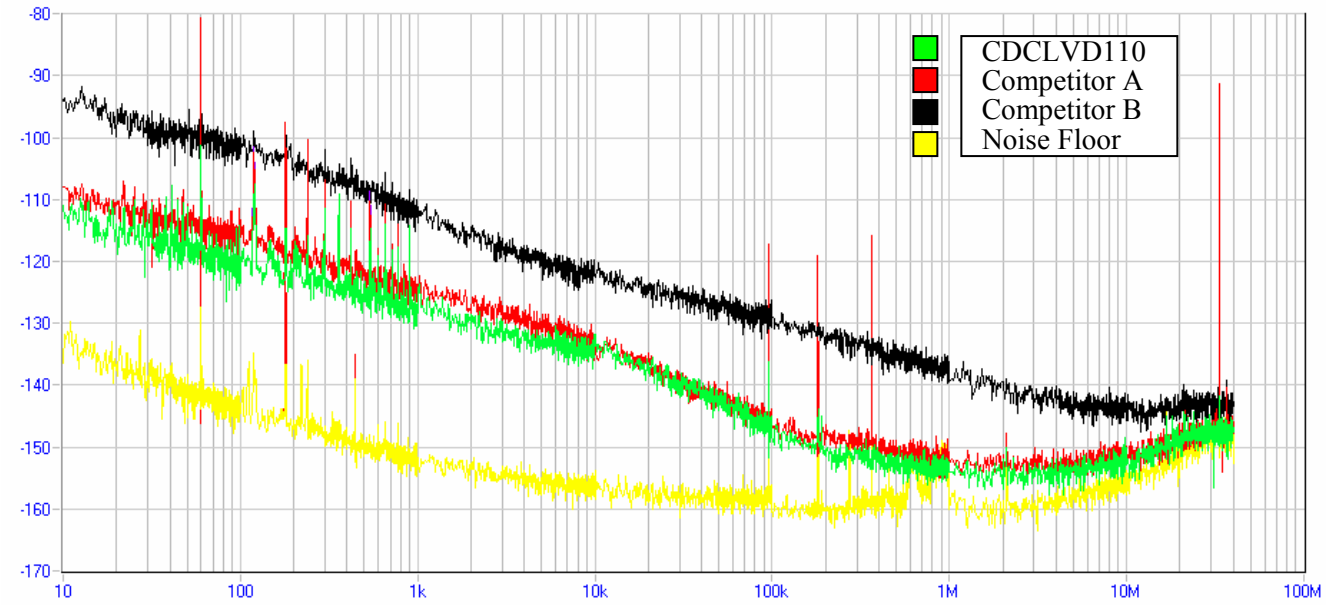


Figure 6. Phase Noise Comparison at 622.08 MHz

When the effect of crosstalk is introduced, as shown in Figure 7, the CDCLVD110 offers again the best phase noise performance amongst the 3 devices under test. The devices were each fed two different signals: the first and selected signal was from the 622.08-MHz VCXO, the second from the HP8656B at 622.18 MHz (100-kHz offset). The spikes in the plots are due to the 0.1 MHz difference between the two input signals and thus are primarily seen at 100-kHz intervals.

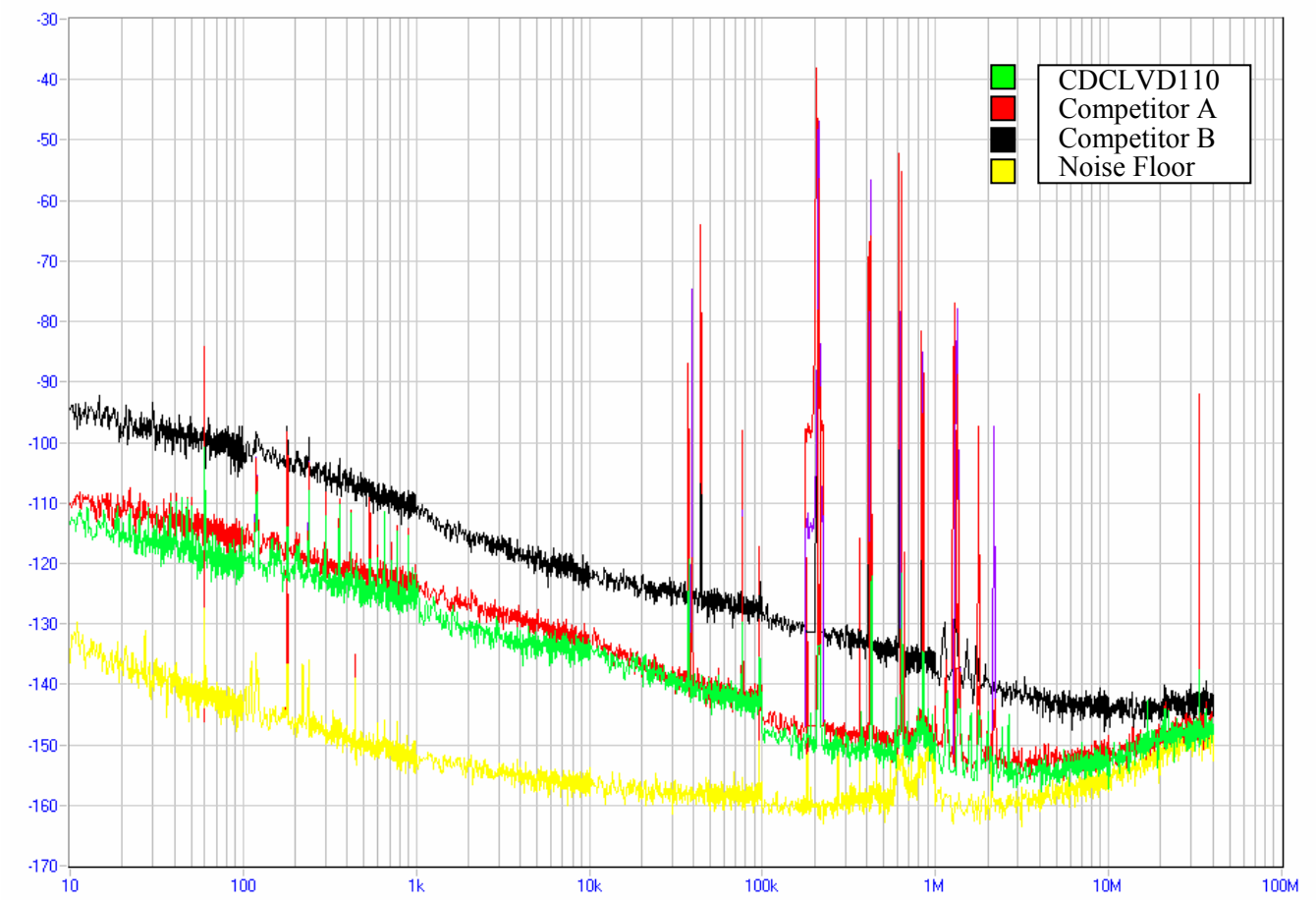


Figure 7. Crosstalk Phase Noise Comparison at 622.08 MHz

3 Summary

While there are numerous jitter measurement systems available, they do not all measure with the same accuracy. The data presented in this report included three different jitter measurement systems. It is evident from the test results that the PN9000 provides the most dependable measurements of the three systems.

When choosing a clock buffer for a system with a timing budget requirement, the choice must be made carefully. It may appear that buffers do not have a significant amount of jitter, but when using two inputs the crosstalk must be considered. The CDCLVD110 causes less jitter than its competitors, and is also least susceptible to crosstalk.

The test conditions must be considered when evaluating data. The data collected through the test setups are likely the best possible results achievable. Real systems based on multiple ICs spaced closely to each other and powered by the same power supply may create more noise and worsen the jitter budget. In addition, the jitter measurements taken with the introduction of crosstalk indicate how susceptible the device is to crosstalk. In an actual system the device would be subject to power supply fluctuations, noise from nearby ICs, and other variables, all of which compromise the performance of the clock buffers. The CDCLVD110 is the most favorable choice to meet total system timing budget, as it is the only device of the three tested that meets the <1ps RMS optical networking specification when crosstalk is taken into account. Ultimately, the designer is still responsible for minimizing the noise floor of his/her system.

4 Appendix A

Table 1. Output Jitter of CDCLVD110 Measured by M1 Software Program

Jitter (in ps)				
Frequency (MHz)	**PP**	**C-C(+)**	**C-C(-)**	**RMS**
50	25	17	18	4.3
	28	20	21	4.64
	27	25	17	4.43
100	17	15	14	4.25
	18	17	15	3.84
	18	18	16	3.38
125	11	10	10	1.54
	10	8	7	1.43
	12	11	11	1.7
155.52	14	12	13	2.82
	14	13	13	2.7
	13	10	12	2.72
156.25	8	8	8	1.36
	9	9	8	1.37
	10	8	9	1.39
311.04	15	15	13	4.09
	15	15	14	4.12
	15	14	15	4.12
622.08	9	8	8	1.36
	9	9	8	1.32
	9	8	8	1.35

Table 2. Output Jitter of Competitor A Measured by M1 Software Program

Jitter (in ps)				
Frequency (MHz)	**PP**	**C-C(+)**	**C-C(-)**	**RMS**
50	30	25	25	7.16
	31	27	28	7.98
	33	27	32	7.79
100	16	15	14	2.88
	14	12	11	2.27
	14	13	12	2.98
125	12	12	11	1.75
	12	9	11	1.91
	11	10	11	2.01
155.52	12	11	9	1.95
	12	11	11	1.93
	13	10	11	1.98
156.25	12	11	9	1.59
	12	12	9	1.65
	11	11	9	1.68
311.04	11	10	10	1.52
	11	9	10	1.45
	10	9	9	1.46
622.08	11	10	10	2.1
	11	10	11	2.09
	11	11	11	2.09

Table 3. Output Jitter of Competitor B Measured by M1 Software Program

Jitter (in ps)				
Frequency (MHz)	**PP**	**C-C(+)**	**C-C(-)**	**RMS**
50	23	20	21	4.24
	25	18	19	4.17
	26	20	18	4.22
100	12	10	10	2.01
	15	12	12	2.4
	14	12	13	2.17
125	13	11	11	2.09
	15	13	12	2.49
	13	11	12	2.19
155.52	20	19	18	5.24
	20	18	19	5.3
	20	18	18	5.12
156.25	16	14	14	3.2
	15	14	13	2.96
	16	14	13	3.26
311.04	19	17	18	4.89
	18	18	17	4.85
	18	17	17	4.87
622.08	15	14	13	2.8
	15	13	13	2.74
	15	14	13	2.79

Table 4. Output Jitter of CDCLVD110 Measured by Tektronix 11801C

Jitter (in ps)		
Frequency (MHz)	**PP**	**RMS**
50	23	2.62
100	16	1.66
125	12.8	1.77
155.52	14.1	1.72
156.25	13.2	1.66
311.04	14	1.72
622.08	14.4	1.65

Table 5. Output Jitter of Competitor A Measured by Tektronix 11801C

Jitter (in ps)		
Frequency (MHz)	**PP**	**RMS**
50	34.2	3.58
100	19.8	2.09
125	24	2.61
155.52	19.5	2.16
156.25	20.4	2.23
311.04	15.9	2.34
622.08	15.1	1.92

Table 6. Output Jitter of Competitor B Measured by Tektronix 11801C

Jitter (in ps)		
Frequency (MHz)	**PP**	**RMS**
50	16.4	2.17
100	19	2.18
125	17.8	2.56
155.52	15.6	2.18
156.25	17	1.92
311.04	21	1.95
622.08	16	2.16

5 References

1. CDCLVD110 data sheet, Texas Instruments, (SCAS684)
2. *Clock Distribution Circuits (CDC)*, Texas Instruments CDC Data Book, (SCAD004)
3. *DC-Coupling Between Differential LVPECL, LVDS, HSTL, and CML*, Texas Instruments application report, (SCAA062)
4. *AC-Coupling Between LVPECL, LVDS, CML, and HSTL*, Texas Instruments application report, (SCAA059)

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