Using the CDCE62005 as a Frequency Synthesizer

Madhu Balasubramanian *Serial Link Products*

ABSTRACT

This application report is a general guide for using the CDCE62005 from Texas Instruments as a frequency synthesizer. This report explains the methods to work with the phase-locked loop of the CDCE62005 for achieving multiple output frequencies from any input frequency. It also describes the basic functionalities and methods for using the device efficiently, and discusses the clock termination method, decoupling the power-supply network, and several general applications.

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1 Introduction

A phase-locked loop (PLL) is a closed-loop system that generates a signal related to the frequency and phase of an input reference signal. It typically involves locking its output (derived from a high-Q device) to its input, which is generally derived from a low-Q device. The PLL responds to variations in frequency and phase of the input by automatically raising or lowering the frequency of the controlled oscillator through feedback, until the output is aligned in phase and frequency of the system. A practical phase PLL usually ensures lock in phase, but a lock in frequency with a 0-ppm error has not yet been demonstrated. Typical commercial PLLs demonstrate ensured frequency lock, but only with a margin of error.

PLLs are widely used for synchronization purposes in several communication and consumer domains, including radio transmission, clock recovery and deskewing, spread spectrum, clock jitter reduction, clock generation, and clock distribution. PLLs typically used in high-performance, high-speed systems are required to have low noise/jitter clock outputs, and low clock skew, among other requirements.

1.1 Recent and Past High-Performance PLL Trends

High-performance, high-speed systems demand components that exhibit close-to-ideal characteristics, such that the precision is not compromised while ensuring that the systems themselves do not become overly complicated. In electronic systems, this approach has led to shifting all processing from the analog domain to the digital domain while the signal transmission and receiving are performed in the analog domain. This shift means that high-performance systems generally have both analog and digital blocks as well as blocks to perform the analog-to-digital (A/D) and digital-to-analog (D/A) signal conversions. All the digital, A/D, and D/A blocks also require high-precision clocking that involves high-performance clock generation and distribution circuitry; typically, this circuitry is a high-performance PLL. For clocking high-performance devices such as medium- to high-resolution A/D converters, recently introduced high-performance PLLs rely on onboard, moderately high-Q, LC-based voltage-controlled oscillators (VCOs) as part of the PLL to ensure high-quality outputs.

Texas Instruments' CDCE62005 is a device that uses an internal VCO for the synchronizing to a backplane reference clock; it provides the option to use external components for setting its PLL loop bandwidth while the other PLL components are on-chip. It also includes an SPI™ programming interface that enables the PLL to cover wide frequency ranges at its output and operate at a wide range of PLL bandwidths while ensuring very low noise/jitter over its entire operating range.

2 Functional Description

The CDCE62005 is a high-performance, low-jitter, and low skew clock synchronizer and jitter cleaner that synchronizes one of three reference clocks to its onboard VCO frequency. The input reference clock can either be an LVPECL, LVDS, or LVCMOS signal. The CDCE62005 input buffers support either differential or single-ended signals, and also provide users the choice of turning on the device internal termination (50 Ω single-ended to the respective V_{BB}) or using external termination for setting the bias voltage. A third reference input can support a parallel resonant crystal, which can be used as a reference clock and also as a backup source during startup in certain applications that use a serialized/deserialized (SerDes) recovered clock as one of the primary sources. In such a case, the crystal input is required to provide accurate clock outputs to maintain error-free system operation. There are two on-chip VCOs: VCO1 covers the range of 1.75 GHz to 2.05 GHz, and VCO2 covers the range of 2.05 GHz to 2.35 GHz. The dual VCO architecture provides wider frequency coverage and also maintains good phase noise performance at the device outputs. The programmable reference and feedback dividers give a high flexibility to the frequency ratio of the reference clock to output clock that operates up to 1.175 GHz.

Through the selection of the internal VCO frequency and loop filter components, the PLL loop bandwidth and damping factor can be adjusted to meet a range of different system requirements. Each of the outputs can be programmed to either a total of five LVPECL/LVDS outputs, 10 LVCMOS outputs, or any combination through programming the SPI. The SPI also allows individual control of the frequency and

enable/disable state of each output. The device operates in a typical 3.3-V environment, and has an onboard EEPROM that allows for saving default startup conditions. The built-in latches ensure that all outputs are synchronized on device power-up or when the PLL is reconfigured after toggling the Reset pin. The device is ensured to be functional up to 1.175 GHz. Each output is also equipped with an Output MUX that allows the output to be selected from either a PLL/VCO or one of the three reference inputs.

The CDCE62005 is characterized for operation from 3.0 V to 3.6 V and from –40°C to +85°C. Figure 1 shows the block diagram for the CDCE62005.

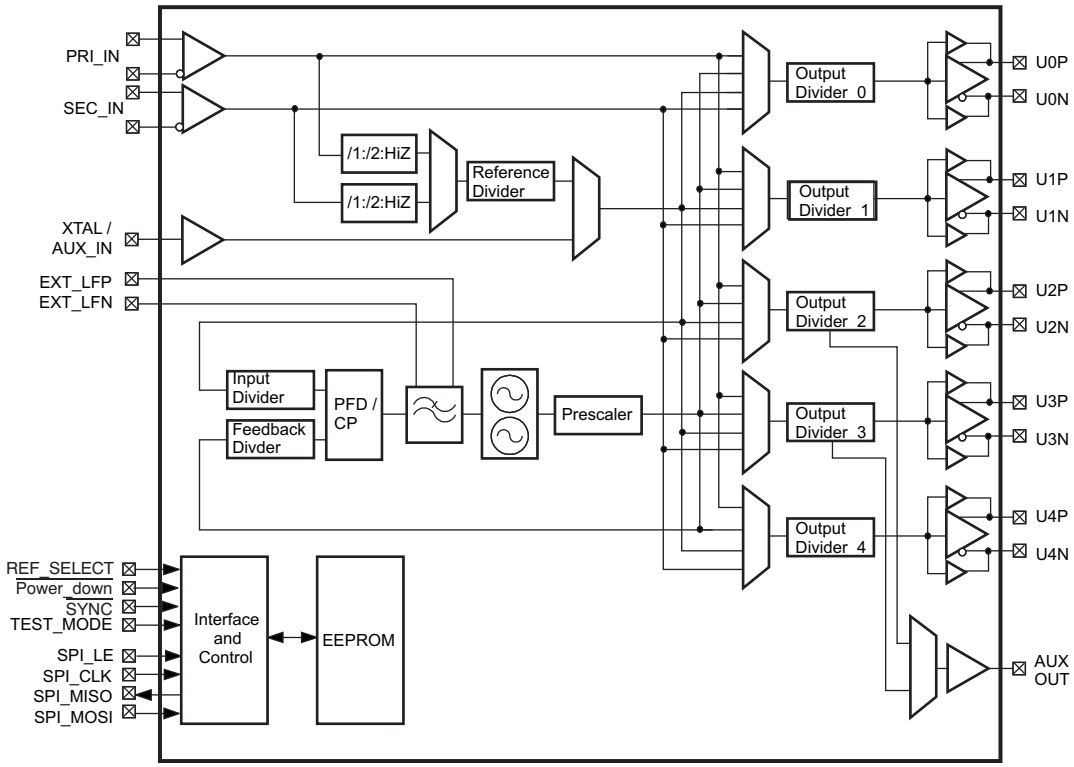


Figure 1. CDCE62005 Block Diagram

2.1 Clock Synthesizer

As seen in Figure 1, the CDCE62005 has internal dividers, twin onboard VCOs, a phase frequency detector, charge pump, partially internal loop filter, and LVPECL/LVDS/LVCMOS input and output buffers, all of which completes a PLL. Through the PLL operation, the VCO clock synchronizes with the reference clock input and ultimately with all clock outputs. All outputs are completely synchronized in terms of phase and frequency with the reference clock input. When powering up from the EEPROM, the $\overline{\text{SYNC}}$ signal synchronizes outputs after device power-up.

2.2 Frequency Multiplication and Division

Through programming the SPI, the input and feedback dividers can be set. Depending on the integer values of these two dividers, the output frequency can be fixed to almost any integer or fractional number of the input frequency within the specified frequency range as stated in the product data sheet (the VCO with the correct frequency is required to generate the application frequency). Choosing the input and feedback dividers determines the reference and feedback frequency for the phase frequency detector (PFD); these two frequencies must be the same. The outputs are directly related to the VCO frequency, and the output frequency can be scaled down by 1, 2, 3, 4, 5, 6, and so on up to 80.

2.3 Jitter Cleaner

The advantage of having a good onboard VCO and loop filter is that a wide range of PLL loop bandwidths can be chosen, depending on the system jitter requirements. The jitter cleaning action depends on the PLL loop bandwidth. Up to the loop bandwidth, all noise (jitter) passes through and above the loop bandwidth, and all signal noise is cleaned. The ideal loop bandwidth for a given application is chosen such that the reference clock source starts to exceed the VCO noise floor. If the input has a great deal of jitter, then by selecting a low loop bandwidth, jitter can be cleaned. For the CDCE62005, a low loop bandwidth (less than 100 Hz) can be achieved. The CDCE62005 itself adds a low noise to its outputs.

2.4 Clock Distribution with Dividing Options

The CDCE62005 has five differential (LVPECL/LVDS) or 10 single-ended (LVCMOS) outputs, or any combination of outputs. The frequency of each output is directly related to the VCO frequency with an output divider of /1, /2, /3, /4, /5, and so on up to /80. Each output can be individually programmed through the SPI.

2.5 Phase Adjustment

Each output on the CDCE62005, can also be phase adjusted; the granularity of the phase adjustment depends on the output divider value. For any output divide from the allowable ratios, the number of phase setting options (including the current zero phase shift) is ***P***. Tthe phase adjust granular step size is ($2\pi/P$) where *P* is the output divider. For example, say P is chosen as 4. Then, the total number of phase offsets that can be chosen for a bank of outputs is 4; the phase adjust granular step size is $\pi/2$, or 90 degrees.

3 CDCE62005 Frequency Synthesis

This section provides some insight on choosing the input frequency, divider, and VCO settings required to obtain a particular set of output frequencies using the multiple outputs of the CDCE62005 device.

3.1 Multiple Frequency Synthesis Example

Assume a typical application, where a total of two 156.25-MHz LVPECL, two 125-MHz LVDS, and two 25-MHz LVCMOS output clocks are desired and should be phase-locked to a single back-plane input reference clock of 25 MHz. The goal of this example is to identify the input (M), prescaler (N), feedback (FB), and output (P) divider values, the VCO frequency to lock to, and the other related PLL settings needed to derive the different output frequencies from the common input and VCXO frequencies. Follow these steps to achieve this goal.

Step 1. From Figure 1, it can be inferred that the relationship between the output frequency and the input frequency is described by these equations:

$$F_{OUT} = F_{IN} \times \frac{(N \times FB)}{(M \times P)}$$

Where:

- $F_{VCO} = F_{OUT} \times P \times N$

Provided that:

- 80 kHz < (F_{IN}/M) < 40 MHz
- 1750 MHz < ($F_{OUT} \times P \times N$) < 2350 MHz

Step 2. Keep in mind the following while satisfying the equations in Step 1:

- The P divider can be chosen to be 1, 2, 3, 4, 5, up to 80
- The internal VCO range is from 1.75 GHz to 2.35 GHz
- The input (M) and prescaler (N) dividers can be chosen from the values shown in the CDCE62005 product data sheet
- The FB divider can be chosen from the values provided in the CDCE62005 product data sheet

3. Given multiple desired output frequencies and the input frequency, the first step would be to establish M, N, and FB divider values for different P divider settings to satisfy these equations:

$$F_{IN} = F_{OUT1} \times (M \times P_1) / (N \times FB)$$
$$F_{IN} = F_{OUT2} \times (M \times P_2) / (N \times FB)$$
$$F_{IN} = F_{OUT3} \times (M \times P_3) / (N \times FB)$$
$$F_{IN} = F_{OUT4} \times (M \times P_4) / (N \times FB)$$
$$F_{IN} = F_{OUT5} \times (M \times P_5) / (N \times FB)$$
$$(F_{VCO}/ N) = F_{OUT1} \times P_1 = F_{OUT2} \times P_2 = = F_{OUT3} \times P_3 = F_{OUT4} \times P_4 = F_{OUT5} \times P_5$$

Such that these parameters are valid:

- The common PFD frequency is always less than 40 MHz
- The VCXO frequency is the same for deriving all outputs

For our example of deriving these outputs, it can be seen that there is not an output divider (P5) that will generate a 25-MHz output. However, the output MUX value of output 5 can be chosen to directly bypass the 25-MHz input clock to output 5. Thus, in order to use a common VCO frequency, the P dividers to be used are:

- P1 = 4
- P2 = 4
- P3 = 5
- P4 = 5
- P5 = 1

The common VCO frequency is 1875 MHz and is VCO1. The output MUX for outputs 1 to 4 are set to the PLL/VCO outputs. Moreover, the FB divider to be used is:

FB = 100

The N divider to be used is:

N = 3

These values ensure that the (F_{IN}/M) ratio is within 40 MHz and is set at 6.25 MHz. Thus, the M divider to be used is:

M = 4

Figure 2 illustrates this configuration.

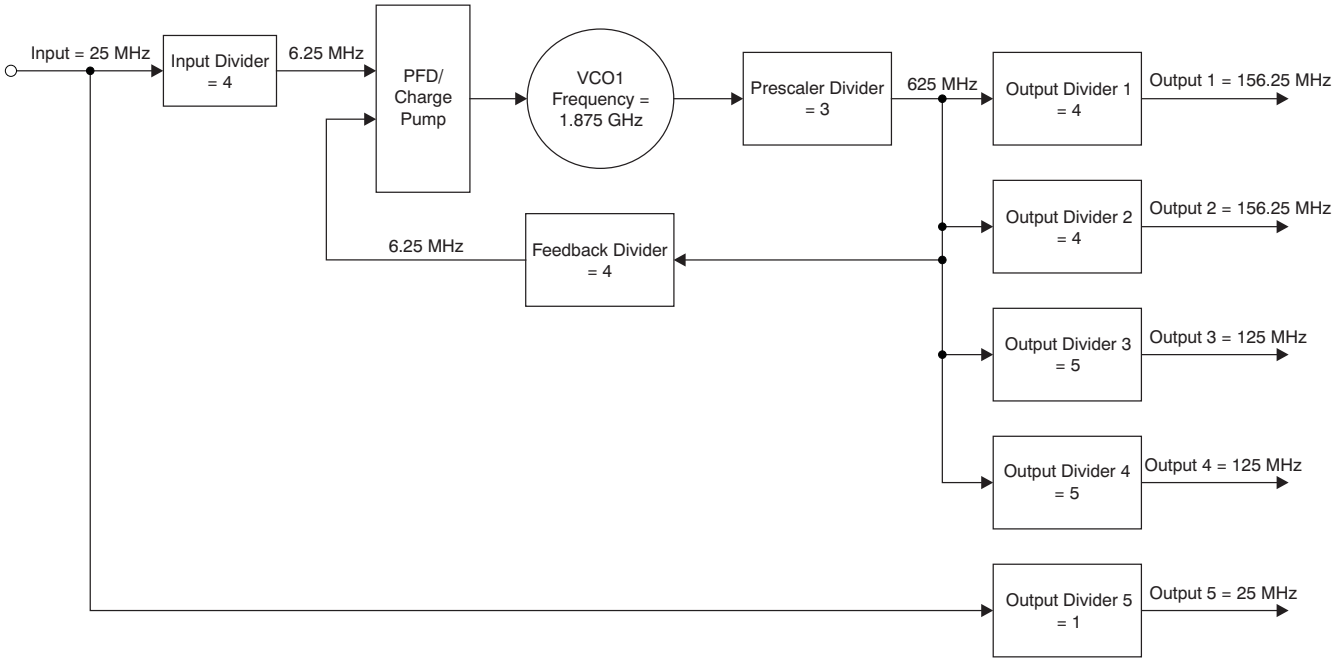


Figure 2. CDCE62005 Settings for Multiple Frequency Synthesis Example

4 Input Crystal Selection Guidelines

The CDCE62005 has an internal 8-pF load on the $X_{IN}1$ pin. Thus, if a crystal within the acceptable input range of the CDCE62005 is chosen with a particular load capacitance rating, extra loading must be added on each of the crystal terminals connected to the $X_{IN}1$ and $X_{IN}2$ pins of the CDCE62005 such that the crystal oscillates at the exact frequency at which it is rated. For example, for a 10-pF load rating and a given crystal, an extra 12-pF load can be added on the $X_{IN}1$ and an extra 20-pF load can be added on the $X_{IN}2$ such that (12 + 8) pF || 20 pF = 10 pF.

Some recommended crystal vendors and specific part numbers are listed in Table 1.

Table 1. Recommended Crystal Manufacturers

Manufacturer	Manufacturer Part Number
KDS	SMD-49
Pletronics	SM13T
Quartzcom	UM-1 MJ

5 CDCE62005 PLL Bandwidth Selection

Unlike other PLLs, the CDCE62005 loop filter components and charge pump current are not fixed. It is possible to choose a loop bandwidth from the sub-100 Hz level to approximately 400 kHz.

5.1 Loop Bandwidth

The PLL bandwidth depends on the loop filter, charge pump current, VCO gain, and phase frequency detector (PFD) update frequency. The pre/post dividers determine the PFD update frequency, as Figure 3 shows.

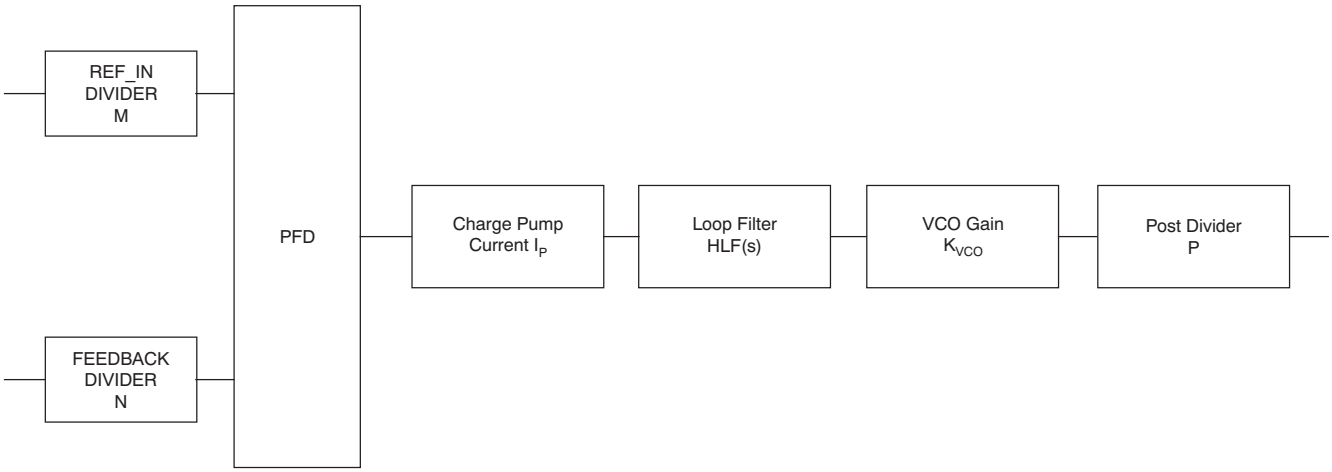


Figure 3. PLL Bandwidth Dependencies

5.2 Jitter Peaking

Around the loop bandwidth, the incoming jitter from the reference clock may be amplified. This phenomenon is called *jitter peaking*. In some applications, this peaking has an adverse effect on overall jitter performance ***if*** the jitter peaking occurs within the band of interest. If the jitter peaking occurs beyond the band of interest, the application generally suffers no adverse effects. In any case, care should be taken to limit jitter peaking to within 10 dB in order to prevent the loop from becoming unstable. An example of a PLL phase response with 2-dB jitter peaking is shown in Figure 4.

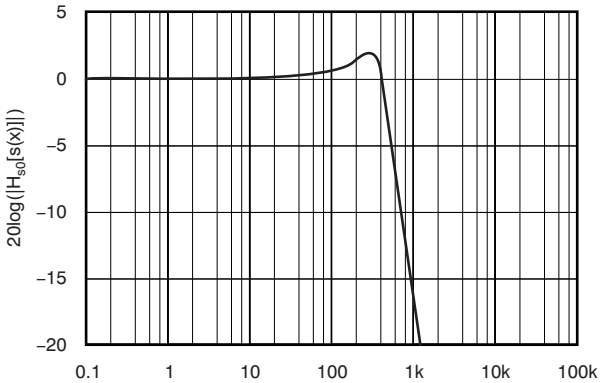


Figure 4. Jitter Peaking Around PLL Bandwidth

5.3 Phase Margin

Phase margin is important for PLL stability and influences the PLL lock time. How quickly the PLL output settles to its final value depends on the PLL phase margin. As a rule of thumb, a minimum 30-degree phase margin is recommended for stable clock operation.

6 Allowable Loop Filter Topologies in CDCE62005

The CDCE62005 includes an on-chip active loop filter that can be used to set larger loop filter bandwidths (that is, greater than 100 kHz); this loop is shown in Figure 5. The device also provides the option of using external components (R and C) that can be used with the onboard active loop filter to provide support for small loop filter bandwidths (as low as 100 Hz or lower); this configuration shown in Figure 6.

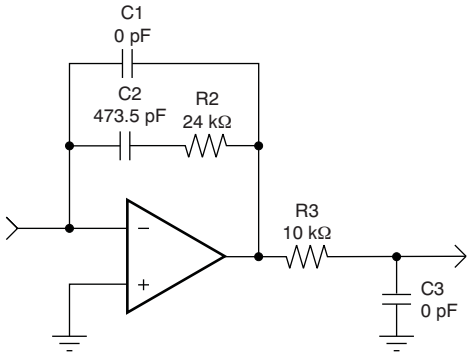
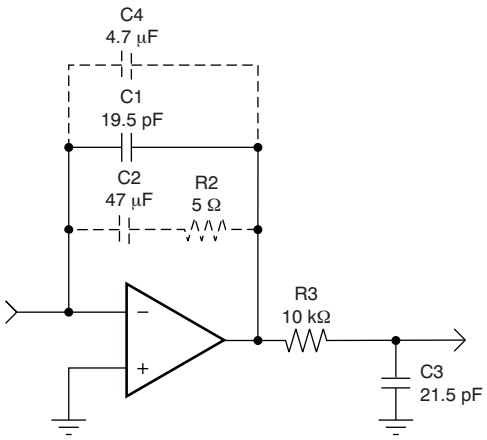


Figure 5. On-Chip Loop Filter Circuit for Large Loop Bandwidth (>100 kHz)



Note: Components shown with a dashed line are off-chip.

Figure 6. Partial On-Chip Loop Filter Circuit for Low Loop Bandwidth (≤100-Hz)

6.1 Recommended PLL Bandwidth

The PLL loop bandwidth of the CDCE62005 is recommended to be set according to the phase noise profile of its reference input and the phase noise profile of the onboard VCO clock. It is recommended to set the PLL loop bandwidth as the crossover point of the reference input phase noise and the phase noise of the VCO clock. When the input clock is clean and any near-frequency offsets are better than the VCO clock, it is beneficial for the PLL bandwidth to be set at several hundred kilohertz as determined by the crossover point.

When the input clock is dirty and at most frequency offsets worse than the VCO clock, it is beneficial for the PLL bandwidth to be as low as possible (that is, at less than 100 Hz) as determined by the crossover point.

7 Output Termination

The CDCE62005 is a 3.3-V clock driver that has three output type options: LVDS, LVPECL, or LVCMOS.

7.1 LVPECL Termination

The CDCE62005 is an open emitter for LVPECL outputs. Therefore, proper biasing and termination are required to ensure correct operation of the device and to maintain signal integrity. The proper termination for LVPECL is a 50-Ω to (V_{CC}– 2 V) supply, but this dc voltage is not readily available on a board. Either a direct termination or ac-coupled termination can be used to terminate the LVPECL outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac-coupling is required.

7.1.1 Direct Coupled LVPECL Termination

In order to eliminate the necessity of having a (V_{CC}– 2 V) supply on the board, a Thevenin equivalent network composed of two resistors with a 3.3-V supply replace the 50 Ω to (V_{CC}–2 V) to ensure required biasing and termination. Figure 7 shows a termination circuit that is generally recommended for direct termination.

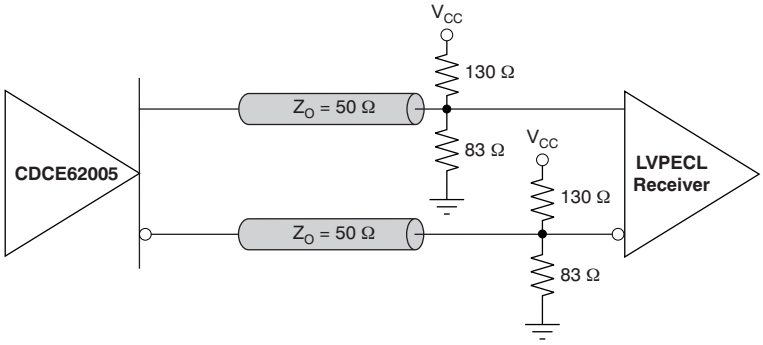


Figure 7. LVPECL DC Termination Circuit

7.1.2 AC-Coupled LVPECL Termination

If ac-coupled termination is used, the input and output stages must be biased properly. The 150-Ω resistor placed close to the CDCE62005 ensures proper output biasing, while the 1.3-kΩ and 2-kΩ resistor network bias the LVPECL receiver input stage. Figure 8 shows a recommended termination circuit for ac-coupled termination.

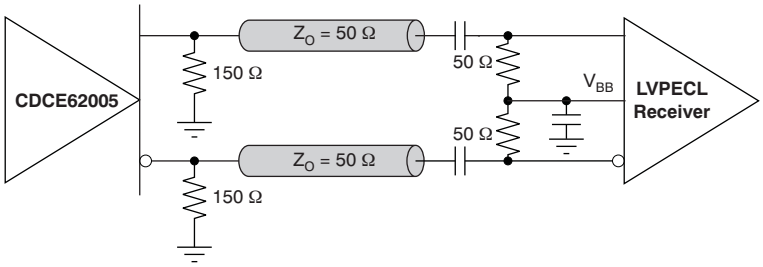


Figure 8. LVPECL AC-Coupled Termination Circuit

7.2 LVDS Termination

The CDCE62005 has on-chip, 100-Ω termination between the two LVDS outputs. Therefore, no additional biasing is needed, but termination is required to maintain signal integrity. The proper termination for signal integrity over two 50-Ω lines is a 100–Ω resistor between the outputs on the receiver end. Either a direct termination or ac-coupled terminations can be used to terminate the LVDS outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac-coupling is required.

7.2.1 Direct Coupled LVDS Termination

Figure 9 shows a recommended termination circuit for direct termination of LVDS outputs for an LVDS receiver that is assumed to have on-chip, 100-Ω termination between the outputs.

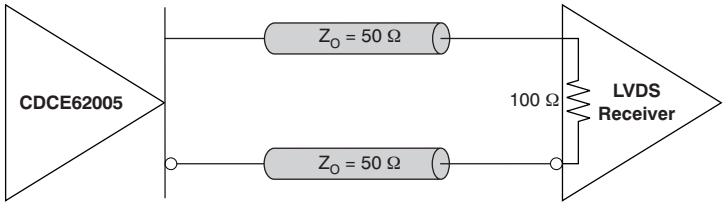


Figure 9. LVDS DC Termination Circuit

7.2.2 AC-Coupled LVDS Termination

Figure 10 shows a recommended termination circuit for ac-coupled termination of LVDS outputs for an LVDS receiver that is assumed to have on-chip, 100-Ω termination between the outputs.

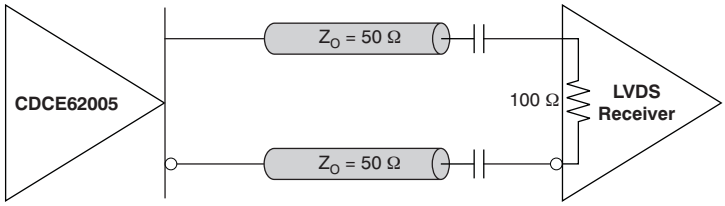


Figure 10. LVDS AC-Coupled Termination Circuit

7.3 LVCMOS Termination

Each differential output of the CDCE62005 can be configured to two single-ended, 3.3-V LVCMOS outputs. For a 3.3-V system, direct coupling is recommended as shown in Figure 11. For other supply voltage systems, direct coupled voltage dividers are recommended to achieve acceptable receiver LVCMOS levels.

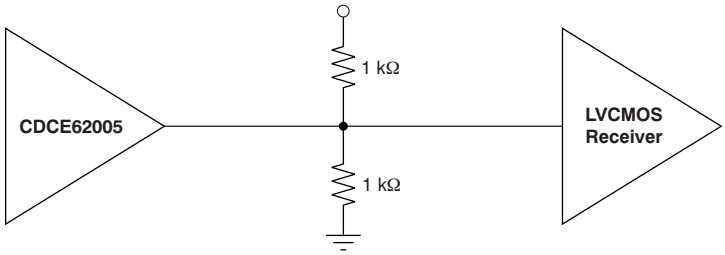


Figure 11. 3.3-V LVCMOS DC-Coupled Termination Circuit

8 Input Termination

The CDCE62005 is a 3.3-V clock driver that has the option of these reference input types: LVPECL, LVDS, or 3.3-V LVCMOS. The device can also interface to a parallel resonant crystal input. For non-crystal inputs, it provides the option of using its internal, 50-Ω, single-ended termination resistors to V_{BB}, which can be set accordingly. In this case, when the input buffer is properly chosen for ac or dc coupling (according to the selected biasing for the driver circuit) along with input termination, no external termination is needed.

8.1 LVPECL Input (No Internal Termination)

The proper termination for LVPECL is a 50-Ω to (V_{cc} – 2 V) supply, but this dc voltage is not readily available on a board. Either a direct termination or terminations for ac-coupling can be used to terminate the LVPECL outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac-coupling is required.

8.1.1 Direct Coupled LVPECL Termination

In order to eliminate the necessity of having a (V_{cc} – 2 V) supply on the board, a Thevenin equivalent network composed of two resistors with a 3.3-V supply replace the 50 Ω to (V_{cc} – 2 V) supply to ensure required biasing and termination. Figure 12 shows a recommended termination circuit for direct termination.

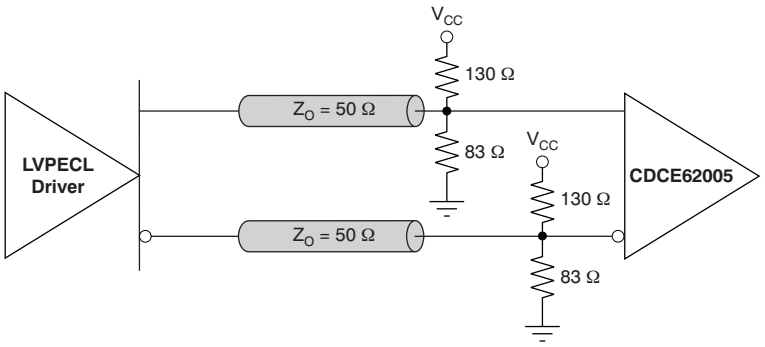


Figure 12. LVPECL DC Termination Circuit

8.1.2 AC-Coupled LVPECL Termination

If ac-coupled termination is used, the input and output stages must be biased properly. The 150-Ω resistor placed close to the driver ensures proper output biasing, while the 1.3-kΩ and 2-kΩ resistor network bias the CDCE62005 LVPECL input stage. Figure 13 shows a recommended termination circuit for ac-coupled termination.

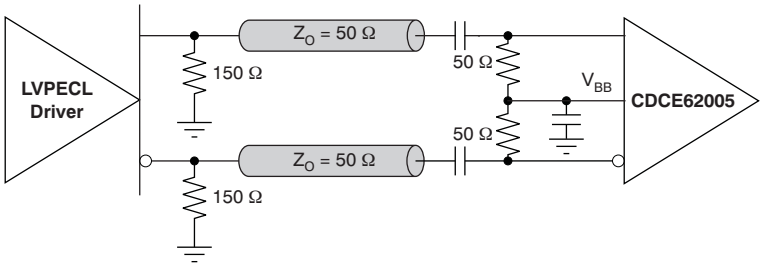


Figure 13. LVPECL AC-Coupled Termination Circuit

8.2 LVDS Termination (No Internal Termination)

The proper termination for signal integrity over two 50-Ω lines is a 100-Ω resistor placed between the outputs on the receiver end. Either direct termination or terminations for ac-coupling can be used to terminate the LVDS outputs. It is recommended to place all resistive components close to either the driver end or the receiver end. If the supply voltages of the driver and receiver are different, ac-coupling is required.

8.2.1 Direct Coupled LVDS Termination

Figure 14 shows a recommended termination circuit for direct termination of the LVDS outputs for LVDS inputs on the CDCE62005.

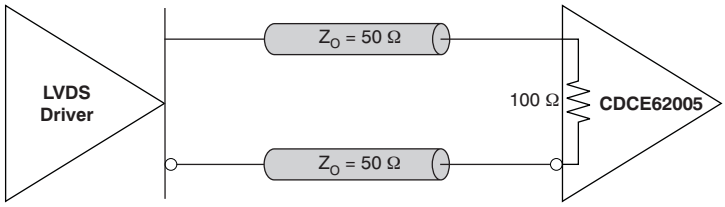


Figure 14. LVDS DC Termination Circuit

8.2.2 AC-Coupled LVDS Termination

Figure 15 shows a recommended termination circuit for ac-coupled termination of the LVDS outputs for LVDS inputs on the CDCE62005.

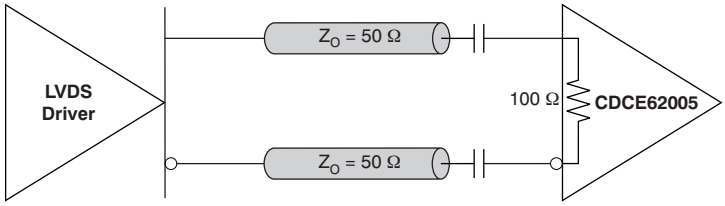


Figure 15. LVDS AC-Coupled Termination Circuit

8.3 LVCMOS Termination

For a 3.3-V driver, direct coupling is recommended as shown in Figure 16 to interface to LVCMOS inputs on the CDCE62005.

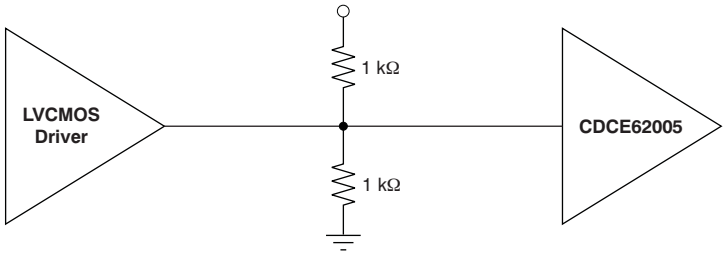


Figure 16. 3.3-V LVCMOS DC-Coupled Termination Circuit

8.4 Crystal Input to CDCE62005

If interfacing the CDCE62005 to a parallel resonant crystal, one of the crystal legs should be connected to the AUX_IN pin of the device, and the other leg should be grounded. Knowing that the on-chip capacitance at the AUX_IN pin is 10 pF maximum, it is recommended to add (C_L – 10 pF) to ground on the trace that connects the crystal and the AUX_IN pin for a good input frequency accuracy, where C_L is the load capacitance rating for the crystal. Figure 17 illustrates this configuration.

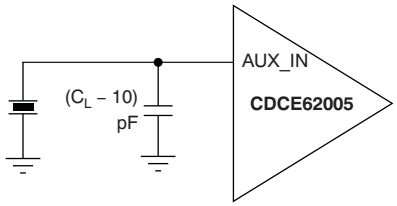


Figure 17. Crystal Input to the CDCE62005

9 Power-Supply Decoupling

PLL-based frequency synthesizers are very sensitive to noise on the power supply, which can dramatically increase the PLL jitter. This characteristic is especially true for analog-based PLLs. Therefore, it is essential to reduce noise from the system power supply, especially when jitter/phase noise is very critical to applications. A PLL would have attenuated jitter because of power-supply noise at frequencies beyond the PLL bandwidth as a result of attenuation by the loop response.

Filter capacitors are used to eliminate the low-frequency noise from power supply, whereas the bypass capacitors provide the very low impedance path for high-frequency noise and guard the power-supply system against induced fluctuations. Inserting a ferrite bead between the board power supply and the chip power supply isolates the high-frequency switching noise generated by the clock driver, preventing it from leaking into the board supply. Choosing an appropriate ferrite bead with low dc resistance is important because it is imperative to maintain a voltage at the CDCE62005 power-supply pin that is over the minimum voltage needed for its proper operation. At dc, the ferrite bead would have a voltage drop across itself; the maximum drop would depend on its maximum dc resistance and the maximum dc current that the CDCE62005 would draw from the 3.3-V power supply.

For correct operation, the CDCE62005 requires a minimum power-supply voltage of 3 V and draws a maximum supply current of 900 mA. The split for the power-supply currents among the power-supply pins on the CDCE62005 follows this configuration:

- VCC_PLL1 and VCC_PLL2 draw a maximum supply current of 100 mA
- Each VCC_IN draws a maximum supply current of 25 mA
- VCC_VCO draws a maximum supply current of 50 mA
- VCC_OUT (for all output supplies) draws a maximum supply current of 600 mA

Assuming a 3.3-V board supply, the ferrite bead maximum dc resistance for each VCC_PLL can be 3 Ω; for each VCC_IN, the resistance can be 12 Ω each; for VCC_VCO, the resistance can be 6 Ω each; and for VCC_OUT, the resistance can be 0.5 Ω. Figure 18 shows a general recommendation for decoupling the power supply for each of the following power-supply pins: VCC_PLL1 and VCC_PLL2, each VCC_IN, VCC_VCO, and VCC_OUT. For each power-supply pin in the device, it is also recommended to add additional 0.1μF to filter out any power-supply noise that might creep into the sensitive PLL power supplies.

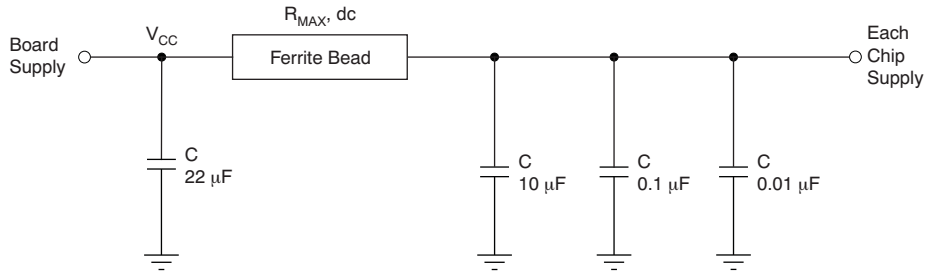


Figure 18. Power-Supply Decoupling

10 Application Example: Providing Low-Phase Noise Clocks to DACs and ADCs

The digital-to-analog converters (DACs) and analog-to-digital converters (ADCs) require low-noise clock signals to ensure adequate signal-to-noise ratios (SNR) and effective numbers of bits (ENOB). The clocking requirement becomes more pronounced at high analog input bandwidths of the data converters. The CDCE62005 can generate low-noise clock signals using an external VCXO and low PLL loop bandwidth. The PLL itself adds less than 0.1ps, RMS (over 12-kHz to 20-MHz bandwidth) jitter to the outputs. Figure 19 shows a clocking solution for typical wireless basestation systems. Figure 20 shows a clocking solution for typical Medical Ultrasound systems.

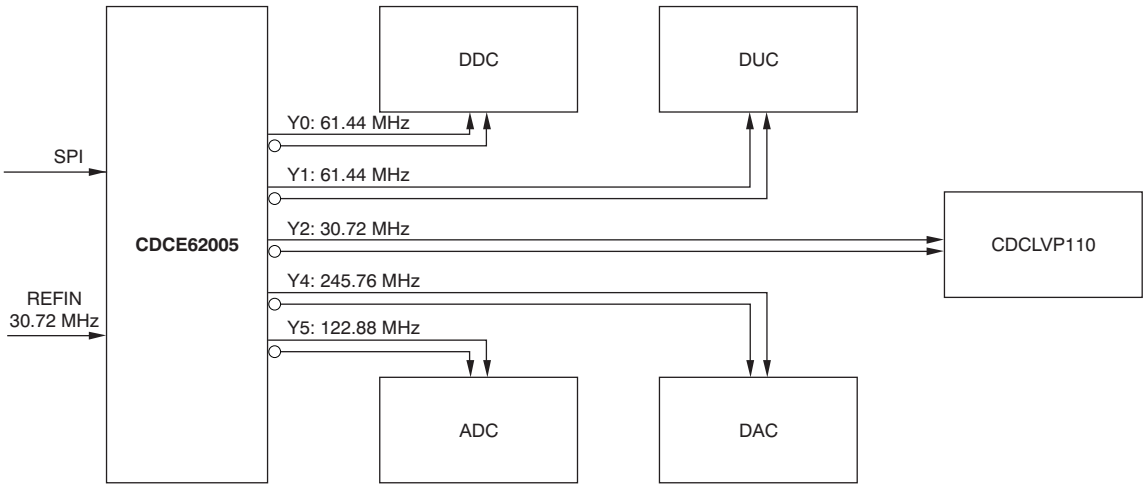


Figure 19. Typical Wireless Basestation System Clocking Solution

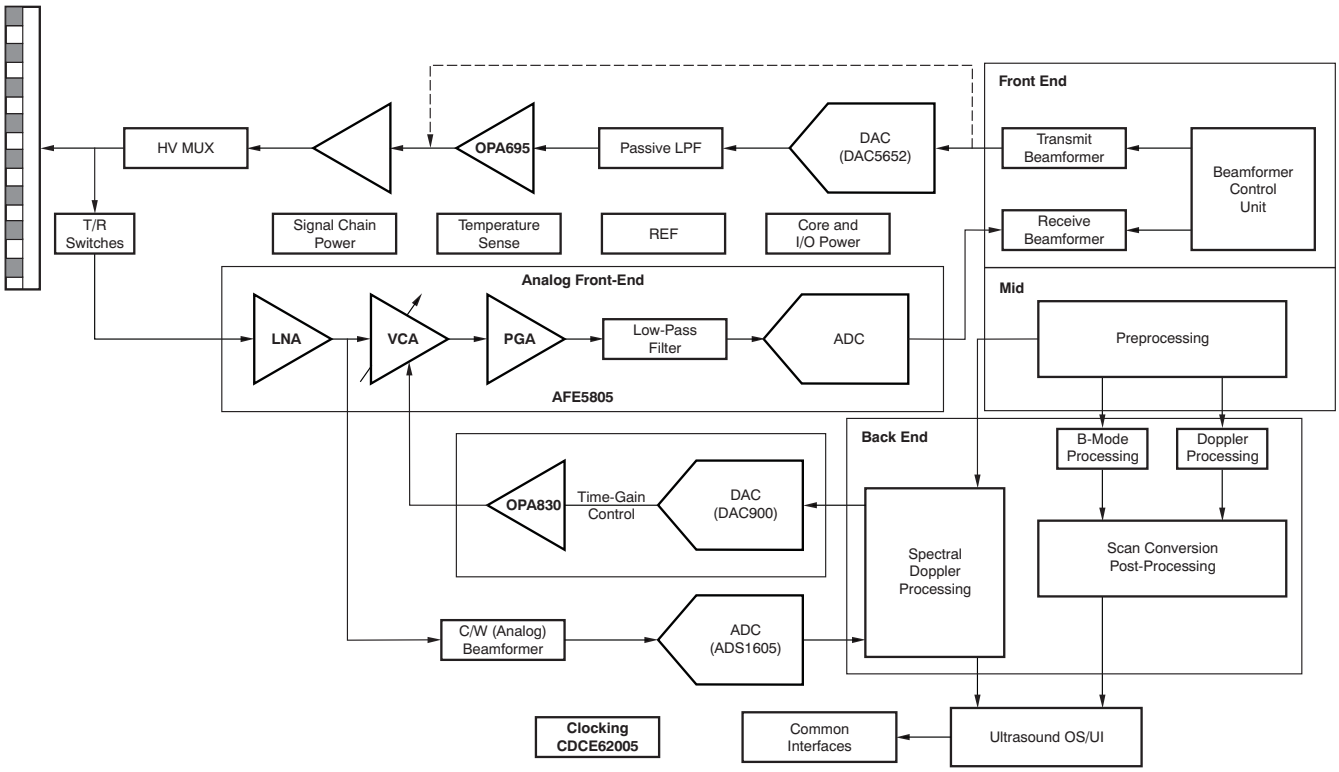


Figure 20. Typical Medical Ultrasound System Clocking Solution

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