Application Report
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CMR Programming for DDR3 Registers

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ABSTRACT

This application report provides direction for programming the Control Words (also known as Control Mode Registers or CMR) of DDR3 Register Buffers which are compliant with the JEDEC SSTE32882 specification.

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1 About CMR Commands

SSTE32882-compliant DDR3 registers have internal control bits (also known as Control Mode Registers or CMR) for adapting the configuration of certain device features.

If the device is operated in Dual Chip Select Mode (QCSEN#=HIGH), then the control bits are accessed by the simultaneous assertion of both DCS0# and DCS1# LOW.

If Quad Chip Select Mode is enabled (QCSEN#=LOW), then the control bits are accessed by the simultaneous LOW assertion of both DCS0# and DCS1# or DCS2# and DCS3# or all four DCS[n:0].

SSTE32882-compliant DDR3 Registers allocate decoding for up to 16 words of control bits, RC0 through RC15. Selection of each word of control bits is presented on inputs DA0 through DA2 and DBA2. Data to be written into the configuration registers must be presented on DA3, DA4, DBA0, and DBA1.

1.1 Control Word Decoding

The values to be programmed into each control word are presented on signals DA3, DA4, DBA0, and DBA1 simultaneously with the assertion of the control word access through DCS0# and DCS1# and the address of the control word on DA0, DA1, DA2, and DBA2.

Table 1. Control Word Decoding With Quad Chip Select Disabled

CONTROL WORD	SYMBOL	SIGNAL						MEANING
		DCS0#	DCS1#	DBA2	DA2	DA1	DA0	
None	n/a	H	X	X	X	X	X	No control word access
None	n/a	X	H	X	X	X	X	No control word access
Control word 0	RC0	L	L	L	L	L	L	Global Features Control Word
Control word 1	RC1	L	L	L	L	L	H	Clock Driver Enable Control Word
Control word 2	RC2	L	L	L	L	H	L	Timing Control word
Control word 3	RC3	L	L	L	L	H	H	CA Signals Driver Characteristics Control Word
Control word 4	RC4	L	L	L	H	L	L	Control Signals Driver Characteristics Control Word
Control word 5	RC5	L	L	L	H	L	H	CK Driver Characteristics Control word
Control word 6	RC6	L	L	L	H	H	L	Reserved
Control word 7	RC7	L	L	L	H	H	H	Reserved
Control word 8	RC8	L	L	H	L	L	L	Additional IBT Settings Control Word
Control word 9	RC9	L	L	H	L	L	H	Weak drive mode, CKE power-down settings
Control word 10	RC10	L	L	H	L	H	L	Encoding for RDIMM Operating Speed
Control word 11	RC11	L	L	H	L	H	H	Operating Voltage VDD Control Word
Control word 12	RC12	L	L	H	H	L	L	Reserved for future use
Control word 13	RC13	L	L	H	H	L	H	Reserved for future use
Control word 14	RC14	L	L	H	H	H	L	Reserved for future use
Control word 15	RC15	L	L	H	H	H	H	Reserved for future use

If QSCEN# is LOW, then the control word access can also be invoked by asserting DCS2# and DCS3# or all four DCS[n:0] simultaneously.

The reset default state of Control Words 0 .. 15 is 0. Control word access is independent of PLL lock and can be accessed at any time input receivers are active.

Table 2. Control Word Decoding With Quad Chip Select Enabled

CONTROL WORD	SYMBOL	SIGNAL					MEANING
		DCS[n:0]#	DBA2	DA2	DA1	DA0	
None	n/a	HXHX	X	X	X	X	No control word access
None	n/a	HXXH	X	X	X	X	
None	n/a	XHXH	X	X	X	X	
None	n/a	XHHX	X	X	X	X	
None	n/a	LLLH	X	X	X	X	Illegal input states
None	n/a	LLHL	X	X	X	X	
None	n/a	LHLL	X	X	X	X	
None	n/a	HLLL	X	X	X	X	
Control word 0	RC0	LLHH Or HHLL Or LLLL	L	L	L	L	Global Features Control word
Control word 1	RC1		L	L	L	H	Clock Driver Enable Control word
Control word 2	RC2		L	L	H	L	Timing Control word
Control word 3	RC3		L	L	H	H	CA Signals Driver Characteristics Control word
Control word 4	RC4		L	H	L	L	Control Signals Driver Characteristics Control word
Control word 5	RC5		L	H	L	H	CK Driver Characteristics Control word
Control word 6	RC6		L	H	H	L	Reserved
Control word 7	RC7		L	H	H	H	Reserved
Control word 8	RC8		H	L	L	L	Additional IBT Settings Control Word
Control word 9	RC9		H	L	L	H	Weak drive mode, CKE power down settings
Control word 10	RC10		H	L	H	L	Encoding for RDIMM Operating Speed
Control word 11	RC11		H	L	H	H	Operating Voltage VDD Control Word
Control word 12	RC12		H	H	L	L	Reserved for future use
Control word 13	RC13		H	H	L	H	Reserved for future use
Control word 14	RC14		H	H	H	L	Reserved for future use
Control word 15	RC15		H	H	H	H	Reserved for future use

1.2 Requirements for Proper CMR Access

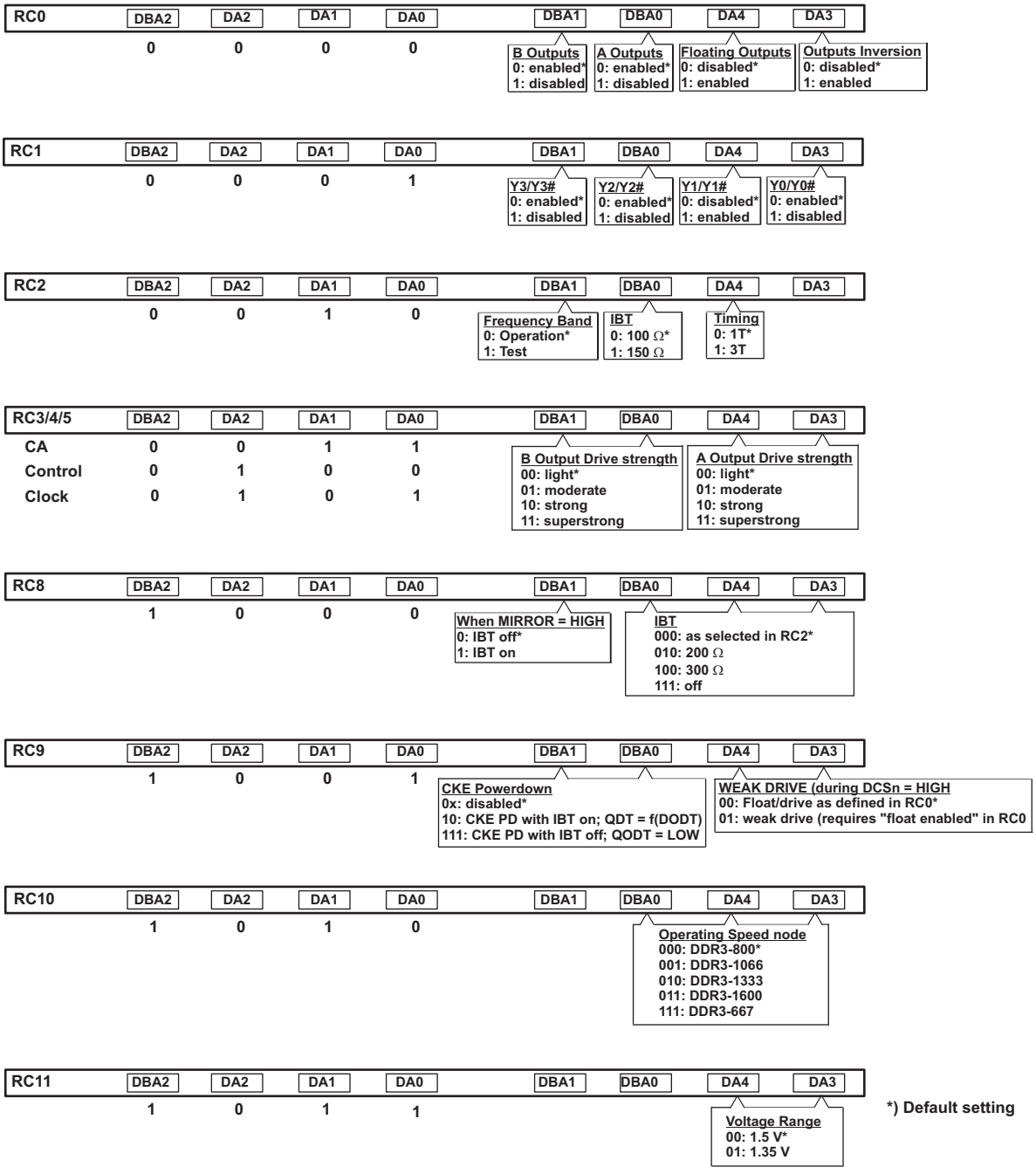
To write a correct CMR command to the register, several requirements must be fulfilled and are listed as follows.

- Parity bit is correct.
  - In all cases address and command parity is checked(1) during control word write operations. DRAS#, DCAS#, and DWE# are included in the parity computation. Remember that the parity bit for the corresponding data is expected one clock cycle after the data. If a parity error is detected, ERROUT# is asserted and the **command is ignored.**
  - Ensure that your test platform is asserting proper parity. Not all test boards may do this correctly. A possible workaround may be changing the number of ones in your CMR command from odd to even or vice versa. This can be done by changing values of unused CMR bits or DRAS#,DCAS#, and DWE#.
- Register is not busy.
  - For correct execution on a CMR access, the device may not be busy with previous tasks like previous CMR access or the second or third cycle of a MRS command. However, CMR accesses are allowed during stabilization of the PLL.
- Register is not in CKE Power-down Mode.
  - If RC9 bit DBA1 is set to 1, then at least one of the inputs DCKE0 or DCKE1 must be HIGH during CMR access and t_{MRD}. Register Qn outputs including QxCKE0, QxCKE1, QxODT0, and QxODT1 remain in their previous state. The device pulls QxCSn# HIGH during control word access.
- Unused Address inputs are LOW.
  - According SSTE32882 JEDEC specification, DA5 through DA15 must be LOW to access the control registers .
- Enough Settling Time
  - Any change to these control words require some time for the device to settle. For changes to the control word setting, the controller needs to wait a certain time after the last control word access before further access to the DRAM can take place.
  - For any changes to the clock timing (RC2 bit DBA1, RC6 bit DA4, and RC10 and RC11 bits DA3 and DA4), this settling may take up to t_{STAB} (= 6 µs) time.
  - In all other cases, t_{MRD} (= 8 clock cycles) applies. All inputs DCS[n:0] must be kept HIGH during that time.

(1) All address and command input signals are added up and the last bit of the sum is compared to the parity signal delivered by the system at the input PAR_IN one clock cycle later. If they don't match the device pulls the open drain output ERROUT# LOW. The control signals (DCKE0, DCKE1, DODT0, DODT1, DCS[n:0]#) are not part of this computation.

2 Overview on Most Frequently Used CMR's

The following illustration shows an overview of all relevant register control words and their possible settings. Reserved control words and functions are not included in this overview.



3 Example Pattern for Two Consecutive CMR Accesses

Cycle	RESET	PAR_IN	DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8	DA7	DA6	DA5	DA4	DA3	DA2	DA1	DA0	DRAS#	DCAS#	DWE#	DBA2	DBA1	DBA0	DCS0	DCS1	DCKE0	DCKE1	DODT0	DODT1	Comment
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
1	1	1	0	0	0	0	0	0	0	0	0	0	0	**1**	**0**	**0**	**0**	**0**	0	0	0	**0**	**0**	**0**	**0**	**0**	1	1	0	0	Write RC0(1), enabling float mode
2	1	**1**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	Set correct parity for CMR access
3	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
4	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	Wait for at least 8 clock cycles.
5	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	Before next transfer or command.…
6	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
7	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
8	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
9	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
10	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
11	1	1	0	0	0	0	0	0	0	0	0	0	0	**0**	**1**	**0**	**0**	**1**	0	0	0	**1**	**1**	**0**	**0**	**0**	1	1	0	0	Write RC9(1), enabling weak drive + CKE PD.
12	1	**0**	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	Set correct parity for CMR access.
13	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
14	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	Wait for at least 8 clock cycles.
15	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	Before next transfer or command
16	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
17	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
18	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1	1	1	0	0	
19	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	0	0	1	0	0	Continue your pattern here.

(1) Register Control Word Selection Bits, Data Bits, and corresponding Parity and CS Bits are marked in bold and colored font

4 References

1. *SN74SSQE32882, 28-Bit to 56-Bit Registered Buffer With Address Parity Test, One Pair to Four Pair Differential Clock PLL Driver* data sheet (SCAS857)
2. *SN74SSQEA32882, 28-Bit to 56-Bit Registered Buffer With Address Parity Test, One Pair to Four Pair Differential Clock PLL Driver* data sheet (SCAS879)
3. SSTE32882 JEDEC Specification

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