How to Apply 1.8-V Signals to 3.3-V CDCLVC11xx Fanout Clock Buffer

Julian Hagedorn   *Clock and Timing Products*

ABSTRACT

The CDCLVC11xx buffer family from Texas Instruments has a nominal voltage supply of 2.5 V and 3.3 V. With the simple employment of an external RC network, this family of devices can handle incoming signals whose voltage levels go up to 1.8 V.

This application report explains how to implement this network and dimension its discrete components, without impacting the specifications of additive jitter and rise and fall times.

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1 Introduction

Depending on the supply voltage applied, the CDCLVC11xx input stage has different input thresholds. These thresholds are the corners to safely detect a low or a high level (Figure 1). They are centered around half-supply voltage (either $V_{dd}/2 \pm 600$ mV at 3.3 V or $V_{dd}/2 \pm 400$ mV at 2.5 V).
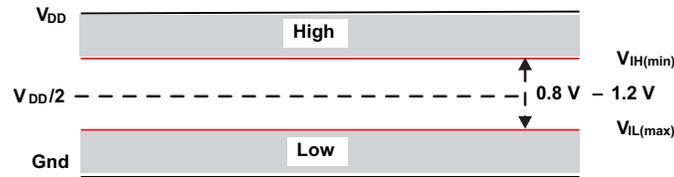

Figure 1. Input Thresholds to Ensure Save Operation

If a 1.8-V signal is supplied to the input of the buffer family, the high level of the signal does not reach $V_{IH(min)}$, and the buffer input stage does not detect the high state (Figure 2a). With the simple ac-coupling, shown in Section 2, the input signal is shifted around $V_{dd}/2$, ensuring the proper detection of high and low levels (Figure 2b).
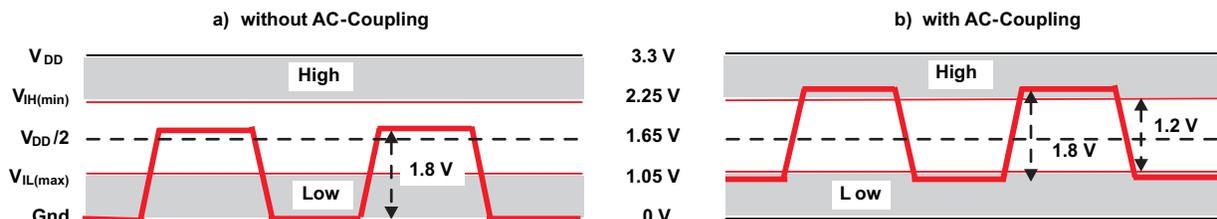

Figure 2. Input Signal With and Without ac-Coupling

2 Network and Test Bench Schematic

The network in Figure 3 shows how the ac-coupling can be done. In Figure 3, U0.1 represents a LVCMOS transmitter with 30-Ω output impedance. The series termination R3 adjusts U0.1 to the 50-Ω environment to avoid signal reflections. Depending on the supply voltage, R1 is either connected to 2.5 V or 3.3 V.
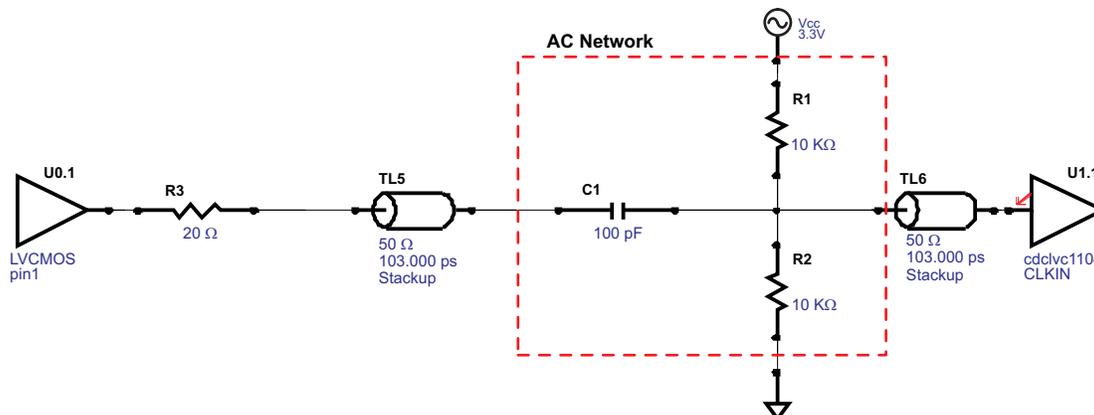
Figure 3. 1.8-V LVCMOS Driver Connected to the 2.5-/3.3-V Tolerant CDCLVC11xx Input

To reach 1.8 V at U1.1, R1 and R2 have to have high resistance. So, the transmission line is equivalently terminated like an open circuit.

C1 has to vary with the frequency. For low frequencies, a small capacitance discharges so fast that the signal becomes degraded (see Figure 4); this is due to the high-pass filter with C1, R1, and R2. If the recommended capacitance is used, the RC time constant (C1 × R1 || R2) is adjusted to the dedicated period of the clock signal.

Figure 4. Signal Degradation With Too Small an ac-Coupling Capacitance

Table 1. Recommended Coupling Capacitance

Frequency Range	Capacitance C1
1 MHz – 10 MHz	1 nF
11 MHz – 100 MHz	500 pF
101 MHz – 250 MHz	100 pF

3   Measurement

All measurements discussed in this application report were taken under nominal conditions: 2.5-/3.3-V supply voltage, at room temperature, with the CDCLVC1104Perf-EVM and after the transient behavior.
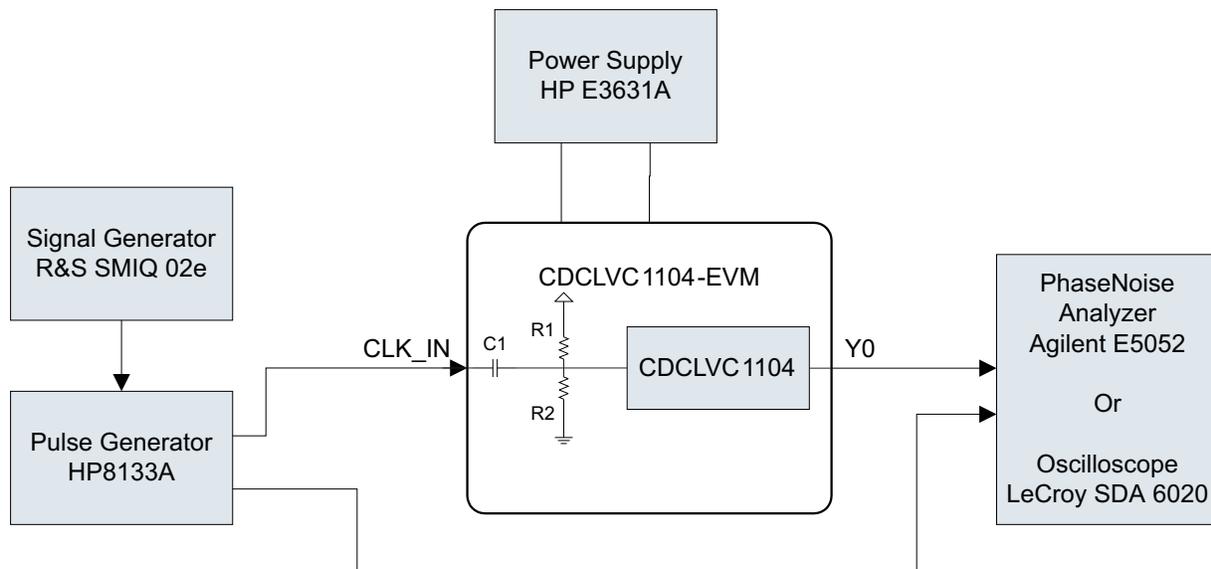
3.1   Test Equipment and Setup

Figure 5. Test Equipment and Setup

The capacitor and resistors (C1, R1, and R2) for the ac-coupling were soldered onto the input path of the CDCLVC1104Perf-EVM. The signal and the pulse generator were used to generate a square wave with amplitude of 1.8 V. The combination of the HP8133A and R&S SMIQ 02e increased the signal quality concerning jitter.

All additive jitter measurements were taken with the phase noise analyzer Agilent E5052. Measurements regarding rise and fall times were taken with a LeCroy HFP2500 high-impedance probe connected to a LeCroy SDA 6020 oscilloscope.

The outputs of the CDCLVC1104 were loaded with the shown application test load. The input with parasitic capacitance, as can be seen in Figure 6, is realized by a high-impedance probe in the used setup.

V_{DD} = 3.3 V or 2.5 V

RS = 10 Ω (V_{DD} = 3.3 V)
RS = 0 Ω (V_{DD} = 2.5 V)

LVCMOS Output

Z_O = 50 Ω

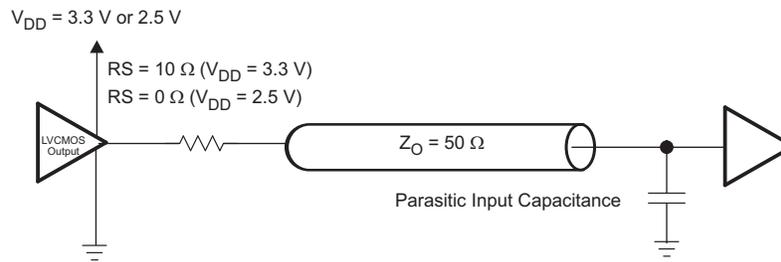Parasitic Input Capacitance

Figure 6. Application Test Load

3.2   *Results*

Several measurements with different frequencies and supply voltage were taken. Table 2 and Figure 10 summarize all results. Figure 7, Figure 8, and Figure 9 show the measurements as an example for 3.3-V supply and 100-MHz I/O frequency.
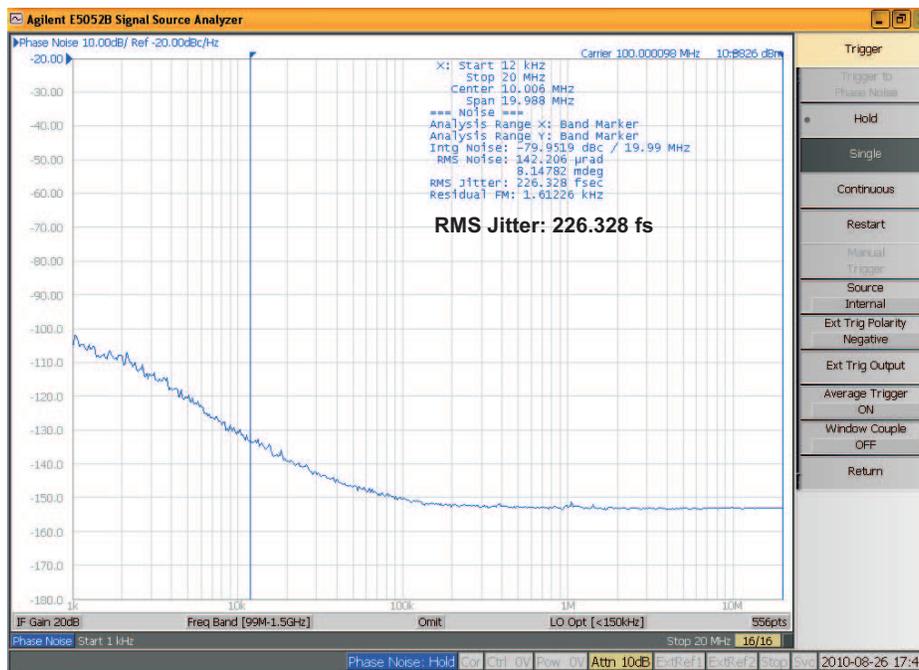
Figure 7. Input Phase Noise Plot to Analyze Additive Jitter at 100 MHz
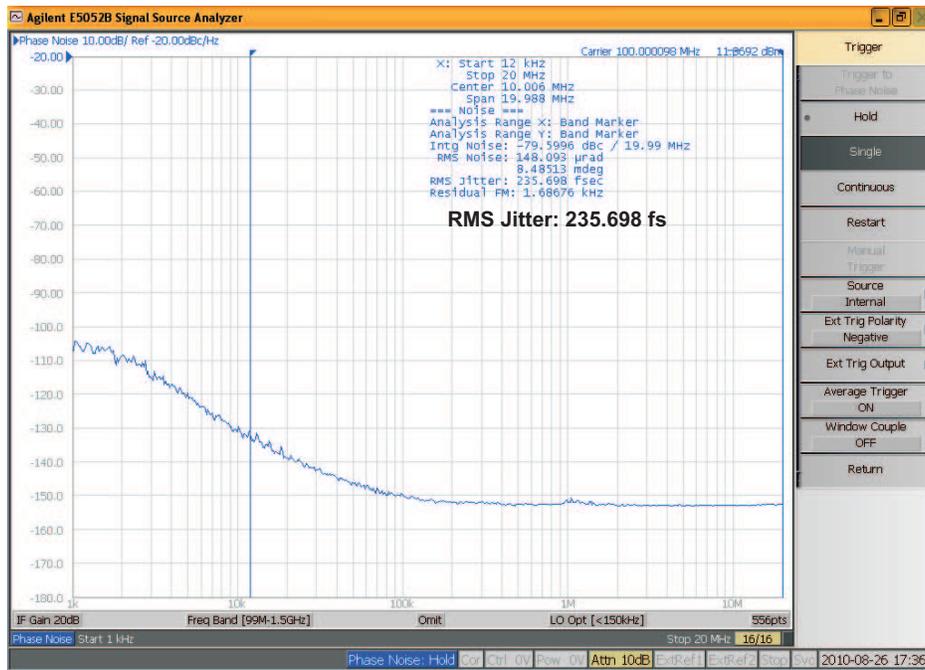
Figure 8. Output Phase Noise Plot at 100 MHz

The additive jitter rms can be calculated with the I/O jitter values and the following formula.

$$J_{rms,add} = \sqrt{J_{rms,out}^2 - J_{rms,in}^2}$$

for example:

$$J_{rms,add,100MHz} = \sqrt{J_{rms,out}^2 - J_{rms,in}^2}$$

$$J_{rms,add,100MHz} = \sqrt{(235.70 \text{ fs})^2 - (226.33 \text{ fs})^2}$$

$$J_{rms,add,100MHz} = 65.80 \text{ fs}$$

For this example, the additive jitter is equal to 65.80 fs. Further results can be found in Table 2.

Figure 9. Output Waveform for tr/tf Measurements at 100 MHz

Table 2. Further Results

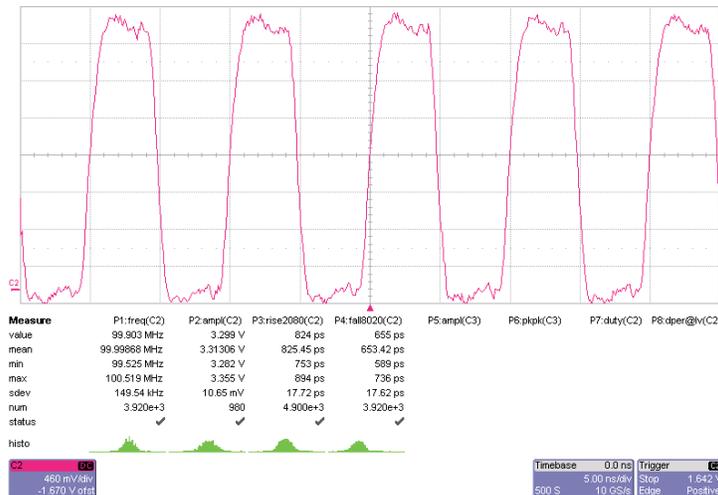| Vdd (V)	Frequency (MHz)	tr (ns)	tf (ns)	Additive Jitter rms (fs)
3.3	180	0.988	0.756	79.0
3.3	100	0.825	0.653	65.8
3.3	50	0.864	0.687	40.8
2.5	180	1.22	0.953	68.6
2.5	100	1.126	0.894	43.8
2.5	50	1.151	0.917	40.8
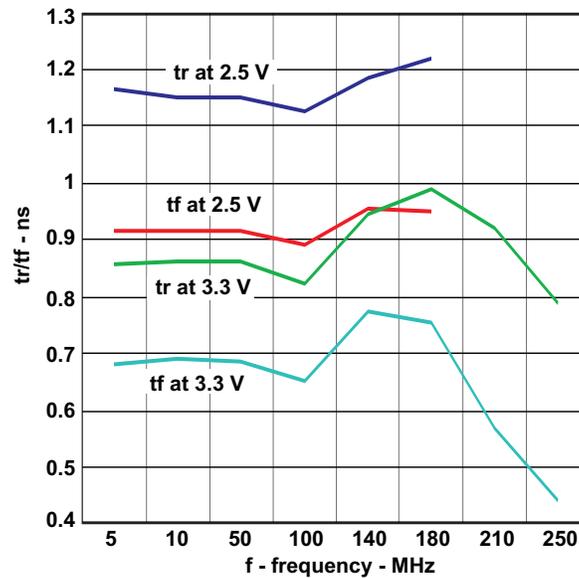
Figure 10. tr/tf vs Frequency With ac-Coupling

4   Tradeoffs

4.1   *Data Input*

If using the CDCLVC11xx for data transmission, the dc component of the signal has to be taken into account. For example, if you have zeros or ones for a long time, the signal level will rise/fall to $V_{dd}/2$ and will cross the thresholds (see Figure 11).

Figure 11. Data Input with Long-Time Ones/Zeros

If the data does not have a dc component, there is no problem. Therefore, data encoding can be used (no dc component, like (differential) Manchester-code) (see Figure 12).

Figure 12. Manchester Code With Example-Signal

4.2 Start-Up
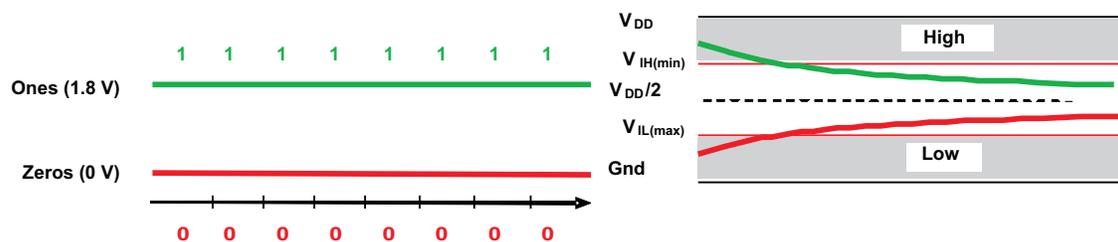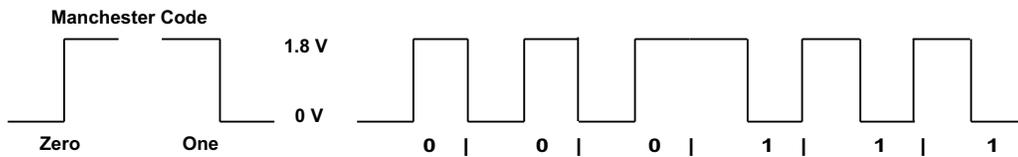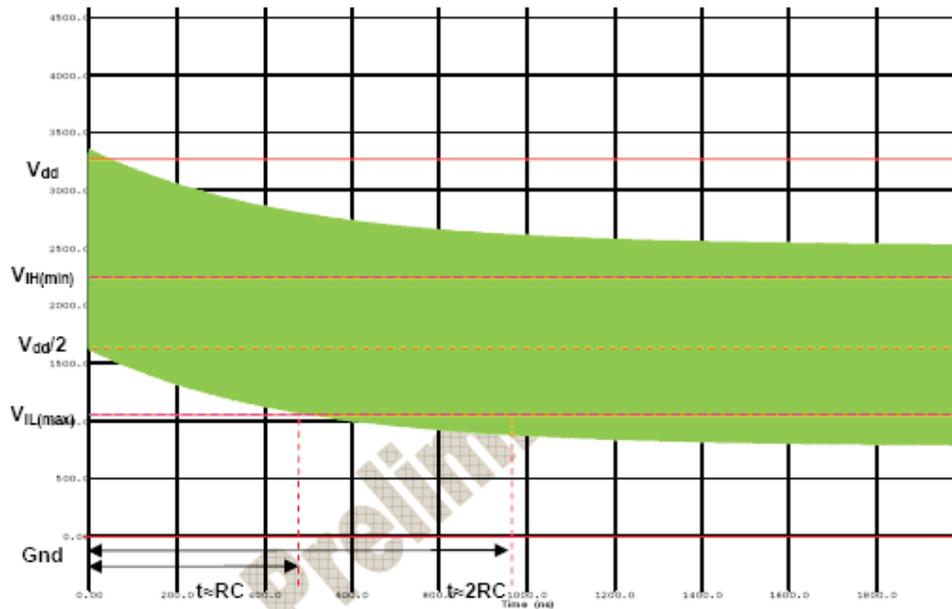

Figure 13. Start-up, C1 = 100 pF, R1 = 10 kΩ, R2 = 10 kΩ at 200 MHz

Another aspect to be considered is the transient time of the capacitor at start-up. Initially, the capacitor is charged to $V_{dd}/2$. As shown in Figure 13, the 1.8-V input signal starts at this level. Because of this, the capacitor has to be discharged so that the signal is centered to $V_{dd}/2$. However, initially, the 1.8-V swing does not reach $V_{IL(max)}$.

After almost the RC time constant t = RC, the input signal reaches both thresholds for the first time. This is because the $V_{IL(max)}$ is $V_{dd}/2$ - 600 mV and the low-level of the input signal after a long time is $V_{dd}/2$ - 900 mV. This means that the capacitor has to be discharged 66%, which is almost the RC time constant.

During this time, the output does not work properly. It is recommended that the outputs are disabled twice this time (2 × RC). Therefore, the CDCLVC11xx supports an asynchronous output enable control (1G), which switches the outputs to a low state if 1G is low.

5 Conclusion

In Figure 14 and Figure 15, the rise and fall times are compared to typical values without ac-coupling. The typical values are measured under nominal conditions on the EVM without input coupling. The input signal amplitude was equal to V_{dd}.

As this application report demonstrates, the ac-coupling does not impact the rise and fall times.
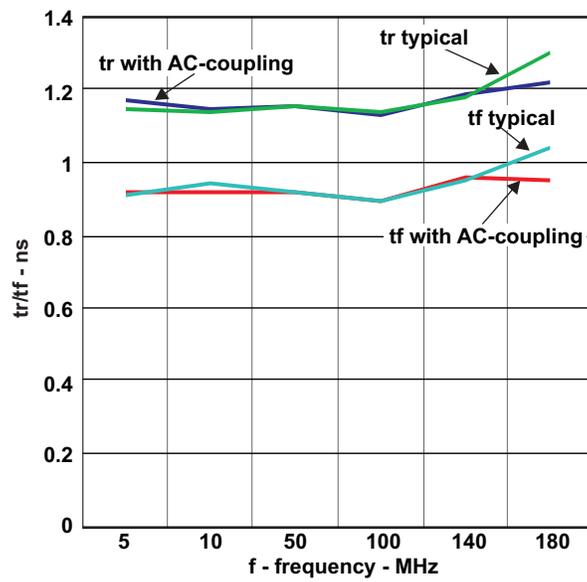
Figure 14. tr/tf With ac-Coupling Compared to Typical Values at 2.5 V
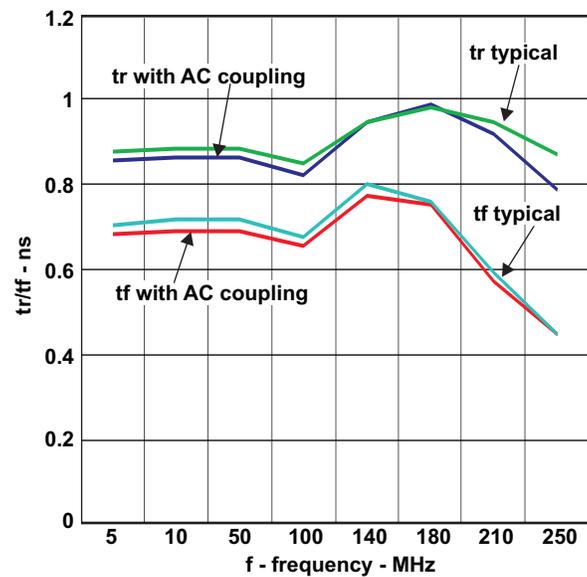

Figure 15. tr/tf With ac-Coupling Compared to Typical Values at 3.3 V

6   References

1. *CDCLVC11xx, 3.3 V and 2.5 V LVCMOS High-Performance Clock Buffer Family* data sheet (SCAS895)
2. *Low-Additive, Phase-Noise LVCMOS Clock Buffer Evaluation Board* user's guide (SCAU041)

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