Application Report

Implications of Slow or Floating CMOS Inputs

ABSTRACT

In recent years, CMOS (AC/ACT, AHC/AHCT, ALVC, CBT, CBTLV, HC/HCT, LVC, LV/LV-A) and BiCMOS (ABT, ALVT, BCT, FB, GTL, and LVT) logic families have further strengthened their position in the semiconductor market. New designs have adopted both technologies in almost every system that exists, whether it is a PC, a workstation, or a digital switch. The reason is obvious: power consumption is becoming a major issue in today's market. However, when designing systems using CMOS and BiCMOS devices, one must understand the characteristics of these families and the way inputs and outputs behave in systems. It is very important for the designer to follow all rules and restrictions that the manufacturer requires, as well as to design within the data-sheet specifications. Because data sheets do not cover the input behavior of a device in detail, this application report explains the input characteristics of CMOS and BiCMOS families in general. It also explains ways to deal with issues when designing with families in which floating inputs are a concern. Understanding the behavior of these inputs results in more robust designs and better reliability.

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1 Characteristics of Slow or Floating CMOS Inputs

Both CMOS and BiCMOS families have a CMOS input structure. This structure is an inverter consisting of a p-channel to VCC and an n-channel to GND as shown in Figure 1-1. With low-level input, the P-channel transistor is on and the N-channel is off, causing current to flow from V_{CC} and pulling the node to a high state. With high-level input, the n-channel transistor is on, the P-channel is off, and the current flows to GND, pulling the node low. In both cases, no current flows from V_{CC} to GND. However, when switching from one state to another, the input crosses the threshold region, causing the N-channel and the P-channel to turn on simultaneously, generating a current path between V_{CC} and GND. This current surge can be damaging, depending on the length of time that the input is in the threshold region (0.8 V to 2 V). The supply current (I_{CC}) can rise to several milliamperes per input, peaking at approximately 1.5-V V_I (see Figure 2-1). This is not a problem when switching states within the data-sheet-specified input transition time limit specified in the recommended operating conditions table for the specific devices. Examples are shown in Table 1-1.

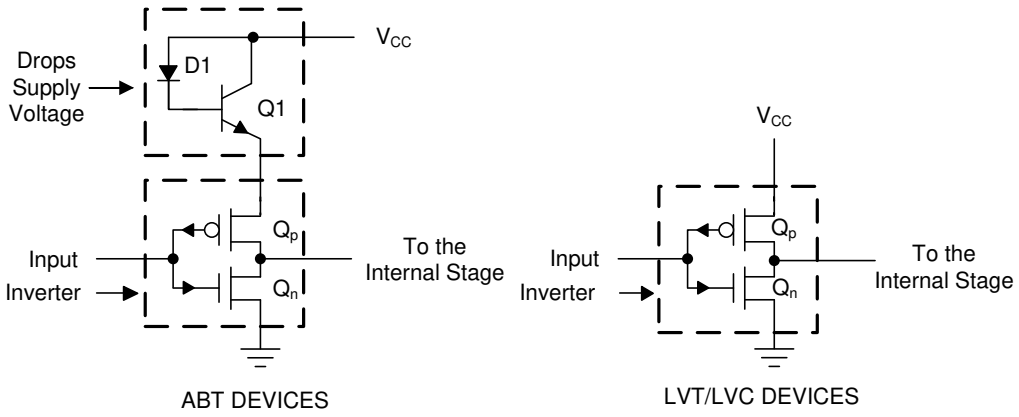
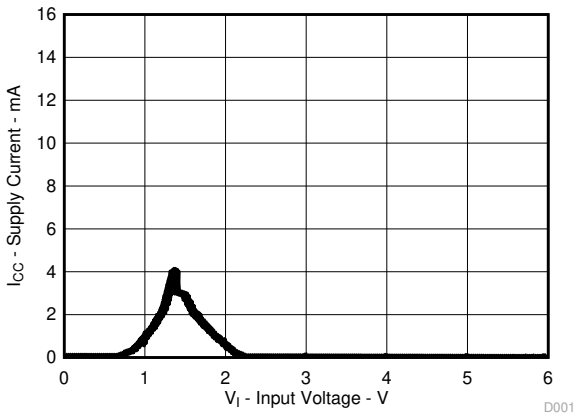


Figure 1-1. Input Structures of ABT and LVT/LVC Devices



V_{CC} = 5 V

T_A = 25°C

One Bit is Driven From 0 V to 6 V

Figure 1-2. Supply Current Versus Input Voltage (One Input)

Table 1-1. Recommended Operating Conditions

Input Transition Rise or Fall Rate as Specified in Data Sheets[1]

				MIN	MAX	UNIT
Δt/Δv	Input transition rise or fall rate	ABT octals			5	ns/V
		ABT Widebus™ and Widebus+™			10	
		AHC, AHCT			20	
		FB			10	
		LVT, LVC, ALVC, ALVT			10	
		LV			100	
		LV-A	V_{CC} = 2.3 V to 2.7 V		200	
			V_{CC} = 3 V to 3.6 V		100	
			V_{CC} = 4.5 V to 5.5 V		20	
t_t	Input transition (rise and fall) time	HC, HCT	V_{CC} = 2 V		1000	ns
			V_{CC} = 4.5 V		500	
			V_{CC} = 6 V		400	

(1) Refer to the latest TI data sheets for device specifications.

2 Slow Input Edge Rate

With increased speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output errors or oscillations. Similar situations can occur if an unused input is left floating or is not actively held at a valid logic level.

These functional problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 2-1). Because the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, inductive voltage spikes, V_{GND}, affect the way signals appear to the internal gate structures. For example, as the voltage at the device's ground node rises, the input signal, V_I', appears to decrease in magnitude. This undesirable phenomenon can then erroneously change the output if a threshold violation occurs.

In the case of a slowly rising input edge, if the change in voltage at GND is large enough, the apparent signal, V_I', at the device appears to be driven back through the threshold and the output starts to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents), the slow input edge is repeatedly driven back through the threshold, causing the output to oscillate. Therefore, the maximum input transition time of the device should not be violated, so no damage to the circuit or the package occurs.

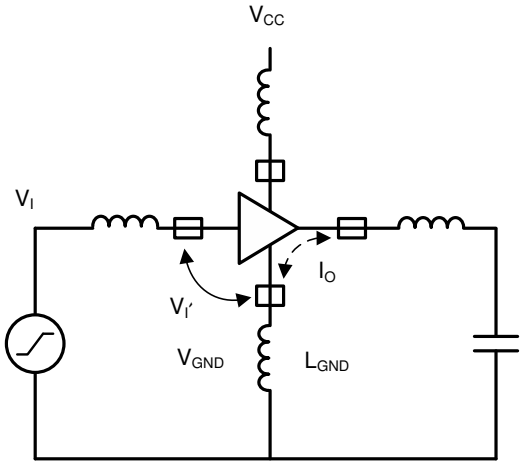


Figure 2-1. Input/Output Model

If a voltage between 0.8 V and 2 V is applied to the input for a prolonged period of time, this situation becomes critical and should not be ignored, especially with higher bit count and more dense packages (SSOP, TSSOP). For example, if an 18-bit transceiver has 36 I/O pins floating at the threshold, the current from V_{CC} can be as high as 150 mA to 200 mA. This is approximately 1 W of power consumed by the device, which leads to a serious overheating problem. This continuous overheating of the device affects its reliability. Also, because the inputs are in the threshold region, the outputs tend to oscillate, resulting in damage to the internal circuit over a long period of time. The data sheet shows the increase in supply current (ΔI_{CC}) when the input is at a TTL level [for ABT V_I = 3.4 V, ΔI_{CC} = 1.5 mA (see Table 2-1)]. This becomes more critical when the input is in the threshold region as shown in Figure 2-2.

These characteristics are typical for all CMOS input circuits, including microprocessors and memories.

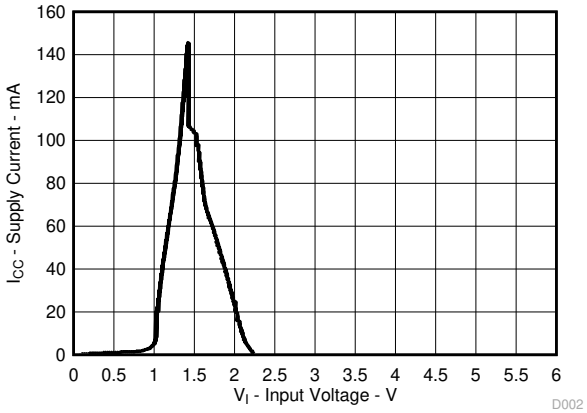
For CBT or CBTLV devices, this applies to the control inputs. For FB and GTL devices, this applies to the control inputs and the TTL ports only.

Table 2-1. Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)

Examples of Supply-Current Change of the Input at TTL Level as Specified in Data Sheets(1)

					MIN	MAX	UNIT
ΔI_{CC} (2)	ABT, AHCT	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		1.5	mA
ΔI_{CC} (2)	CBT Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		2.5	mA
ΔI_{CC} (2)	CBTLV Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND		750	µA
ΔI_{CC} (2)	LVC	V_{CC} = 3 V to 3 6 V,	One input at V_{CC} - 0.6 V,	Other inputs at V_{CC} or GND		0.2	mA
	LVC, ALVC, LV					0.5	

(1) Refer to the latest TI data sheets for device specifications.
(2) This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.



V_{CC} = 5 V

T_A = 25°C

All 36 Bits are Driven From 0 V to 6 V

Figure 2-2. Supply Current Versus Input Voltage (36 Inputs)

As long as the driver is active in a transmission path or bus, the receiver's input is always in a valid state. No input specification is violated as long as the rise and fall times are within the data-sheet limits. However, when the driver is in a high-impedance state, the receiver input is no longer at a defined level and tends to float. This situation can worsen when several transceivers share the same bus. Figure 2-3 is an example of a typical bus system. When all transceivers are inactive, the bus-line levels are undefined. When a voltage that is determined by the leakage currents of each component on the bus is reached, the condition is known as a *floating state*. The result is a considerable increase in power consumption and a risk of damaging all components on the bus.

Holding the inputs or I/O pins at a valid logic level when they are not being used or when the part driving them is in the high-impedance state is recommended.

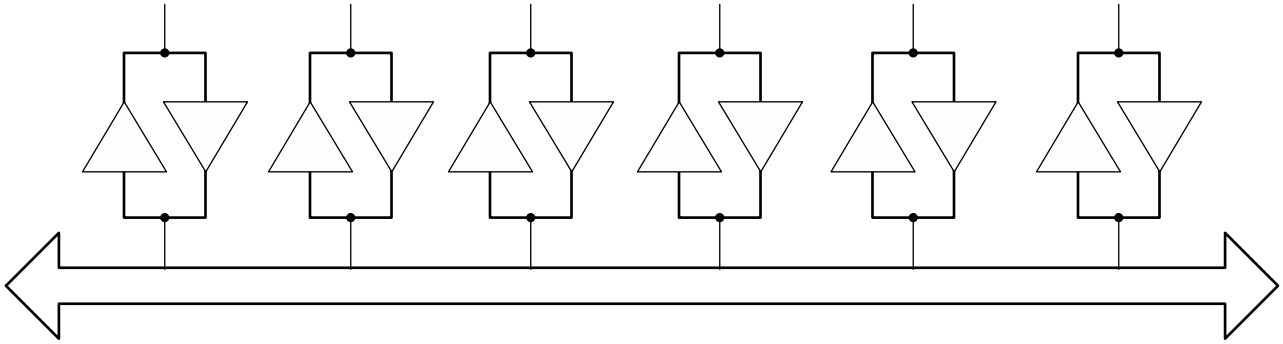


Figure 2-3. Typical Bidirectional Bus

3 Recommendations for Designing More-Reliable Systems

4 Bus Control

The simplest way to avoid floating inputs in a bus system is to ensure that the bus always is either active or inactive for a limited time when the voltage buildup does not exceed the maximum V_{IL} specification (0.8 V for TTL-compatible input). At this voltage, the corresponding I_{CC} value is too low and the device operates without any problem or concern (see Figure 1-2 and Figure 2-1).

To avoid damaging components, the designer must know the maximum time the bus can float. First, assuming that the maximum leakage current is I_{OZ} = 50 mA and the total capacitance (I/O and line capacitance) is C = 20 pF, the change in voltage with respect to time on an inactive line that exceeds the 0.8-V level can be calculated as shown in Equation 1.

$$\Delta V/\Delta t = \frac{I_{OZ}}{C} = \frac{50\ \mu A}{20\ pF} = 2.5\ V/\mu s \tag{1}$$

The permissible floating time for the bus in this example should be reduced to 320 ns maximum, which ensures that the bus does not exceed the 0.8-V level specified. The time constant does not change when multiple components are involved because their leakage currents and capacitances are summed.

The advantage of this method is that it requires no additional cost for adding special components. Unfortunately, this method does not always apply because buses are not always active.

5 Pull-up or Pull-down Resistors

When buses are disabled for more than the maximum allowable time, other ways should be used to prevent components from being damaged or overheated. A pull-up or a pull-down resistor to V_{CC} or GND, respectively, should be used to keep the bus in a defined state. The size of the resistor plays an important role and, if its resistance is not chosen properly, a problem may occur. Usually, a 1-kΩ to 10-kΩ resistor is recommended. The maximum input transition time must not be violated when selecting pull-up or pull-down resistors (see Table 1-1). Otherwise, components may oscillate, or device reliability may be affected.

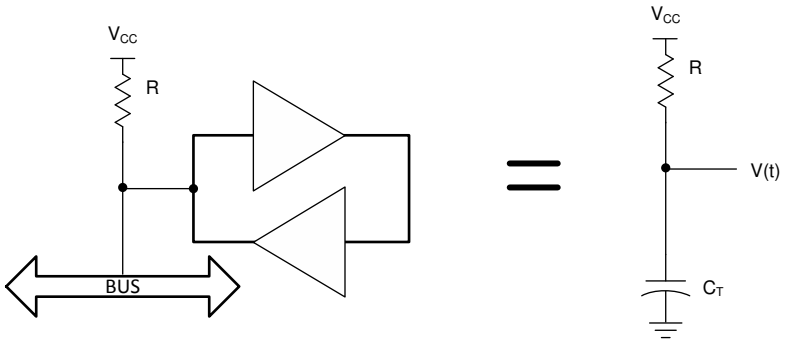


Figure 5-1. Inactive-Bus Model With a Defined Level

Assume that an active-low bus goes to the high-impedance state as modeled in Figure 5-1. C_T represents the device plus the bus-line capacitance and R is a pull-up resistor to V_{CC}. The value of the required resistor can be calculated as shown in Equation 2.

$$V(t) = V_{CC} - \left(e^{-t/RC_T}\left(V_{CC} - V_i\right)\right) \tag{2}$$

where

- V(t) = 2 V, minimum voltage at time t
- V_i = 0.5 V, initial voltage
- V_{CC} = 5 V
- C_T = total capacitance
- R = pull-up resistor
- t = maximum input rise time as specified in the data sheets (see Table 1-1).

Solving for R, the equation becomes:

$$R = \frac{t}{0.4 \times C_T} \tag{3}$$

For multiple transceivers on a bus:

$$R = \frac{t}{0.4 \times C \times N} \tag{4}$$

where

- C = individual component and trace capacitance
- N = number of components connected to the bus

Assuming that there are two components connected to the bus, each with a capacitance C = 15 pF, requiring a maximum rise time of 10 ns/V and t = 15-ns total rise time for the input (2 V), the maximum resistor size can be calculated by Equation 5:

$$R = \frac{15\ \text{ns}}{0.4 \times 15\ \text{pF} \times 2} = 1.25\ \text{k}\Omega \tag{5}$$

This pull-up resistor method is recommended for ac-powered systems; however, it is not recommended for battery-operated equipment because power consumption is critical. Instead, use the bus-hold feature that is discussed in the next section. The overall advantage of using pull-up resistors is that they ensure defined levels when the bus is floating and help eliminate some of the line reflections, because resistors also can act as bus terminations.

6 Bus-Hold Circuits

The most effective method to provide defined levels for a floating bus is to use Texas Instruments (TI™) built-in bus-hold feature on selected families or as an external component like the SN74ACT1071 and SN74ACT1073 (see Table 6-1).

Table 6-1. Devices With Bus Hold

DEVICE TYPE	BUS HOLD INCORPORATED
SN74ACT1071	10-bit bus hold with clamping diodes
SN74ACT1073	16-bit bus hold with clamping diodes
ABT Widebus+ (32 and 36 bit)	All devices
ABT Octals and Widebus	Selected devices only
AHC/AHCT Widebus	TBA (Selected devices only)
Low Voltage (LVT and ALVC)	All devices
LVC Widebus	All devices

Bus-hold circuits are used in selected TI families to help solve the floating-input problem and eliminate the need for pull-up and pull-down resistors. Bus-hold circuits consist of two back-to-back inverters with the output fed back to the input through a resistor (see Figure 6-1). To understand how the bus-hold circuit operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit. Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor. The current requirement of the bus-hold circuit is determined only by the leakage current of the circuit. The same condition applies when the bus is in the low state and then goes inactive.

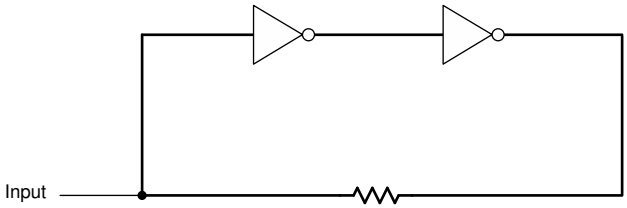


Figure 6-1. Typical Bus-Hold Circuit

As mentioned previously in this section, TI offers the bus-hold capability as stand-alone 10-bit and 16-bit devices (SN74ACT1071 and SN74ACT1073) with clamping diodes to V_{CC} and GND for added protection against line reflections caused by impedance mismatch on the bus. Because purely ohmic resistors cannot be implemented easily in CMOS circuits, a configuration known as a transmission gate is used as the feedback element (see Figure 6-2). An N-channel and a P-channel are arranged in parallel between the input and the output of the buffer stage. The gate of the N-channel transistor is connected to V_{CC} and the gate of the P-channel is connected to GND. When the output of the buffer is high, the p-channel is on, and when the output is low, the N-channel is on. Both channels have a relatively small surface area — the on-state resistance from drain to source, R_{dson}, is about 5 kΩ.

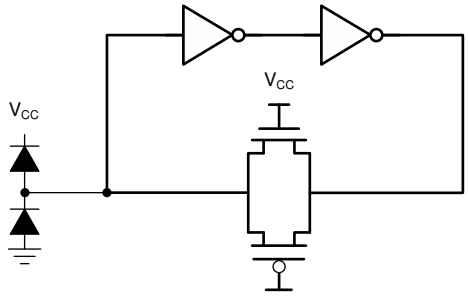
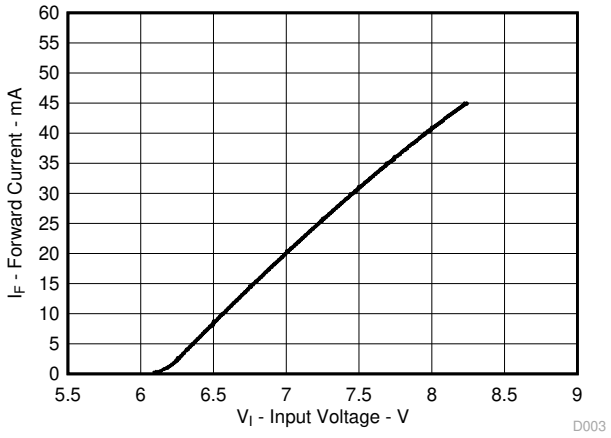


Figure 6-2. Stand-Alone Bus-Hold Circuit (SN74ACT107x)

Assume that in a practical application the leakage current of a driver on a bus is I_{OZ} = 10 mA and the voltage drop across the 5-kΩ resistance is V_D = 0.8 V (this value is assumed to ensure a defined logic level). Then, the maximum number of components that a bus-hold circuit can handle is calculated by Equation 6:

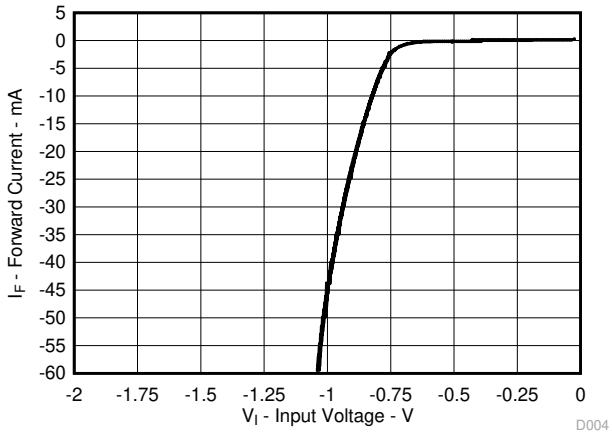
$$N = \frac{V_D}{I_{OZ} \times R} = \frac{0.8\ V}{10\ \mu A \times 5\ k\Omega} = 16\ \text{components} \tag{6}$$

The 74ACT1071 and 74ACT1073 also provide clamping diodes as an added feature to the bus-hold circuit. These diodes are useful for clamping any overshoot or undershoot generated by line reflections. Figure 6-3 and Figure 6-4 show the characteristics of the diodes when the input voltage is above V_{CC} or below GND. At V_I = –1 V, the diode can source about 50 mA, which can help eliminate undershoots. This can be very useful when noisy buses are a concern.



V_{CC} = 5 V

Figure 6-3. Upper Clamping Diode Characteristics (SN74ACT107x)



V_{CC} = 5 V

Figure 6-4. Lower Clamping Diode Characteristics (SN74ACT107x)

TI also offers the bus-hold circuit as a feature added to some of the advanced-family drivers and receivers. This circuit is similar to the stand-alone circuit, with a diode added to the drain of the second inverter (ABT and LVT only, see Figure 6-5). The diode blocks the overshoot current when the input voltage is higher than V_{CC} (V_I > V_{CC}), so only the leakage current is present. This circuit uses the device's input stage as its first inverter; a second inverter creates the feedback feature. The calculation of the maximum number of components that the bus-hold circuit can handle is similar to the previous example. However, the advantage of this circuit over the stand-alone bus-hold circuit is that it eliminates the need for external components or resistors that occupy more area on the board. This becomes critical for some designs, especially when wide buses are used. Also, because cost and board-dimension restrictions are a major concern, designers prefer the easy fix: drop-in replaceable parts. TI offers this feature in most of the commonly used functions in several families (refer to Table 6-1 for more details).

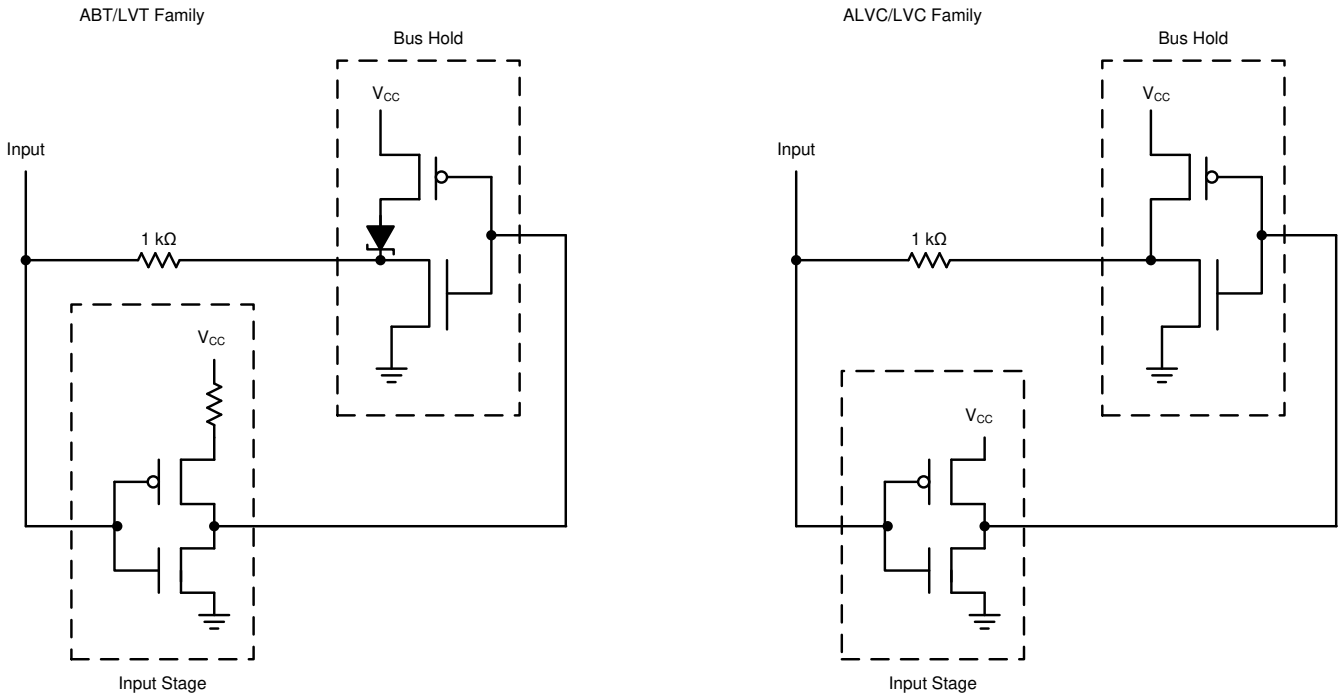


Figure 6-5. Input Structure of ABT/LVT and ALVC/LVC Families With Bus-Hold Circuit

Figure 6-6 and Figure 6-7 show the input characteristics of the bus-hold circuit at 3.3-V and 5-V operations, as the input voltage is swept from 0 to 5 V. These characteristics are similar in behavior to a weak driver. This driver sinks current into the part when the input is low and sources current out of the part when the input is high. When the voltage is near the threshold, the circuit tries to switch to the other state, always keeping the input at a valid level. This is the result of the internal feedback circuit. The plot also shows that the current is at its maximum when the input is near the threshold. $I_{I(hold)}$ maximum is approximately 25 mA for 3.3-V input and 400 mA for 5-V input.

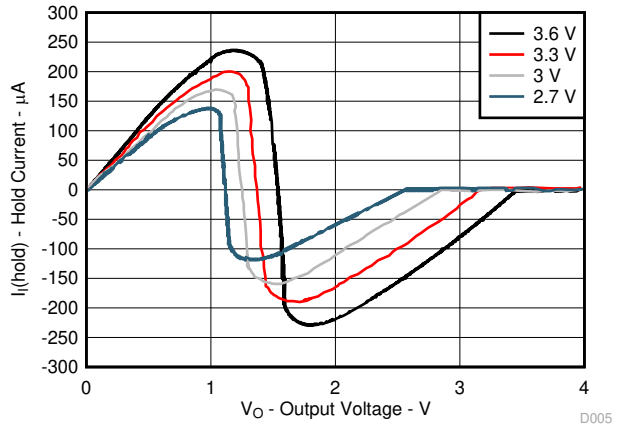


Figure 6-6. V_O —Output Voltage—V Bus-Hold Input Characteristics

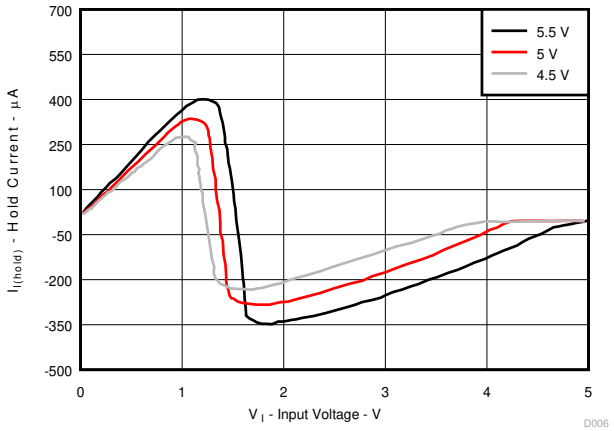


Figure 6-7. V_I —Input Voltage—V Bus-Hold Input Characteristics

When multiple devices with bus-hold circuits are driven by a single driver, there may be some concern about the ac switching capability of the driver becoming weaker. As small drivers, bus-hold circuits require an ac current to switch them. This current is not significant when using TI CMOS and BiCMOS families. Figure 6-8 shows a 4-mA buffer driving six LVTH16244 devices. The trace is a 75-Ω transmission line. The receivers are separated by 1 cm, with the driver located in the center of the trace. Figure 6-9 and Figure 6-10 show the bus-hold loading effect on the driver when connected to six receivers switching low or high. Figure 6-9 and Figure 6-10 also show the same system with the bus-hold circuit disconnected from the receivers. Both plots show the effect of bus hold on the driver's rise and fall times. Initially, the bus-hold circuit tries to counteract the driver, causing the rise or fall time to increase. Then, the bus-hold circuit changes states (note the crossover point), which helps the driver switch faster, decreasing the rise or fall time.

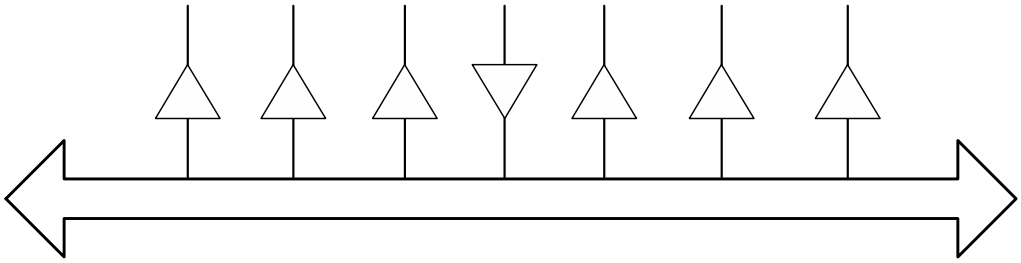
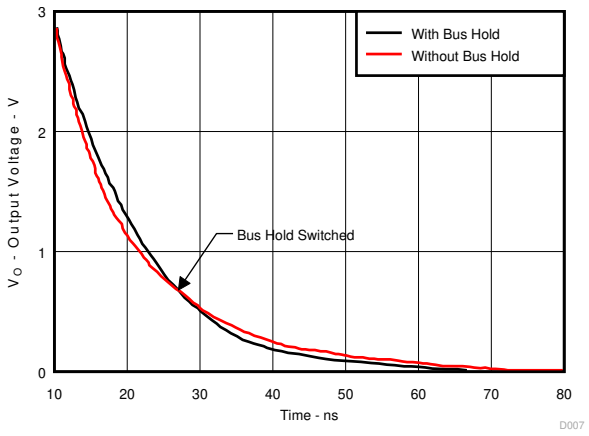
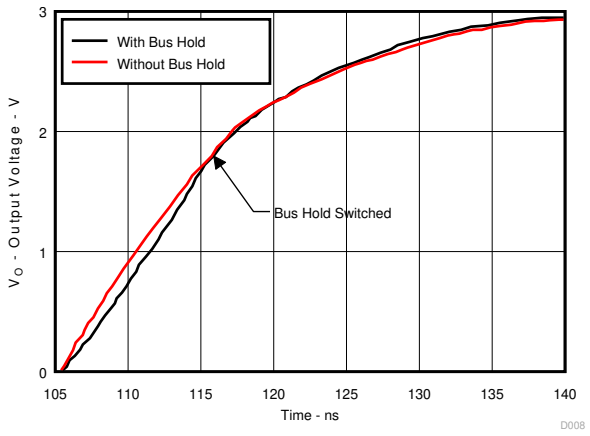


Figure 6-8. Driver and Receiver System



V_{CC} = 3.3 V T_A = 25°C

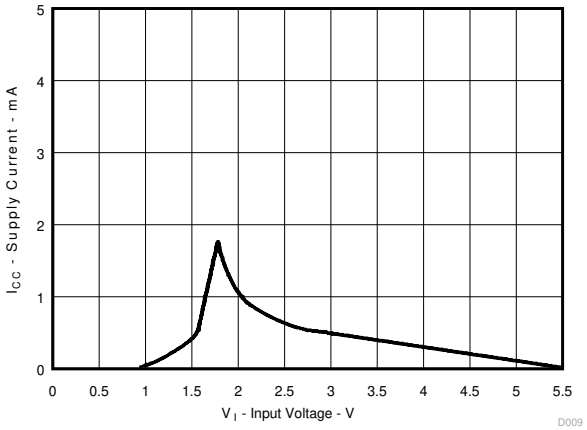
Figure 6-9. Driver Switching From High to Low Output Waveforms of Driver With and Without Receiver Bus-Hold Circuit



V_{CC} = 3.3 V T_A = 25°C

Figure 6-10. Driver Switching From Low to High Output Waveforms of Driver With and Without Receiver Bus-Hold Circuit

Figure 6-11 shows the supply current (I_{CC}) of the bus-hold circuit as the input is swept from 0 to 5 V. The spike at about 1.5-V V_I is due to both the N-channel and the P-channel conducting simultaneously. This is one of the CMOS transistor characteristics.



V_{CC} = 5 V

Figure 6-11. Bus-Hold Circuit Supply Current Versus Input Voltage

The power consumption of the bus-hold circuit is minimal when switching the input at higher frequencies. Figure 6-12 and Figure 6-13 show the power consumed by the input at different frequencies, with or without bus hold. The increase in power consumption of the bus-hold circuit at higher frequencies is not significant enough to be considered in power calculations.

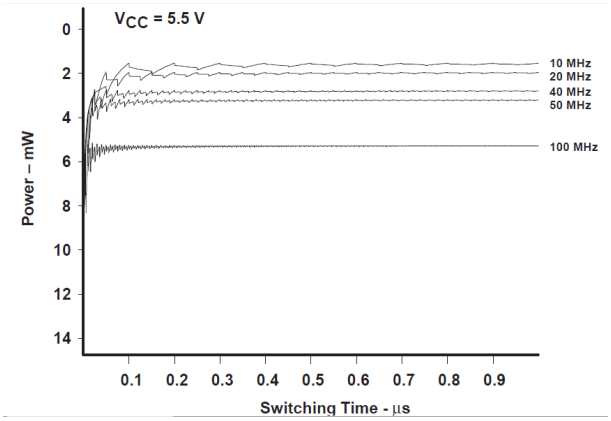


Figure 6-12. Power Plot of the Input Power With Bus Hold at Different Frequencies

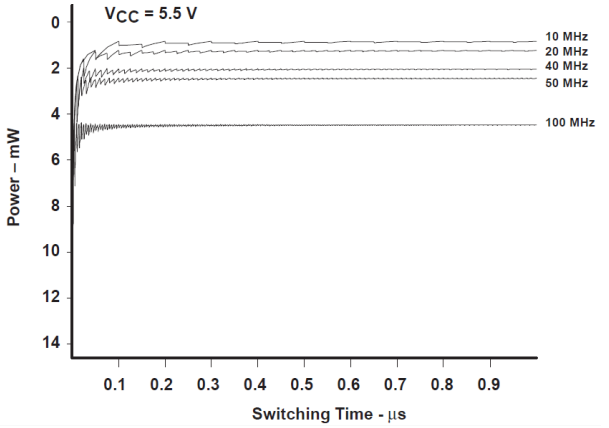


Figure 6-13. Power Plot of the Input Power Without Bus Hold at Different Frequencies

Table 6-2 shows the data-sheet dc specifications for bus hold. The first test condition is the minimum current required to hold the bus at 0.8 V or 2 V. These voltages meet the specified low and high levels for TTL inputs. The second test condition is the maximum current that the bus-hold circuit sources or sinks at any input voltage between 0 V and 3.6 V (for low-voltage families) or between 0 V and 5.5 V (for ABT). The bus-hold current becomes minimal as the input voltage approaches the rail voltage. The output leakage currents, I_{OZH} and I_{OZL}, are insignificant for transceivers with bus hold because a true leakage test cannot be performed due to the existence of the bus-hold circuit. Because the bus-hold circuit behaves as a small driver, it tends to source or sink a current that is opposite in direction to the leakage current. This situation is true for transceivers with the bus-hold feature only and does not apply to buffers. All LVT, ABT Widebus+, and selected ABT octal and Widebus devices have the bus-hold feature (see Table 6-1 or contact the local TI sales office for more information).

Table 6-2. Example of Data Sheet Minimum Specification for Bus Hold

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range (Unless Otherwise Noted)(1)

					MIN	MAX	UNIT
$I_{I(hold)}$	Data inputs or I/Os	LVT, LVC, ALVC	V_{CC} = 3 V	V_I = 0.8 V	75		µA
				V_I = 2 V	–75		
		LVC, ALVC	V_{CC} = 3.6 V	V_I = 0 to 3.6 V		±500	
		ABT Widebus+ and selectedABT	V_{CC} = 4.5 V	V_I = 0.8 V	100		
				V_I = 2 V	–100		
I_{OZH}/I_{OZL}	Transceivers with bus hold	ABT	This test is not a true I_{OZ} test because bus hold always is active on an I/O pin. Bus hold tends to supply a current that is opposite in direction to the output leakage current.			±1	µA
		LVT, LVC, ALVC					
	Buffers with bus hold	ABT	This test is a true I_{OZ} test since bus hold does not exist on an output pin.			±10	
		LVT, LVC, ALVC				±5	

(1) Refer to the latest TI data sheets for device specifications.

7 Summary

Floating inputs and slow rise and fall times are important issues to consider when designing with CMOS and advanced BiCMOS families. It is important to understand the complications associated with floating inputs. Terminating the bus properly plays a major role in achieving reliable systems. The three methods recommended in this application report should be considered. If it is not possible to control the bus directly, and adding pull-up or pull-down resistors is impractical due to power-consumption and board-space limitations, bus hold is the best choice. TI designed bus hold to reduce the need for resistors used in bus designs, thus reducing the number of components on the board and improving the overall reliability of the system.

8 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (September 2016) to Revision E (December 2020) **Page**

- Updated the numbering format for tables, figures, and cross-references throughout the document.....2
- Updated the format of the *Example of Data Sheet Minimum Specificaiton for Bus* figure.....7

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