

***SN74CBTS3384 Bus Switches
Provide Fast Connection
and Ensure Isolation***

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Contents

	<i>Title</i>	<i>Page</i>
Introduction		1
The Mechanics of the MOSFET Switch Leading to False Switching		1
Disruption of the Bus		2
The SN74CBTS3384 Solution		3
Conclusion		4
Acknowledgment		4

List of Illustrations

<i>Figure</i>	<i>Title</i>	<i>Page</i>
1	The SN74CBTS3384 With Schottky Diodes Attached at Both Ports	1
2	Switching Mechanics of the NMOS Switch	1
3	Mechanics Behind False Switching	2
4	The Effect of Bus Interruption on Data Flow and Signal Integrity	2
5	Test Conditions of the SN74CBTS3384 With Switch Disabled	3
6	V_O Versus V_I of the SN74CBTS3384 and a SN74CBT3384A in the Disabled State	3
7	Input Current Versus V_I of SN74CBTS3384 in the Disabled State	4

Introduction

Buses are the pathways for communication between the CPU, memory, and I/O ports in electronic systems. Today's standards demand both fast connection as well as isolation of these buses. Bus switches are usually used to address these demands because the use of a single MOSFET provides negligible propagation delay, low power dissipation and bidirectional switching; however, the use of a single transistor also can allow large negative undershoots below -1 V to cause unwanted switching and possible disruption of the bus. To prevent this problem from occurring, the SN74CBTS3384 bus switches are developed with Schottky diodes at the inputs that clamp any undershoot to approximately -300 mV (see Figure 1).

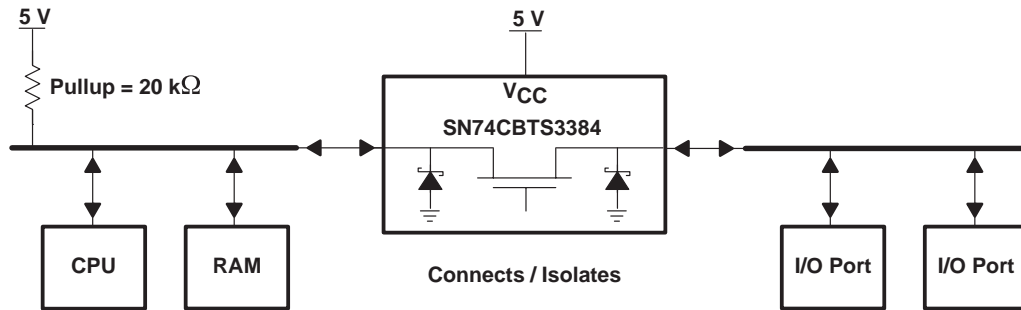
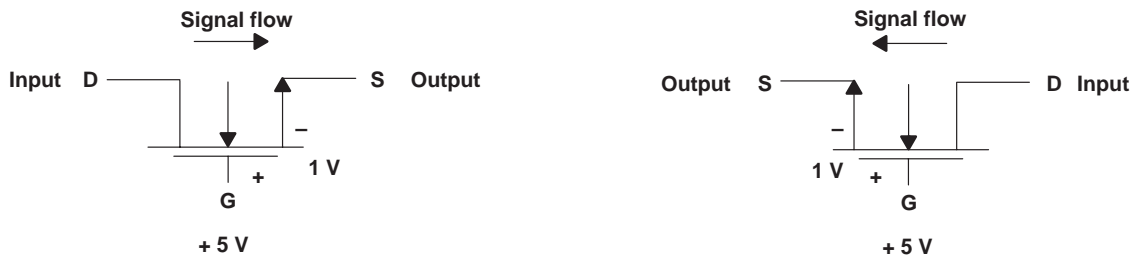


Figure 1. The SN74CBTS3384 With Schottky Diodes Attached at Both Ports

The Mechanics of the MOSFET Switch Leading to False Switching

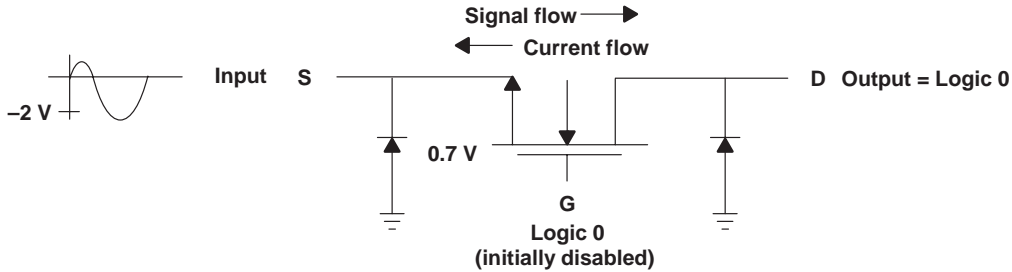
The MOSFET is used for bus switches because of its enabling and disabling speed, its low on-state resistance, and its high off-state resistance. The substrate of the N-channel MOSFET is grounded and the two n-type doped regions are interchangeable. As shown in Figure 2, when a logic high is applied to the gate, the region with a voltage of 1 V or more below the gate becomes the source and the other region the drain. At this point, the switch turns fully on and a signal flows from the input side. While this physical structure of the MOSFET provides bidirectional capability in a switch, it also allows large negative undershoots on either port to turn on a disabled switch.



The interchangeability of the source and drain provides bidirectional signal flow.

Figure 2. Switching Mechanics of the NMOS Switch

As Figure 3 shows, even though the switch is initially disabled and there is a logic low at the gate, large negative undershoots at the input cause the existing clamping diode to clamp to approximately -650 mV . Since this voltage is parallel to the gate-to-source voltage of the transistor and lasts for a few nanoseconds, the transistor starts conducting a certain amount of current. This causes a logic low to appear on the bus and disrupts any signals on it.

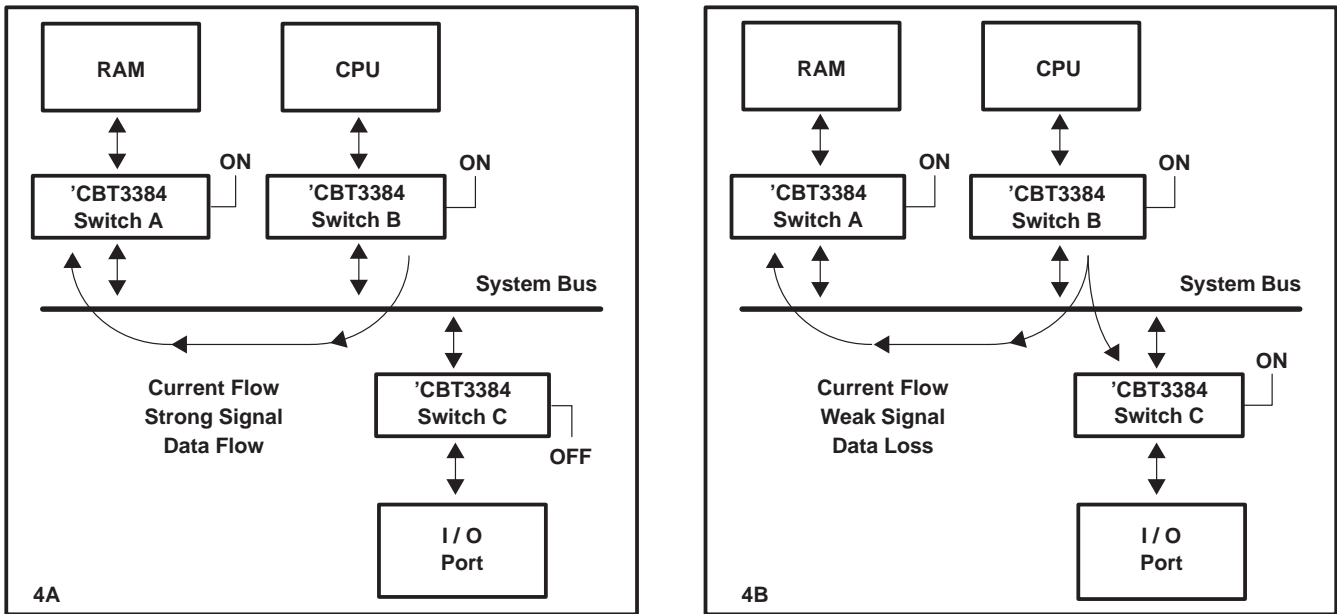


Output enable ($\overline{\text{OE}}$) is high, but large negative undershoot causes NMOS switch to turn on.

Figure 3. Mechanics Behind False Switching

Disruption of the Bus

False switching can disrupt the bus in many ways. Bus switches connect two buses or several components on a bus when on, and isolates them when off. Because each component has a certain amount of capacitance, an unexpected connection loads the bus with additional capacitance. Under normal circumstances, a signal is given enough drive to charge the expected capacitance on the bus and then switch voltage levels at the receiver. A signal propagating on the disrupted line may not have enough drive to overcome the additional load capacitance. In fact, the logic low introduced to the bus by the false connection can absorb some of the drive current from the signal. In any case, the end result is signal weakening, loss of speed, and failure to switch voltage levels at the receiver. Figure 4A shows a transaction between a CPU and a RAM chip connected by switches A and B. When switch C is off, the data flow is uninterrupted. As shown in Figure 4B, switch C can turn on unexpectedly and connect the I/O port to the bus. This results in signal degradation and data loss.



Uninterrupted data flow from CPU to RAM

Resulting bus interruption and data loss

Figure 4. The Effect of Bus Interruption on Data Flow and Signal Integrity

False switching also can cause bus contention, a case occurring when two or more transmitters on a bus are active at the same time. If the logic levels of these outputs are different, a high current flows on the line, possibly damaging the line or the components connected to it. These problems can cause serious setbacks to the high performance and reliability demands of today's systems. The use of the SN74CBTS3384 bus switch helps prevent false switching and addresses many of these problems.

The SN74CBTS3384 Solution

The SN74CBTS3384 utilizes Schottky diode at the inputs to clamp undershoot to about 300 mV below ground (see Figure 5). With the gate grounded in the disabled state, the Schottky diode prevents the gate-to-source voltage from exceeding the threshold voltage of the NMOS transistor, thus preventing weak enabling. In addition, a disabled SN74CBTS3384 switch offers a very low capacitance of about 6 pF and very low leakage current. Figure 5 shows total leakage current of only 2 μ A. As a result, the disabled SN74CBTS3384 bus switch succeeds in isolating its output from any unwanted undershoots at the input. The buses are left uninterrupted and the signals on the buses are not disturbed.

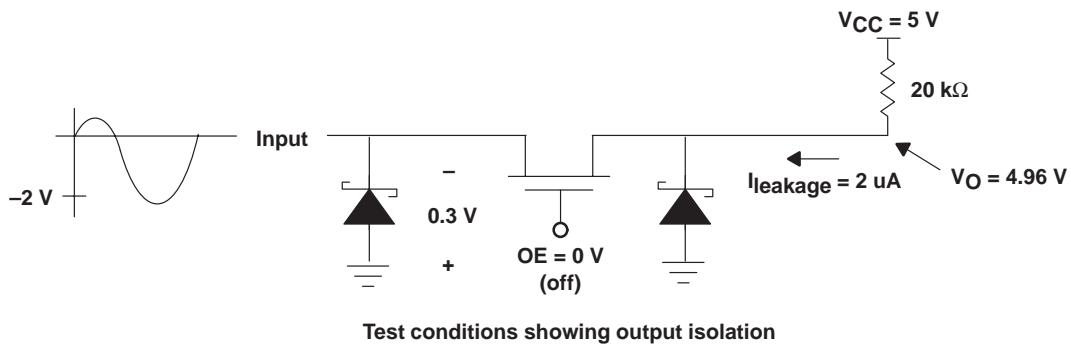


Figure 5. Test Conditions of the SN74CBTS3384 With Switch Disabled

Figure 6 shows the output of a disabled SN74CBT3384A (without Schottky diodes) as it turns on and follows the input to a negative level. This level is low enough to possibly disrupt the bus. Figure 6 also shows the SN74CBTS3384 where the Schottky diode prevents any switching throughout the wide input sweep and keeps the output at a steady level. Figure 7 shows the input current of the SN74CBTS3384 as the Schottky diode turns on, conducting about 10 mA from ground.

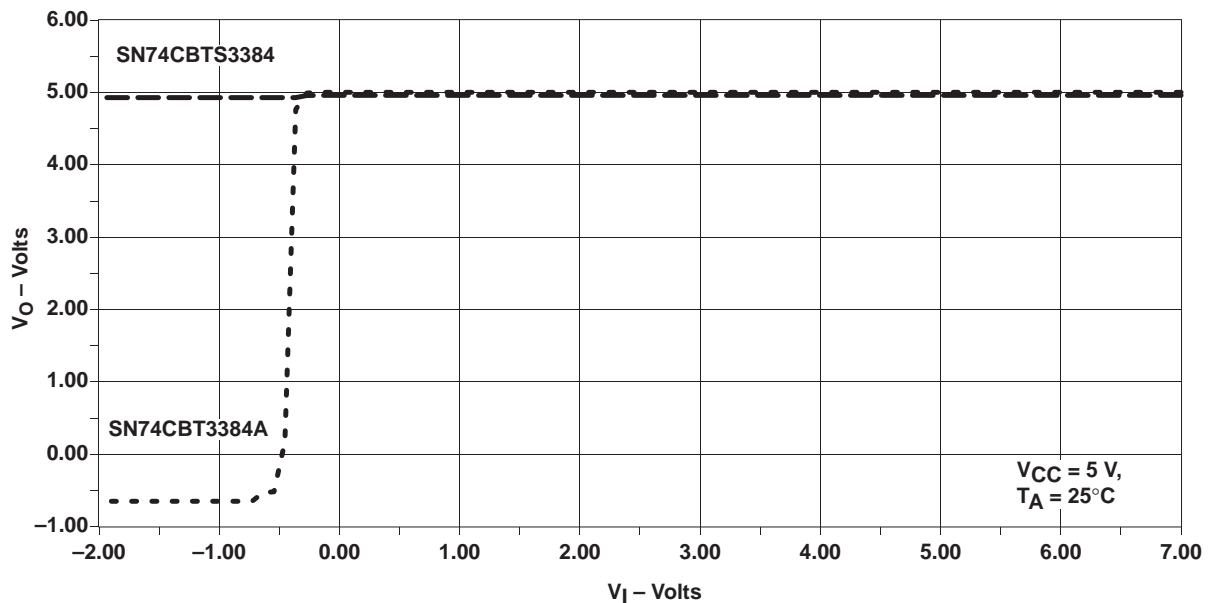


Figure 6. VO vs VI of the SN74CBTS3384 and a SN74CBT3384A in the Disabled State

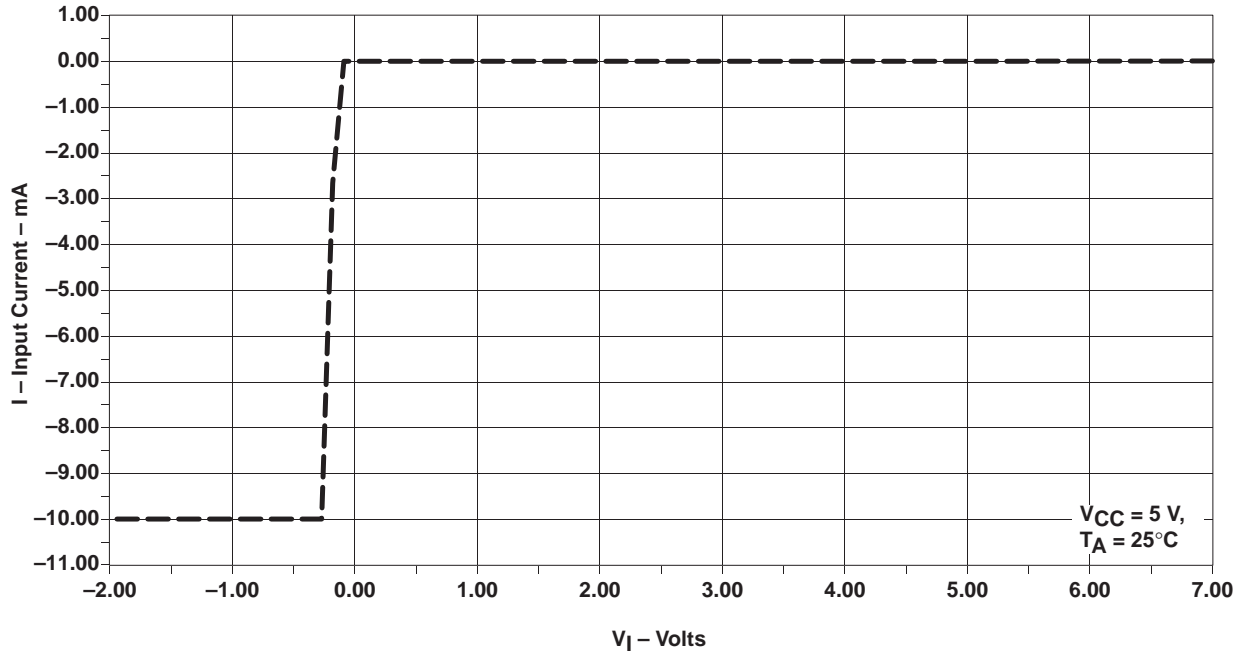


Figure 7. Input Current vs V_I of SN74CBTS3384 in the Disabled State

Conclusion

The SN74CBTS3384 bus switch provides a high-speed, low-power solution to bus connection, while providing a reliable solution to bus isolation. As a result, buses function properly without any problematic interruptions and the high-performance demands of today's systems are easily reached.

Acknowledgment

The author of this report is Nalin Yogasundram.