Application Report

Using Latch-Up Immune Multiplexers to Help Improve System Reliability

1 Abstract

In CMOS based IC's there is an undesirable phenomena known as latch-up; where the system's operating conditions or transient events can create a short circuit between the power rails of the IC. What the source is for latch-up, the causes of latch-up, what latch-up immunity means to an analog multiplexer, and how using latch-up immune multiplexers can improve system reliability are briefly discussed in this application note.

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Trademarks

2 The Causes of Latch-Up in CMOS Devices

In CMOS based IC's, the P-doped and N-doped regions of different NMOS and PMOS circuits can create a parasitic PNPN structure that acts similarly to a silicon controlled rectifier, a SCR. Figure 2-1 shows the SCR that forms in a typical CMOS process inverter with a P-type substrate and an N-well. A PNP BJT is created with the emitter on the P+ source or drain of the PMOS, the base located in the N-Well, and the collector is formed in the P-substrate. The NPN BJT is formed with the collector located in the N-Well, the base in the P-substrate, the emitter tied to the N+ source or drain of the NMOS. The resulting Equivalent Circuit is found in Figure 2-2.

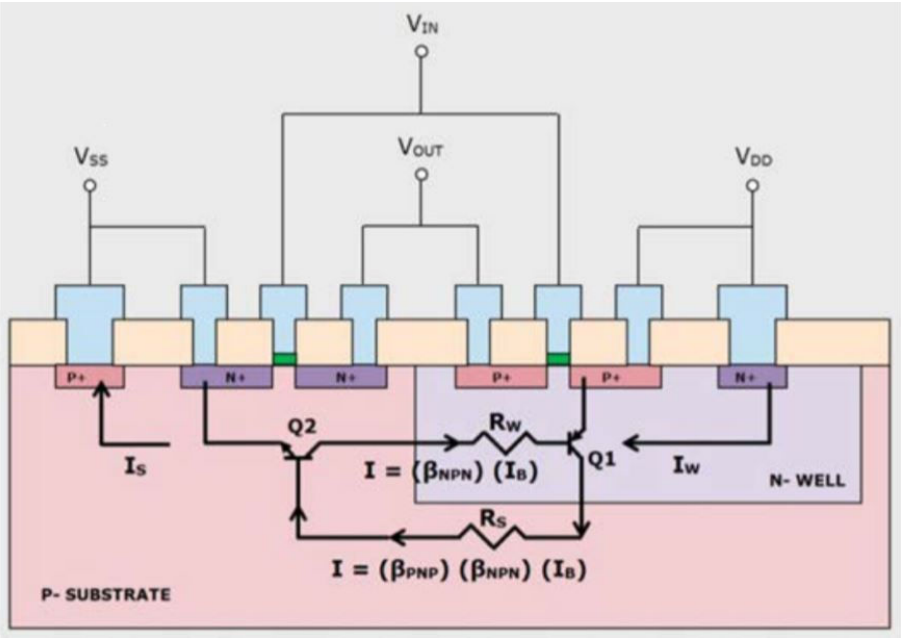

Figure 2-1. SCR Formation In CMOS Process: Inverter

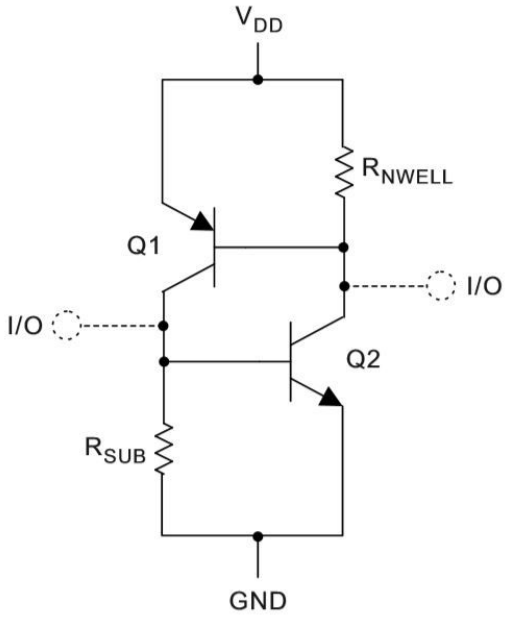

Figure 2-2. SCR Equivalent Circuit

Under normal operating conditions, where the I/O voltage is greater or equal to ground and less than or equal to VDD, both of the parasitic transistors are in the cutoff region. This means there is no low-impedance pathway while the BJT's are not conducting. However, if an event on the I/O occurs that causes either of the BJT's to begin to conduct, the other one will too. Both BJT's will be in the saturation region of operation until the power is cycled, or the device is destroyed due to overcurrent.

There are three common causes of a latch-up event in a system:

1. Applying a voltage beyond the supply rails on the I/O pins of the CMOS system. Looking back towards the circuit in Figure 2-2, if any of the I/O voltages go beyond the supply rails this can cause the BJT's to start conducting and initiate a latch-up event.
2. A current injection into the I/O of the device. If the current injection event causes enough charge to flow into the parasitic SCR, the device will begin to conduct, initiating a latch-up event.
3. Leakage currents present on the I/O of a device can be large enough to cause the SCR to conduct which will lead to a latch-up event.

3 Latch-Up Immunity and Analog Multiplexers

The likelihood of PNPN Thyristor forming, also called Silicon Controlled Rectifiers (SCRs), increases in analog multiplexers, much like other anlaog IC's, because process technology allows for a smaller feature size and higher density placement of transistors. If any pin, excluding the VSS and VDD pins, is connected to a thyristor a latch-up event can occur.

Analog multiplexers that are not latch-up immune can operate safely within the recommended ratings of the device. A latch-up event can be triggered, however, if an event causes any of the multiplexer's pins to either violate the absolute maximum current or voltage. During this event the multiplexer will short the VDD rail to the VSS rail. This structure will continue to conduct until the power is cycled or the device is destroyed due to overcurrent. These types of devices are not well suited for harsh operating environments conditions due to the fact that overshoots or current injections may cause the multiplexer to fail, leading to possible system failure.

Ideally there wouldn't be a need to operate past the recommended operating conditions but due to harsh environments, overvoltage spikes, transients, or current injection can lead to exceeding maximum ratings and cause latch-up. This creates the need for parts that can handle more extreme environments. Multiplexers that are latch-up immune are constructed so that latch-up events will not be triggered due to overvoltage or current injections.

Using silicon on insulator (SOI) based processes can prevent parasitic structures from forming by adding an oxide layer in-between the P and N type MOSFETs. The oxide layer is also known as an insulating trench, a simplified model of this is shown in Figure 3-1. Without these structures the Latch-Up Event does not occur. However, insulators cannot be placed everywhere in all IC's, so other methods are implemented such as guard rings as shown in Figure 3-2. These guard rings act as charge siphons so that during an overvoltage or current injection event, charge can be siphoned away from the parasitic structure helping prevent it from triggering a latch-up event.

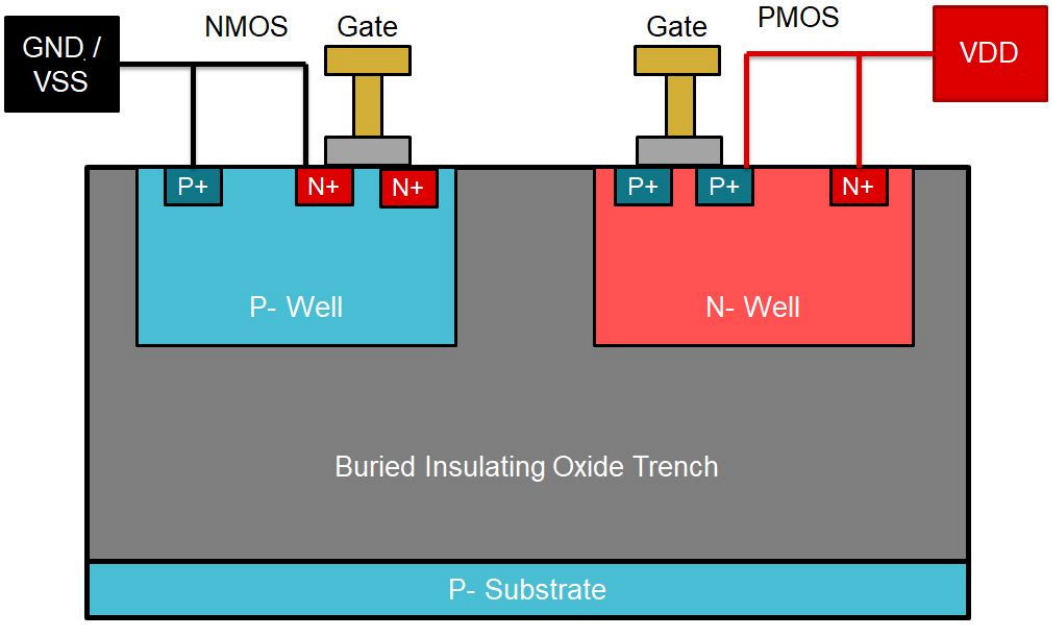

Figure 3-1. Latch-Up Prevention: Buried Insuluting Oxide Trench

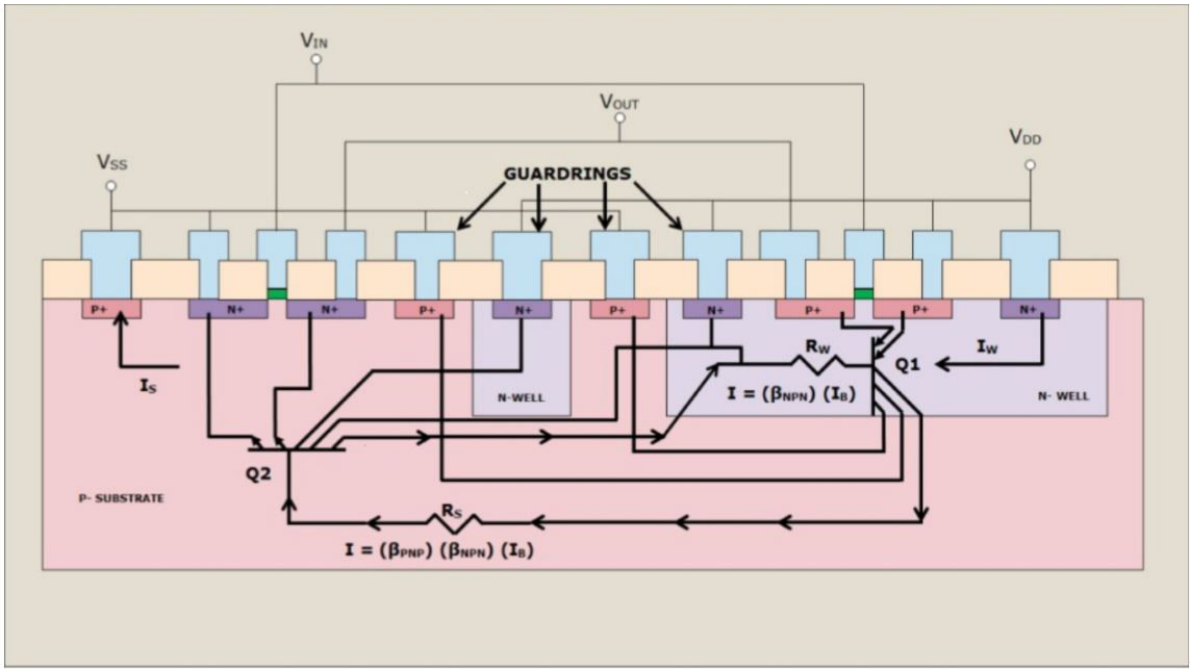

Figure 3-2. Latch-Up Prevention: Guard Ring Usage

4 Latch-Up Immune Multiplexers and System Reliability

One of the most important objectives of any system designer is to ensure that the system will continue to operate as intended for the environment it was designed for. In harsh environments electrical systems are often subjected to transient events that violate the typical operating conditions of the system. A typical system diagram is shown in Figure 4-1.

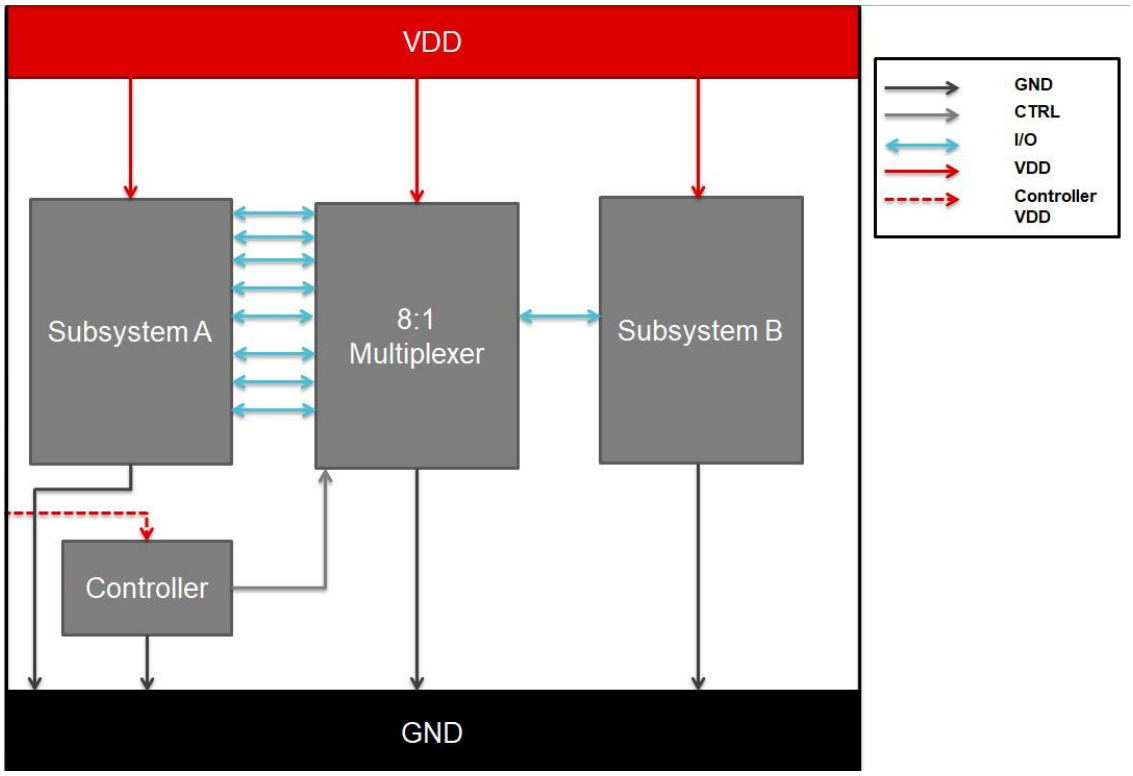

Figure 4-1. Generic 8:1 Multiplexer Application

In Figure 4-1, if the multiplexer being used is not latch-up immune, a transient spike on either the through paths or control pins of the multiplexer could trigger a latch-up event. The multiplexer will be ruined by overcurrent if the power is not cycled quickly enough; however, this is not the only concern. When the power supply rails are shorted together, causing any system directly powered or derives its power from the rail in which a device is suffering from latch-up, then the multiplexer becomes damaged and other parts of the system will face sudden unexpected loss of power.

A latch-up immune multiplexer, such as TI's mid voltage range TMUX72xx and TMUX73xxF families, is needed to avoid a situation like this and to simplify the design process. The TMUX72xx family provides latch-up immunity, preventing undesirable high current events between parasitic structures within the device typically caused by overvoltage events. A latch-up condition typically continues until the power supply rails are turned off and can lead to device failure. The latch-up immunity feature allows the TMUX72xx family of switches and multiplexers to be used in harsh environments

See Table 4-1 for a list of TI's latch-up immune multiplexers.

Table 4-1. TI's Latch-Up Immune Multiplexers

Device	Configuration	Channels	Supply Rails
TMUX7208	8:1	1	44V – Single ±22 V - Bipolar
TMUX7211	1:1	4	44V – Single ±22 V - Bipolar
TMUX7212	1:1	4	44V – Single ±22 V - Bipolar
TMUX7213	1:1	4	44V – Single ±22 V - Bipolar
TMUX7219	2:1	1	44V – Single ±22 V - Bipolar

5 References

- Texas Instruments, Marty Johnson, Roger Cline, Scott Ward, Joe Schichl, Latch Up White Paper
- Texas Instruments, Eilhard Haseloff, Latch Up, ESD, and Other Phenomena Application Report
- Texas Instrument, TMUX7219 44-V, Latch-Up Immune, 2:1 (SPDT) Precision Switch with 1.8-V Logic data sheet

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