Application of the Texas Instruments AUC Sub-1-V Little Logic Devices

Chris Maxwell and Tomdio Nana *Standard Linear & Logic*

ABSTRACT

Power consumption and speed are always concerns in electronic system logic design. Texas Instruments (TI) announces the industry's first sub-1-V logic family that provides significant benefits to portable consumer electronics by operating at low power and high speed, while maintaining overall system signal integrity. TI's next-generation logic family is the advanced ultra-low-voltage CMOS (AUC) family. Although optimized for 1.8-V operation, AUC logic supports mixed-voltage systems because it is compatible with 0.8-V, 1.2-V, 1.5-V and 2.5-V devices. The AUC logic inputs tolerate 3.6-V signals, thus enabling level-translation down from 3.3-V nodes to lower-voltage nodes. Further, AUC logic has the I_{off} feature, which supports the partial-power-down mode of operation. This application report discusses AUC Little Logic device features, characteristics, and applications.

Keywords: 0.8 V, 1.2 V, 1.5 V, 1.8 V, 2.5 V, 3.3-V tolerant, AUC, electrical performance, I_{off}, level translation, Little Logic, open drain, overvoltage protection, partial power down, signal integrity, ULTTL

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1 Introduction

Many electronic applications have shifted from the legacy bipolar TTL interface to CMOS rail-to-rail interface. The CMOS technology has facilitated supply-voltage migration from 5 V to 3.3 V, 2.5 V, 1.8 V, 1.5 V, 1.2 V, and 0.8 V. These lower-voltage nodes allow decreased power consumption in the system. To facilitate migration to lower-voltage nodes, TI has released the advanced ultra-low-voltage CMOS (AUC) family, which is optimized for 1.8-V operation and is compatible with 0.8-V, 1.2-V, 1.5-V, 1.8-V, and 2.5-V devices.

TI offers the AUC functions in Widebus™, octal, gates, and Little Logic (single, double, and triple gate) options. The widebus, octal, and gate AUC devices are designed for high-speed data throughput and enhanced signal integrity to target bus applications in telecommunications and computing systems. The Little Logic AUC devices have high speed, low power consumption, and low-noise characteristics, which make them suitable for portable consumer electronics applications.

This application report discusses AUC Little Logic device features, characteristics, and applications.

2 AUC Little Logic Features

The AUC Little Logic devices are designed for use in battery-operated portable consumer electronics or to fix design bugs in electronic systems. The characteristic output structure, level-translation support capability, and partial-power-down support features of the AUC Little Logic facilitate the use of these devices in their targeted applications.

2.1 Novel Output Structure

The AUC Little Logic features the ultra-low-voltage transistor-transistor logic (ULTTL) output driver. The ULTTL is a new CMOS-technology interface driver designed for applications requiring high-speed, low power consumption, and optimal signal integrity, while maintaining the bipolar TTL output characteristic of reduced line-reflection noise. With the migration from bipolar TTL technology to CMOS technology for lower-operating-voltage nodes, the ULTTL output driver was developed to minimize switching noise, which is inherent in high-speed applications.

The ULTTL output driver of the AUC Little Logic changes impedance during transition. Three basic output features are critical for optimal performance in low-voltage high-speed applications. First, the device must provide low-impedance (i.e., high dynamic current) drive during the initial phase of the transition through the ac threshold (i.e., $V_{CC}/2$). This initial high drive provides the quick transition to the desired logic level and ensures that system timing is preserved. During the second phase of the transition, the impedance must be equal to that of the transmission-line medium it is driving, to minimize ringing and optimize signal integrity. A major cause of ringing in point-to-point applications is the result of a mismatch or discontinuity between the output impedance of the driver and the impedance of the transmission line (i.e., PCB trace). AUC Little Logic devices have been optimized for transmission lines of 50 Ω to 65 Ω, which is typical of most portable PCB applications. Finally, the output should stabilize at an impedance low enough to provide the required dc drive. For most portable applications, 4-mA dc drive is sufficient; however, for nonportable applications, more drive current might be required.

The majority of application loads targeted for the AUC Little Logic family can be represented as a transmission line rather than a dc load. Thus, ac operation is dominated by the inductance and capacitance of the load and, in most cases, heavy drive capabilities are not required, although they are provided up to 8 mA at 1.8-V V_{CC}.

AUC Little Logic devices provide 8-mA dc drive current at the 1.8-V V_{CC} node for nonportable applications, while maintaining the signal-integrity performance of a 4-mA dc driver. The ULTTL output used in the AUC Little Logic family is designed to address each of the three critical performance requirements previously noted. Figure 1 shows a schematic of the ULTTL output structure.

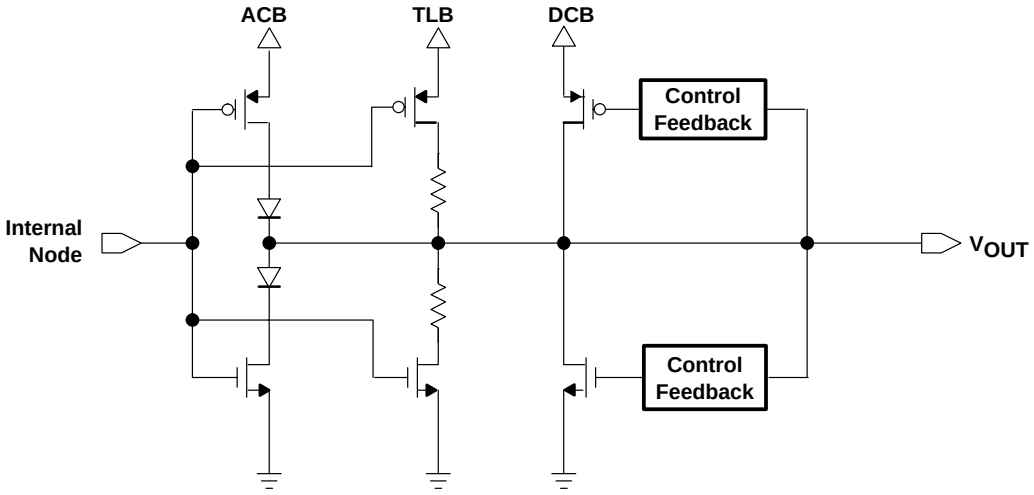


Figure 1. ULTTL Output Structure

To achieve the three impedance phases, the ULTTL output utilizes a three-branch p-channel upper-output (UOP) and three-branch n-channel lower-output (LOP) structure (see Figure 1). For the purpose of illustration, the three branches are referred to in this application report as the ac branch (ACB), the transmission-line branch (TLB), and the dc branch (DCB). The first branch, which uses the diode in the output structure, provides the high dynamic current required to drive through the ac threshold. The second branch, which contains a series resistor, provides optimized impedance matching into the transmission line. The third branch provides the additional dc current drive for applications requiring more than 4 mA of output drive current at 1.8-V V_{CC}.

Each independent branch posses a unique on-state resistance (r_{on}). As the output transitions from a low to high (or high to low), the equivalent resistance of all branches varies in a controlled manner by adjusting the individual resistance of each branch. The low-to-high transition functions similarly to the high-to-low transition. The output impedance is controlled during the low-to-high transition sequential action outlined below and shown in Figure 2.

1. During the initial phase of the transition, all three legs are turned on. The parallel r_{on} of all three legs provides very low combined impedance.
2. During the second phase of the transition, the ACB and DCB are turned off, and the output transitions to a higher impedance. As the output voltage level approaches V_{CC}, the series diode begins to saturate and, eventually, becomes reverse biased, causing the current through the ACB to be reduced to less than 1 mA (basically, turned off). A threshold-controlled feedback circuit turns off the DCB. The thresholds are adjusted, to minimize the effect of oscillations directly at the output of the driver before entering the transmission line. (NOTE: A major advantage for the DCB being turned on in the initial stage is to provide support for the ACB at lower V_{CC} ranges where speed often is sacrificed.) The TLB r_{on} is 50 Ω to 65 Ω and, because it is the last branch remaining on, it provides the impedance matching to the transmission line.

3. In the final phase of the transition, the DCB is turned on by the threshold-controlled feedback circuit to provide a combined DCB and TLB equivalent resistance that is satisfactory for driving applications requiring more than 4 mA of output drive current at 1.8-V V_{CC}.

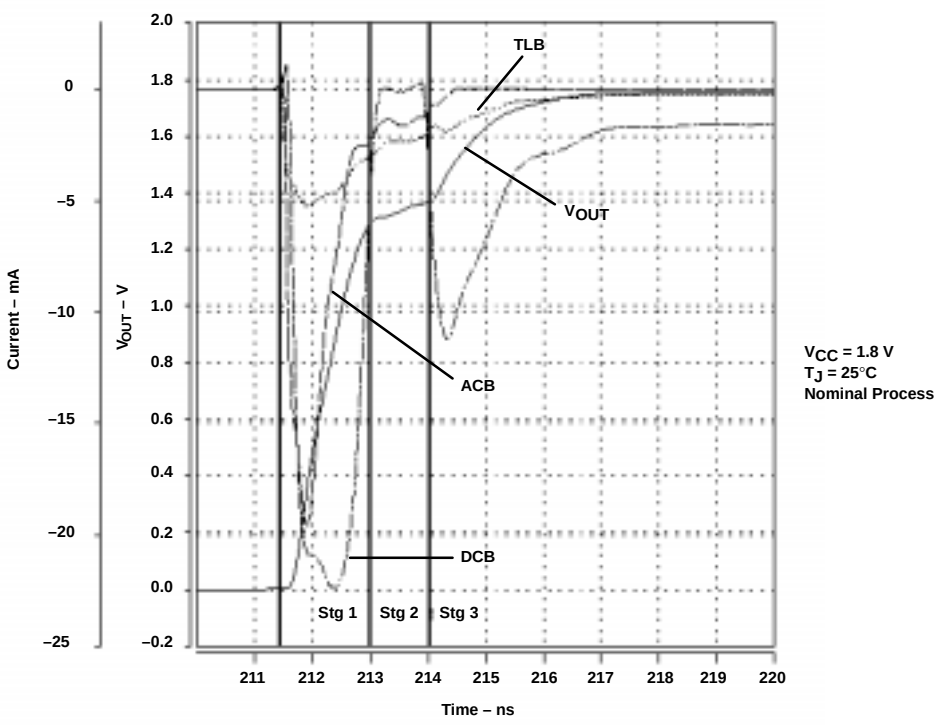


Figure 2. Output Drive Current of UOP During Low-to-High Transition

2.2 Level-Translation Support

Because the AUC Little Logic family uses a 0.8-V to 2.5-V power supply, interfacing AUC Little Logic devices with other components that use a 3.3-V power supply becomes a concern. If an AUC Little Logic device is subjected to 3.3-V at its inputs, it is critical that the device not be damaged. The term 3.3-V tolerance implies that the presence of 3.3-V at either the input or the output of the AUC device will not damage it. This feature enables AUC Little Logic devices to be used for level-translation support from higher-voltage nodes to lower-voltage nodes within the 0.8-V and 3.3-V nodes.

Whether a device can tolerate 3.3-V only at the input, only at the output, or at both the input and output must be considered. Every AUC Little Logic device TI produces can be subjected to 3.3-V at its input and not be damaged. Thus, all TI AUC Little Logic devices are 3.3-V input tolerant.

Whether or not an AUC Little Logic device can be subjected to 3.3-V at its output requires consideration. For the term 3.3-V output tolerant to be meaningful, the outputs of the device must be capable of being placed in the high-impedance state. Only the SN74AUC1G06, SN74AUC1G07, SN74AUC1G125, SN74AUC1G126, and SN74AUC1G240 have high-impedance outputs, and it is to these devices only that the term 3.3-V output tolerant applies. For those devices with outputs capable of being placed in the high-impedance state, 3.3-V output tolerance means that 3.3 V at its output does not damage the device.

The AUC Little Logic functions that do not have high-impedance-state outputs should not be connected to 3.3-V. This means that 3.3-V output tolerance does not make sense for these devices because their outputs cannot be placed in the high-impedance state.

2.3 Power-Off Support

The inputs and outputs of the AUC family have a blocking diode in the reversed-current paths to V_{CC}. In this configuration, the maximum leakage current into or out of the input or output transistors is negligible when forcing the input or output to 3.3 V and V_{CC} = 0 V. This off-state leakage current (I_{off}) is small enough to allow the device to remain electrically connected to a bus during partial power down without loading the remaining live circuits. This feature also allows the use of this family in a mixed-voltage environment.

3 AUC Little Logic Device Characteristics

3.1 Input Characteristics

3.1.1 Input Capacitance

The AUC Little Logic devices provide a low input capacitance-to-speed ratio relative to similar products (see Table 1). Two major design factors influence input capacitance: speed and capacitive-load-driving requirements. As speed requirements become more critical, the number of internal stages for a given integrated circuit must be reduced to minimize propagation delay. In addition to a reduction in stages, unless the requirement to drive large capacitive loads is reduced (especially for nonportable applications), the output stage must be large enough to drive these loads. In most cases, the combination of these two factors results in a higher input capacitance because the large input capacitance of the output stage is transferred to the input stage. Simply placing a small (low input capacitance) input stage in front of the large output stage does not result in less propagation delay.

Table 1. Input Capacitance and Speed Comparison for Comparable Families

Device	Input Capacitance (pF)	t_{pd} at 1.8-V V_{CC} (ns)
SN74AUC1G00	3.0	2.5
SN74LVC1G00	4.0	8.0
SN74ALVC00	4.5	4.4

The AUC Little Logic devices can maintain a comparable low input capacitance of 3 pF (typical), while providing high dynamic drive capability for larger loads and providing a propagation delay less than 2.5 ns at 1.8-V V_{CC} (see Table 1).

3.1.2 Input Voltage Tolerance

As previously mentioned, AUC Little Logic devices operate with a 0.8-V to 2.7-V V_{CC}. Therefore, interfacing AUC Little Logic with other components that use 3.3-V V_{CC} might be a concern. In such systems, AUC Little Logic devices must have tolerance for input levels up to and exceeding 3.3 V, as well as below 0 V, without causing damage to the inputs. The AUC Little Logic devices allow input voltages to exceed 3.3 V, up to 3.6 V, to allow extra protection for the following reasons:

- The 3.3-V system power supply might not stabilize at 3.3 V, but reach 3.6 V. Consequently, the output of the device driving the AUC Little Logic device could reach 3.6 V as well.
- The 3.3-V system power supply may stabilize at 3.3 V, but overshoots and undershoots can cause the input voltage into the AUC Little Logic devices to exceed the 0-V to 3.3-V range.

The AUC Little Logic devices support input voltages up to 3.6 V and must be operated within the following guidelines:

- The recommended operating conditions specified in the data sheets restrict the input voltage to 0 V to 3.6 V, while the absolute maximum ratings specify the input voltage to be –0.5 V to 4.1 V. As the data sheet indicates, stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. The absolute maximum ratings are stress ratings only, and functional operation of the device at those or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions may affect device reliability.
- Because the input-voltage range is limited from 0 V to 3.6 V, for 3.3-V systems, proper termination must be used on the inputs of AUC Little Logic devices to ensure that overshoot does not exceed 3.6 V.

3.1.3 Slow-Input-Edge-Rate Compatibility

The AUC Little Logic devices are designed and tested for high-speed systems (i.e., systems requiring a fast input edge rate) with input transition signals less than 1 ns/V. However, there may be several applications where it is desired to operate the device at a low frequency. In such applications, an input edge rate greater than 1 ns/V might be required. AUC Little Logic devices support such low-frequency applications.

A slow-input test sheds light on the integrity of the device, specifically, how the device responds when the input voltage is slowly ramped from 0 V to V_{CC} and, conversely, when the input voltage is ramped slowly from V_{CC} to 0 V. As the input voltage is ramping, the output voltage is monitored and, when it begins to switch, the waveform is observed. If nonmonotonic behavior is observed as the output traverses the threshold region, the device may be sensitive to a slow input, which can cause the output to oscillate or cause false triggering.

Figure 3 shows a passing case of slow-input-transition-rate tests. The test was done in the laboratory using the SN74AUC1G00 with V_{CC} = 2.7 V and the device at –40°C, with both inputs tied together for the worst-case condition. In Figure 3, the input transition rate is fast enough (11.69 ns/V) to not cause any oscillation at the output.

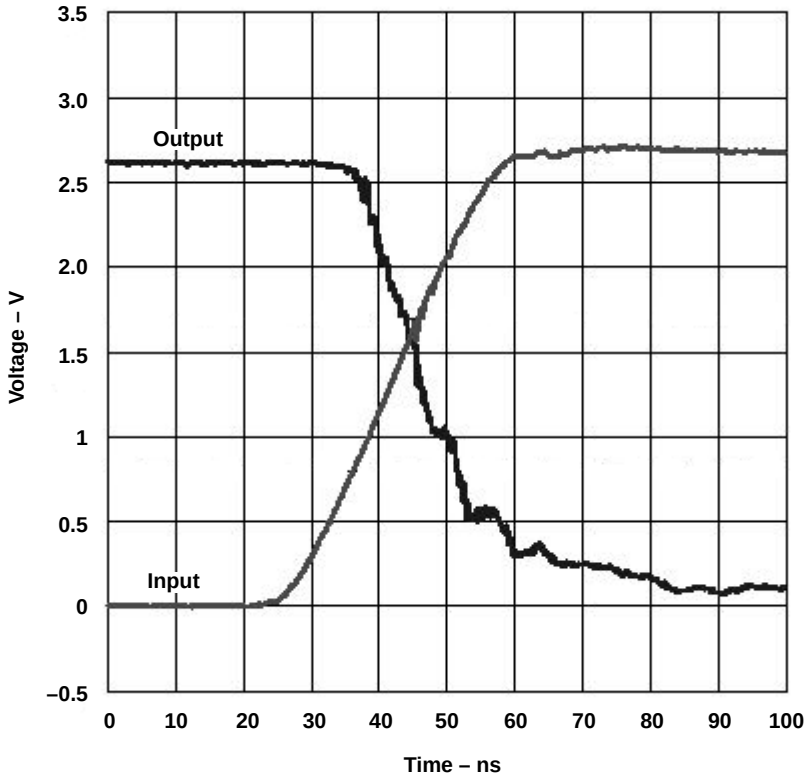


Figure 3. SN74AUC1G00 Slow-Input-Transition-Time Plot, $\Delta t/\Delta V$ = 11.69 ns/V

Figure 4 shows a failure case of slow-input-transition-rate tests. The test was done in the laboratory using the SN74AUC1G00 with V_{CC} = 2.7 V and the device at –40°C, with both inputs tied together for the worst-case condition. In Figure 4, the input transition rate is too slow (23.19 ns/V) and causes oscillations at the output.

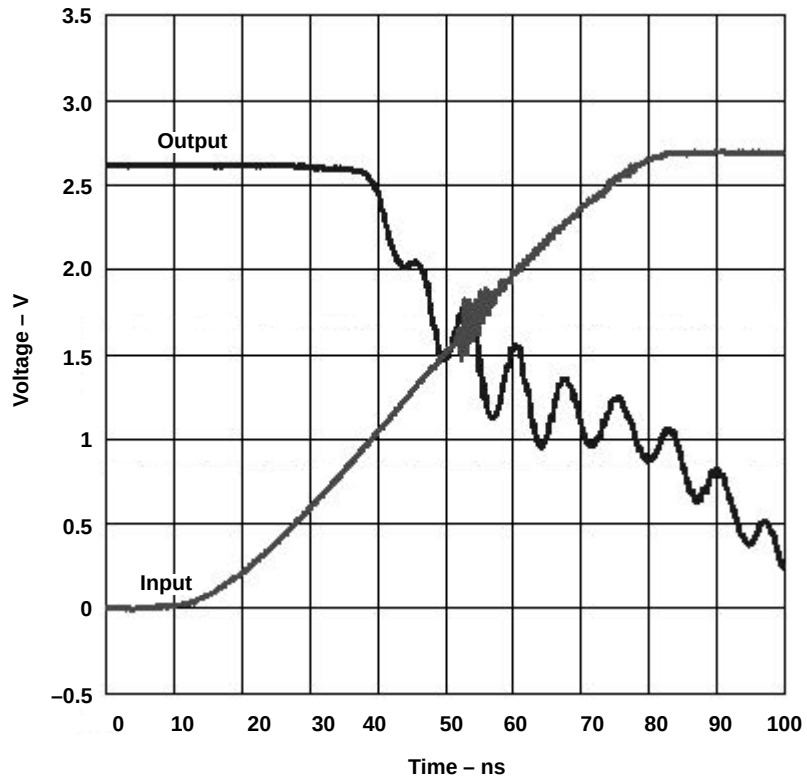


Figure 4. SN74AUC1G00 Slow-Input-Transition-Time Plot, $\Delta t/\Delta V$ = 23.19 ns/V

Table 2 shows the maximum input transition rise or fall rate for some AUC Little Logic devices at different voltage nodes. At the optimized voltage node, all AUC Little Logic devices show noncritical responses to the slow-input test.

Table 2. Input Transition for Some AUC Little Logic Devices

Device	Maximum Input Transition Rise or Fall Rate, $\Delta t/\Delta V$ (ns/V)				
	V_{CC} = 0.8 V	V_{CC} = 1.3 V	V_{CC} = 1.6 V	V_{CC} = 1.95 V	V_{CC} = 2.7 V
SN74AUC1G00	20	20	20	20	10
SN74AUC1G04	20	20	20	20	5
SN74AUC1G07	20	20	20	20	15
SN74AUC1G14	20	20	20	20	20
SN74AUC1G17	20	20	20	20	20
SN74AUC1G32	20	20	20	20	20

Table 2 shows that the AUC Little Logic devices can operate with slow signals ($\Delta t/\Delta V$ > 1 ns/V) at the inputs. However, power consumption increases significantly with increased input transition rise or fall rates.

3.2 Electrical Characteristics

In most electronic-system applications, it is important for the integrated circuit drivers to provide balanced high and low drive during ac transition, which ensures balanced output edge rates and improved signal integrity. Also, balanced high and low drive ensures that the difference between the low-to-high transition time (t_{PLH}) and the high-to-low transition time (t_{PHL}) is minimized. In general, as the supply voltage lowers, the p-channel becomes weaker at a faster rate than the n-channel transistor, due to their respective positive and negative carrier-mobility-degradation characteristics. For devices with active p-channel pullups, this causes t_{PLH} to increase at a faster rate than t_{PHL}; consequently, the $|t_{PLH} – t_{PHL}|$ increases respectively. The three-branch ULTTL output mentioned previously works to minimize this effect across V_{CC} by distributing the high drive across the r_{on} of the transistor with that of the resistor (i.e., resistor in the TLB). The resistance of the resistor does not vary with supply voltage, thus reducing the effective variation in r_{on} of the high and low drives.

As the supply voltage lowers, the ACB output branch provides less support for the ac transition due to the series diode. The propagation delay performance is then affected primarily by the TLB and DCB. Again, by inserting the series resistance, the balance between the high-drive transistor and low-drive transistor is preserved better at lower V_{CC} nodes.

The electrical characteristics of the AUC family are critical aspects of a successful system design. The following sections discuss the ac and dc performance of the devices.

3.2.1 AC Performance

Table 3 shows a comparison of the propagation delay for different AUC Little Logic devices operating at different voltage nodes. These results are from laboratory tests using the standard load specifications in the parameter measurement information (see Appendix A).

Table 3. Timing Characteristics of AUC Little Logic Devices

Device	t_{pd} (ns)									
	V_{CC} = 0.8 V	V_{CC} = 1.2 ± 0.1 V		V_{CC} = 1.5 ± 0.1 V		V_{CC} = 1.8 ± 0.15 V			V_{CC} = 2.5 ± 0.2 V	
	TYP	MIN	MAX	MIN	MAX	MIN	TYP	MAX	MIN	MAX
SN74AUC1G00	4.7	0.9	3.5	0.5	2.3	0.7	1.3	2.5	0.5	2.1
SN74AUC1G02	4.6	0.9	3.4	0.5	2.2	0.7	1.3	2.5	0.5	2.1
SN74AUC1G04	4.4	0.8	3.3	0.5	2.2	0.6	1.2	2.5	0.5	1.9
SN74AUC1G06	5.0	0.3	3.1	0.2	2.5	0.5	1.6	2.9	0.2	1.9
SN74AUC1G07	4.7	0.3	3.3	0.2	2.4	0.8	1.9	2.5	0.2	1.8
SN74AUC1G08	4.7	0.9	3.5	0.6	2.6	0.7	1.3	2.5	0.5	2.1
SN74AUC1G14	5.8	0.7	4.2	0.6	2.7	0.7	1.6	2.8	0.5	2.5
SN74AUC1G17	5.7	0.8	4.0	0.7	2.4	0.8	1.4	2.5	0.7	2.6
SN74AUC1G32	4.8	1.0	3.5	0.6	2.3	0.8	1.4	2.5	0.6	2.1

Table 3 shows that the AUC Little Logic devices have very low propagation delay. The devices appear to be optimized at the 1.5-V node because the t_{pd} is lowest when V_{CC} = 1.5 V. However, the t_{pd} values are measured under different load conditions (see Appendix A). The AUC Little Logic devices are optimized at the 1.8-V node but, because the 1.8-V node test load (R_L = 1 kΩ; C_L = 30 pF) is heavier than the 1.5-V test load (R_L = 2 kΩ; C_L = 15 pF), the devices appear to be slower at the 1.8-V node than they are at the 1.5-V node. The test loads used for characterizing the devices are the standard JEDEC test loads at the respective voltage nodes.

A true comparison of the propagation delays of the AUC Little Logic devices at different voltage nodes is obtained by measuring the propagation delays at different voltage nodes when the device is under the same loading condition. Figure 5 shows typical variations of propagation delay with respect to capacitive loading for 1.5-V, 1.8-V, and 2.5-V V_{CC}. In all three cases, a resistive load of 1 MΩ was connected between the output and ground. The data were collected under nominal-process conditions from the SN74AUC1G00 at 25°C. Similarly, Figure 6 shows typical variations of propagation delay with respect to capacitive loading for 0.8-V and 1.2-V V_{CC}. The data also were collected under the same conditions as for Figure 5.

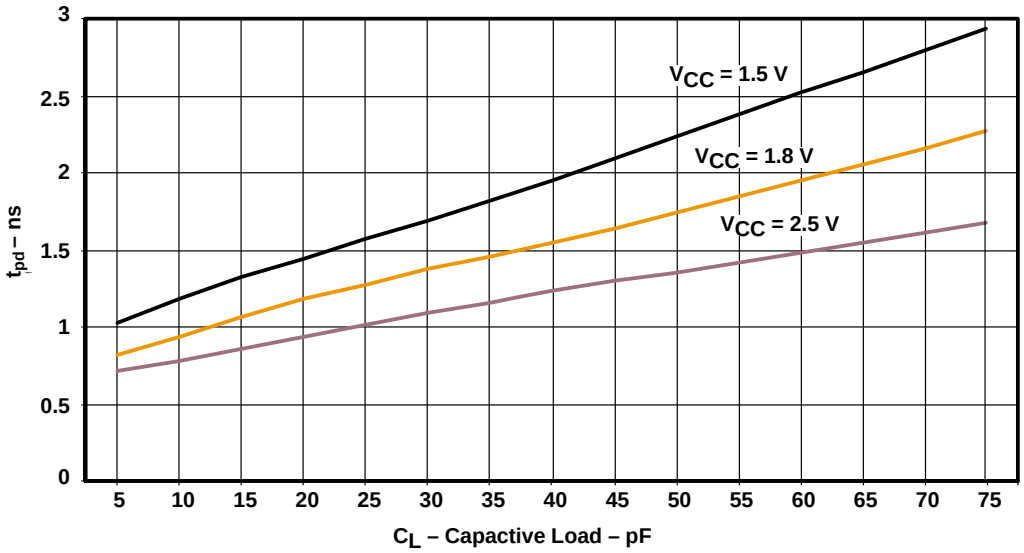


Figure 5. t_{pd} vs Capacitive Load at 2.5-V, 1.8-V, and 1.5-V V_{CC}

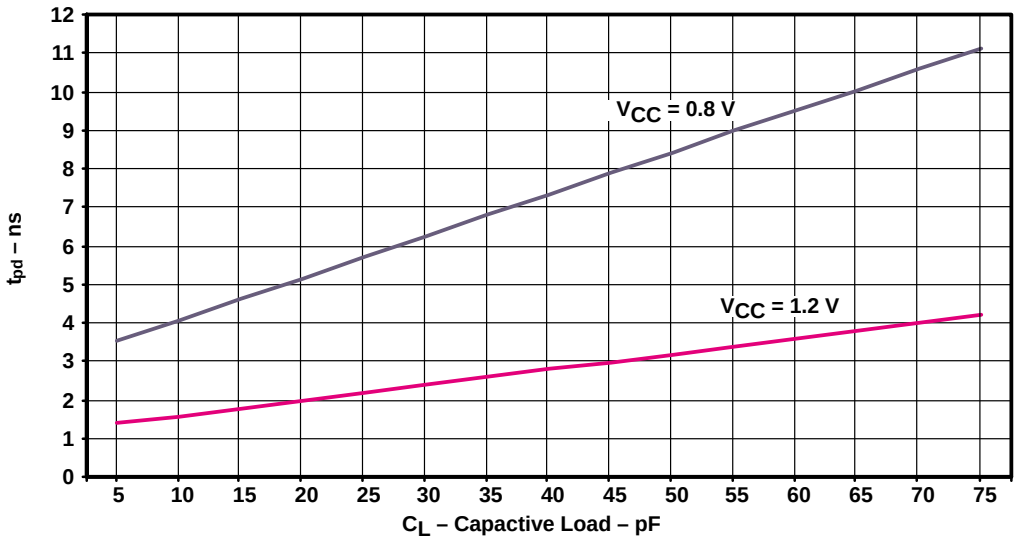


Figure 6. t_{pd} vs Capacitive Load at 1.2-V and 0.8-V V_{CC}

3.2.2 DC Performance

The V_{OH} vs I_{OH} and V_{OL} vs I_{OL} characteristics are unique for the ULTTL output used in the AUC Little Logic devices. Figures 7 and 8 show the typical V_O vs I_O performance of the AUC1G devices. These curves can be used to determine an approximate output resistance at each supply-voltage node. These figures are provided to demonstrate the dc drive performance of the integrated circuit, but do not relate directly to the ac performance.

It is common to use the V_O vs I_O curves to generate Bergeron plots for analyzing the effective signal integrity of the driver (see *The Bergeron Method: A Graphical Method for Determining Line Reflections in Transient Phenomena)*.[1] A simple V_O vs I_O plot is not accurate for this purpose unless the device is biased in an ac mode before generating the curve. For a low-to-high transition, the ac mode is defined as biasing the input so as to generate a high logic level on the output, then sweeping the load current from high current (between 70 mA and 80 mA) to 0 mA and monitoring the corresponding output waveform. Sweeping the current from a high to low represents the actual operation during ac operation because the current is highest at the beginning of the transition and reduces as the output reaches the desired logic level. The same concept applies for a high-to-low transition.

As previously mentioned, the AUC Little Logic devices are optimized to drive a 50-Ω to 65-Ω transmission line, and provide 8-mA output current at 1.8-V V_{CC}. The majority of application loads targeted for the AUC Little Logic family can be represented as a transmission line rather than a dc load. Therefore, 4 mA (~70 Ω) of dc drive current should be sufficient.

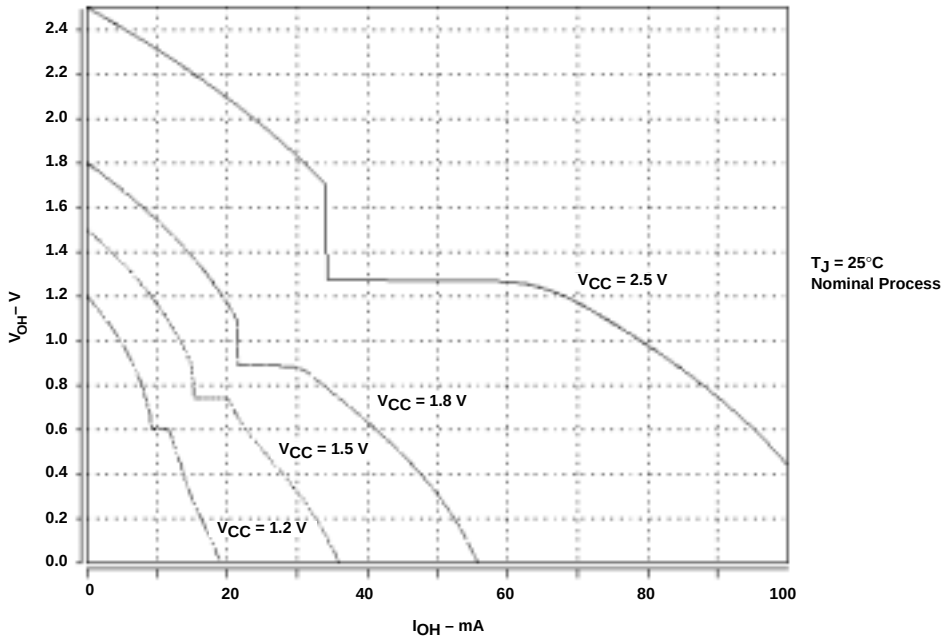


Figure 7. V_{OH} vs I_{OH} for AUC1G Devices

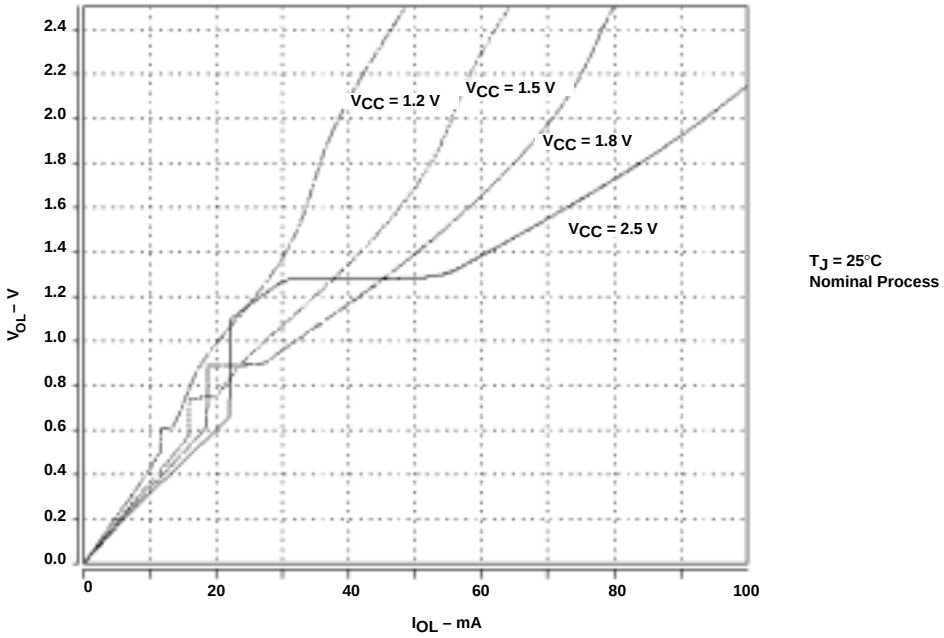


Figure 8. V_{OL} vs I_{OL} for AUC1G Devices

With each trace on the V_{OH} vs I_{OH} and V_{OL} vs I_{OL} plots, a small step function is present outside the drive conditions of the data sheet. This step in the waveform should not cause any problems in performance because it occurs at the point when the ACB and DCB are both turned off, and affects only the ac-signal-integrity performance, for which it is designed (refer to the Novel Output Structure section for more detailed operation).

3.3 Power Consumption

System designers, especially of portable applications, are becoming more concerned with the power consumption of each integrated circuit. The power consumption of an integrated circuit determines how much energy is consumed during operation (especially important for battery-powered systems), and how much heat the integrated circuit dissipates (especially important in personal-computer applications). The AUC Little Logic devices are designed for optimum efficiency in power consumption.

Two components establish the level of power consumption in a CMOS circuit:

1. Static dissipation caused by continuous leakage current from the power supply while the output is in a static (nonswitching) state
2. Dynamic dissipation caused by switching-transient current, which is a combination of the short-circuit current (current pulse from V_{CC} to GND during a transition) and load current (current required to charge the capacitive load on the output)

Although system designers desire integrated circuits with minimal power consumption, lower power often results in slower propagation delays. For CMOS designs, the propagation delay and the power consumption of an integrated circuit are related. For a given gate topology, the product of power consumption and propagation delay usually is a constant. This is referred to as the power-delay product (PDP) and is a quality measure for analyzing the speed vs power efficiency of a given device. The AUC Little Logic devices provide a low-power solution, without sacrificing speed. Figure 9 shows the relative power efficiency of the AUC Little Logic devices compared with other Little Logic devices. The data represented in Figure 9 were measured at the supply-voltage node at which the different devices are optimized (see Table 4).

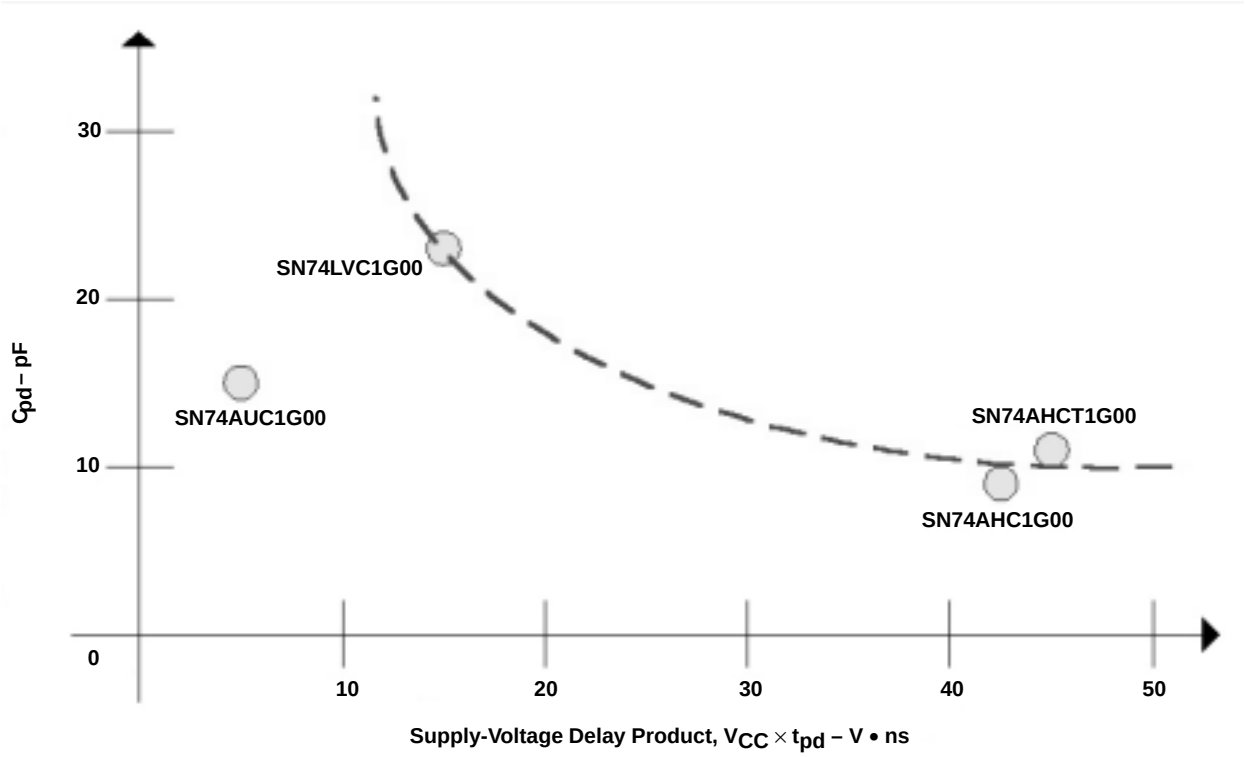


Figure 9. Relative Power Efficiency of Selected Little Logic Devices

Table 4. Power Consumption and Speed of Selected Little Logic Devices at Their Optimized Supply-Voltage Nodes

Device	Optimized V_{CC}	C_L	Maximum t_{pd}	Typical C_{pd}
SN74AUC1G00	1.8 V	30 pF	2.5 ns	15 pF
SN74LVC1G00	3.3 V	30 pF	4.7 ns	23 pF
SN74AHC1G00	5.0 V	50 pF	8.5 ns	9.5 pF
SN74AHCT1G00	5.0 V	50 pF	9.0 ns	10.5 pF

4 Design Issues and AUC Little Logic Solutions

4.1 Signal Integrity

As power-supply voltages decrease, signal integrity becomes a major issue. The noise margin required for a device to be considered operable reduces proportionately with a reduction in power-supply voltage. In addition to the requirement for better signal integrity and smaller noise margins, system designers, especially for portable applications, need a solution that requires no external termination (i.e., damping resistors, clamping diodes, etc.). Additional components use valuable board space, and space also is at a premium in portable applications. The AUC Little Logic devices provide the best possible solution for systems with these design constraints.

The ULTTL output provides great signal integrity without the need for external termination when driving traces of moderate length (less than 15 cm). Figure 10 shows a typical application environment. The driver represents an AUC Little Logic device and the receiver represents a CMOS device whose interface is compatible with the AUC logic levels. The transmission line corresponds to a PCB trace of 50 Ω to 65 Ω for a portable system application, consisting of short trace length (less than 15 cm). During the second phase of the three distinctive transitional phases of the ULTTL output (see Section 2.1), the AUC output impedance changes to a level close to that of the transmission line (see Figure 11), thus minimizing overshoots and undershoots.

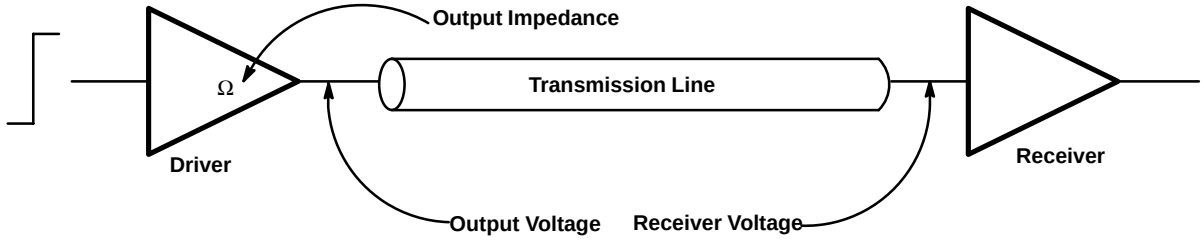


Figure 10. Transmission-Line Test Points for Simulations

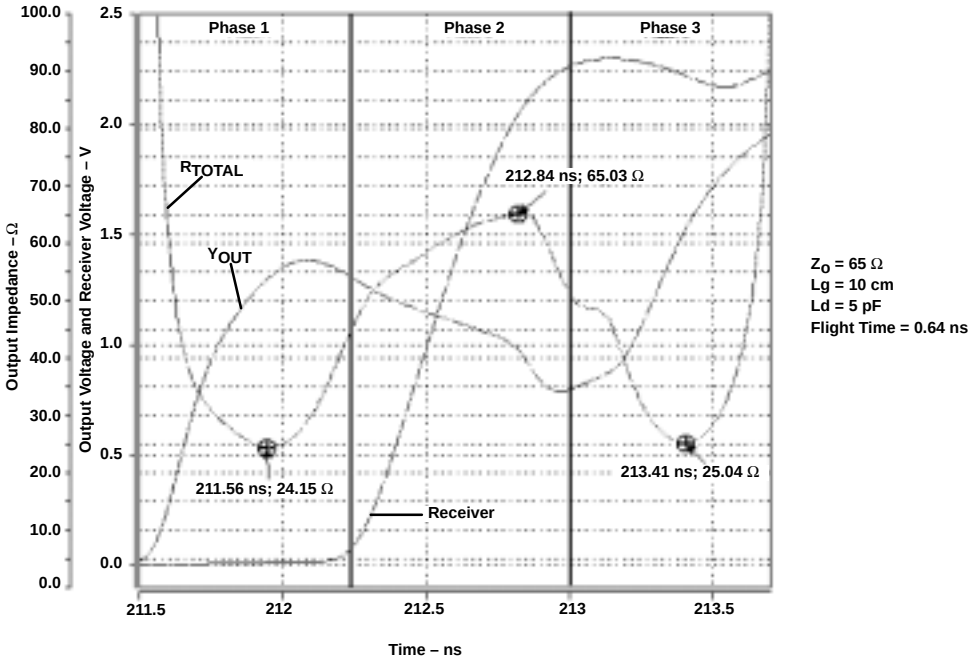


Figure 11. Output Impedance, Output Voltage, and Receiver Voltage of AUC Single-Gate Transmission-Line Simulation

The simulation results in Figure 12 show typical operation into a 10-cm PCB trace, with a line impedance of 65 Ω and a 5-pF capacitive load at the receiver end. The simulation was completed at 10 MHz, with an input edge rate of 1 ns/V.

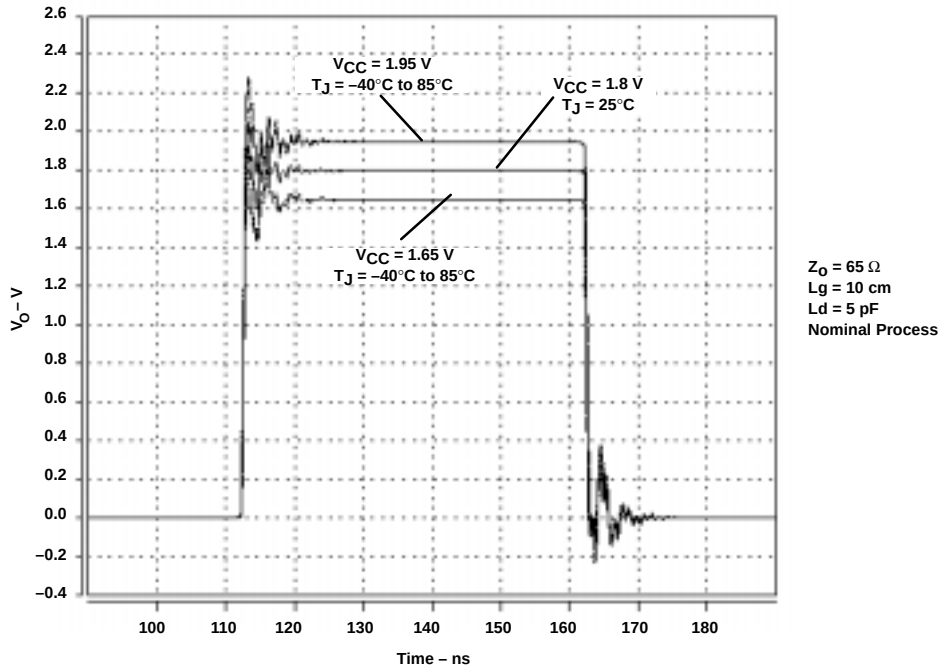


Figure 12. Simulation of 65-Ω Transmission Line Across Supply Voltage and Temperature

Although the AUC Little Logic devices are optimized for 50-Ω to 65-Ω loads, some applications might require operation into 30-Ω to 75-Ω loads. The unique characteristic of the ULTTL output provides adequate performance into these wider-range loads (see Figures 13 and 14).

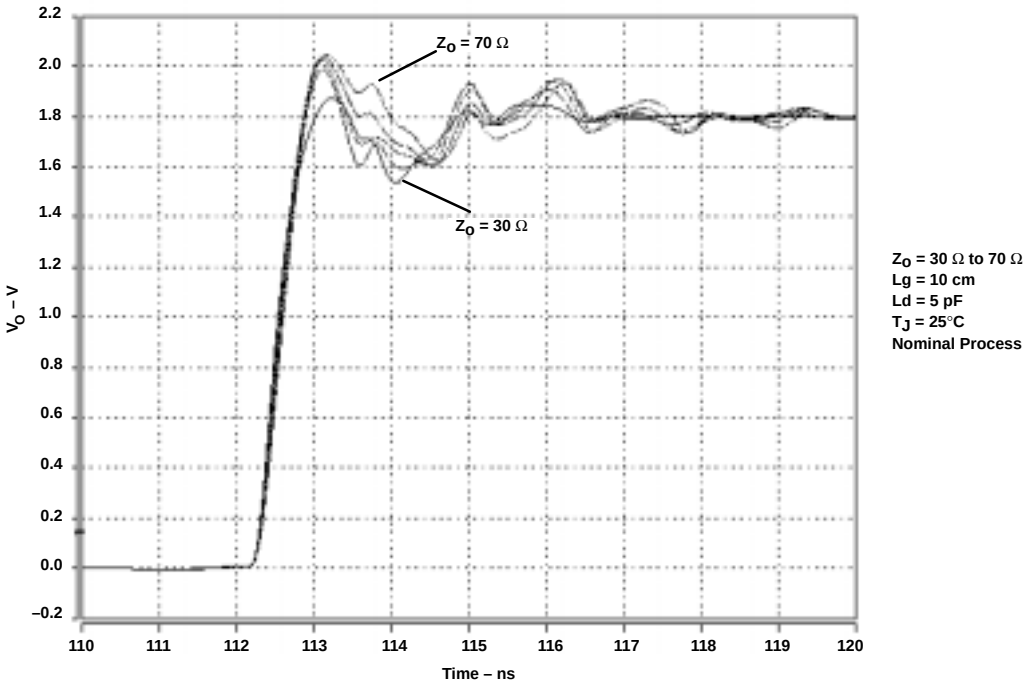


Figure 13. Simulation of Low-to-High Transition into 30-Ω to 70-Ω Transmission Line

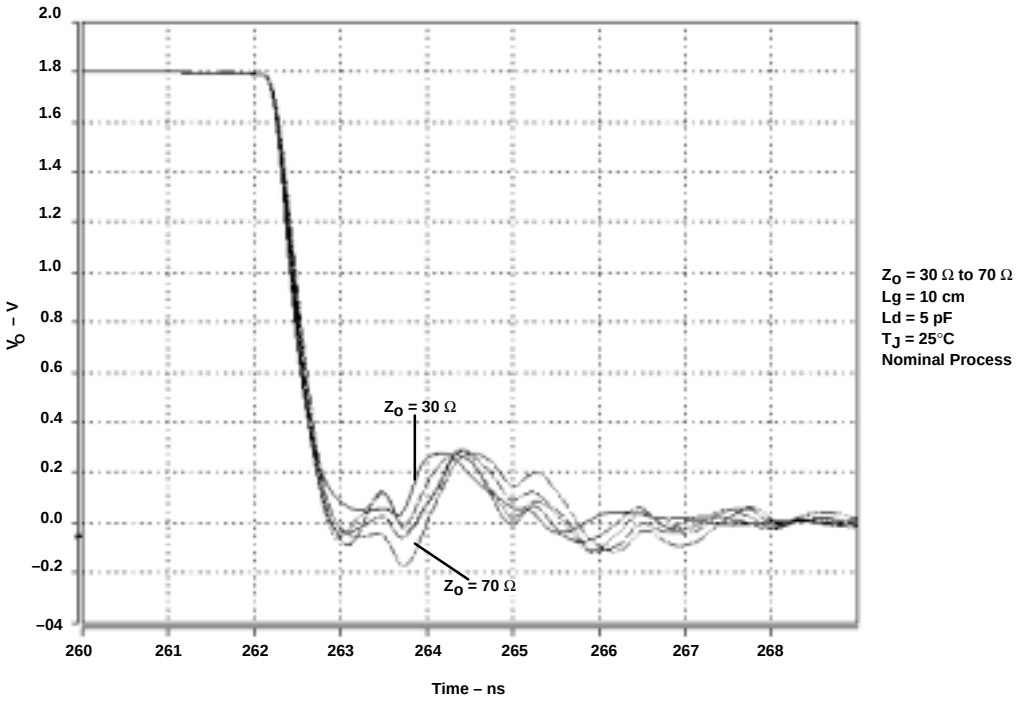


Figure 14. Simulation of High-to-Low Transition into 30-Ω to 70-Ω Transmission Line

4.2 Mixed-Voltage-Mode Data Communication

In designing electronic systems, proper interfaces between buses with incompatible logic levels must be provided. Voltage-level translation is necessary to allow the interconnection with flexibility to provide a future migration path to lower-voltage input/output (I/O) levels.

Voltage translation between buses with incompatible logic levels can be accomplished using AUC Little Logic devices. With a unidirectional AUC driver powered with 1.8-V V_{CC}, data communication from 2.5-V or 3.3-V devices can occur (see Figure 15). In this case, the inputs of the AUC devices are tolerant of the higher voltages and accept the higher switching levels. Likewise, the outputs of the AUC driver are valid 1.8-V signal levels.

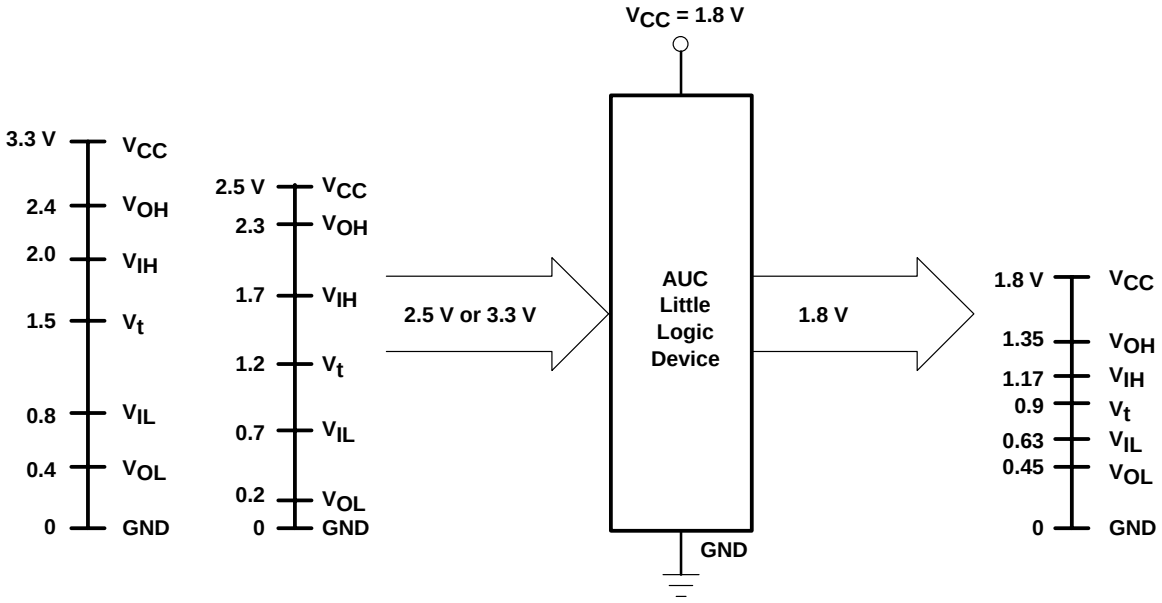


Figure 15. Device at 1.8-V V_{CC}, With 2.5-V or 3.3-V Inputs, Showing Switching Levels

Generally, a unidirectional AUC driver powered with 0.8-V, 1.2-V, 1.5-V, or 1.8-V V_{CC} can be used to down-translate from a higher voltage node to the voltage node of the supply voltage.

Similarly, up-translation and down-translation can be achieved by using the SN74AUC1G06 or the SN74AUC1G07. The SN74AUC1G07 is a noninverting buffer with an open-drain output, and the SN74AUC1G06 is the inverting buffer (the SN74AUC1G07 plus an extra stage of inversion). These buffers are designed to operate in the 0.8-V to 2.7-V V_{CC} range; however, inputs and outputs can interface with 3.3-V signals.

This section focuses on the application of the SN74AUC1G07 in voltage-level translation. However, the SN74AUC1G06 can be used in such applications as well, only with an extra inversion.

The open-drain feature of the SN74AUC1G07 is useful in voltage translation. The fact that the input and output structure of this device can accept voltages from 0.8-V to 3.3-V enables the device to support voltage translation from a lower voltage to a higher voltage, or vice versa. Without the p-channel pullup on the output structure of the SN74AUC1G07, the entire output voltage drops across the n-channel transistor (see Figure 16). With the help of a pullup resistor that is connected to the designer's choice of voltage (not exceeding 3.6 V), voltage translation is achieved.

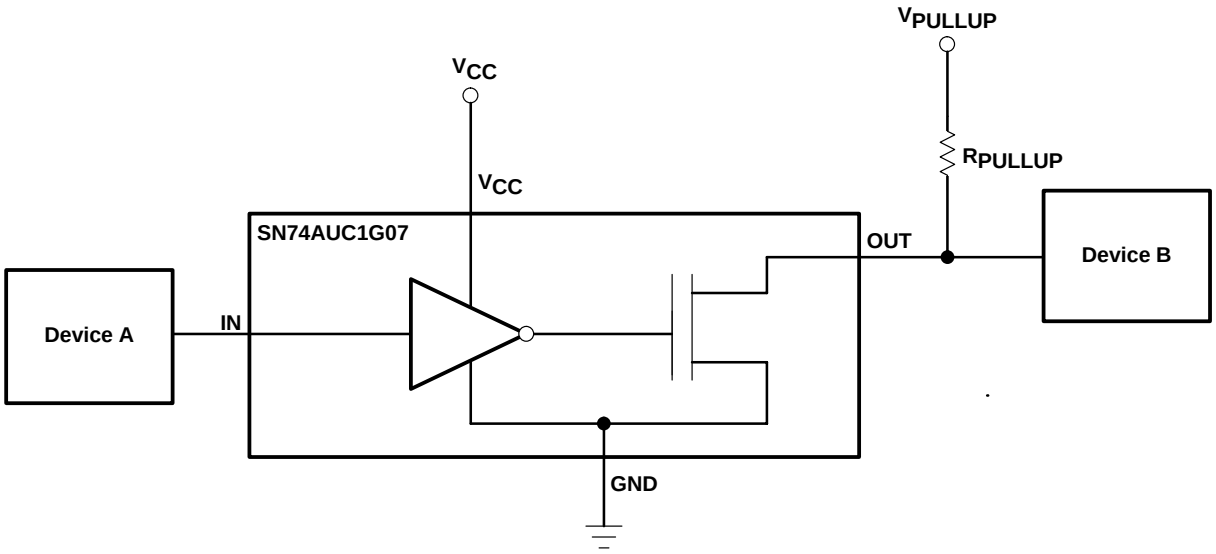


Figure 16. Circuit for Voltage Translation Using the SN74AUC1G07

The voltage translation provided by the SN74AUC1G07 can be used between wide CMOS voltage nodes. Table 5 illustrates parameters necessary for some example voltage translations between devices A and B.

Table 5. Requirements for Voltage Translation Between Devices A and B

Device A	Device B	V_{CC}	V_{PULLUP}	Function
3.3-V CMOS	1.2-V LVCMOS	0.8 V to 2.5 V	1.2 V	Down translation
3.3-V CMOS	1.8-V LVCMOS	0.8 V to 2.5 V	1.8 V	Down translation
2.5-V LVCMOS	1.8-V LVCMOS	0.8 V to 2.5 V	1.8 V	Down translation
3.3-V CMOS	3.3-V CMOS	0.8 V to 2.5 V	3.3 V	Buffer
1.8-V LVCMOS	1.8-V LVCMOS	0.8 V to 1.8 V	1.8 V	Buffer
1.2-V LVCMOS	1.2-V LVCMOS	0.8 V to 1.2 V	1.2 V	Buffer
1.8-V LVCMOS	3.3-V CMOS	0.8 V to 1.8 V	3.3 V	Up translation
1.8-V LVCMOS	2.5-V LVCMOS	0.8 V to 1.8 V	2.5 V	Up translation
1.2-V LVCMOS	3.3-V CMOS	0.8 V to 1.2 V	3.3 V	Up translation

In Table 5, note that the SN74AUC1G07 also can be used as a buffer in some applications. In such configurations, the device can be used as an active-high wired-AND or for active-low wired-OR functions. This is achieved by tying outputs of two or more open-drain devices.

4.3 Partial Power Down

Electronic systems usually have power-saving or suspended modes of operation, whereby some circuitry in the system is powered down to reduce power consumption. During such modes of operation, the supply voltage of the circuitry is turned off. This mode of operation is known as partial-power-down mode, as part of the system is powered down. The AUC Little Logic devices support partial-power-down applications and it is important that the designer understands the data-sheet-specified parameters related to this feature.

To partially power down a device, no direct path from the input to V_{CC} or from the output to V_{CC} can exist. Consequently, when the device is powered down (V_{CC} = 0 V), independent of the logic level at the I/O terminal, no current can flow from the I/O terminal to the power-supply pin, which is at 0 V. In the partial-powered-down mode, therefore, other devices interfacing with the powered-down device may be powered up with valid logic levels at the I/O terminals.

With the AUC Little Logic, there is no direct path from the I/O terminal to V_{CC}. Consequently, these devices support partial-power-down modes of operation. This feature is specified on the data sheet with the I_{off} parameter. The I_{off} parameter is the maximum leakage current into (or out of) the input (or output) transistors when forcing the input (or output) to 2.7 V and V_{CC} = 0 V. With the AUC Little Logic, I_{off} is specified at ±10 μA. This is a very small current and represents leakage current at the I/O terminal.

4.4 Low Power Consumption

The migration to lower voltage nodes is becoming increasingly important in digital electronics, especially with portable and consumer electronics, because of the benefits of reduced power consumption. If power consumption is reduced, these electronics can use smaller batteries, thus reducing form factors, while getting the maximum life of the power supply between charges.

The AUC Little Logic devices enable low-power, high-performance designs. The power consumption reduction decreases heat dissipation in compact designs. This reduced heat dissipation simplifies heat removal and decreases the amount of package space needed, thus saving valuable board space in compact designs.

Figure 17 shows plots of supply current vs frequency for different AUC Little Logic devices. For each of the devices, the test was done with only one input switching from 0 V to 1.8 V at 1 ns/V. Note that the supply current increases with increased input transition. A 1.8-V power supply was used, and the tests were done at 25°C.

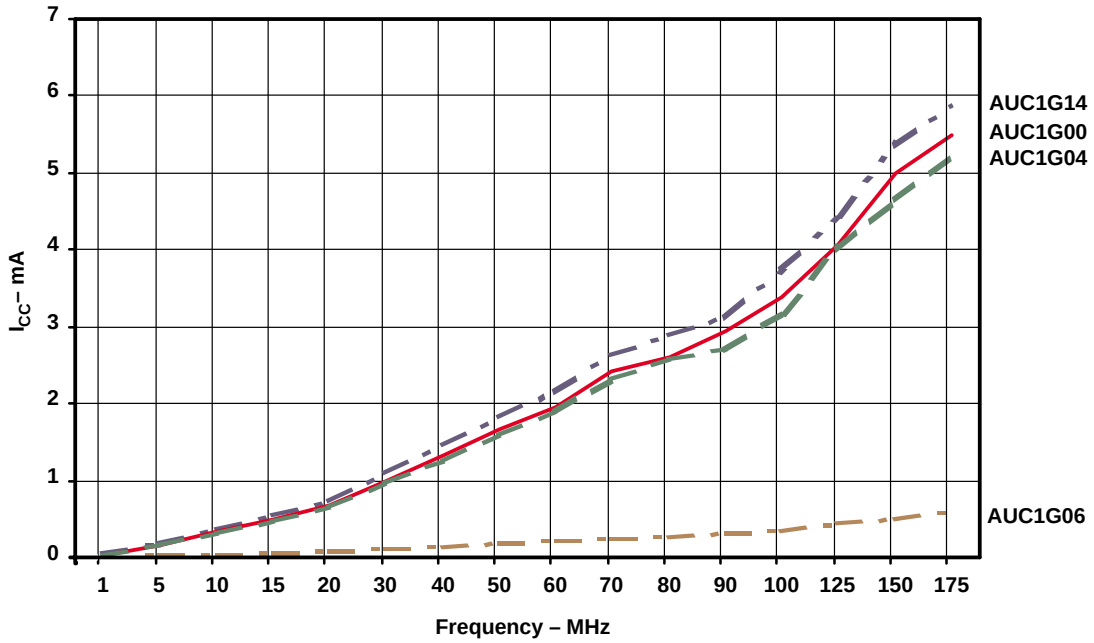


Figure 17. I_{CC} vs Frequency for Different AUC Little Logic Devices

Generally, the AUC Little Logic devices consume less power than the corresponding Little Logic devices of other families. Figure 18 provides a comparison of the supply current vs frequency for the SN74LVC1G06 and the SN74AUC1G06. Both devices were tested under the same conditions as those used to obtain the results in Figure 17.

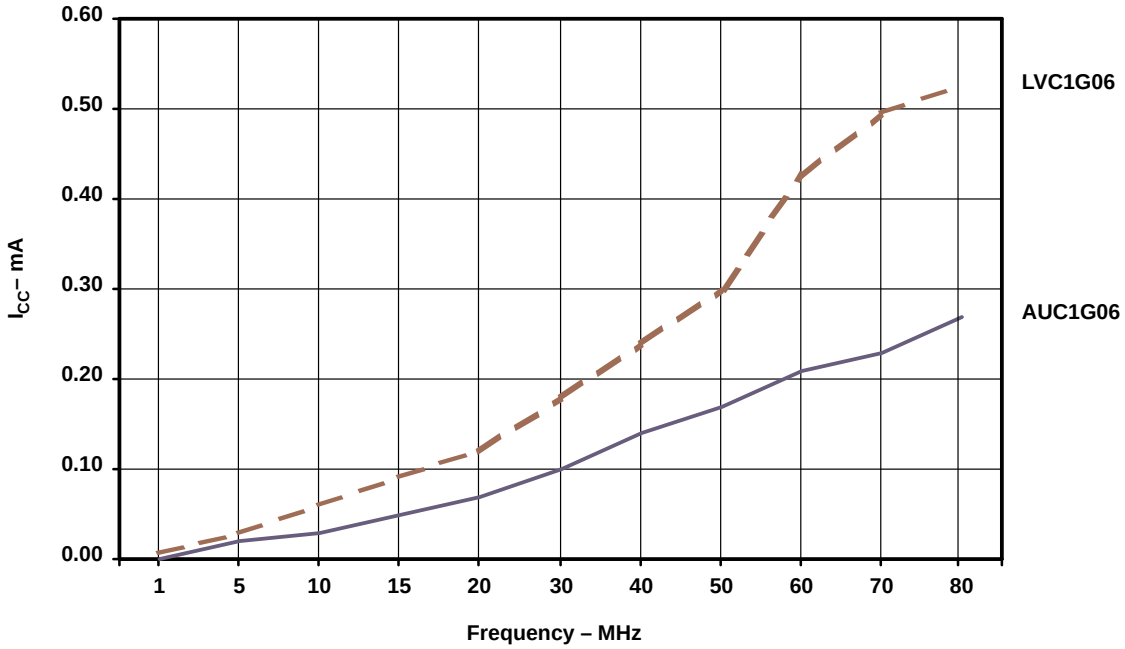


Figure 18. I_{CC} vs Frequency for SN74AUC1G06 and SN74LVC1G06 Devices

5 Package Information

The devices discussed in this application report are available in a variety of packages, including SOT-23 (DBV), SC-70 (DCK), tin-lead (SnPb) NanoStar™ (YEA), and lead-free NanoFree™ (YZA). TI's *Little Logic Data Book*, literature number SCED010, lists devices and packages in which they are available. The mechanical data information for these packages is provided in Appendix B of this application report.

The mechanical data for the YEA and YZA packages are the same. The only difference between the two packages is that the YEA package is leaded, while the YZA package is lead-free. The NanoStar and NanoFree packages comply with JEDEC MO-211.

6 Features and Benefits

Table 6 summarizes the features and benefits of AUC Little Logic devices.

Table 6. Features and Benefits of AUC Little Logic Devices

FEATURES	BENEFITS
Low power consumption	Use in portable electronics and battery-operated systems
Supports I_{off} at inputs	Use in applications that require partial power-down modes
3.6-V I/O tolerant	Use in level-translation applications. Eases migration to lower-voltage nodes. Enhances system safety.
Sub-1-V operable	Flexibility for future migration. Operable at lower-voltage nodes means less power consumption.
Small low-profile packages	Saves board space. Simplify large PCB routing. Use as quick fix for design errors.
Cost effective	Inexpensive compared to redesign. Used as quick fix for design errors. Reduces time-to-market and maximized design investment in all types of electronic systems.

7 Conclusion

The AUC Little Logic devices provide simple cost-effective solutions for portable electronics and battery-operated systems and facilitates quick fixes in system design errors. The devices are optimized at 1.8 V and are compatible with 2.5-V, 1.5-V, 1.2-V, and 0.8-V systems. The AUC family features TI's ULTTL output circuitry, 3.6-V I/O tolerance, low power consumption capability, and partial power-down support. Features, electrical characteristics, and applications of the AUC Little Logic devices are presented in this application report.

8 Frequently Asked Questions (FAQs)

Question 1: *What is AUC?*

Answer: The advanced ultra-low-voltage CMOS (AUC) is the new logic family that is optimized at 1.8 V, has an operating voltage range from 0.8 V to 2.5 V, and is tolerant of 3.3-V input and output voltages.

Question 2: *What is ULTTL?*

Answer: The ultra-low-voltage transistor-transistor logic (ULTTL) is a new interface driver designed for high-speed with low EMI noise, low power consumption, and optimal signal integrity.

Question 3: *How do I get copies of the AUC family data sheets and samples?*

Answer: The AUC family data sheets can be obtained by accessing http://www.ti.com. Samples of the AUC devices can be obtained by contacting your local TI sales representative.

Question 4: *How do I get copies of AUC family SPICE and IBIS models?*

Answer: The SPICE models for AUC devices can be obtained by contacting your local TI sales representative. The IBIS model can be obtained by accessing http://www.ti.com.

Question 5: *What are the advantages of migrating to the AUC family?*

Answer: The advantages of migrating to the AUC family include:

- Lowered power consumption enables use in portable electronics and battery-operated systems.
- Partial-power-down mode is supported.
- Level-translation is feasible and migration to lower-voltage nodes is easy.
- Future migration to sub-1-V applications is possible.
- Board space is saved and large-PCB routing is simplified.
- Capability for fixing design errors is flexible and redesign cost is lower.

Question 6: *What should I do if it appears that the device is producing a noisy signal?*

Answer: The most common reason an AUC device may appear to be producing a noisy signal is that the outputs have not been terminated properly. To reduce or eliminate reflections that are inherent with long trace lengths and transmission lines, one of five techniques must be used to match the impedance of the transmission line and thereby properly terminate the output. These five techniques are: single-resistor termination, parallel split-resistor termination, series-resistor termination, resistor-and-capacitor termination, and diode termination. For a detailed explanation of the techniques and the advantages and disadvantages of each method, refer to the *Advanced Schottky Load Management* Application Report.[3]

Question 7: *What is the maximum voltage the input pin of an AUC Little Logic can sustain when the device is powered down or when the device is powered up?*

Answer: The AUC Little Logic devices are 3.6-V tolerant at the inputs. Therefore, within the supply-voltage operational range (0.8 V = V_{CC} = 2.7 V), the input voltage can be as high as 3.6 V. Further, the AUC Little Logic devices have the I_{off} feature. Therefore, if V_{CC} = 0 V, the inputs can tolerate a 3.6-V signal.

Question 8: *What is the maximum voltage the output pin of an AUC Little Logic device can sustain when the device is powered down, and how can this information be inferred from the data sheet?*

Answer: With older family devices, there is a parasitic diode connected from the output to V_{CC}. With those devices, if V_{CC} = 0 V and the output is driven about 1 V above V_{CC}, the diode is forward biased and conducts current from the output pin to the V_{CC} pin. Under this condition, the device can be damaged. Therefore, the data sheet of a device with a power-clamp diode has a positive limit on the output clamp current (I_{OK}).

The AUC Little Logic, however, have no parasitic diode from the output to V_{CC}. The data sheets specify an absolute maximum rating I_{OK} of –50 mA, with no positive limit for this specification. Therefore, the output can be driven above V_{CC}, but caution should be taken to ensure that the I_{OK} limit is not exceeded when the output is driven below GND.

The above explanation applies only for the absolute maximum rating of the device. Under the recommended operating conditions, the AUC Little Logic devices with outputs incapable of being placed in the high-impedance state are recommended to be between 0 V and V_{CC}.

Question 9: *What is the maximum operating frequency of the AUC Little Logic devices?*

Answer: The maximum operating frequency of a device depends upon the load that the AUC device is driving. Using the specified data sheet load, the AUC Little Logic devices have been tested in the laboratory to operate at frequencies greater than 175 MHz.

9 References

1. The Bergeron Method: A Graphical Method for Determining Line Reflections in Transient Phenomena, application report, literature number SDYA014.
2. Little Logic Data Book (SCED010), November 2001.
3. Advanced Schottky Load Management, application report, literature number SDYA016.

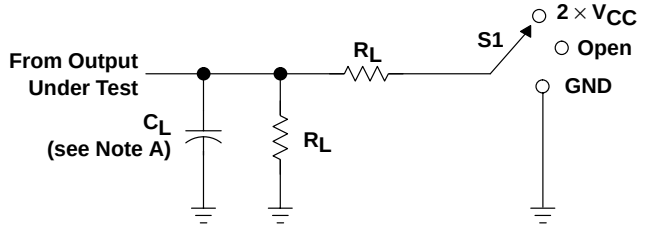
10 Glossary

ac	Alternating current
ACB	ac branch
AUC	Advanced ultra-low-voltage CMOS
CMOS	Complementary metal-oxide silicon; a device technology that has balanced drive outputs and low power consumption
dc	Direct current
DCB	dc branch
EMI	Electromagnetic interference
IBIS	I/O buffer information specification
I_{off}	The maximum leakage current into/out of the input/output transistors when forcing the input/output to 2.7 V and V_{CC} = 0 V
I_{OH}	High-level output current. The current out of an output with input conditions applied that, according to the product specification, establishes a high level at the output.
I_{OK}	Output clamp current. The absolute maximum current that can be sourced from an output pin when the voltage is taken below 0 V
I_{OL}	Low-level output current. The current into an output with input conditions applied that, according to the product specification, establishes a low level at the output.

JEDEC	Joint Electron Device Engineering Council
LOP	Lower-output transistor
LVCMOS	Low-voltage complementary metal-oxide silicon
PCB	Printed circuit board
PDP	Power-delay product
r_{on}	On-channel resistance
SPICE	Simulation program with integrated circuit emphasis
TI	Texas Instruments
TLB	Transmission-line branch
t_{pd}	Propagation delay time. The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level ($t_{pd} = t_{PHL}$ or t_{PLH}).
t_{PHL}	Propagation delay time, high-to-low level output. The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined high level to the defined low level.
t_{PLH}	Propagation delay time, low-to-high level output. The time between the specified reference points on the input and output voltage waveforms, with the output changing from the defined low level to the defined high level
TTL	Transistor-transistor logic
ULTTL	Ultra-low-voltage transistor-transistor logic
UOP	Upper-output transistor
V_{OH}	High-level output voltage. The voltage at an output terminal with input conditions applied such that, according to product specification, it establishes a high level at the output.
V_{OL}	Low-level output voltage. The voltage at an output terminal with input conditions applied such that, according to product specification, it establishes a low level at the output.

Appendix A. Parameter Measurement Information

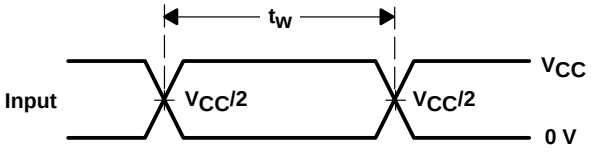
PARAMETER MEASUREMENT INFORMATION



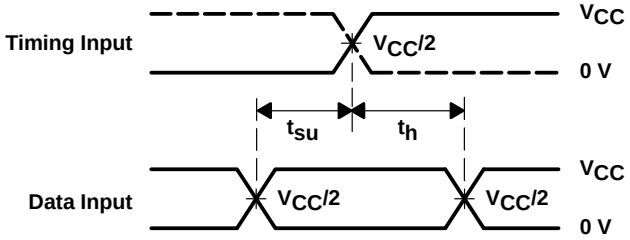
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND

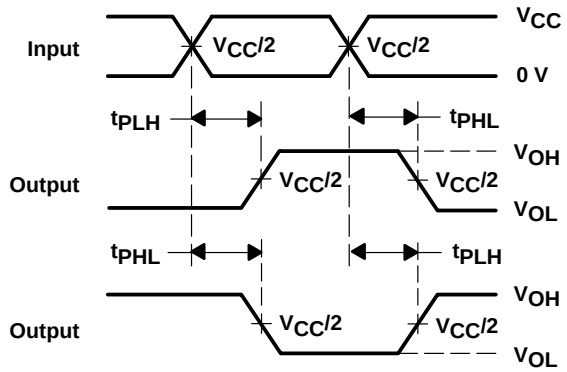
V_{CC}	C_L	R_L	V_Δ
0.8 V	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V



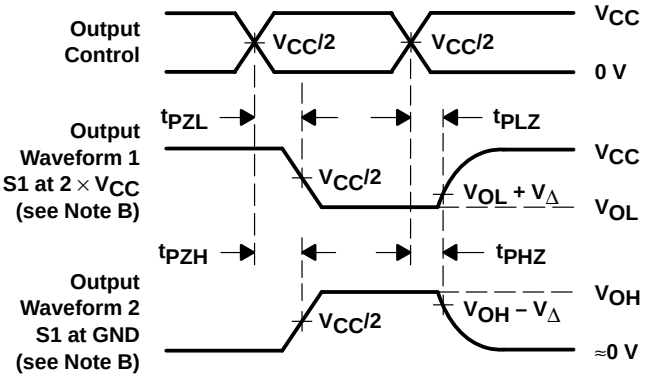
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS

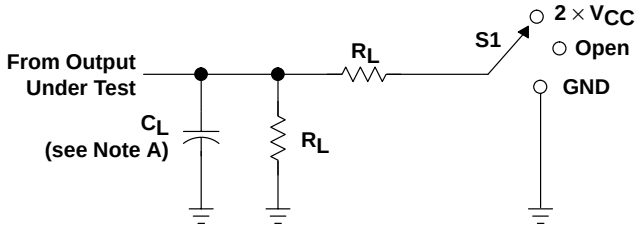


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

Figure 19. AUC Little Logic (with ULTTL Outputs) Load Circuit and Voltage Waveforms

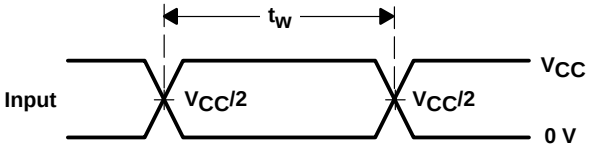
PARAMETER MEASUREMENT INFORMATION
(OPEN DRAIN)



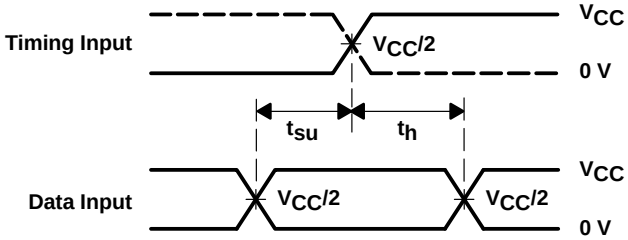
LOAD CIRCUIT

TEST	S1
t_{PZL} (see Note F)	$2 \times V_{CC}$
t_{PLZ} (see Note G)	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	$2 \times V_{CC}$

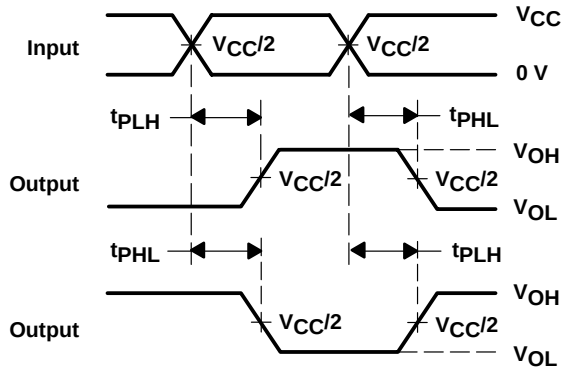
V_{CC}	C_L	R_L	V_Δ
0.8 V	15 pF	2 kΩ	0.1 V
1.2 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.5 V ± 0.1 V	15 pF	2 kΩ	0.1 V
1.8 V ± 0.15 V	30 pF	1 kΩ	0.15 V
2.5 V ± 0.2 V	30 pF	500 Ω	0.15 V



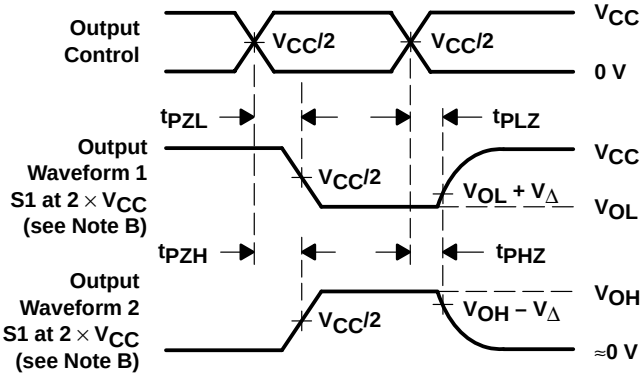
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



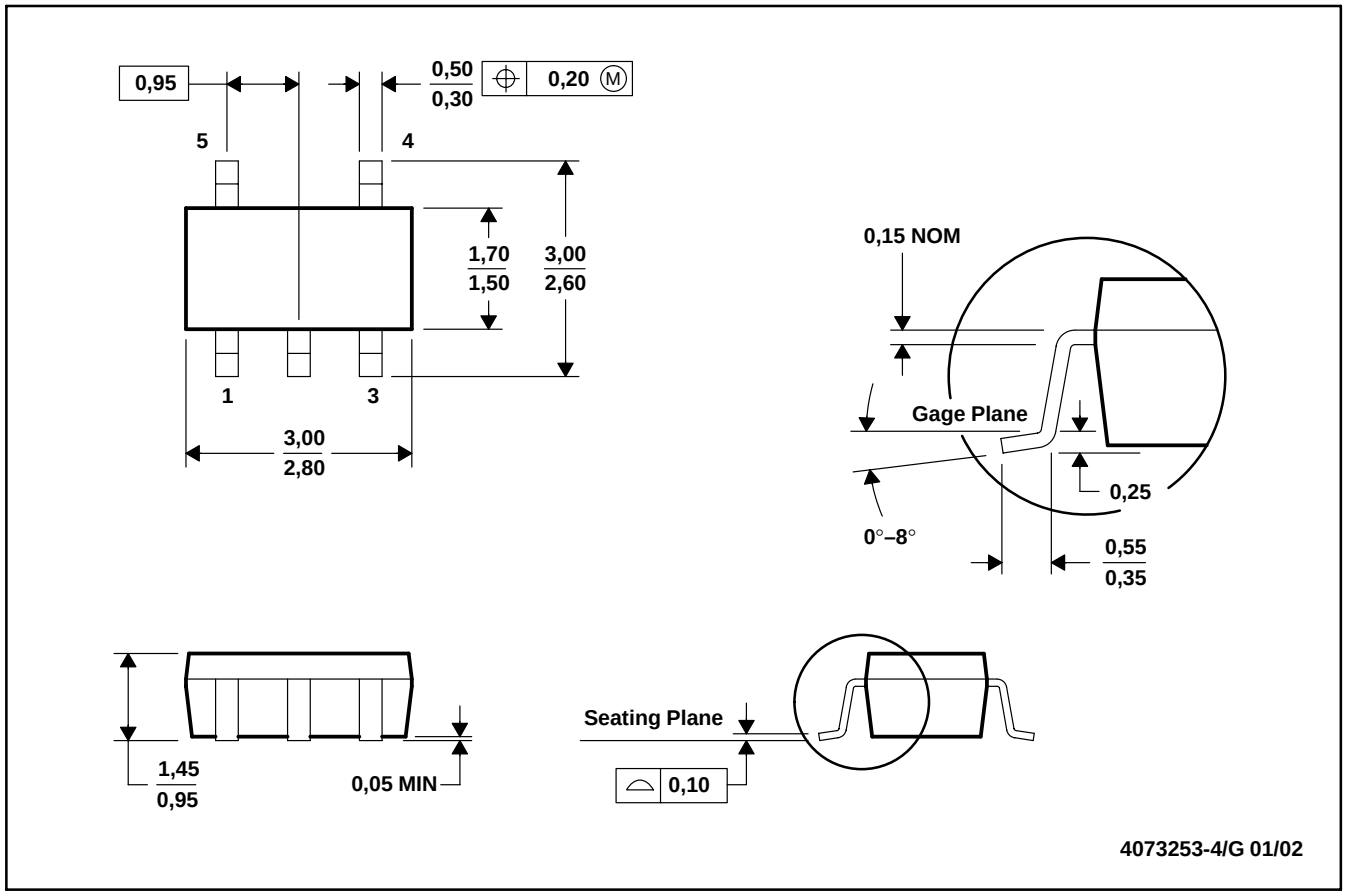
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES:
I. C_L includes probe and jig capacitance.
J. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
K. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, slew rate ≥ 1 V/ns.
L. The outputs are measured one at a time with one transition per measurement.
M. For open-drain outputs, t_{PLZ} and t_{PZL} are the same as t_{pd}.
N. t_{PZL} is measured at $V_{CC}/2$.
O. t_{PLZ} is measured at $V_{OL} + V_\Delta$.
P. All parameters and waveforms are not applicable to all devices.

Figure 20. AUC Little Logic (with Open-Drain Outputs) Load Circuit and Voltage Waveforms

Appendix B. Mechanical Data

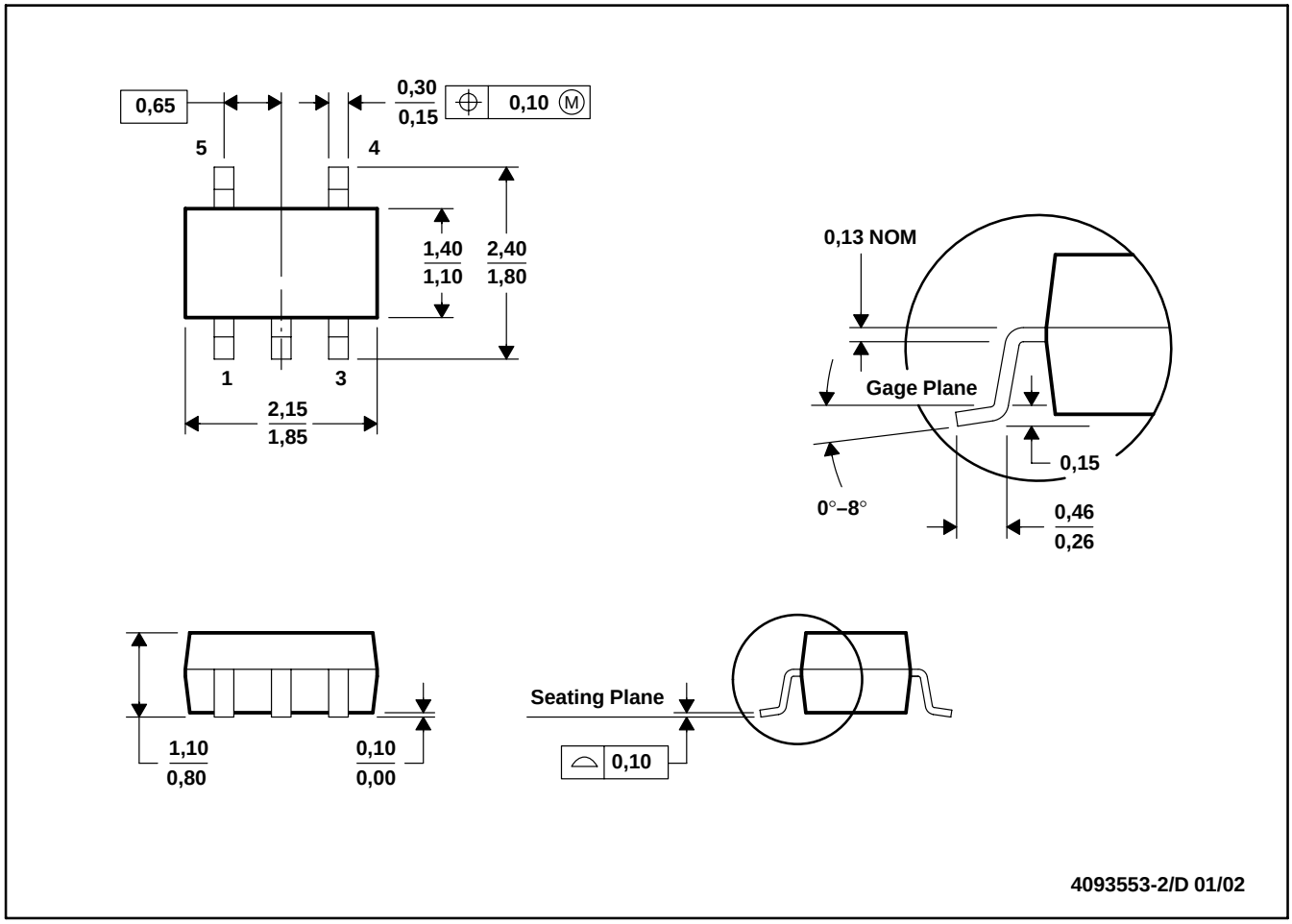
DBV (R-PDSO-G5)
PLASTIC SMALL-OUTLINE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-178

Figure 21. Plastic Small Outline (DBV)

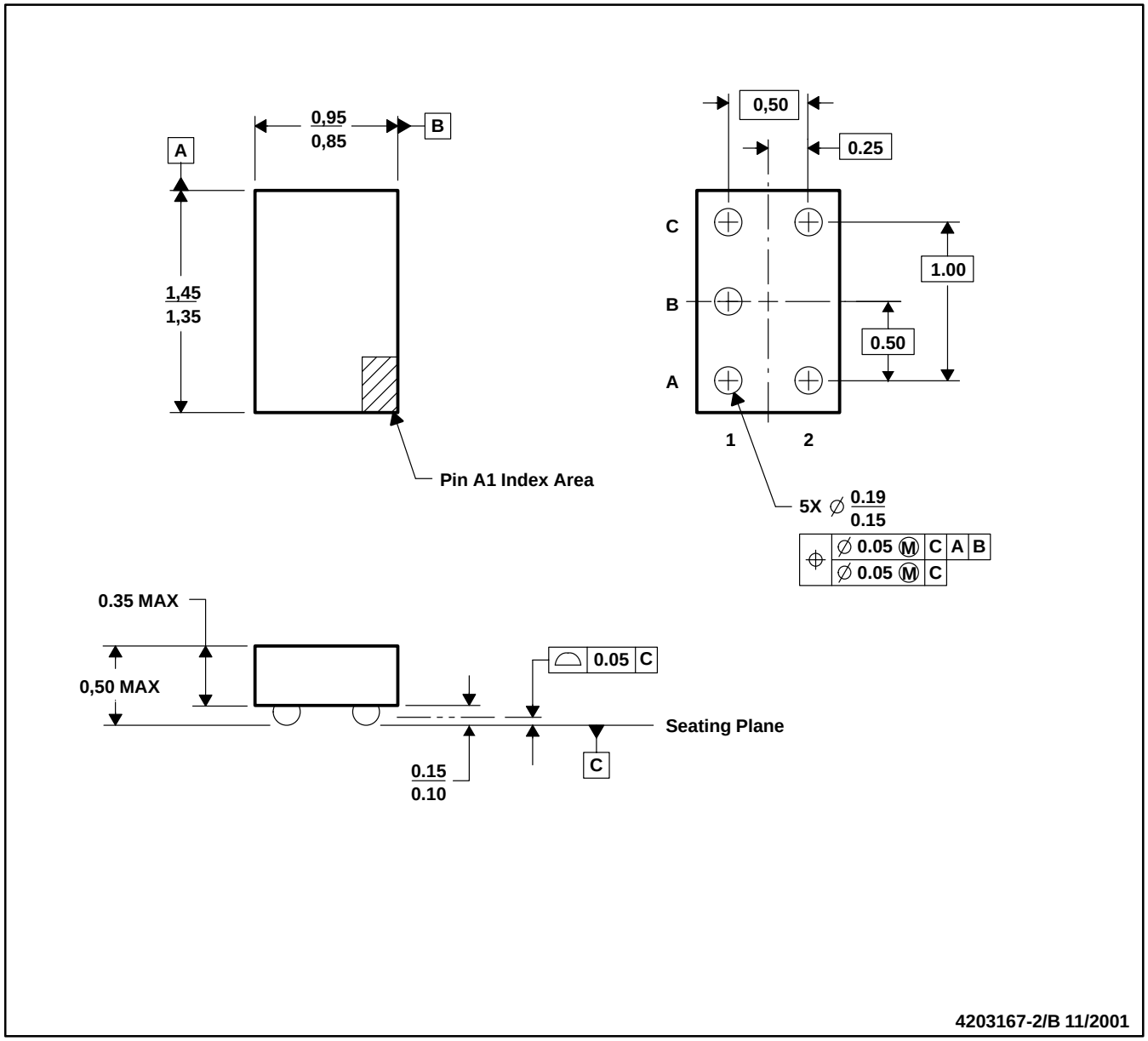
DCK (R-PDSO-G5)
PLASTIC SMALL-OUTLINE PACKAGE



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO-203

Figure 22. Plastic Small Outline (DCK)

YEA (R-XBGA-N5)
DIE-SIZE BALL GRID ARRAY



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. NanoStar™ package configuration.
D. Package complies to JEDEC MO-211.

Figure 23. Die-Size Ball Grid Array (YEA or YZA)

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Mailing Address:

Texas Instruments
Post Office Box 655303
Dallas, Texas 75265