Application Report
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Wave Solder Exposure of SMT Packages

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ABSTRACT

Attaching surface mount components to the bottomside of a printed circuit board (PCB) by wave solder processing is common practice. Because surface mount components are normally soldered using a reflow oven process the impact of wave soldering and wave solder simulation methods must be understood.

Process characterization was performed to compare the wave solder reflow method, the solder dip method, and standard reflow oven processing. Units processed through the solder dip method see a very quick rise time to peak temperature which is quite different from the other two methods. The solder dip method has excessive thermal shock.

A designed experiment compared the contribution of moisture soak, wave time, and PCB design. Both moisture soak and wave time have a strong effect on the variation seen in delamination. Reliability stressing demonstrated passing results for the units.

Testing demonstrated that the solder dip method is not a good simulation method for wave solder exposure of surface mount components. DOE testing demonstrated that moisture soak and wave time are significant factors in the process. Reliability stressing showed that units passed even with variations seen in package delamination.

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1 Introduction

It is common practice to attach surface mount components to the underside of a printed circuit board (PCB) by processing the PCB through a wave soldering operation after gluing the components to the PCB. This paper summarizes results of several tests performed to understand the performance of surface mount components when exposed to the conditions outlined in JESD22A111, *Evaluation Procedure for Determining Capability to Bottom Size Board Attach by Full Body Solder Immersion of Small Surface Mount Solid State Devices* (see Reference 1).

JESD22A111 allows for processing of components by either of two different methods, wave soldering or solder dip. The first experiment was performed to see the difference in the profile exposures for the different methods of wave soldering, solder dip, and reflow profile.

The wave solder simulation conditions in JESD22A111 are as shown in Table 1 .

Table 1. Wave Solder Simulation Conditions in JESD22A111

TEST CONDITIONS		REFLOW METHOD	
		WAVE SOLDER	SOLDER DIP
Preheat temperature		25 to 140°C	145°C
Preheat time		80 seconds	15 seconds min
Solder temperature	245°C classification	245°C +5/–0°C	245°C +5/–0 C
	260°C classification	260°C +5/–0°C	260°C +5/–0°C
Solder immersion time	Single wave simulation	5+/–1 seconds	5 +/–1 seconds
	Dual wave simulation	First wave: 5+/–1 sec	10 +/–1 seconds
		Second wave: 5+/–1 sec	

The flow for testing per JESD22A111 is as follows:

1. Initial inspection: Baseline is determined using visual inspection and acoustic microscope examination.
2. Bake: Units are baked for 24 hours at 125°C to remove moisture.
3. Moisture soak: Units are submitted to appropriate soak conditions based on moisture sensitivity level of the package.
4. Reflow: Units are subjected to either the wave solder reflow method or the solder dip procedure per conditions in Table 1.
5. Failure Criteria: After exposure to the reflow conditions units are tested electrically, inspected using acoustic microscope, inspected for external package cracks, and cross-sectioned for internal cracks.

2 Process Characterization

A trial test compared performance between the wave solder reflow method, the solder dip method, and reflow soldering. The reflow soldering profile used was based on IPC/JEDEC J-STD-020D Pb-free assembly reflow profile (see Reference 2). In trial test we followed the recommended solder dip procedure per 22-A111 solder dip parameters. Section 5.6.2b of 22-A111 says to hold devices within one inch above the hot solder for 15 seconds to simulate preheat. However, the temperature profile obtained did not match exactly with preheat temperature. We determined that when using the method described in 5.6.2b preheat did not reach the desired 145°C for 15 seconds minimum.

A visual comparison of the time/temperature profiles for each of the three soldering methods is shown in Figure 1.

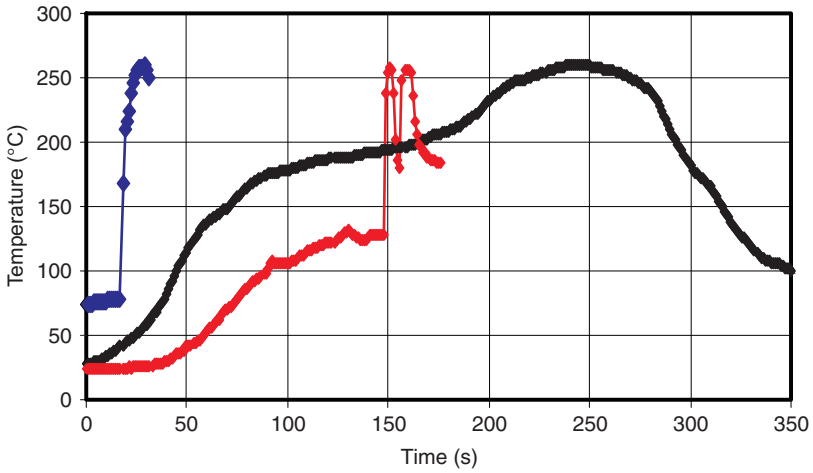

Figure 1. Comparison of Time/Temperature Profiles for Three Soldering Methods

Units exposed to the solder dip method (shown in blue) reach peak temperature much more quickly than units exposed to either the wave solder method or surface mount reflow. The units processed through the wave solder reflow (shown in red) see a slow rise to preheat temperature before rising to peak temperature of the solder in the wave. The reflow soldering profile shows a normal rise to the preheat range and then a gradual rise to peak temperature.

Comparison of the profiles shows similar peak temperatures for all three profiles. However, the solder dip method has excessive thermal shock with the component going from ≈75°C to ≈260°C very quickly. This transition does not compare to the transition seen in the wave solder profile or the reflow soldering profile.

Test units were exposed to the three different reflow conditions described above.

The test vehicle used was a 16-pin narrow body small outline integrated circuit (SOIC) package.

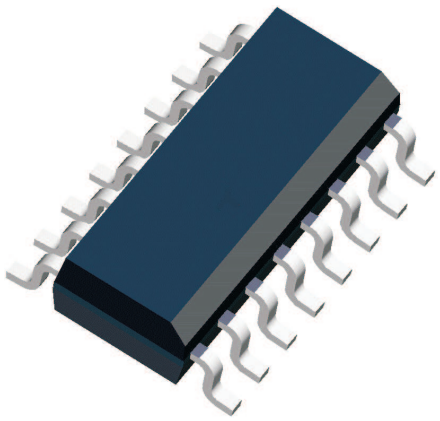

Figure 2. Isometric View of SOIC Gull-Wing Package

Prior to reflow exposure the units were baked (24 hours minimum at 125 +5–0°C) to dry the packages and then soaked. After reflow exposure, the units were processed through electrical test and SAM. Results are shown in Table 2.

Table 2. Test Results

TEST GROUP	METHOD	SOAK	ELECTRICAL TEST SAMPLE SIZE/ NO. OF FAILS	SAM SAMPLE SIZE/ NO. OF FAILS
1	Wave	MSL 1: 168 hrs at 85°C/85 RH	10 / 0	10 / 0
2	Wave	MSL 3: 192 hrs at 30°C/60 RH	10 / 0	10 / 0
3	Solder dip	MSL 1: 168 hrs at 85°C/85 RH	4 / 0	4 / 2
4	Solder dip	MSL 3: 192 hrs at 30°C/60 RH	4 / 0	4 / 0
5	Reflow	MSL 1: 168 hrs at 85°C/85 RH	10 / 0	10 / 0
6	Reflow	MSL 3: 192 hrs at 30°C/60 RH	10 / 0	10 / 0

The results of this experiment support the claim that the solder dip method imposes more severe thermal shock and is not equivalent to the standard reflow conditions used for MSL characterization.

The authors agree with the note in section 4 of 22-A111 that reads: "Assessment by dipping in a solder post usually exposes devices to higher stresses than the wave solder procedure, which results in induced failures."

Based on these results TI has decided not to use the solder dip method as a wave solder simulation.

3 Designed Experiment

A designed experiment was performed to understand the effect of processing SOIC units through wave soldering. A 16-pin SOIC package was used for this experiment.

The three factors and the factor level setting are shown in Table 3.

Table 3. Experiment Factors

LEVEL	SOAK	WAVE TIME	PWB DESIGN
1	Soak 1: bake only	5 s	Low-K
2	Soak 2: 192 hours at 30°C/60 RH	10 s	High-K
3	Soak 3: 168 hours at 85°C/85 RH		

Three different soak conditions were used to see the impact of moisture absorption. The time that the components saw in the solder wave was varied between 5 seconds and 10 seconds. Two different PWB designs were used – JEDEC Low-K (see Reference 3) and JEDEC High-K (see Reference 4) .

Table 4. Experimental Layout

RUN	WAVE TIME	PWB	SOAK
1	10 s	High-K	Soak 1
2	10 s	High-K	Soak 2
3	10 s	High-K	Soak 3
4	10 s	Low-K	Soak 1
5	10 s	Low-K	Soak 2
6	10 s	Low-K	Soak 3
7	5 s	High-K	Soak 1
8	5 s	High-K	Soak 2
9	5 s	High-K	Soak 3
10	5 s	Low-K	Soak 1
11	5 s	Low-K	Soak 2
12	5 s	Low-K	Soak 3

Four replicates for each factor level combination (FLC) shown above were processed for a total of five units per FLC.

Initial electrical test, visual inspection, and acoustic microscope examination were performed to establish a baseline. The units were baked for 24 hours at 125°C. Immediately after bake, units were exposed to the soak conditions in Table 4. Bake and soak of the units was scheduled to overlap so that all units would exit the soak chambers at the same time. Units were processed through reflow within four hours to meet the requirement of the standard which indicates "not sooner than 15 minutes and not longer than 4 hours after removal from the temperature/humidity chamber, subject the sample to the reflow conditions."

For the wave soldering operation the preheat temperature, preheat time, and solder temperature were all set according to the requirements in Table 1 of J-STD-22A111. The time in the solder was was alternated between 5 and 10 seconds depending upon the run being processed.

After completion of the wave solder processing the units were tested electrically. Then acoustic microscope examination was performed to determine the post reflow delamination. The average delta of pre-reflow delamination to post-reflow delamination was calculated for each group.

The average effects table for individual factors is shown in Table 5. An effects table shows the mean value for each factor level setting in all runs. For instance under the column heading “Soak” the average value for Soak 1 was 1.319 and the average values for Soak 2 and Soak 3 were 6.244 and 6.174 respectively. This tells us that Soak 1 provided the lowest delamination results, which is intuitive. The result seen for the wave time factor is counter intuitive with the longer wave time exposure giving the lower delamination value.

Effects plots are shown in Figure 3. An effects plot is a graphical representation of the average effects data. An effects plot is used because it provides and easy to understand visual representation of the average effects data. Basically if the effects plot is “flat” (horizontal line) then there is little to no effect. If the effects plot has a slope (slanted line) then there is some effect from the factor. The greater the slope of the line, the greater the effect.

Table 5. Average Effects

LEVEL	SOAK	MEAN VALUE	WAVE TIME	MEAN VALUE	PWB	MEAN VALUE
1	Soak 1	1.319	5 s	6.26	Low-K	3.99
2	Soak 2	6.244	10 s	2.90	High-K	5.17
3	Soak 3	6.174				

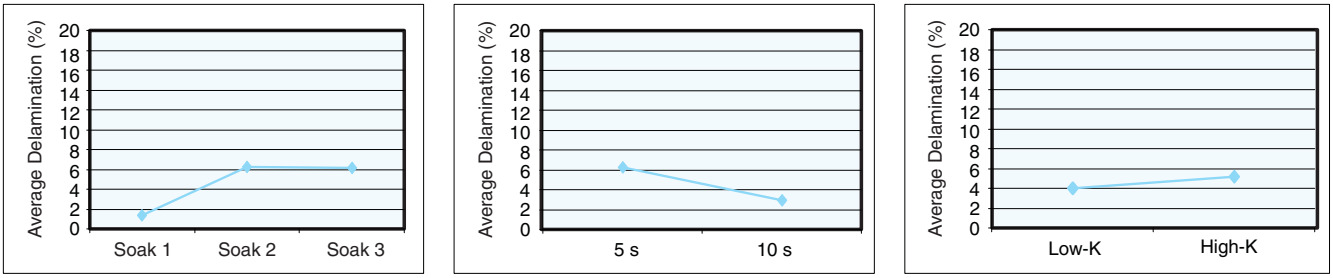

Figure 3. Effects Plots

The effects table and effects plots show that soak and wave time have a strong effect. The effect of the PWB variation is minor.

Analysis of variance (ANOVA) was used to determine contribution of each factor to the variance seen in the experiment (shown in Table 6).

Table 6. ANOVA Results

RANK	SOURCE	SS	MSE	F-RATIO	PROB > F	PERCENT CONTRIBUTION (100% total)
1	X3 (Soak)	212.09446	106.0472	4.2966	0.0236	45.41%
2	X1 (Wave Time)	108.30849	108.3085	4.3882	0.0454	23.19%
	X1*X3	61.0795	30.53975	1.2373	0.3055	13.08%
	X1*X2	44.69765	44.69765	1.8109	0.1892	9.57%
	X1*X2*X3	25.70661	12.85331	0.5208	0.5997	5.50%
	X2 (PWB)	13.5375	13.5375	0.5485	0.4651	2.90%
	X2*X3	1.59337	0.796685	0.0323	0.9683	0.34%

If $p < 0.05$, then that factor is statistically significant with 95% confidence. The ANOVA analysis showed that the main factors of soak and wave time were significant to the delamination. The main factor of PWB and all interactions were not significant.

After final CSAM data was collected and analyzed the units were cross-sectioned to inspect for package cracks. No package cracks were seen on any of the cross-sectioned units.

3.1 Reliability Stressing

JEDEC Std 22-A111 indicates that to evaluate the impact of delamination on device reliability, the product must either meet the delamination requirements listed or reliability assessment. In our evaluation we saw a few cases where a measureable delamination change (10% absolute change between pre and post reflows) was noted. Thus, we proceeded to perform a reliability assessment on packages built with the same device used in the DOE.

The following flow was used to assess the reliability performance of the units:

1. Electrical test
2. Units submitted to bake + soak
   a. Soak 1: Bake only
   b. Soak 2: 192 hrs at 30°C/60 RH
   c. Soak 3: 168 hrs at 85°C/85 RH
3. Processed through wave solder with 10 seconds exposure
4. Electrical test
5. Reliability exposure
   a. One set: unbiased HAST (130°C/85 RH)
   b. One set: temp cycle (–65°C/150°C)
6. Electrical test

Results for the reliability assessment are shown in Table 7.

Table 7. Reliability Assessment Results

	UNBIASED HAST (96 hrs at 130°C/85 RH)			TEMPERATURE 1K CYCLES (–65°C/150°C)		
ELECTRICAL TEST RESULTS (NO. TESTED/NO. FAILED)	GROUP 1	GROUP 2	GROUP 3	GROUP 1	GROUP 2	GROUP 3
Prior to bake + soak	22/0	22/0	22/0	22/0	22/0	22/0
After wave solder processing	22/0	22/0	22/0	22/0	22/0	22/0
After reliability stressing	22/0	22/0	22/0	22/0	22/0	22/0

The results of all testing are summarized in Table 8.

Table 8. Summary of Test Results

	CONDITION 1	CONDITION 2	CONDITION 3
CRITERIA	BAKED DRY	MSL3–192 hrs 30°C/60 RH	MSL1–168 hrs 85°C/85 RH
Electrical test	Pass	Pass	Pass
Die delamination	Pass	Pass	Pass
External cracks	Pass	Pass	Pass
Internal cracks	Pass	Pass	Pass
Die pad delamination	Pass	Pass	Pass
Lead finger delamination	Pass	Pass	Pass

4 Summary/Conclusions

Results of the process characterization showed that the solder dip method has the quickest rise time to peak temperature because of very short preheat. Excessive thermal shock is experienced when the components go from 140°C to 260°C very quickly. A designed experiment showed that moisture soak and wave time have a strong effect on delamination seen during wave solder processing. Units exposed to wave solder processing passed electrical test after reliability stressing (unbiased HAST and temperature cycle).

4.1 Conclusions

- The solder dip method imposes excessive thermal shock on the components. The temperature transition in the solder dip method is not comparable to what is seen in the wave solder profile or the reflow soldering profile. The solder dip method is not a good method for evaluating capability of surface mount components to be exposed to bottom side board attach.
- Independent of variation seen in delamination, all units passed electrical test after wave solder processing and reliability stressing. The 16-pin SOIC units tested passed the criteria outlined in JESD22A111.

5 References

1. *Evaluation Procedure for Determining Capability to Bottom Size Board Attach by Full Body Solder Immersion of Small Surface Mount Solid State Devices*, JESD22A111, May 2004.
2. *Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices*, IPC/JEDEC J-STD-020D, June 2007.
3. *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, EIA/JESD51-3, August 1996.
4. *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*, EIA/JESD51-7, February 1999.

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