Application Report
SCEA055–August 2017

Designing and Manufacturing with TI's X2SON Packages

Emrys Maier, Tim Claycomb

ABSTRACT

Board layout and stencil information for most Texas Instruments (TI) Extra Small Outline No-Lead (X2SON) devices is provided in their data sheets. This document helps printed-circuit board (PCB) designers understand and better use this information for optimal designs.

Using the X2SON packages allows users to condense PCB layouts and implement a design using minimal space due to the X2SON small package dimensions. When working with this space saving package, understanding some key PCB manufacturing and assembly limitations can reduce the complexity of a final product. This application report will discuss some of the limitations when manufacturing and assembling a PCB containing the X2SON package. There are three primary factors that affect manufacturing of printed circuit boards (PCBs) with regard to package size and pitch. These are: PCB manufacturing, solder application, and component placement.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

Figure 1. X2SON-5 (DPW) Package

Figure 2. X2SON-6 (DTB) Package

Board layout and stencil information for most Texas Instruments (TI) Extra Small Outline No-Lead (X2SON) devices is provided in their data sheets. This document helps printed-circuit board (PCB) designers understand and better use this information for optimal designs.

Using the X2SON packages allows users to condense PCB layouts and implement a design using minimal space due to the X2SON small package dimensions. When working with this space saving package, understanding some key PCB manufacturing and assembly limitations can reduce the complexity of a final product. This application report will discuss some of the limitations when manufacturing and assembling a PCB containing the X2SON package. There are three primary factors that affect manufacturing of printed circuit boards (PCBs) with regard to package size and pitch. These are: PCB manufacturing, solder application, and component placement.

2 PCB Manufacturing

PCBs must be designed to meet the manufacturing specifications of the PCB manufacturer. PCB manufacturability is dependent on the required clearance specifications. Tighter clearance specifications lead to an increase in complexity, limiting the number of capable manufacturers.

Most established PCB manufacturers can produce copper layers with spacing and traces as fine as 0.1 mm (~4 mil) and drill holes down to 0.1 mm (~4 mil). The basic PCB footprint for the X2SON line of packages only requires spacing of 0.208 mm (8.2 mil) – which is well within manufacturing limits.

The primary concern for manufacturing with these packages comes from the method used to connect to the center pin(s). The PCB's manufacturability will be affected by four main clearance specifications: trace-to-trace clearance, trace width, drill diameter, and annular ring diameter. Figure 3 gives a visual representation of each specification.

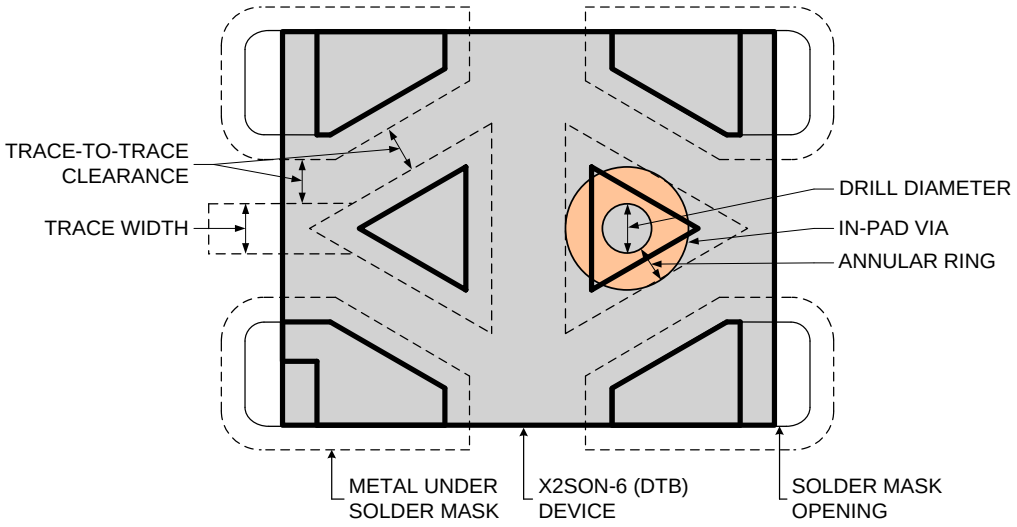

Figure 3. Clearance Specifications

Figure 4 displays the first option access the center pin. This option is to route a trace on the same layer as the X2SON-5 (DPW) package between two pins. This will introduce trace-to-trace clearance and trace width limitations. The maximum space between the corner pads is 0.26 mm (10.2 mil) and assuming that the minimum trace width allowed to be manufactured without increasing complexity is 0.1 mm (~4 mil), the trace-to-trace minimum spacing is 0.08 mm (3.15 mil). A trace-to-trace clearance requirement of less than 0.1 mm (~4 mil) will increase the complexity to manufacture may not be possible to manufacture at some PCB fabrication houses. Major PCB manufacturers can achieve detail accuracy of 0.05 mm (~2 mil) as of this writing.

Figure 5 displays a second option to route a trace to the center pin. This option routes a trace on a separate signal layer from the X2SON-5 (DPW) package pads and uses a via to connect to the center pin. By routing the trace on the bottom layer, tight trace-to-trace and trace width clearance is avoided on the top layer. This layout method will introduce additional limitations related to the drill size and annular ring. The drill diameter must be kept greater than 0.1 mm (~4 mil) to avoid an increase in complexity and possible manufacturing issues. Additionally, the via diameter must be less than 0.35 mm (13.78 mil) so that the via is smaller than the center pin. This requires a minimum annular ring specification of 0.125mm (~5 mil). This option provides the most efficient solution as an annular ring specification of 0.125 mm is easily accomplished by most PCB fabrication houses.

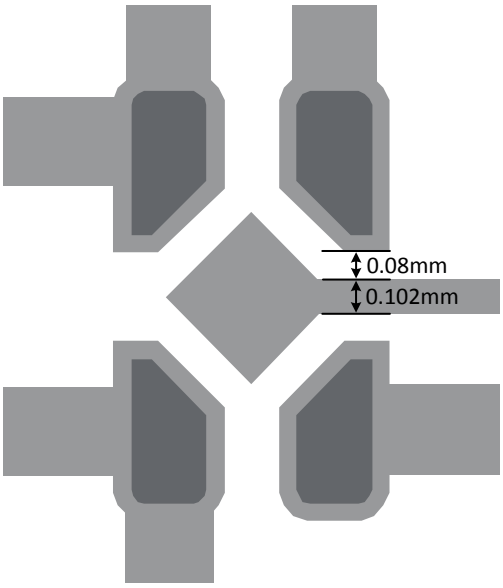

Figure 4. X2SON-5 (DPW) Package Center Pin Layout Option 1

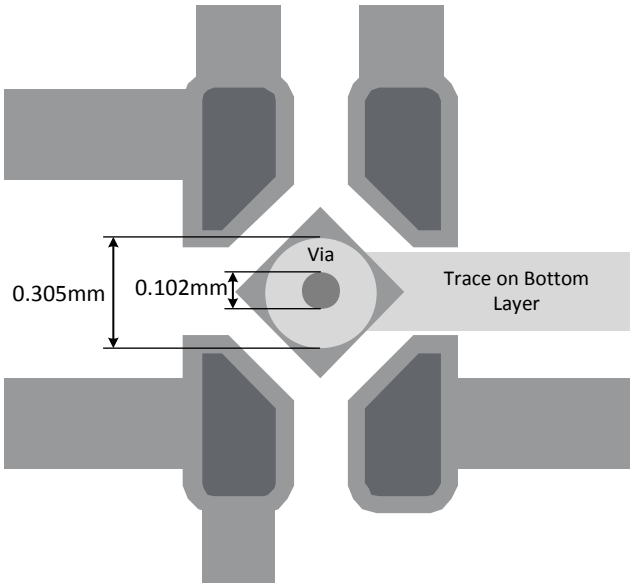

Figure 5. X2SON-5 (DPW) Package Center Pin Layout Option 2

Drill size limitations must be considered when a via is placed in the center pad. Use a 0.1 mm (~4 mil) diameter or smaller drill to place vias directly in the center pads. Figure 7 shows a 0.1 mm via to scale in the center pad. Note that a slightly larger solder aperture in the solder stencil is recommended if this approach is used, since some solder will wick into the via. Even if solder is placed slightly outside the pad, it will be drawn to the pad as long as it does not contact any other pads or solder.

Figure 6 and Figure 7 show layout examples with the appropriate devices overlaid upon them. Note that the solder mask openings are larger than the exterior pads, which allows for visual solder inspection of those pads. Additionally, the solder pad metal extends underneath the solder mask specifically to add physical strength to the pads. The exact measurements are provided in the mechanical drawing sections of each device's datasheet.

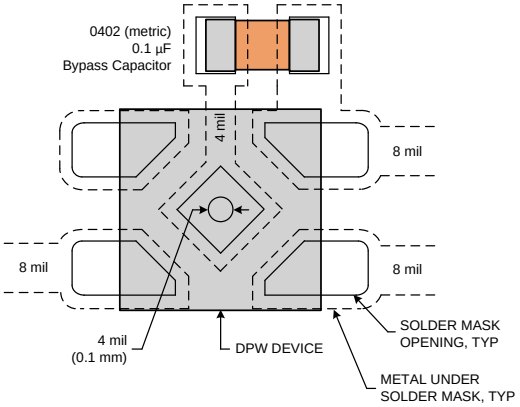

Figure 6. X2SON-5 (DPW) Package PCB Complete Footprint Example with Bypass Capacitor Shown

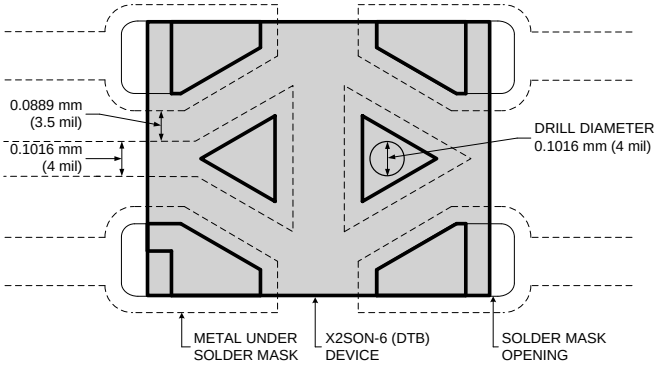

Figure 7. X2SON-6 (DTB) Package PCB Footprint Example Without Bypass Capacitor Shown

3 Solder Paste Application

Solder paste application is the most concerning area for very small parts due to the number of issues involved. The correct amount of solder needs to be placed on the pads. The amount of solder is affected by stencil thickness, solder type, and aperture size and shape. This becomes more difficult for packages with pitch smaller than 0.4 mm (15.7 mil). TI's X2SON packages maintain 0.4 mm (15.7 mil) pitch while reducing overall package size, which allows for more error in the assembly process without a significant impact to production yield.

TI recommends using a 0.1 mm (~4 mil) thick solder stencil with apertures sized to between 92% and 100% of the pad size for proper solder deposition. This should be increased by 10% when a via-in-pad approach is used. Figure 8 and Figure 9 show the solder paste recommendations for TI's X2SON-5 (DPW) and X2SON-6 (DTB) packages, respectively.

Solder stencil aperture size is linked to solder paste selection. There are two primary types of solder paste used for SMT soldering today: Type III and Type IV. Type III solder paste has become the standard today, and Type IV solder paste is used when more consistent and finer particles are required. Type III solder paste contains particles with diameters of 25-45 µm (0.98-1.77 mil), and Type IV solder contains particles with diameters of 20-38 µm (0.79-1.50 mil). A typical rule of thumb is that aperture width should be at least 5 times the solder ball size. Given the 0.24 mm (9.45 mil) aperture shown in Figure 8, solder ball diameter must be less than 0.048 mm (1.89 mil), which means that Type III paste can be used.

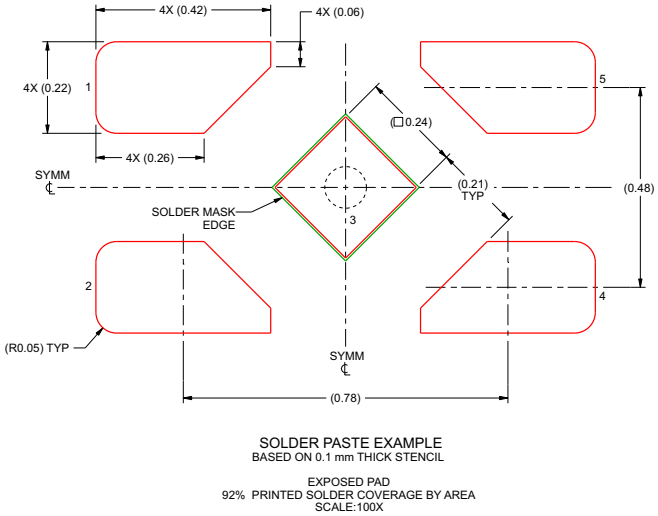

Figure 8. X2SON-5 (DPW) Package Solder Stencil Example

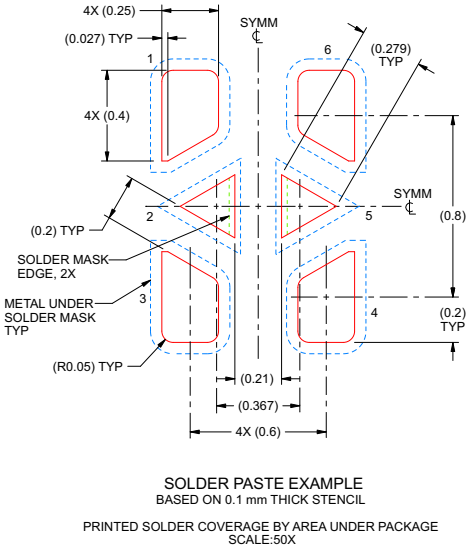

Figure 9. X2SON-6 (DTB) Package Solder Stencil Example

4 Component Placement

Component placement by pick and place machines is typically very accurate, on the order of ±30 µm accuracy. Figure 10 and Figure 11 show a one third pad placement error for the X2SON packages. In order to seat the part properly, an accuracy of ±83 µm (3.28 mil) or better is required for the X2SON-5 package, and ±72 µm (2.94 mil) for the X2SON-6 package. This enables all pins to make good contact with the solder paste and prevents them from being more than one third off of alignment with their pads. Surface tension from the melted solder will align the part during the soldering process. Since many pick and place machines have better than the required accuracy values, this issue should not be a concern for major PCB assembly companies.

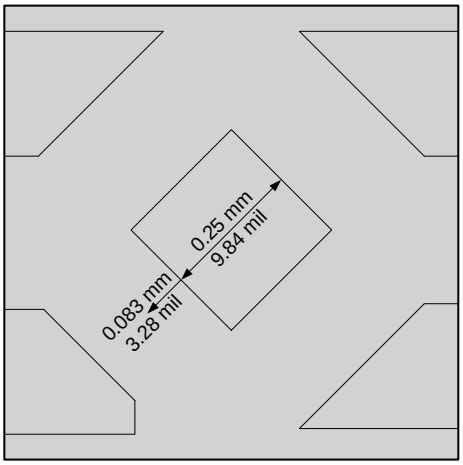

Figure 10. X2SON-5 (DPW) Package Maximum Offset

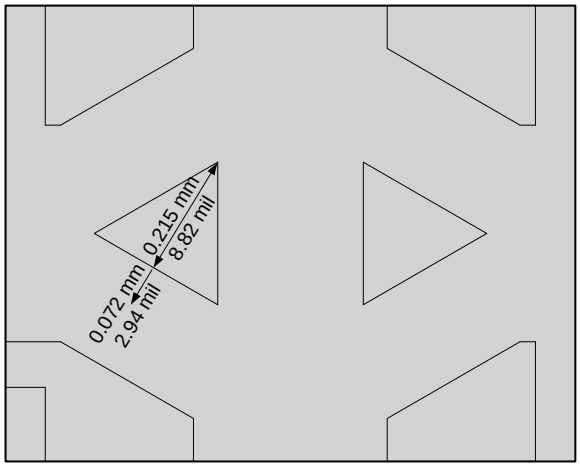

Figure 11. X2SON-6 (DTB) Package Maximum Offset

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265