

Enabling Optimal Solar Inverter Power Stage Designs with Logic



Atul Patel

Green energy has become a critical component of the overall energy strategy for governments, corporations, and individuals. At the heart of green energy is the growing impact of solar power generation. Solar panel installations have increased dramatically in recent years as advancements in technology has significantly reduced the cost of photovoltaic cells that make up solar panels. One technology that has contributed to the increase in solar installations is the availability of low cost and efficient *String* and *Micro* inverter technologies. Solar inverters help address efficiency and scalability concerns often associated with investing in solar power generation. Solar Inverter technology is essential for synchronizing a solar installation with the grid so that maximum utility can be realized from the generated power.

Solar inverters perform the critical function of converting the Direct Current (DC) generated by solar panels to usable Alternating Current (AC). Converted alternating current can be used on site for home and commercial uses or synchronized back to the grid enabling cost savings through net metering. As solar power generation continues to grow, string and micro inverters have become enabling technologies. Robust and efficient inverter designs have become critical to the solar ecosystem. Inverter system designers face multiple design challenges such as enabling robust solutions that can support high temperatures as well as efficient operation and compact implementation size. To help with overcoming common [design challenges in their inverter designs, system designers can leverage robust multi-gate logic and level translations solutions](#). One of those challenges is implementing the power stage subsystems. Power stage subsystems are often comprised of gate drivers and associated FETs and Power Transistors (Insulated-Gate Bipolar Transistors).

The power stage implementations of inverter designs need robust logic buffers and gate logic to implement control logic for coordinating the gate drive functionality. Logic gates and buffers become

indispensable in helping designers connect and scale microcontroller unit (MCU) GPIO to Gate Driver links See [Figure 1](#). Often MCUs are selected for their cost effectiveness and low power at the expense of drive strength. Inverter system designers can use robust single and multi-channel logic buffers in between the MCU outputs and gate driver inputs to ensure sufficient input signaling levels at the gate driver input. Buffers are especially important in larger implementations such as central and string inverters where the MCU may be located farther from the gate drivers of the power subsystems.

The example, [Figure 1](#) can serve as a common implementation approach for [buffering signals](#) between the MCU and gate drivers for solar inverters. Component selection can be critical when selecting buffers for a solar inverter design. Criteria such as drive strength, channel count, voltage range, temperature range, and package size can all play a critical role in a design. Table 1 provides a guide for selecting buffers and other commonly used logic devices based on a matrix of these key criteria. As solar inverter designers continue to drive designs to be lower cost, higher performance, and more robust, they will need to leverage simple logic devices like buffers and gate logic. Simple logic building blocks can enable designers to not only bring their systems together but also scale them to the requirements of larger and more complex solar power installations that are expected in the future.

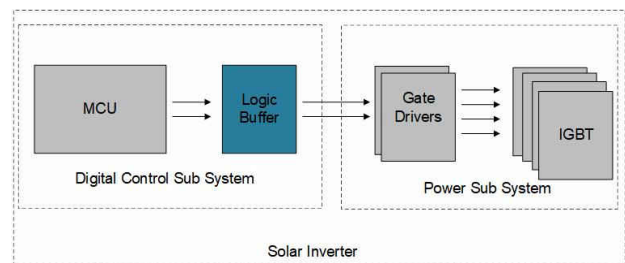


Figure 1. Buffer Use Case for Inverter Gate Drives

Table 1. Device Selection Table

| Device | Voltage | Type | Channels | Drive Strength | Temp Range | Multi-Sourced foot prints | Small Package Options | Suitable For | Q100 Availability |
|------------------------------|-----------------|----------|----------|----------------|--------------|---------------------------|-----------------------|----------------------------|-------------------|
| SN74LVC1G125 | 1.65 V to 5.5 V | Buffer | One | 24ma | -40C to 125C | Yes | uQFN | Micro & String Inverters | Yes |
| SN74LVC2G125 | 1.65 V to 5.5 V | Buffer | Two | 24ma | -40C to 125C | Yes | BGA | Micro & String Inverters | Yes |
| SN74HCS125 | 2 V to 6 V | Buffer | Quad | 7.8ma | -40C to 125C | Yes | uQFN | String & Central Inverters | Yes |
| SN74HCS08 | 2 V to 6 V | AND Gate | Quad | 7.8ma | -40C to 125C | Yes | uQFN | String & Central Inverters | Yes |
| SN74LVC1G14 | 1.65 V to 5.5 V | Inverter | One | 24ma | -40C to 125C | Yes | uQFN | Micro & String Inverters | Yes |
| SN74HCS14 | 2 V to 6 V | Inverter | Six | 7.8ma | -40C to 125C | Yes | uQFN | String & Central Inverters | Yes |

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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