

Translate Voltages for MDIO



Management Data Input or Output (MDIO) is a control protocol designed primarily for use with ethernet PHY devices. It typically utilizes an unidirectional 2.5 MHz clock signal (MDC) and bidirectional data bus line (MDIO). See [Translate Voltage for RGMII](#) for details on the accompanying RGMII translation.

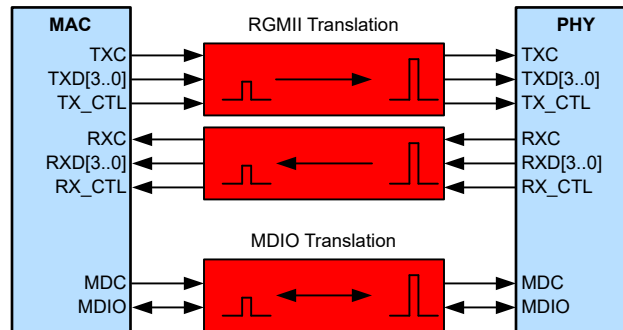


Figure 1-1. Example MAC to PHY Voltage Translation Block Diagram

See more about auto-bidirectional voltage translation in [Translation Between Communication Modules and System Controllers](#)

Design Considerations

- Translators enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Use a fixed-direction translator for the clock (MDC) if higher speeds are required; some newer devices use a clock as high as 50 MHz
- Open-drain compatible translators are required for the data line; although the protocol is not open-drain, pull-up resistors are required on the MDIO signal bus because there are times when the bus is not actively driven
- See answers to our most frequently asked technical questions on [\[FAQ\] Voltage Translators](#)
- Need additional assistance? Ask our engineers a question on the [TI E2E™ Logic Support Forum](#)

Recommended Parts

Part Number	AEC-Q100 Qualified	Voltage Translation Range	Features
SN74AXC1T45		0.65 V – 3.6 V	Glitch-free power supply sequencing Outputs are disabled when either supply is 0 V Active translation architecture Up to 500 Mbps for 1.8 V to 3.3 V translation
SN74AXC1T45-Q1	✓		
TXS0102		1.65 V – 5.5 V	Auto-bidirectional Open-drain compatible Integrated pull-up resistors
TXS0102-Q1	✓		

For more devices, browse through the [online parametric tool](#) where you can sort by desired voltage, channel numbers, and other features.

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