Using High-Speed CMOS and Advanced CMOS Logic in Systems With Multiple $V_{CC}$ Supplies or Partial Power Down

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CMOS devices offer a designer many desirable features, the most important one being low-power consumption. However, in some systems a designer finds that even the low-power consumption of CMOS is insufficient to meet power supply constraints. Therefore, some designers use partial system power-down or multiple $V_{CC}$ supplies to meet their system power requirements.

When a system uses multiple $V_{CC}$ supplies or partial power down, designers must take into account several important device parameters when high-speed CMOS (HC) or advanced CMOS (ACL) devices are used. This is necessary to avoid excessive power dissipation and prevent damage that could lead to a degradation in the reliability of the device. These parameters are the continuous input and output diode currents ($I_{IK}$ and $I_{OK}$) and the continuous output current ($I_{O}$). $I_{IK}$ and $I_{OK}$ refer to the continuous current flowing through the input and output electrostatic discharge (ESD) protection circuits. Figure 1 shows functionally equivalent schematics of the ESD structures for HC and ACL devices.

$I_{O}$ is the continuous current flowing through one of the two output transistors. Table 1 shows the absolute maximum rating for $I_{IK}$, $I_{OK}$, and $I_{O}$ for both HC and ACL devices, as listed on device data sheets.
Table 1. Absolute Maximum Values for $I_{IK}$, $I_{OK}$, and $I_O$

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>ABSOLUTE MAXIMUM</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>HIGH-SPEED CMOS (HC)</td>
</tr>
<tr>
<td>$I_O$</td>
<td>±25 mA (standard)</td>
</tr>
<tr>
<td></td>
<td>±35 mA (high-current)</td>
</tr>
<tr>
<td>$I_{IK}$</td>
<td>±20 mA</td>
</tr>
<tr>
<td>$I_{OK}$</td>
<td>±20 mA</td>
</tr>
</tbody>
</table>

To understand how $I_{IK}$, $I_{OK}$, and $I_O$ can affect a system design, consider an example of a partial system power down. Figure 2 shows a partial power-down situation where a device powered with $V_{CC} = 5$ V is driving a device without power applied. The input voltage to the nonpowered device exceeds $V_{CC}$ by more than the threshold voltage (0.6 V to 0.8 V), causing the ESD protection structure to conduct whenever the output of the driver is in a high state. Therefore, the driving device powers up the receiving device and any other device sharing the same $V_{CC}$ line. If no current limiting is provided, the maximum $I_O$ of the driving device and the maximum $I_{IK}$ of the receiving device could be exceeded.

Several methods are available to protect the driving and receiving devices during partial system power down. If the driving device has 3-state outputs, placing the outputs in the high-impedance state provides the best solution. However, if this is not a viable option, some method of current limiting must be provided. Figure 3 shows several methods that can be used, with current-limiting series resistors being the simplest. The value of the resistor is chosen to limit the current into the receiving device to less than 20 mA. The major drawback to using a current-limiting resistor is power dissipation. Another drawback is the effect that the resistor has on the input transition time at the receiving device during normal system operation. If the total capacitance of the interconnects and receiving devices is high (i.e., a high-capacitance bus), a current-limiting resistor increases the input transition time. A system designer must ensure that the addition of the resistor does not increase the input transition time above the maximum input transition time of the receiving device.

A second method of current limiting involves the use of a pullup resistor and a diode (see Figure 3). The advantage of this method is that it allows the use of a large resistance, thereby holding power dissipation to a minimum. The disadvantage of this method is that it requires the use of additional components and results in a higher value of $V_{IL}$ at the receiving device.
A second example of how a partial power down can cause unwanted operation is the case of two drivers connected to the same bus with one device powered down, as shown in Figure 4. In this case, the first bus driver attempts to power up the second bus driver and any other devices sharing the same $V_{CC}$ line through the output ESD structure of the unpowered device.

Several methods are available to solve this type of problem. One method is simply to use a current-limiting resistor as outlined above. Another solution is to isolate the unpowered driver from the $V_{CC}$ line by putting a diode between the power pin and the $V_{CC}$ supply. If the unpowered device is a transceiver, pullup or pulldown resistors are required on the output control inputs to disable the outputs. Not disabling the transceiver outputs allows the transceiver to power up the unpowered devices that are driven by its outputs. When an isolating diode is used, the $V_{CC}$ at the driver is always a diode forward drop below the voltage of the supply, resulting in a degradation of $V_{OH}$. Figure 5 illustrates these circuit solutions.

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**Figure 4. Partial Power Down With Bus Drivers**

**Figure 5. Current Limiting for Bus Drivers During Partial Power Down**
Another example of a system that could require current-limiting protection is one that uses multiple \( V_{CC} \) supplies, or a system that provides each card with its own on-board voltage regulator. If the \( V_{CC} \) supplies of two connecting devices differ by more than 0.5 Vdc, a current-limiting scheme should be considered if the driving device is a CMOS device and is connected to the high \( V_{CC} \). This is necessary because \( V_{OH} \) of a CMOS device is the same as \( V_{CC} \) when the \( I_{OH} \) requirement is very small. Therefore, the input ESD protection diode could conduct if the \( V_{CC} \) of the driver (or \( V_{OH} \)) exceeds the \( V_{CC} \) of the receiver by more than 0.5 Vdc. The resulting current flow causes the degradation of the diode, not the voltage.

**NOTE:**

This applies only to supplies that vary by more than 0.5 Vdc. Dynamic switching currents could cause transient voltage spiking on \( V_{CC} \) lines such that a 0.5-V difference between supplies could easily exist. These transients do not cause a problem if they have a short duration (less than 20 ns).

Partial system power down offers a designer a convenient method to save on system power consumption. However, when a partial power-down scheme is used, a designer must ensure that no damage occurs to devices and that excessive power dissipation is avoided. The designer also must take similar precautions when using multiple \( V_{CC} \) supplies if the supplies of two connecting devices differ by more than 0.5 Vdc.