Impact of JTAG/1149.1 Testability on Reliability

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Introduction

Increasingly aggressive testability requirements on modern electronics development programs are being imposed by the industry. These requirements usually increase the size of the hardware design. Traditionally, the addition of hardware for testability functions such as readback, pattern generation, pattern insertion, and functional hardware test control is known as ad hoc testability. In general, testability hardware can increase design factors such as part count, connector pins, board "real estate," cost, and power.

JTAG/1149.1 Overview

Advances in testability methodology have led to the development of bus-based observability and controllability systems instead of the traditional ad hoc methods. One of these bus-based systems was proposed by the Joint Test Action Group (JTAG). The specification developed by JTAG evolved into IEEE Std 1149.1 (1149.1)[1] for a four-wire test-bus interface and boundary-scan architecture. Boundary scan is a specialized scan path that provides observability and controllability to device or board input/output pins. The 1149.1 architecture is designed to improve a circuit's fault detection and isolation capabilities. Products such as test-bus transceivers have been developed to incorporate the boundary-scan protocols.

Testability Design Tradeoffs

Testability can impact related design-support disciplines such as reliability, maintainability, or predictability. The addition of testability circuitry can reduce test costs and time, improving the ease and accuracy of fault detection and isolation. Testability can improve maintainability calculations for mean time to repair (MTTR) by decreasing the test isolation time but can impact the reliability calculation for mean time between failure (MTBF) negatively by increasing the failure rate.

The ad hoc testability approach typically adds 10 to 15 percent extra hardware to the functional design. The Texas Instruments (TI) approach to the application of 1149.1 is to place testability features into already required functional parts.

TI offers specialized test buffers, latches, transceivers, and registers that conform to 1149.1. The bus-interface products offered by TI also incorporate additional testability features such as Parallel Signature Analysis (PSA) and Pseudo-Random Pattern Generation (PRPG) (see Table 1).

Comparing products compliant to 1149.1, a System Controlability and Observability Partitioning Environment (SCOPE) test octal to a standard article, the test octal has approximately 800 gates compared to fewer than 100 gates in a standard octal. The majority of the additional gate count in the scan parts is not in the functional path but in the scan-path control logic. The addition of boundary scan to a buffer places only two gates in each functional signal path. Only 16 gates are added to the normal operational mode. A failure in the scan-path logic does not affect the chip's normal function in most cases. A failure in the scan-path control and scan logic can be isolated by using the inherent parallelism of the boundary-scan logic. The extra gate count impacts the chip-level failure rate, but the benefits for board- and system-level testing can justify the increased failure rate.

Table 1. Feature Comparison for Standard Octal and SCOPE Testability Octal Parts

FEATURES	STANDARD OCTAL PARTS	TESTABILITY OCTAL PARTS
Pin count	20	24
Gate count	< 100	~800
Failure rate: at 0°C at 60°C	 0.0401 0.1500	 0.0563 0.2762
Normal functions	Buffer, latch, transceiver, register	Buffer, latch, transceiver, register
Internal test functions for testing of other parts	None	Signature analysis Pseudorandom pattern generation Boundary scan Readback and latch (245) 1/0 toggle mode
External test purposes	Readback latch control register	Readback latch Control register Pattern generator

Memory-Board Example

This paper illustrates the impact of 1149.1 on reliability using a basic memory-board example. The memory-board example was selected because it is a common design architecture, and because it requires additional testability for fault detection and isolation. To fully illustrate the design tradeoffs involved, the memory board is implemented in the following three different configurations:

- No-testability baseline design (see Figure 1)
- Ad hoc testability design (see Figure 2)
- 1149.1 testability design (see Figure 3)

Each of these three designs has different trade-offs for reliability, testability, and other design considerations.

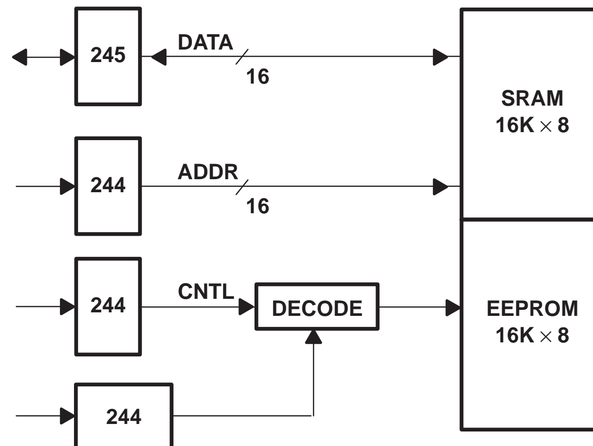

Figure 1. No-Testability Baseline Design

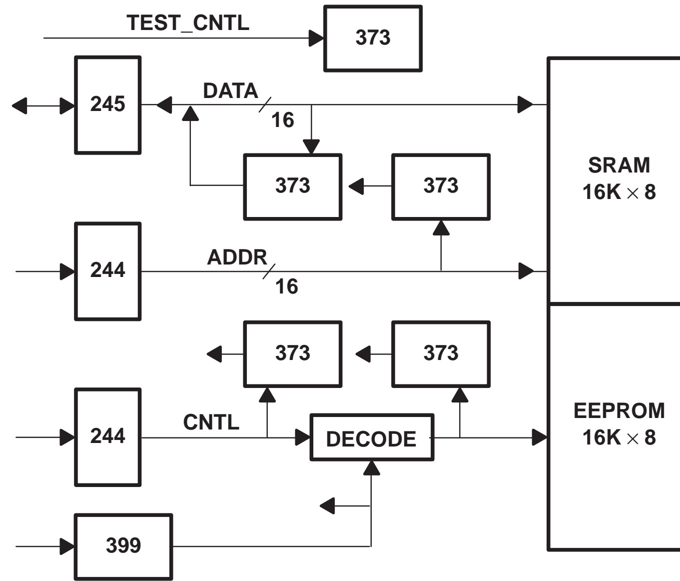

Figure 2. Ad Hoc Testability Design

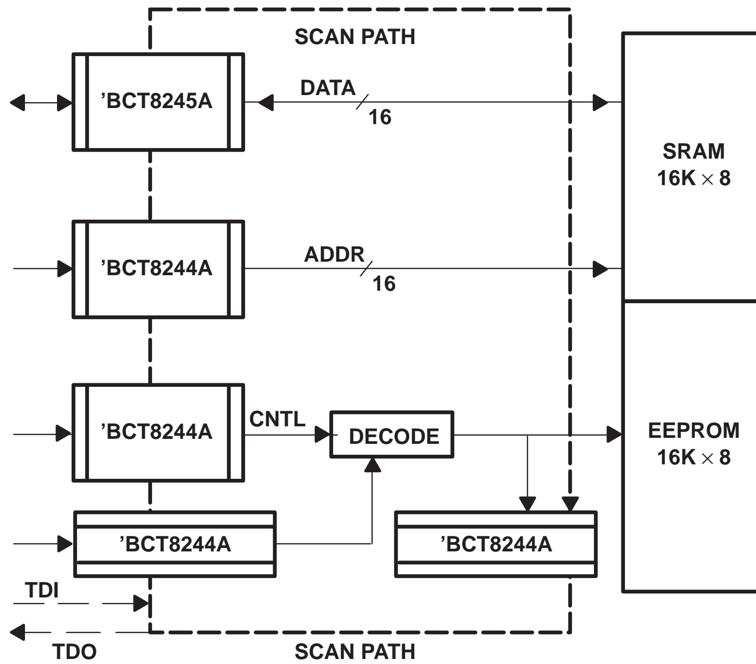

Figure 3. 1149.1 Testability Design

Baseline Memory-Board Design

The baseline memory board is a straightforward design consisting of 17 parts on a Versabus Modular European (VME) type board (see Figure 1 and Table 2). The data and address buses are each 16-bits wide, and the processor control bus is 8-bits wide. These buses are pulled up and buffered between the memory and the connector. The decode function consists of a comparator for the board base address select and a Programmable Array Logic (PAL) to implement memory select, address decode, and read/write control. The board's base address is jumpered and buffered. Some additional control logic (such as write-protect enable) is implemented with combinational gates.

The baseline memory board is not inherently testable for isolation purposes. To meet today's requirements, component ambiguity groupings of four or less must have isolation percentages in the high 90s. Despite the simplicity of the board, it cannot meet these requirements.

For an example of the poor fault-isolation capability, consider the following case. A failure is detected by a test sequence that writes to the Static Random-Access Memory (SRAM) and reads back the written value for comparison. The following are possible candidates for the fault location if the test fails.

- A stuck-at bit in the SRAM — returns the wrong value on the read
- The bidirectional transceiver — disrupts the data bus transfer
- The decode logic — chooses the wrong memory device or wrong peripheral device [the identification (ID) buffer]
- The address decode — chooses the wrong memory location
- The control logic — chooses wrong memory action (read versus write)
- Identification jumper/buffer — chooses the wrong board in the system or maps memory incorrectly
- The connector — passes incorrect data
- The resistor pack — causes a bus line to float

Table 2. Baseline Memory Parts List With Failure Rates

QUANTITY	PART	FAILURE RATE AT 0°C	FAILURE RATE AT 60°C
1	54LS85	0.0294	0.0997
1	PAL–16L8	0.2904	1.6314
1	54ALS04	0.0237	0.0519
2	SRAM–HM6264	1.6259	23.6086
2	EEPROM–X2864A	1.0582	9.4955
2	Transceiver–'245	0.0802	0.3000
4	Buffer–'244	0.1604	0.6000
1	Jumper	0.0000	0.0000
2	Resistor pack	0.0807	0.7631
2	96-pin connector	0.0646	0.2908
	Failure-rate totals:	3.4135	36.8410

Any of these failures can cause the return of an incorrect data value. Only two types of tests can be run on this board: an end-to-end test of the SRAM or of the Electrically Erasable Programmable Read-Only Memory (EEPROM). An intermediate test cannot be performed to reduce the ambiguity groupings. All testing requires a memory storage and retrieval to detect a fault. The ambiguity for most faults is most of the board (see Table 3).

To reduce the ambiguity requires long, complicated testing algorithms that run specific pattern sequences through the memory space to characterize the fault. This only can reduce the ambiguity in some cases and results in long test times because of extended pattern generation.

Table 3. Baseline Memory-Board Test Flow and Fault-Isolation Ambiguity Groupings

BASELINE TEST FLOW	AMBIGUITY GROUPINGS
SRAM tests	17 — Connector, pullups, buffer, comparator, PAL, SRAM, EEPROM, ID buffer, jumpers, transceiver, NANDs
EEPROM tests	17 — Connector, pullups, buffer, comparator, PAL, SRAM, EEPROM, ID buffer, jumpers, transceiver, NANDs

Ad Hoc Testability Memory Board

The ad hoc version of the memory board is derived from the baseline board by placing readback latches on the data, address, and control buses; by replacing the ID buffer with a 4-bit multiplexer/latch; and by placing a test-control register on the board (see Figure 2 and Table 4). The design contains the minimum testability required to bring the ambiguity groupings to four components or less. The testability improvement results in adding seven parts to the board and replacing another.

Table 4. Ad Hoc Memory-Board Parts List With Failure Rates

QUANTITY	PART	FAILURE RATE AT 0°C	FAILURE RATE AT 60°C
1	54LS85	0.0294	0.0997
1	PAL–16L8	0.2904	1.6314
1	54ALS04	0.0237	0.0519
2	SRAM–HM6264	1.6259	23.6086
2	EEPROM–X2864A	1.0582	9.4955
2	Transceiver–’245	0.0802	0.3000
3†	Buffer–’244	0.1604	0.6000
1	Jumper	0.0000	0.0000
2	Resistor pack	0.0807	0.7631
1†	Multiplexer latch	0.0564	0.1267
7†	Octal D-register	0.2807	1.0500
2	96-pin connector	0.0646	0.2908
†	>60 extra pins used		
	Failure-rate totals:	3.7105	37.8677

† Differences from the baseline memory board

The ad hoc testability simplifies the isolation of a detected fault. Table 5 identifies a specific test sequence that will result in the minimum ambiguity groupings.

The first test should be to write a base address to the ID latch through the added multiplexer. This allows the tester to test all memory boards identically, regardless of the jumpered address. Next, all buses should be written to and read back by the ’373 latches. This intermediate test allows faults on the connectors, buffers, and transceiver to be isolated. The next test should ensure that the decode function selects the correct memory and addresses. Finally, the memory is tested.

By partitioning the test as shown in Table 5, the fault can be isolated by a divide-and-conquer approach. The benefits are fewer patterns, faster test time, and a higher confidence of isolating a fault. The cost is seven added parts and the related design penalties.

Table 5. Ad Hoc Memory-Board Test Flow and Fault-Isolation Ambiguity Groupings

AD HOC TEST FLOW	AMBIGUITY GROUPINGS
ID overwrite	1 — Latched multiplexer
Pattern data	4 — Connector, buffer, latch, pullup
Pattern address	4 — Connector, latch, transceiver, pullup
Pattern control	4 — Connector, buffer, latch, pullup
Pattern decode	2 — Comparator, PAL
SRAM tests	3 — SRAMs, NANDs
EEPROM tests	3 — EEPROMs, NANDs

1149.1-Compliant Memory Board

In this case, scannable buffers and transceivers replaced the original buffers and transceiver (see Figure 3 and Table 6). One additional part provides observability and controllability on the memory side of the decode block. Then, the SCOPE octal parts were connected into a single scan path.

Table 6. 1149.1-Compliant Memory-Board Parts List With Failure Rates

QUANTITY	PART	FAILURE RATE AT 0°C	FAILURE RATE AT 60°C
1	54LS85	0.0294	0.0997
1	PAL–16L8	0.2904	1.6314
1	54ALS04	0.0237	0.0519
2	SRAM–HM6264	1.6259	23.6086
2	EEPROM–X2864A	1.0582	9.4955
2†	Test transceiver–’BCT8245A	0.1126	0.2762
5†	Test buffer–’BCT8244A	0.2815	1.3810
1	Jumper	0.0000	0.0000
2	Resistor pack	0.0807	0.7631
2	96-pin connector	0.0646	0.2908
†	Four extra pins used		
	Failure-rate totals:	3.5670	37.8744

† Differences from the baseline memory board

The 1149.1-compliant board is more inherently testable than the ad hoc board since the boundary scan allows the insertion and overwrite of signals on the device output pins. The ID jumpers can be reconfigured without using a discrete multiplexer. The scan path allows patterns to be read back between the buffer and the connector. This removes the connector from the ambiguity group. By inserting the patterns through the scan path and following the same test sequence as the ad hoc board, the isolation percentages are improved. No ambiguity group has more than two components (see Table 7).

Table 7. 1149.1-Compliant Memory-Board Test Flow and Fault-Isolation Ambiguity Groupings

1149.1 TEST FLOW	AMBIGUITY GROUPINGS
Scan path	1 — Each test part
ID overwrite	1 — ID register
Pattern connector	1 — Connector
Pattern data	2 — Test buffer pullup
Pattern address	2 — Test transceiver, pullup
Pattern control	2 — Test buffer, pullup
Pattern decode	2 — Comparator, PAL
SRAM tests	3 — SRAMs, NANDs
EEPROM tests	3 — EEPROMs, NANDs

An additional advantage of the scan-path method is that the memories do not have to be tested last in the sequence. The generated patterns and control of the memory can be done via the scan path directly, without having to use the decode logic. This allows isolation without the restriction of a specific test sequence. The test sequence can be redesigned to a failure-rate priority that would have a probability of finding a fault earlier in the test sequence.

The overall advantages of using the SCOPE octal parts versus an ad hoc solution is a reduction in board space and the ability to modify the test sequence.

Analysis of Results

The failure-rate analysis was conducted in accordance with MIL-HDBK-217E.[2] Each of the three boards described above was analyzed using a ground mobile model at 0°C ambient (with an equivalent junction temperature of 50°C) and at 60°C ambient (with an equivalent junction temperature of 110°C). The devices were modeled as full MIL-qualified parts. To keep the comparison similar, all the added parts involved were bipolar complementary metal-oxide semiconductor (BiCMOS) process.

The overall reliability comparison figures for the three boards are shown in Table 8.

Table 8. Reliability Comparisons

RELIABILITY COMPARISON	BASELINE BOARD	AD HOC BOARD	1149.1 BOARD
Failure rate			
at 0.0°C	3.4135	3.7105	3.5670
at 60.0°C	36.8410	37.8677	37.8744
Mission failure (FM) f/mh	20.1273	20.7891	20.7207
MTBF hours	49,700	48,100	48,300

The percentage of test circuitry added to the baseline board is shown in Table 9.

Table 9. Percentage Added Because of Testability Circuit

IMPACT OF TESTABILITY	AD HOC BOARD (%)	1149.1 BOARD (%)
Part count	41.17	5.88
Failure rate		
at 0.0°C	8.70	4.45
at 60.0°C	2.79	2.80

Conclusion

The memory-board examples analyzed above are a single, small test case. Therefore, the testability modifications have a greater impact on reliability than when used on more realistic designs.

As shown in Table 8, the ad hoc solution has a higher failure rate at low temperature where the predominant failure mode is the interconnect. The 1149.1 solution has a slightly higher failure rate at the high temperature where the predominant failure mode is the silicon process. These results are expected since the ad hoc solution adds parts to the board and the 1149.1 solution adds gates to the parts.

From a reliability point of view, the ad hoc and 1149.1 solutions have similar impacts on board failure rate (see Table 9). For this example, 1149.1 has an improved overall numerical impact. In terms of percentage of failure rate added to the board, the 1149.1 actually has the least maximum impact with 4.45 percent additional failure rate versus the ad hoc maximum of 8.70 percent.

The 1149.1-compliant board surpassed the isolation requirement of four components with no ambiguity group larger than two (see Table 7), whereas the ad hoc board just met the requirement (see Table 5).

If the ad hoc board were implemented with all of the testability functionality contained within the test octals, the part count would increase significantly. The ad hoc board failure rate would then surpass the 1149.1 solution significantly.

Another advantage the 1149.1 solution has over the ad hoc solution is the number of test points required. The 1149.1 requires only four connector pins to be added. In this case, the ad hoc solution required more than 60 test points at the connector.

The 1149.1 solutions, as compared to ad hoc testability solutions, offer the following advantages:

- Improved observability and controllability
- Improved fault detection and isolation
- Improved reliability
- Fewer test points
- Reduced part count
- Reduced pattern sets
- More flexible test-flow structure
- Lower power consumption
- Better thermal profile

Acknowledgment

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References

1 IEEE Std 1149.1–1990, *IEEE Standard Test Access Port and Boundary-Scan Architecture.*

2 MIL-HDBK-217E. *Reliability Prediction for Electronic Equipment.*