Hardware-Based Extensions to the JTAG Architecture

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IEEE 1149.1 Overview

The 1149.1 IEEE standard provides an IC-level test framework consisting of a four-wire Test Access Port (TAP) controller and related scan path architecture, as shown in Figure 1. The TAP controller receives external control input via Test Clock (TCK) and Test Mode Select (TMS) signals, and outputs control signals to the internal scan paths.

The scan path architecture consists of a single serial instruction register and two or more serial data registers. The two required data registers are a boundary scan register and a scan bypass register bit. The instruction and data registers are connected in parallel between a serial Test Data Input (TDI) signal and serial Test Data Output (TDO) signal. The TDI input is connected directly to the serial inputs of the instruction and data registers. The TDO output is connected via multiplexer 1 to either the serial output of the instruction or data registers. The selection control for multiplexer 1 comes from the TAP controller. Since multiple data registers can be used, multiplexer 2 is required to route a selected data register's serial output into multiplexer 1 to drive the TDO output. The selection control for multiplexer 2 comes from the instruction register.

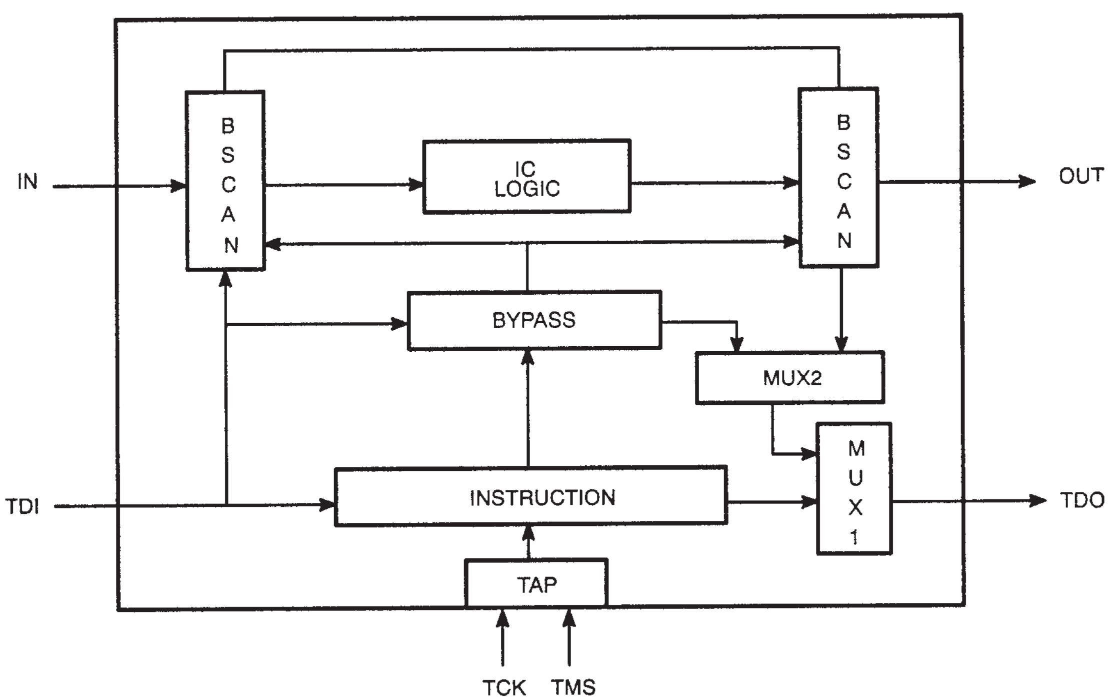

Figure 1. 1149.1 Architecture

When boundary testing is not being performed, the boundary scan register is transparent, allowing input and output signals to pass to and from the IC logic. However, during boundary testing, the boundary scan register disables the normal flow of input and output signals to allow the boundary signals of the IC to be controlled and observed via scan operations. The 1149.1 standard details how multiple ICs incorporating this scan architecture can operate together to perform external wiring interconnect tests between the boundaries of ICs in a circuit.

SCOPE Octal ICs

The SCOPE octals are a first in a series of standard components to be offered by TI that blend functionality with embedded board-level testing features [1,2]. The initial products include an octal register type 'BCT8374, latch type 'BCT8373, buffer type 'BCT8244, and transceiver type 'BCT8245. Along with the normal function pins associated with each part, four pins are added to support the 1149.1 test bus interface signals, TDI, TMS, TCK, and TDO. These devices can be substituted for their nontesting counterparts in a variety of board-level design applications such as: pipeline registers, board I/O buffers, address and data buffers/transceivers, and finite state machine designs.

An architectural illustration of the 'BCT8374 octal register type is shown in Figure 2. The functional architecture of the 'BCT8374 octal consists of an 8-bit register (REG), eight data inputs (IN), eight data outputs (OUT), a clock input (CK), and a tristate output control input (OC). The 1149.1 architecture consists of a Test Access Port (TAP) controller, an instruction register (IREG), and a data register section. The data register section consists of a bypass register, a boundary control register (BCR), and a boundary scan register. The boundary scan register consists of SCOPE Test Cells 1 and 2 (TC1, TC2) coupled to the CK and OC inputs, SCOPE Test Cell Register 1 (TCR1) coupled to the IN inputs, and SCOPE Test Cell Register 2 (TCR2) coupled to the OUT outputs. The other SCOPE octals have a similar 1149.1 test architecture placed around buffer, transceiver, and latch functions.

The TAP controller receives external input from the TMS and TCK signals, and outputs internal control to either the IREG or a selected data register to cause a shift operation to occur from the TDI input to the TDO output. The IREG is used to store a test instruction to be executed by the IC. The bypass register is used to shorten the scan path length through the IC to a single bit during data register operations. The BCR is used to store boundary configuration control bits to extend the test capabilities of the boundary scan register. The boundary scan register provides the mandatory test features required for 1149.1 compatibility as well as extended test features developed for SCOPE products.

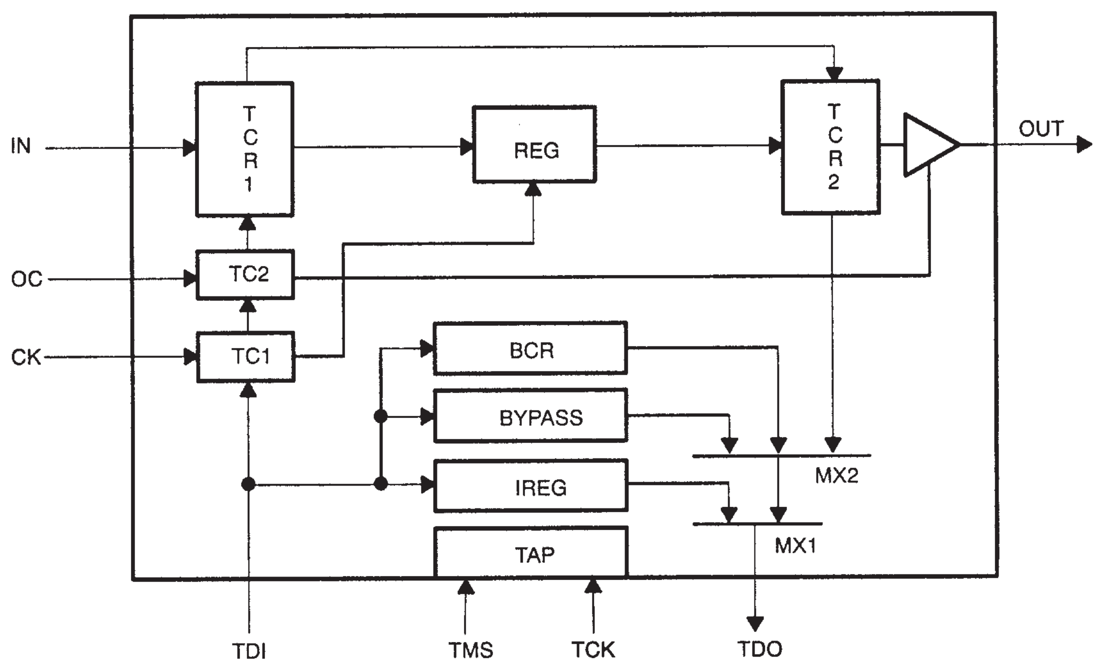

Figure 2. Scope Octal Register

Normal Mode Operation

During normal operation, the boundary scan register is transparent, allowing input and output signals to pass freely through the test cells, enabling the device to perform its intended function. While in normal operation, the TAP can receive control from the TMS and TCK inputs to shift data through the device from the TDI input to the TDO output. Three test instructions can be executed while the device is in normal mode: 1149.1 SAMPLE and BYPASS instructions and a SCOPE cell self-test instruction. The SAMPLE instruction allows the data flowing through the boundary to be sampled, then shifted out for inspection. The BYPASS instruction selects the bypass register to be shifted during data register scan operations, reducing the scan path length through the device to 1 bit. The self-test instruction executes a self check of each SCOPE cell in the boundary scan register. While the SAMPLE instruction at first may appear very attractive, the user of these and other 1149.1-compatible devices must know when to sample in order to obtain meaningful data.

Test Mode Operation

When placed in an off-line test mode, the normal operation of the SCOPE octal is inhibited. In test mode, instructions can be input to the device to perform all mandatory 1149.1 instructions as well as an extended set of test instructions designed for SCOPE products. The test-mode instructions incorporated into all SCOPE octals are described below. Prior to loading these test-mode instructions, the boundary scan path should be set so that a desired first test control pattern is applied to the REG inputs, tristate buffers, and device outputs (OUT). This procedure ensures that the device will be in a known state when the test mode is entered.

When an 1149.1 external or internal boundary test (EXTEST or INTEST) instruction is input to the device, the boundary register (TC1, TC2, TCR1, TCR2) is set to allow simultaneous observation of signals input to the test cells and control of signals output from the test cells. Simultaneous control and observation is achieved by the design of the test cells used to construct the boundary register. Each test cell contains two memories (flip-flops), one to observe input data and the other to control output data.

During 1149.1 EXTEST or INTEST, the TAP receives external input to cause the boundary register to capture data on the CK, OC, and IN inputs as well as on the internal REG outputs. The input memories maintain a desired control output logic state to internal as well as external logic inputs. For example, TC1 maintains a desired control input to the OUT tristate buffers, while also capturing data input on the OC pin. After the data is captured, the TAP receives additional input to shift the stored data out via the TDO outputs. While captured data is shifted out, the next test control pattern to be output from the boundary register is shifted in via the TDI input. The boundary register outputs remain in their present state during the shift operation. At the end of the shift operation, the TAP receives further input to cause the next test control pattern to be output from the boundary register. This process of capturing input data, shifting the boundary register to extract stored data and to load new test control data, followed by the application of the new test control data from the boundary register outputs, is repeated as required to perform a particular EXTEST or INTEST operation.

Test Extensions

To support extended testing capabilities, additional instructions, control logic and test pins are defined in the SCOPE architecture. Some of the SCOPE test extensions are included in the octal devices. The benefits of developing an extended test architecture is that all TI parts will share a consistent test instruction set, compatible testing modes, and reduced complexity in the development of test and maintenance software tools. The following paragraphs describe some of the SCOPE instructions that are included in the octal devices.

TRIBYP Instruction

When a SCOPE TRISTATE outputs and BYPASS (TRIBYP) instruction is input to the device, the outputs are placed in a high-impedance state and the bypass register is selected. This instruction is designed primarily to facilitate a blend of in-circuit and boundary scan testing. By disabling the outputs of the device, an in-circuit tester can drive the inputs of another device coupled to the outputs of the octals without damaging the octal's output buffers. While this instruction is in effect, the bypass register is selected to provide a minimum data register scan length through the device.

SETBYP Instruction

When a SCOPE SET outputs and BYPASS (SETBYP) instruction is input to the device, the boundary outputs are set to a prescanned combination of logic 1's and 0's and the bypass register is selected. This instruction allows the boundary test cells to output a prescanned control pattern to the REG inputs, tristate buffers, and device outputs (OUT). The SETBYP instruction allows placing the octal device in a preferred static input and output state while testing of neighboring components is being performed. While this instruction is in effect, the bypass register is selected to provide a minimum data-register scan length through the device.

READB Instruction

When a SCOPE Read Boundary (READB) instruction is input to the device, the contents of the boundary register can be shifted out. This instruction differs from the 1149.1 EXTEST or SAMPLE instruction in that the capture operation that normally occurs in the TAP's data-register capture state is replaced with a data-register hold operation. The data-register hold operation causes the boundary register test cells to capture their present state instead of the data values input to the test cells. This instruction is primarily used to allow a signature that has been collected in the boundary register to be shifted out for inspection.

RUNT Instruction

To support a boundary Built-In Self-Test (BIST) approach, a Run Test (RUNT) instruction was developed for SCOPE devices. RUNT is a generic instruction that executes the boundary BIST operation setup by control bits programmed in the BCR, shown in Figure 2. The BCR control-bit settings must be set up via a scan operation prior to loading the RUNT instruction. All RUNT programmations execute while the TAP controller is in the Run Test/Idle state. The length of a particular RUNT test operation is controlled by the number of TCK inputs applied while the TAP is in the Run Test/Idle state.

The four programmations of the RUNT instruction implemented in the octals include: 16-bit Parallel Signature Analysis (PSA) of the IN inputs, 16-bit Pseudo-Random Pattern Generation (PRPG) from the OUT outputs, simultaneous PSA of IN inputs and PRPG of OUT outputs, and simultaneous SAMPLE of IN inputs and TOGGLE of OUT outputs.

During the 16-bit PSA RUNT programmation, the 8-bit TCR1 and TCR2 boundary sections are linked together to form a single 16-bit Linear Feedback Shift Register (LFSR). The parallel inputs to TCR1 are enabled to accept data from the IN bus and the parallel inputs to TCR2 are disabled. In this configuration TCR2 acts as an 8-bit LFSR extension to TCR1. During test, the parallel inputs from the IN bus are compressed into the 16-bit LFSR on the rising edge of TCK. Linking TCR1 to TCR2 allows the SCOPE octal to receive an extended sequence of 8-bit patterns from the IN bus. At the end of the PSA operation, the 16-bit signature can be shifted out of TCR1 and TCR2 for inspection. While TCR1 and TCR2 are collecting the signature, the outputs of TC1 and TC2 remain in their present state. TC2 can be set to enable or disable the OUT buffers during the test.

During the 16-bit PRPG RUNT programmation, the 8-bit TCR1 and TCR2 boundary sections are linked together to form a 16-bit LFSR as described in the 16-bit PSA test. During the 16-bit PRPG test operation, both parallel inputs to TCR1 and TCR2 are disabled so that both act only as LFSRs. During test, the parallel output from TCR2 drives pseudorandom patterns to the OUT bus on each falling edge of TCK. By linking TCR1 and TCR2 together, an extended set of pseudorandom pattern sequences is produced. Since the width of the OUT bus is 8 bits, individual patterns will be repeated during every 256 pattern output sequence. However, the test circuit will produce 256 sets of unique 256 pattern output sequences. During this test, TC2 must be set to enable the OUT buffers.

During the simultaneous PSA and PRPG RUNT programmation, TCR1 and TCR2 operate as two separate 8-bit LFSRs. The parallel inputs to TCR1 are enabled to accept data from the IN bus and the parallel inputs to TCR2 are disabled. During test, TCR2 outputs pseudorandom patterns to the OUT bus on the falling edge of TCK, and TCR1 compresses input data from the IN bus on the rising edge of TCK. Combinational logic residing in the external path between the OUT and IN buses can be quickly tested using the RUNT instruction. During this test, TC2 must be set to enable the OUT buffers.

During the simultaneous Sample Inputs/Toggle Outputs RUNT programmation, TCR2 outputs alternating data patterns to the OUT bus on the falling edge of TCK, and TCR1 accepts data input from the IN bus on the rising edge of TCK. By adjusting the frequency of TCK, this test can be used to measure propagation delays through external logic residing between the OUT and IN buses. During this test, TC2 must be set to enable the OUT buffers.

SCOPE Octal Applications

A typical statement from a design engineer/manager may be "These parts are interesting, but they are more expensive than ordinary registers and buffers. Where is the payback?" As with any new product, the historical data required to substantiate any cost savings claims is not available, and even if it were, it would be based on a specific benchmark example application, not in general. Functionally, these parts offer no advantages over existing parts. However, if an interest exists in reducing the cost associated with product manufacturing and test, these parts deserve a second look. The following example illustrates how the octals can be used to improve test and diagnostics in a production environment.

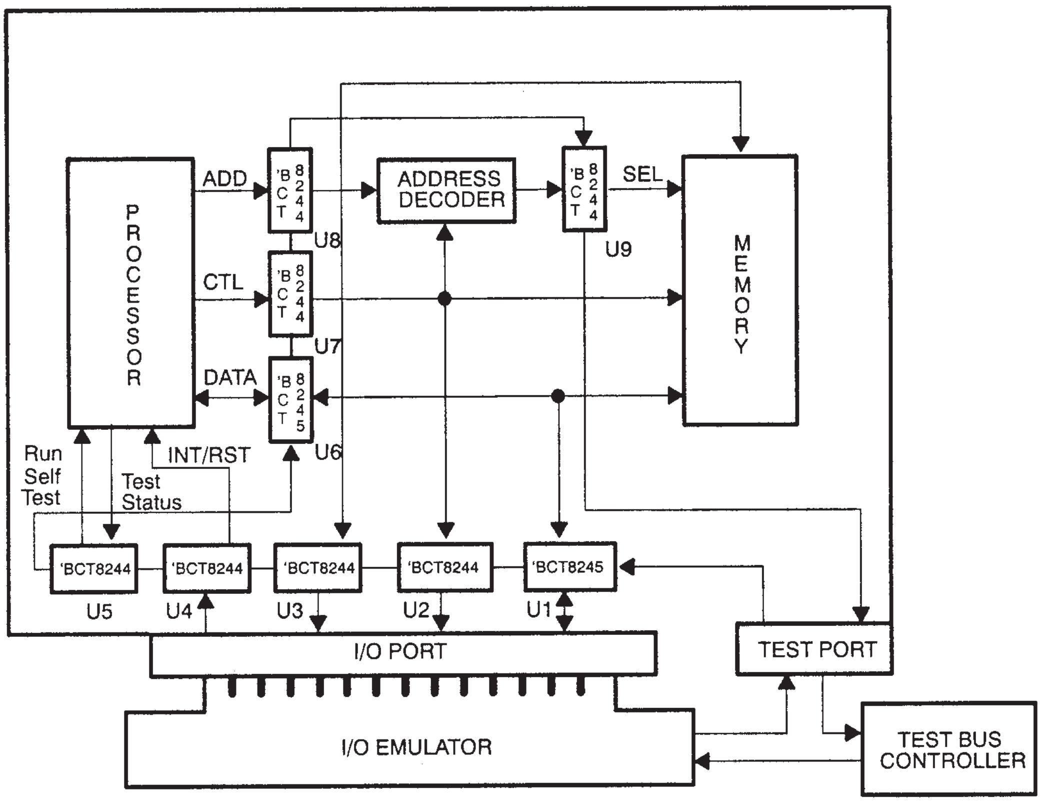

Figure 3. Microprocessor Board Design

A typical microprocessor board design is shown in Figure 3. The design includes a processor, address decoder, memory, buffering logic, and an input/output port. The processor has address, control, data, and interrupt buses that are routed to onboard memory and off-board peripherals via the I/O port. The address decoder consists of combinational logic and decoders. The memory consists of ROM and RAM. The buffering logic consists of SCOPE octal 'BCT8244 buffers and 'BCT8245 transceivers. These octals are placed on the busing paths to provide functional buffering and embedded testing features between the major circuits in the design, as well as external I/O circuitry.

Proper steps have been taken in the design to ensure the board can be manufactured in a cost-effective manner. While several processors meet the functional requirements established for the design, one has been selected that includes an embedded BIST capability that can be initiated at power up or by a Run-Self-Test pin to verify the processor's internal logic. The processor includes a Test Status output pin that outputs a particular sequence to indicate whether the internal BIST operation passed or failed. Test pins Run-Self-Test and Test Status are coupled to an extra octal (U5) to allow the processor BIST to be initiated and the results to be monitored via scan. If the processor BIST fails, no further testing occurs until the failure is diagnosed and repaired.

In addition to the processor's internal BIST, memory locations in the onboard ROM are allocated to support an overall board-level BIST routine. If the processor passes the internal BIST test, it will proceed to the next test step of executing the board-level BIST routine. This ROM-resident board-level BIST is designed to cause the processor to execute an effective pattern test of the onboard RAM, a Cyclic Redundancy Check (CRC) of the contents of the onboard ROM, and I/O operations to external circuits attached to the I/O port. Since this test follows the processor BIST, it is executed at power up and can also be retriggered by invoking the processor BIST using the Run-Self-Test input pin.

If the board-level BIST passes, the board is considered good and requires no further internal functional testing. A pass or fail condition is recognized by reading a BIST status code written into a particular address location of the external I/O emulation circuitry. The I/O emulation circuitry is inserted into the I/O port connector to allow the processor to exercise off-board memory accesses. The I/O emulator includes an 1149.1 test bus to allow scan access of the board-level BIST status code. Also, the scan path allows verification of the electrical interconnection between the board and emulator connectors.

The design contains all the right BIST features to ensure that the most sophisticated logic components on the board are tested. However, a majority of the manufacturing faults do not involve the internals of the processor or memories. The assembly process that installs the ICs onto the printed circuit board is where most of the manufacturing problems will appear in the form of solder shorts, cold solder joints, bent/broken pins, shorted/open board traces, insertion of the wrong logic component, etc.

Some of the payback in using the octals in place of their nontesting counterparts is that they provide a method to diagnose assembly-related problems without having to resort to test equipment and fixturing. Since the octals include the 1149.1 test bus, scan access to the parts can be achieved using a cost-effective PC-based test bus controller cabled into the board via the test port connector. In addition, this scan-based diagnostic approach applies equally well to field service applications, producing still further cost savings over the life cycle of the board.

Scan-Based Test and Diagnostics

As mentioned, the design includes two levels of BIST — a processor self check and a board-level self check. If both BIST operations are successful, the board is good and requires no further testing. However, if one of the BIST approaches fail, the 1149.1 test bus controller can scan the octals into their test mode and perform diagnostic tests to identify the problem that caused the BIST to fail. The following is an example design that illustrates how the octals can be used to test for failures at the board level.

Diagnosing Processor BIST Failures

Since the processor's BIST verifies its internal circuitry, a failure output sequence on the Test Status pin indicates this failure. Upon receiving this failure sequence, the processor should be replaced. However, if the processor's BIST fails to output the correct pass or fail sequence, the problem may not be in the processor. In this case, further investigation is required to see if the BIST is being affected by external conditions.

As shown in Figure 3, octal U4 inputs reset and interrupt signals to the processor from the off-board I/O emulator. If one or more of these signals is faulty, the operation of the processor's BIST could be affected. To determine if this is occurring, all the octals are placed in test mode via an EXTEST instruction. During EXTEST the octals output a preloaded test pattern in place of normal system signals, effectively partitioning the system buses. The data bus outputs of octal U6 are tristated to avoid bus contention with the processor. The interrupt and reset outputs of octal U4 are set to a disabled logic state so they do not interfere with the processor's BIST operation. After this setup procedure, the processor's BIST is retriggered using the Run-Self-Test output from octal U5. If the test passes, it appears that the problem lies in the interrupt and reset inputs from the I/O emulator circuit; if not, a more detailed diagnostic test approach is required. Assuming the BIST passes, the cause of the failure can be determined by reading the inputs from the I/O port on octal U4, via scan. The inputs read can be compared to the expected values to determine the failing signal or signals.

Diagnosing Board-Level BIST Failures

The board-level BIST is relied upon to fully test each function in the design. During the board-level BIST, the octals must be in the normal mode to allow data, address, and control buses to operate normally. If the BIST is not totally disabled by a major fault, it can reliably diagnose and report test problems such as failing RAM locations, ROM CRC or I/O access failures. However, if a major fault exists, such as a short or open condition on the address, data, or control bus, the processor will be unable to access the BIST code in ROM and the test will be disabled. In the event the board-level BIST is disabled, the following series of diagnostic tests can be executed by the octals.

Testing for Shorts and Opens Between Octals

If the board-level BIST is disabled, the octals can be configured to test for board trace shorts and opens. To initiate the test, the octals are loaded with the EXTEST instruction. The EXTEST instruction places the octals in test mode and allows the external test bus controller to input control to capture data appearing on the octal inputs and to control data from the octal outputs. During this test, the octals not involved with shorts and opens testing should output a safe static pattern to the logic they drive. In the case of U5, the reset output should be set to force the processor into a reset state during test.

Using this approach, wiring interconnects between the octals can be tested for shorts and opens. Octals U8 and U3 test the address bus for shorts and opens. Octals U7 and U2 test the control bus for shorts and opens. Octals U6 and U1 test the data bus for shorts and opens. While the onboard buses are being tested, a shorts and open test can also be performed between the I/O port and the emulator circuit, using octals U1, U2, U3, and U4. If any faults are detected using this approach, they should be corrected and the board-level BIST repeated to determine if the detected faults were the ones disabling the BIST operation. If no faults are detected with this test, the octals can be configured to test for other faults.

Testing for Opens Between Octals and Memory/Address Decoder

The interconnect tests between the octals only verify that the board traces between the octals are intact and that no shorts exists. However, an open trace condition could still exist between the octals and address decoder and/or memory. To test the integrity of the interconnections to the address decoder and memory, the octals can be set up to emulate processor write and read operations. During this test, octals U8, U7, and U6 are loaded with the EXTEST instruction, octals U1, U2, U3, U4, and U5 are loaded with the SETBYP instruction, and octal U9 remains in the normal mode by loading a BYPASS instruction. Octal U9 remains in the normal mode to allow transferring the select outputs from the address decoder to the memory. During this test, all octals containing SETBYP instruction output a safe static pattern to the logic they drive.

By placing octals U8, U7, and U6 in the EXTEST boundary scan mode, the address, control and data buses can be operated by the external test bus controller to perform write and read memory accesses. If data can be transferred to and from all the memory address locations, no open trace or other failure conditions exist between the memory/address decoder and octals. However, if all or some of the data cannot be transferred to and from memory, two failure possibilities exist. The first possibility is that the address decoder is faulty. The second possibility is that an open trace may exist on the address decoder's select outputs.

To test for the second possibility, octal U9 is loaded with the EXTEST instruction to allow the select outputs to be controlled by the test pattern scanned into octal U9. This eliminates the address decoder from the test. By repeating the memory write/read test with U9 outputting the memory select signals in place of the address decoder, it is possible to determine if an open trace exists in the select signals. If the memory access test passes, the busing paths between the octals and memory are intact and the problem lies in the address decoder. If the memory access test fails, one or more open traces exist between the octals and memory. In the event the test fails, intelligent test patterns can be used to help diagnose where the open trace conditions exist.

Boundary Testing the Address Decoder

After verifying that opens do not exist on the data, control, select, or address buses, the address decoder needs to be thoroughly tested. To verify the logic inside the address decoder, octals U9, U8, and U7 are loaded with the EXTEST instruction. The other octals are loaded with the SETBYP instruction to allow them to output a safe static pattern while the address decoder is tested. During EXTEST, the external test bus controller inputs control to allow octals U8 and U7 to drive the inputs of the address decoder, and octal U9 to read the response outputs from the address decoder. The responses read by octal U9 are compared to expected values to see if the decoder is operating properly. If proper operation is determined, a timing-related problem could still exist and cause the address decoder to fail during BIST testing. The RUNT instruction is used to test for timing-related failures.

At-Speed Testing the Address Decoder

At-speed testing of the address decoder can be achieved by two of the RUNT programmations offered in the octals — the PSA/PRPG or the Toggle/Sample. During either of these RUNT tests, octals U7, U6, U5, U4, U3, U2, and U1 should contain the SETBYP instruction to allow their outputs to remain set at a safe static value. Also, the outputs of U9 should be set tristate during these tests to guard against the memory receiving multiple select inputs. Pull-up resistors placed on the outputs of U9 disable the select signals while they are tristate.

If the PSA/PRPG RUNT programmation is used, octal U8 outputs a pseudorandom pattern to the inputs of the address decoder on the falling edge of TCK, and octal U9 compresses the data from the address decoder into a signature on the rising edge of TCK. The TCK frequency determines the speed at which the test operates. After a predetermined number of TCKs, the signature collected in U9 is scanned out and compared to an expected signature. If the signature collected matches the expected value, the test passed; otherwise, the address decoder has a timing-related failure. If a failing signature is obtained, the Toggle/Sample RUNT programmation can be used to further diagnose the timing problem.

The Toggle/Sample RUNT programmation is primarily used for propagation delay testing. If the PSA/PRPG programmation is changed to the Toggle/Sample programmation, octal U8 outputs a toggling pattern to the inputs of the address decoder on the falling edge of TCK, and octal U9 samples the data output from the address decoder on the rising edge of TCK. The TCK frequency determines the speed at which the test operates. After each Toggle/Sample operation, the sampled outputs are scanned out of U9 for inspection, the next address value to toggle is scanned into U8, and the test is repeated. The advantage of this test over the PSA/PRPG test is that it provides deterministic delay testing of the address decoder. In other words, instead of indicating a failing signature, this test identifies each output signal that fails to transfer through the address decoder between the falling and rising edge of TCK.

SCOPE Octal Application Summary

The described test approaches are made possible by substituting SCOPE octals in place of standard buffers and transceivers in a board design. The capability to provide the types of embedded scan-based tests described in this example can prove to be a cost-effective alternative to existing board design and manufacturing approaches. It is important to note that all the test features described are achieved by only having scannable octals in the board design. If the processor and memories were also scannable, the board could be tested even more thoroughly.

Conclusion

The 1149.1 standard provides the framework for a structured test approach. Devices described in this paper implement the boundary test functions required by the standard. In addition, the devices contain test extensions to improve their ability to test for timing-related faults that are not detectable using boundary scan techniques alone. Additional SCOPE products are being developed to provide additional test features to support board-level design for testability.

References

[1] *SCOPE Octal Data Sheets*, Local Texas Instruments Sales Office.

[2] A. Halliday, G. Young, and A. Crouch. *Prototype Testing Simplified by Scannable Buffers and Latches,*. Proceedings IEEE International Test Conference, 1989.