Application Note

How to Solve Power Failure During BQ500212A Power Up

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ABSTRACT

This application note discusses the root cause of random power failure during BQ500212A power up, and describes several designs to solve the issue.

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1 Introduction

BQ500212A is a Qi-certified value design that integrates all functions required to control wireless power delivery to a single WPC1.1 compliant receiver. BQ500212A is WPC1.1 compliant and designed for 5V systems as a wireless power consortium type A5 or A11 transmitter. The snooze pin and the sleep pin of BQ500212A allow wireless charger system to decrease power consumption when nothing is on the transmitter pad by pinging the surrounding environment at fixed intervals. Besides, the bq500212A IC is designed to operate from a well regulated 3.3V power supply. This can be a low switching power supply or linear regulator. The 3.3V supply is integrated into a total transmitter design that is powered from a 5V supply capable of supporting the output load of 5W plus conversion losses in the system.

2 Other Information

2.1 Root Cause of Power Failure

BQ500212 Typical Application Block Diagram is a block diagram of BQ500212A typical application. A 5V adapter is often used to supply the wireless charger system. Sleep and snooze signal can be used to control the LDO output to power down system for consumption optimization.

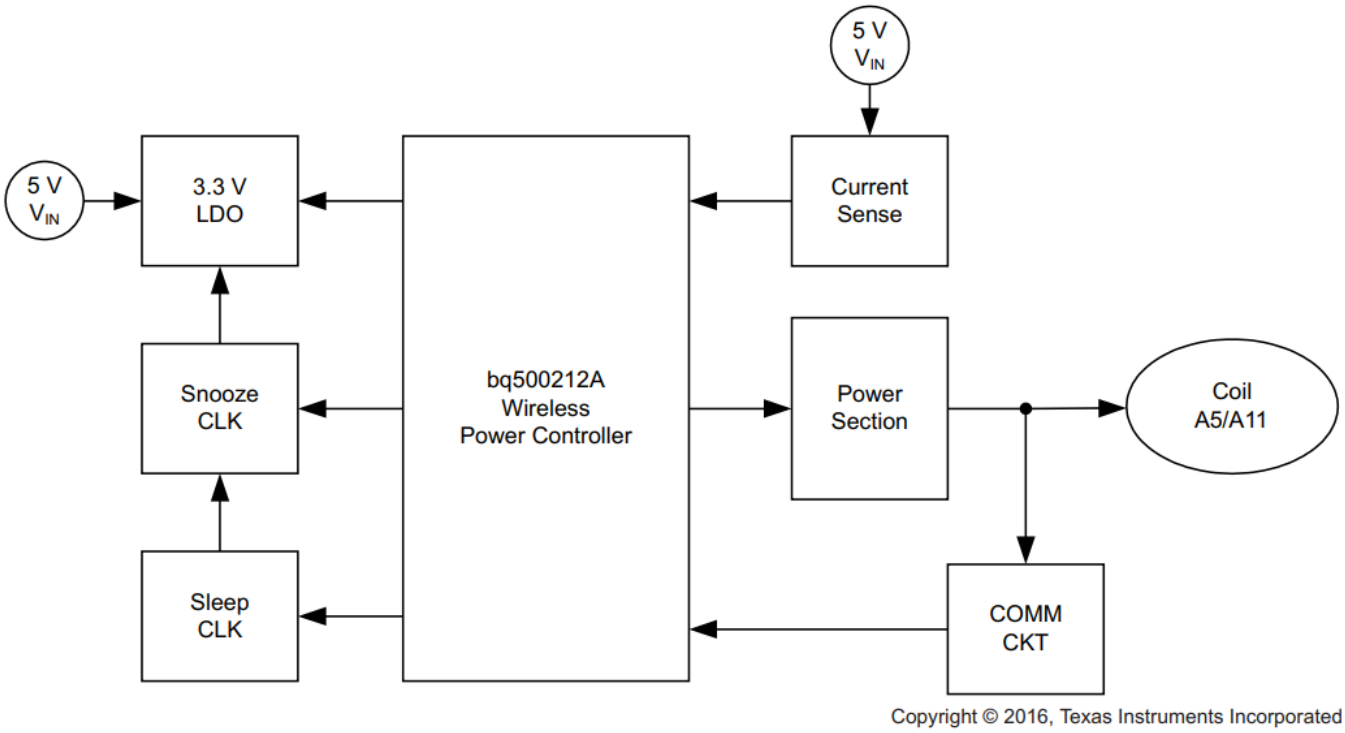

Figure 2-1. BQ500212 Typical Application Block Diagram

1. Typical Application Block Diagram Power Failure Issue

   In actual design, as shown in Figure 2-2, TI recommends connecting SLEEP and SNOOZE pin of the BQ500212A to the gate electrode of MOSFET and EN pin of LDO to drain electrode of MOSFET. When the sleep pin or the snooze pin give out intervals, MOSFET turns on and EN is pulled low to disable LDO and power down BQ500212A.

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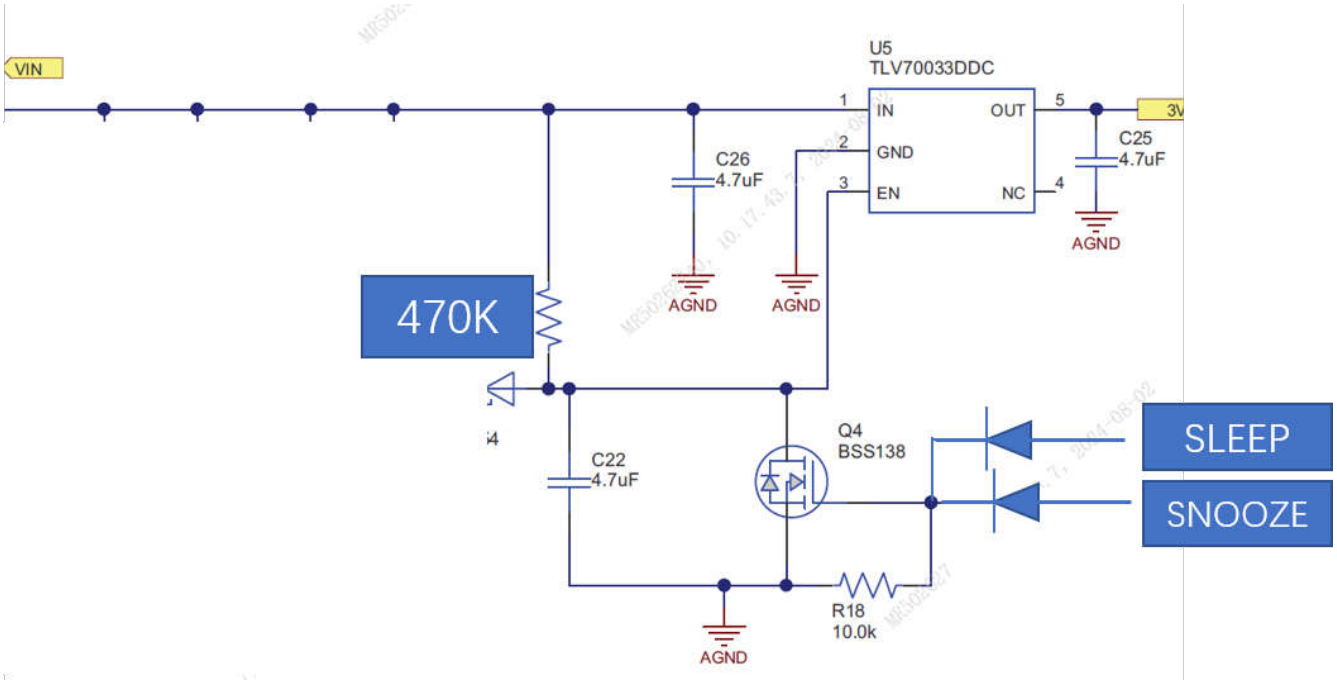

Figure 2-2. LDO Control Circuit

2. LDO Control Circuit

   In actual tests, as shown in Figure 3, during BQ500212A power up, sleep pin gives out glitches. These glitches reach to gate threshold and cause MOSFET turn on. Then LDO is disable, which lead to power failure of BQ500212A.

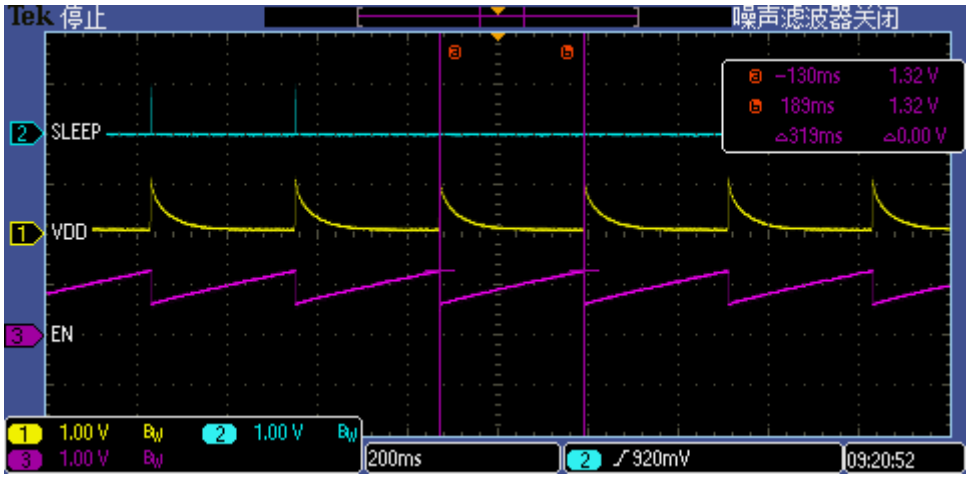

Figure 2-3. Test Waveform of Power Failure

3. Test Waveform of Power Failure Root Cause Analysis

   BQ500212A has an internal 1.8V core regulator, which supplies all IO pins of BQ500212A. BPCAP pin is the output of internal regulator, where requires to connect bypass capacitor to GND. The bypass capacitor will affect power up rate of 1.8V core supply. If the internal 1.8V power up unproperly, IO pins including sleep pin are affected by an external 3.3V power rail.

   By testing power rails during power failure, Figure 2-4 shows that the glitch that is given out by sleep pin matches power up period of external 3.3V. Figure 2-5 shows that if 1.8V core supply powers up faster, the sleep pin is not affected by the external 3.3V.

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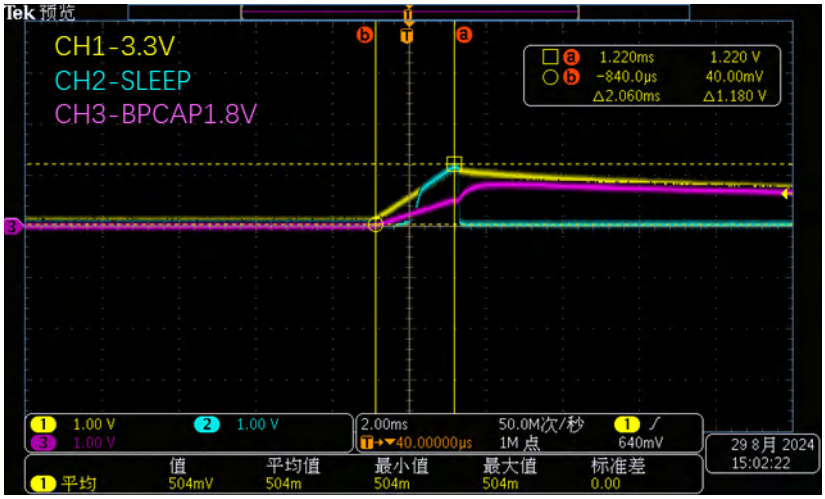

Figure 2-4. Problem Sleep Glitch Caused at Power Up

4. Sleep Glitch Caused by Unproper Power Up

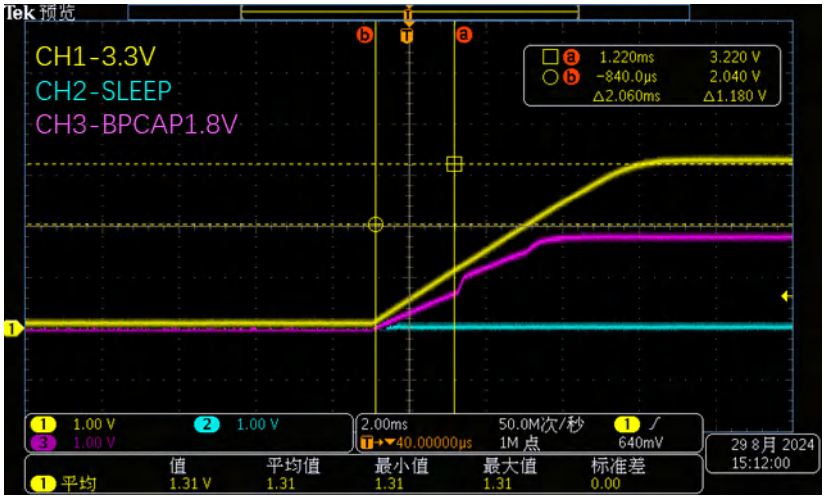

Figure 2-5. Proper Power Up

5. Proper Power Up

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2.2 Designs: Increase Power Up Rate of Internal 1.8V Core Supply

To increase the power up rate of internal 1.8V core supply, TI recommends selecting a larger bypass capacitor from 3.3V to BPCAP pin. Table 2-1 compares performance of 1uF and 2.2uF from 3.3V to BPCAP pin. When the power up rate increase to 0.34V/ms, power failure can be avoided.

1. Core Supply Power Rate

Table 2-1. Core Supply Power Rate

Bypass Capacitor from 3.3V to BPCAP pin	1uF	2.2uF
1.8V Power-Up Rate	0.24V/ms	0.34V/ms
Power failure	Yes	No

The BPCAP pin is the output from an internal 1.8V regulator, capacitor connected to BPCAP pin is a filter. The 1.8V regulator is powered by the 3.3V supply (pin 33). The 1.8V powers a digital core of the device while 3.3V powers the IO lines. If the IO lines power up before the core, the IO lines can generate unexpected pulse that interfere with startup.

To prevent this, TI recommends using a capacitive divider on BPCAP pin, as this boosts the 1.8V at startup. Capacitor between BPCAP pin and 3.3V, 1uF capacitor between BPCAP and Ground.

2.3 Workaround Methods: Add a Resistor at Gate of Resistor

In the current system, keeping the MOSFET turned off during power up can avoid an LDO disable. As a result, adding a resistor at the gate electrode of MOSFET can help to decrease the voltage applied on the gate when the the sleep pin output glitches.

2.4 Workaround Methods: Select a Higher Gate Threshold MOSFET

By analyzing the glitch on sleep pin, the width is approximately 1.2ms, and the amplitude is approximately 1.2V. As a result, selecting a higher gate threshold MOSFET can help MOSFET keep turn off to avoid power failure.

3 Summary

The power up glitch can cause startup problems under the right conditions. As shown in this application note, designs are available which eliminate the problem.

4 References

1. Texas Instruments, *bq500212A Low System Cost, Wireless Power Controller for WPC TX A5 or A11*, data sheet.

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5 Revision History

Changes from Revision * (October 2025) to Revision A (November 2025)	Page
• Updated author name	2

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