TEXAS INSTRUMENTS

Design Considerations for Logic Products

Application Book

Volume 2

September 1999

Logic Products

Texas Instruments

Printed in U.S.A.
0899–CP

SDYA018

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INTRODUCTION

This collection of application reports and articles provides the design engineer with a valuable technical reference for Texas Instruments (TI™) products. It contains reports written or revised between March 1997 and July 1999. This book is divided into seven sections, each focusing on different aspects of design decisions, and an appendix listing application reports published in the 1997 *Design Considerations for Logic Products* Application Book, literature number SDYA002.

Section 1, ***5-V Logic Design***, includes discussions on the ABT (Advanced BiCMOS Technology) and AHC (Advanced High-Speed CMOS) logic families. ABT and AHC devices are the recommended families for medium- to high-performance 5-V designs.

Section 2, ***3.3-V Logic Design***, focuses on the LVT (Low-Voltage BiCMOS Technology) logic family. The LVT family has performance specifications ideal for networking and telecommunication applications. This section includes application reports explaining the LVT-to-LVTH conversion. When using the new LVT or LVTH devices in existing applications, some customers may need to deal with timing of the marginally faster devices, or they may have used resistors at the input to the bus-hold circuitry that would need to be resized because of a change in the maximum bus-hold current.

Section 3, ***2.5-V Logic Design***, addresses the migration from 3.3-V to 2.5-V logic devices in current designs. Additionally, this section focuses on the use of the AVC (Advanced Very-Low-Voltage CMOS) logic family in next-generation, high-performance PCs, workstations, and servers.

Section 4, ***Device-Specific Design Aspects***, covers damping resistors, dynamic output control (DOC™), I^2C interface, and other device-specific characteristics and features not covered in the 1997 edition of *Design Considerations for Logic Products* application book.

Section 5, ***DIMM Applications***, explains logic buffering solutions for dual inline memory modules (DIMM) using ALVC (Advanced Low-Voltage CMOS) and SSTL (Stub Series-Terminated Logic) and memory interleaving using for the 440BX and other core-logic chipsets using CBT and CBTLV.

Section 6, ***Backplane Applications***, addresses basic aspects of designing a backplane system, focusing on the GTL+ switching standard and design with the TI SN74GTL1655.

Section 7, ***Packaging***, gives an overview of standard packages for logic products. From DIP to the advanced low-profile, fine-pitch ball grid array (LFBGA) package, this section covers shelf-life evaluation, steam-age evaluation, thermal characteristics, and other considerations when selecting a package for a design.

For more information on these or other TI Products, please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI logic home page at http://www.ti.com/sc/logic. Application reports published in the previous *Design Considerations for Logic Products* Application Book (see appendix A) also are available through links on the TI logic home page.

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ABT
Advanced BiCMOS Technology
Characterization Information

SCBA008B
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Appendixes

Introduction

The purpose of this document is to assist the designers of high-performance digital logic systems in using the advanced BiCMOS technology (ABT) logic family.

Detailed electrical characteristics of these bus-interface devices are provided and tables and graphs have been included to compare specific parameters of the ABT family with those of other logic families.

In addition, typical data is provided to give the hardware designer a better understanding of how the ABT devices operate under various conditions.

The major subject areas covered in the report are as follows:

- AC Performance
- Power Considerations
- Input Characteristics
- Output Characteristics
- Signal Integrity
- Advanced Packaging
- Characterization Information

The characterization information provided is typical data and is not intended to be used as minimum or maximum specifications, unless noted as such.

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AC Performance

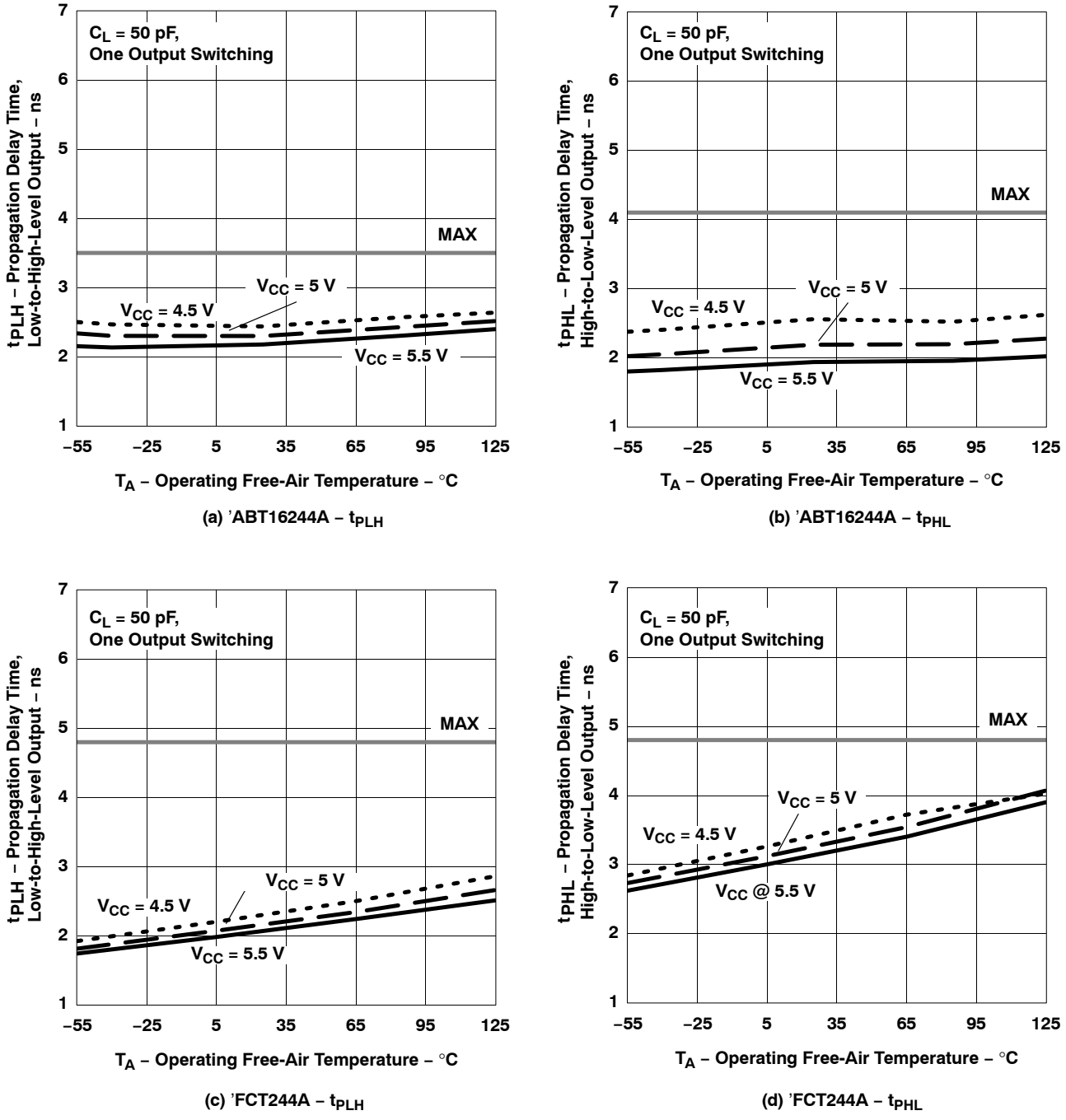
As microprocessor operating frequencies increase, the period of time allotted for operations, such as memory access or arithmetic functions, decreases. With this in mind, TI developed a family of bus-interface devices – ABT – utilizing advanced BiCMOS technology. The goal of the ABT family of devices is to give system designers one bus-interface solution that provides high drive capability, good signal integrity, and propagation delays short enough to appear transparent with respect to overall system performance.

Advances in IC process technology, including smaller minimum feature size, tighter metal pitch, and shallower junctions, combine to provide stronger drive strengths and smaller parasitic capacitances. As a result, internal propagation delays have become extremely short. With the advent of the 0.8-µm, EPIC-IIB™ BiCMOS process and new circuit innovations, the ABT family offers typical propagation delays as low as 2-3 ns as shown in Figure 1. Maximum specifications are as low as 3–5 ns, depending on the device type.

Figure 2 shows the propagation delay versus change in both temperature and supply voltage for an ’ABT16244A, ’FCT244A, and a ’F244 device. The graphs highlight two important aspects of the ABT logic family. First, ABT interface devices have extremely short propagation delay times. The figures clearly show the improvement in speed of an ABT device over that of a 74F and 74FCTA device. Second, the variance in speed with respect to both temperature and supply voltage is minimal for ABT. At low temperatures, the increase in CMOS performance compensates for the decrease in bipolar device strength. At high temperatures, the reverse occurs. This complementary performance of both CMOS and bipolar devices on a single chip results in a slope that is virtually flat across the entire temperature range of −55°C to 125°C.

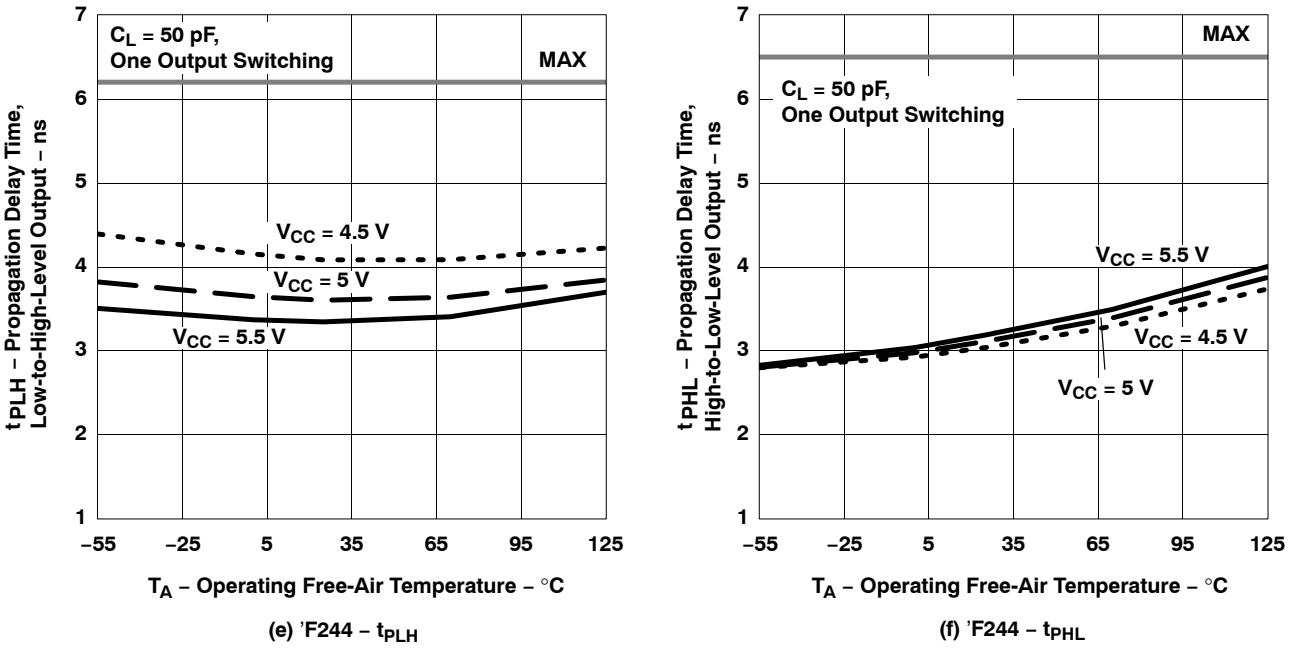
For most applications, the data sheet specifications may not provide all of the information a designer would like to see for a particular device. For instance, a designer might benefit from data such as propagation delay with multiple outputs switching or with various loads. This type of data is extremely difficult to test using automatic test equipment; therefore, it is provided in this document as family characteristics shown in Figure 2 and Figure 3.

To get a clear picture of where ABT stands in reference to other logic families, data is shown for a comparable (same function) 74F and 74FCTA device. It is clear that ABT is the designer's best choice for bus-interface applications that require consistent speed performance over various conditions.



NOTE: MAX is data sheet specification

Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y



NOTE: MAX is data sheet specification.

Figure 1. Propagation Delay vs Operating Free-Air Temperature A to Y (Continued)

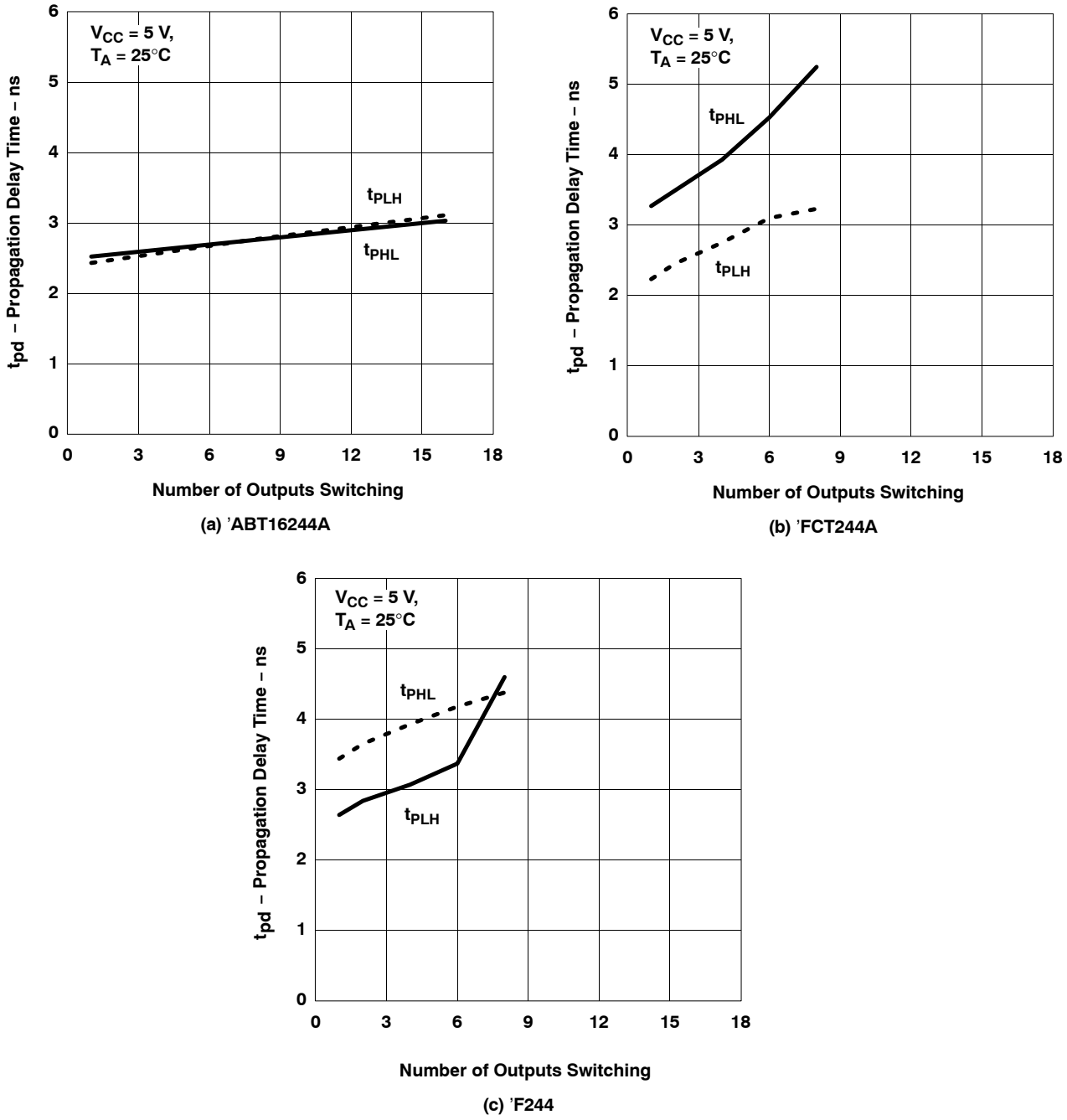
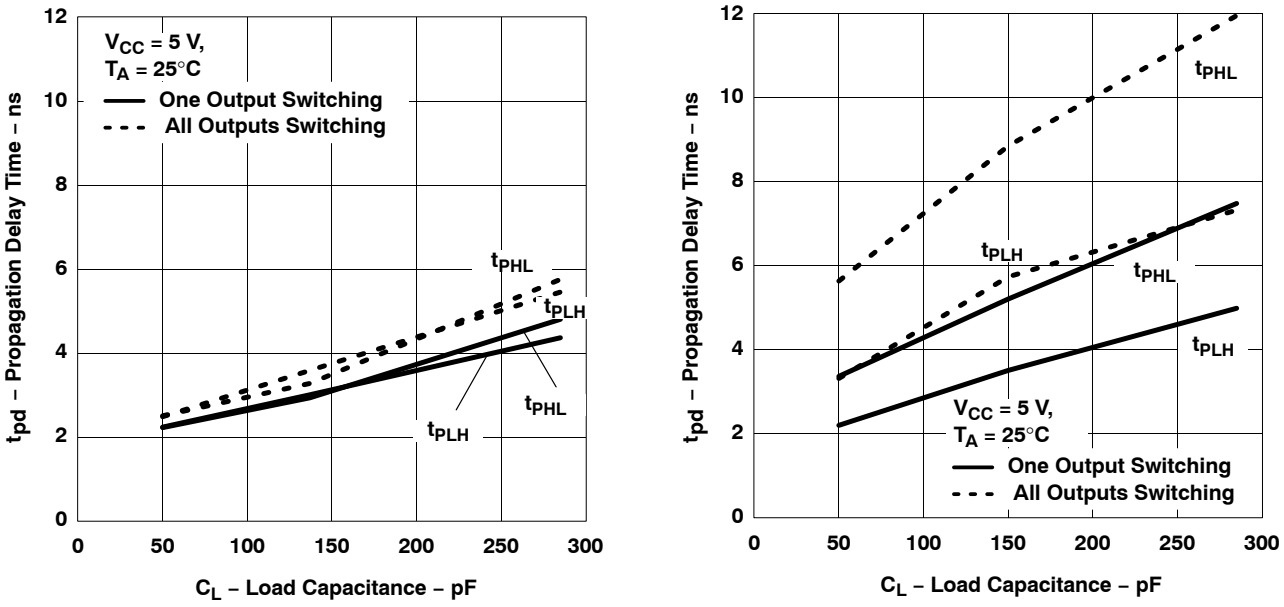
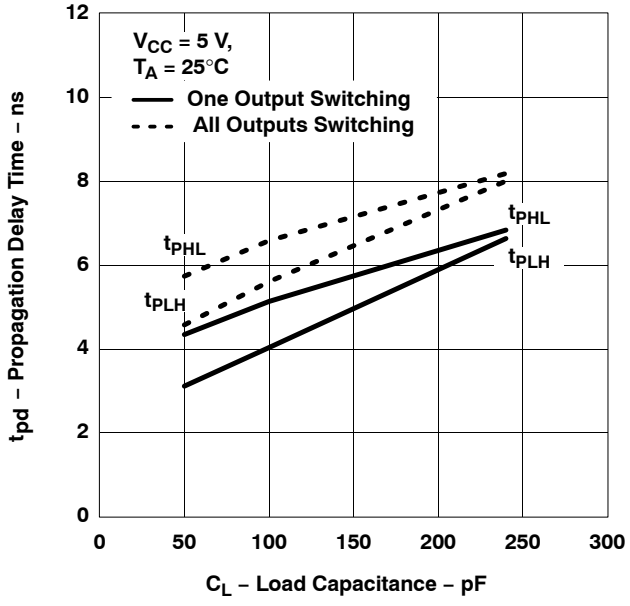


Figure 2. Propagation Delay Time vs Number of Outputs Switching



(a) 'ABT16244A

(b) 'FCT244A



(c) 'F244

Figure 3. Propagation Delay vs Capacitive Load

Power Considerations

With the challenge to make systems more dense while improving performance comes the need to replace power-hungry devices without compromising speed. The ABT family of drivers provides a solution with low CMOS power consumption and high-speed bipolar technology on a single device.

There are two basic things to consider when calculating power consumption, static (dc) power, and dynamic power. Static power is calculated using the value of I_{CC} as shown in the data sheet. This is a dc value with no load on the outputs. To understand the relationship between pure CMOS, pure bipolar, and advanced BiCMOS for dc power rating, see Table 1, which shows the various data sheet values. The bipolar device shows the highest I_{CC} values, with little relief, regardless of the state of the outputs. This is not the case with ABT octals, which offer the low static power consumption of CMOS while in the high-impedance state, or when the outputs are high (I_{CCZ}, I_{CCH}).

Table 1. Supply Current

PARAMETER	TEST CONDITIONS		'F244		'FCT244		SN74ABT244	
			MIN	MAX	MIN	MAX	MIN	MAX
I_{CC}	V_{CC} = 5.5 V, I_O = 0, V_I = V_{CC} or GND	Outputs high		60 mA				250 μA
		Outputs low		90 mA				30 mA
		Outputs disabled		90 mA				250 μA
	V_{CC} = maximum, V ≥ V_{CC} − 0.2 V, V ≤ V_{CC} − 0.2 V					1.5 mA		

Dynamic power involves the charging and discharging of internal capacitances, as well as the external load capacitance. It is this dynamic component that makes up the majority of the total power dissipation. Figure 4 shows power as a function of frequency for ABT, FCT, and F devices. Although bipolar devices tend to have extremely high static power, there is a point on the frequency curve, commonly referred to as the crossover point, where the CMOS device no longer consumes less power. With ABT devices, the power increase at higher frequencies is less than that of the pure CMOS FCT.

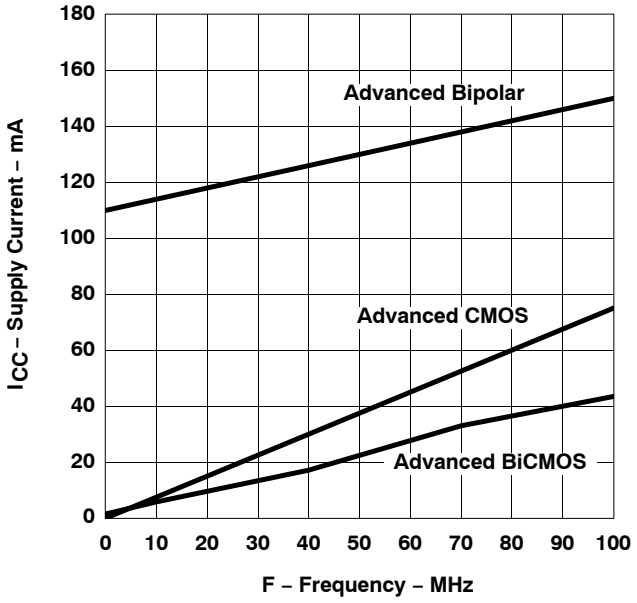


Figure 4. Supply Current vs Frequency

The use of bipolar transistors in the output stage is advantageous in two ways. First, the voltage swing is less than with a CMOS output, reducing the power consumed when charging or discharging the external load. Second, bipolar transistors are capable of turning off more efficiently than CMOS transistors, thus reducing the flow of current from V_{CC} to GND. Combined, these features allow for better power performance at high frequencies.

Input Characteristics

ABT bus-interface devices are designed to ensure TTL-compatible input levels switching between 0.8 V and 2 V (typically 1.5 V). Additionally, these inputs are implemented with CMOS circuitry, resulting in high impedance (low leakage) and low capacitance, which reduces overall bus loading. This section is an overview of the circuitry utilized for a typical ABT input, the corresponding electrical characteristics, and guidelines for proper termination of unused inputs.

ABT Input Circuitry

Figure 5 shows a typical ABT input schematic. A pure CMOS-input threshold is normally set at one-half of V_{CC}. To shift the threshold voltage to be centered around 1.5 V (see Figure 6), the supply voltage of the input stage is dropped by the diode, D1, and the transistor, Q1. Reducing the voltage at the source of Q_p enables it to turn off more efficiently when flow is from V_{CC} to GND (ΔI_{CC}). When the input is in the low state, Q_r raises the voltage of the source of Q_p to V_{CC} to ensure proper operation of the following stage. This feedback circuit provides approximately 100 mV of input hysteresis, which increases the noise margin and helps ensure the device is free from oscillations when operated within specified input ramp rates.

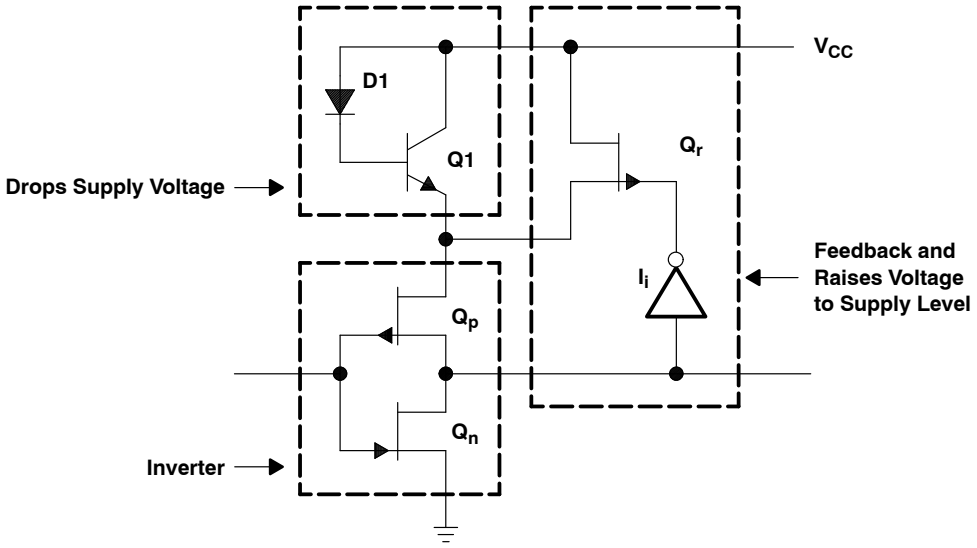


Figure 5. Simplified Input Stage of an ABT Circuit

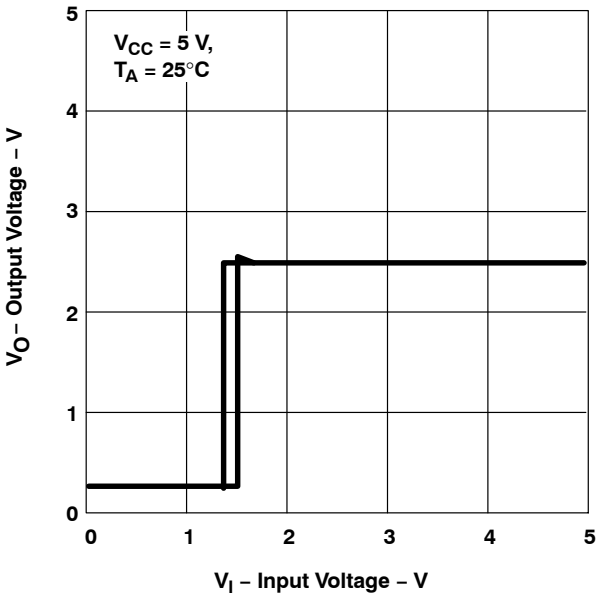


Figure 6. Output Voltage vs Input Voltage

Input Current Loading

The utilization of submicron (0.8-µm) CMOS technology for the input stage of ABT devices causes minimal loading of the system bus due to low leakage currents and low capacitance. The small geometries of the EPIC-IIB process have resulted in capacitances as low as 3 pF for inputs and 8 pF for C_{io} of a transceiver. Figure 7 and Table 2 indicate the low input current performance and specifications. Considering this low capacitance along with the negligible input current, systems designers can decrease their overall bus loading.

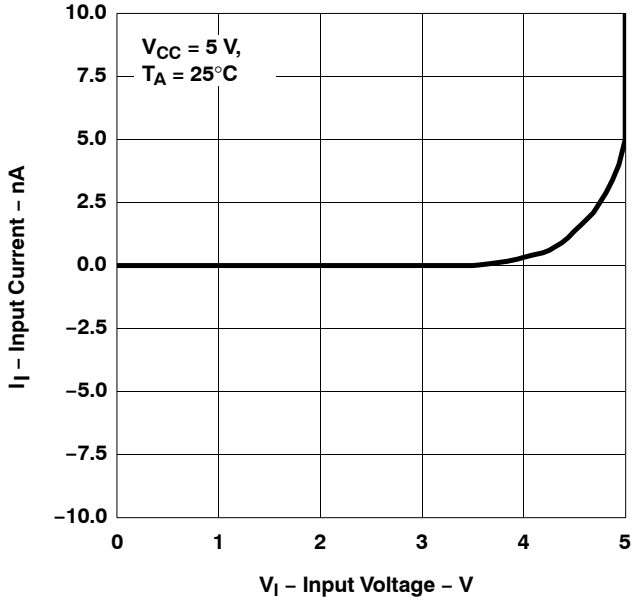


Figure 7. Input Current vs Input Voltage

Table 2. Input Current Specifications

PARAMETER	TEST CONDITIONS		T_A = 25°C			SN54ABT245		SN74ABT245		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
I_I	V_{CC} = 5.5 V,	V_I = V_{CC} or GND			±1		±1		±1	µA
I_{OZH}†	V_{CC} = 5.5 V,	V_O = 2.7 V			50		50		50	µA
I_{OZL}†	V_{CC} = 5.5 V,	V_O = 0.5 V			–50		–50		–50	µA

† The parameters I_{OZH} and I_{OZL} include the input leakage current.

Supply Current Change (ΔI_{CC})

Because ABT devices utilize a CMOS-input stage but operate in a TTL-level signal environment, there is a current specification unique to this set of conditions known as ΔI_{CC}. Given a CMOS inverter with the input voltage set so that both the p and n channel devices are on, current flows from V_{CC} to GND. This can occur when the input to an ABT device is at a valid high level (>2 V), which turns on the n-channel, but not high enough to completely turn off the p-channel device. The current that flows under these conditions is specified in the data sheet (ΔI_{CC}) and is measured one input at a time with the input voltage set at 3.4 V. Figure 8 shows the change in I_{CC} as the input is ramped from 0 V to 5 V. For ABT non-storage devices, a feature is added that turns off the input when the outputs are disabled to reduce power consumption (see Table 3 for an example. Refer to individual data sheets for this specification).

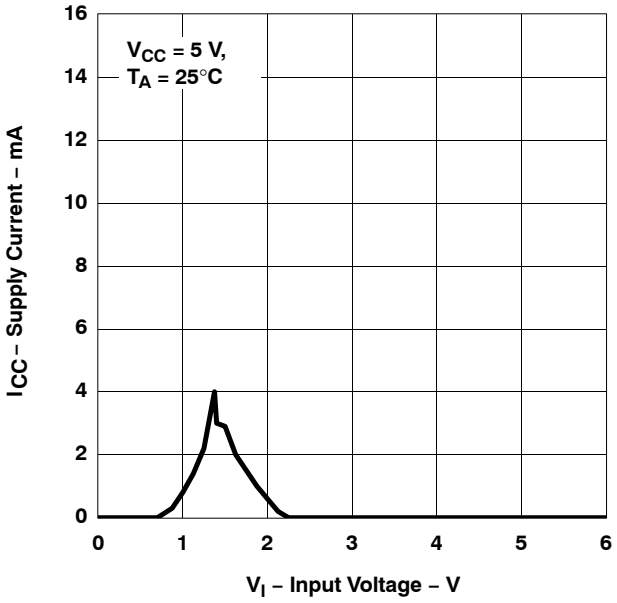


Figure 8. Supply Current vs Input Voltage

Table 3. Supply Current Change (ΔI_{CC})

PARAMETER	TEST CONDITIONS		T_A = 25°C		SN54ABT244		SN74ABT244		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
ΔI_{CC}‡	V_I = 5.5 V, One input at 3.4 V, Other inputs at V_{CC} or GND	Outputs enabled		1.5		1.5		1.5	mA
		Outputs disabled		50		50		50	µA

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Proper Termination of Unused Inputs

With advancements in speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output glitching or, in some cases, oscillations. Similar situations can occur if an unused input is left floating or not being actively held at a valid logic level.

These problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 9). Since the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, the inductive voltage spikes (V_{gnd}) affect the way signals appear to the internal gate structures. For instance, as the voltage at the device's ground node rises, the input signal (V_i') appears to decrease in magnitude. This undesirable phenomena can erroneously change the output's transition if a threshold violation takes place.

In the case of a slowly rising input edge, if the ground movement is large enough, the apparent signal, V_i', at the device appears to be driven back through the threshold and the output starts to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents) the slow input edge is repeatedly driven back through the threshold, resulting in output oscillation.

ABT devices are recommended to have input edge rates faster than 5 ns/V for standard parts, and 10 ns/V for the Widebus™ series of products when the outputs are enabled. A critical area for this edge rate is in the transition region between 1 V and 2 V. It is also recommended to hold inputs or I/O pins at a valid logic high or low when they are not being used or when the part driving them is in the high-impedance state.

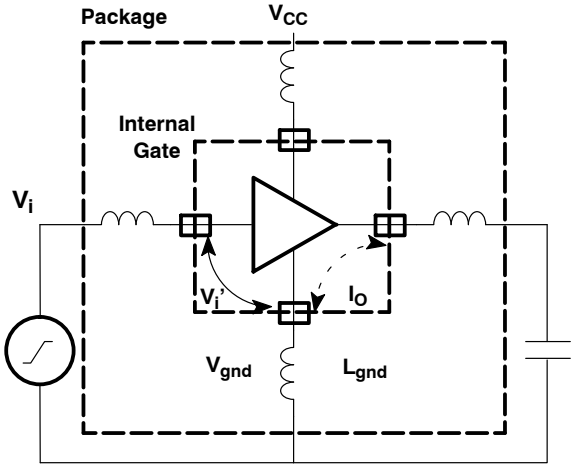


Figure 9. Sample Input/Output Model

Output Characteristics

The current trend is consolidation of the functionality of multiple logic devices into complex, high pin-count ASICs and programmables. There are a number of important advantages for utilizing bus-interface devices in standard high-volume packages. These include the need for high drive capability and good signal integrity. The use of bipolar circuitry in the output stage makes it possible to provide these requirements, along with increased speed, using the ABT family.

Figure 10 shows a simplified schematic of an ABT output stage. Data is transmitted to the gate of M1, which acts as a simple current switch. When M1 is turned on, current flows through R1 and M1 to the base of Q4, turning it on and driving the output low. At the same time, the base of Q2 is pulled low, thus turning off the upper output. For a low-to-high transition, the gate of M1 must be driven low, turning M1 off. Current through R1 charges the base of Q2, pulling it high and turning on the Darlington pair, consisting of Q2 and Q3. Meanwhile, with its supply of base drive cut off, Q4 turns off, and the output switches from low to high. R2 is used to limit output current in the high state, and D1 is a blocking diode used to prevent reverse current flow in specific power-down applications.

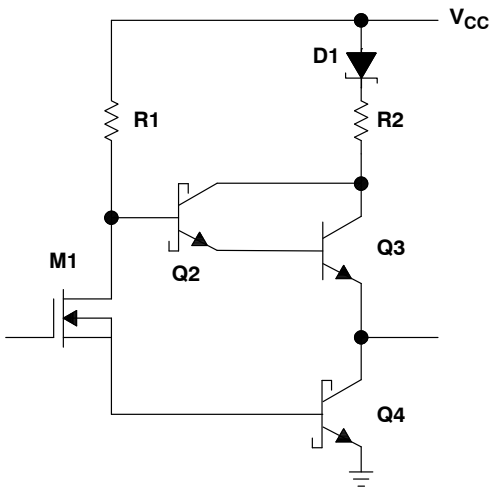


Figure 10. Simplified ABT Output Stage

A clear advantage of using bipolar circuitry in the output stage (as opposed to CMOS) is the reduced voltage swing. This helps to lower ground noise and reduce power consumption. Refer to *Signal Integrity* and *Power Considerations* in this document for further information.

Output Drive

The I_{OH} and I_{OL} curves for a typical ABT output are shown in Figure 11. With a specified I_{OL} of 64 mA and I_{OH} of −32 mA, ABT accommodates many standard backplane specifications. However, these devices are capable of driving well beyond these limits. This is important when considering switching a low-impedance backplane on the incident wave.

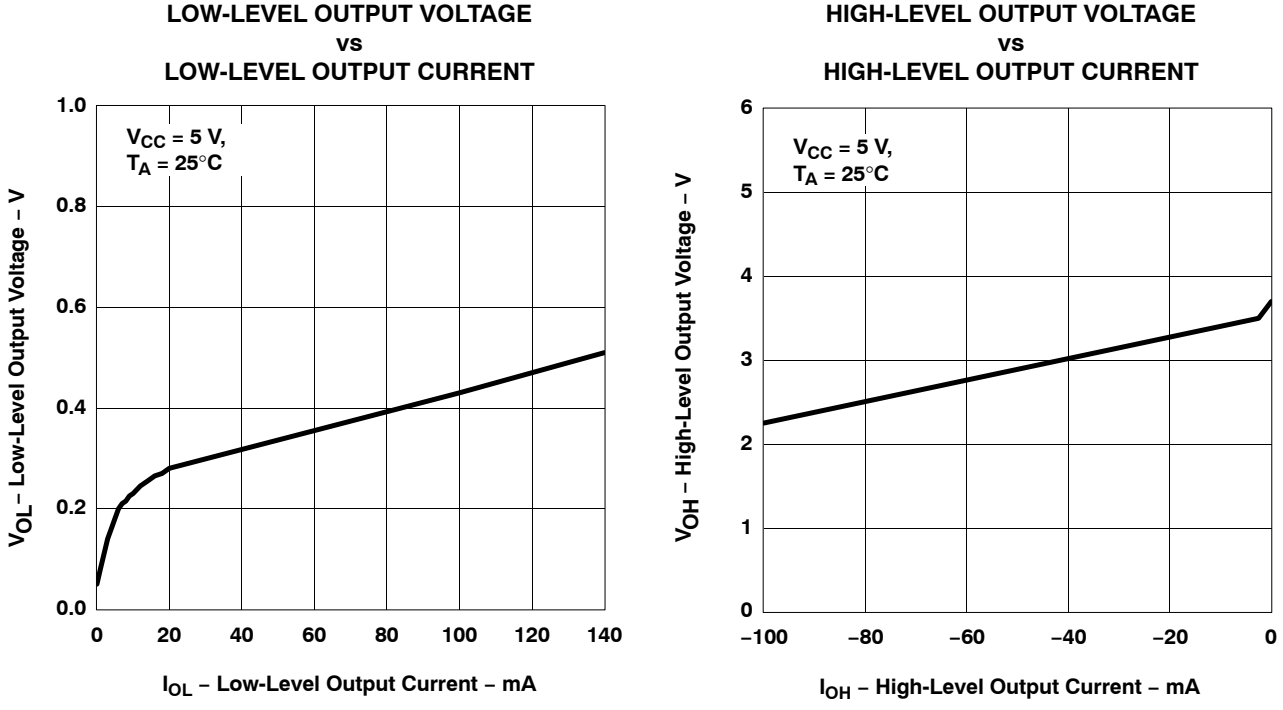


Figure 11. Typical ABT Output Characteristics

Incident-wave switching ensures that for a given transition (either high-to-low or low-to-high) the output reaches a valid V_{IH} or V_{IL} level on the initial wave front (i.e., does not require reflections). Figure 12 shows the problems a designer might encounter when a device does not switch on the incident wave. A shelf below $V_{IL(max)}$, signal A, causes the propagation delay to slow by the amount of time it takes for the signal to reach the receiver and reflect back. Signal B shows the case in which there is a shelf in the threshold region. When this happens, the input to the receiver is uncertain and could cause several problems associated with slow input edges, depending on the length of time the shelf remains in this region. A signal as shown in example C does not cause a problem because the shelf does not occur until the necessary V_{IH} level has been attained.

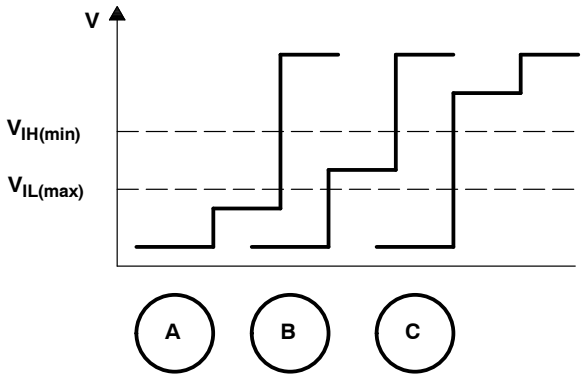


Figure 12. Reflected Wave Switching

Using typical V_{OH} and V_{OL} values along with data points from the curves, ABT devices can typically drive lines in the 25-Ω range on the incident wave.

For a low-to-high transition, (I_{OH} = 85 mA @ V_{OH} = 2.4 V)

$$Z_{LH} = \frac{V_{OH}(min) - V_{OL}(typ)}{I_{OH}} = \frac{2.4\ V - 0.3\ V}{85\ mA} - 25\ \Omega \quad (1)$$

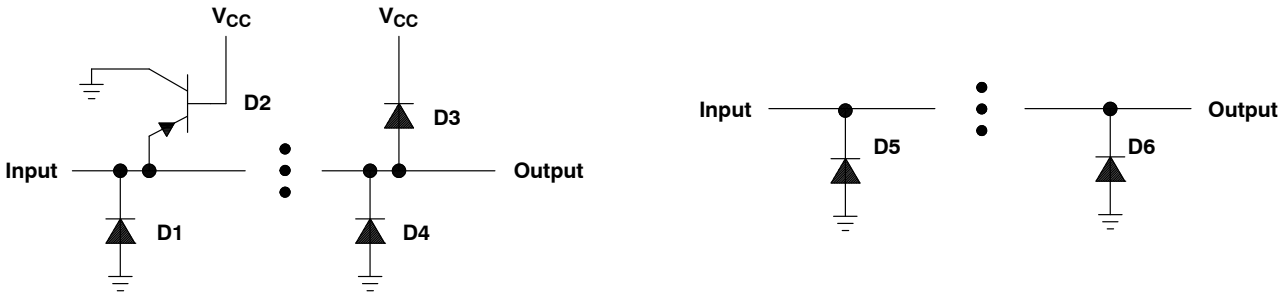
For a high-to-low transition, (I_{OL}= 135 mA @ V_{OL}= 0.5 V)

$$Z_{HL} = \frac{V_{OH}(typ) - V_{OL}(max)}{I_{OL}} = \frac{3.5\ V - 0.5\ V}{135\ mA} - 22\ \Omega \quad (2)$$

Partial Power Down

One application, addressed when designing the ABT family, is partial system power down. When using a standard CMOS device, there is a path from either the input or the output (or both) to V_{CC}. This prevents partial power down for such applications as hot-card insertion without adding current limiting components. This is not the case with ABT as these paths have been eliminated with the use of blocking diodes. Figure 13 shows functionally equivalent schematics of the input structures for CMOS and ABT devices.

Consider the situation shown in Figure 14. The driving device is powered with V_{CC} = 5 V, while the receiving device is powered down (V_{CC} = 0). If these devices are CMOS, the receiver can be powered up through diode D2 when the driver is in a high state. ABT devices do not have a comparable path and are thus immune to this problem, making them more desirable for this application.



(a) CMOS EQUIVALENT INPUT STRUCTURE (b) ABT EQUIVALENT INPUT STRUCTURE

Figure 13. Simplified Input Structures for CMOS and ABT Devices

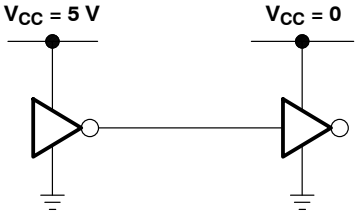


Figure 14. Example of Partial System Power Down

Signal Integrity

A frequent concern of system designers is the performance degradation of ICs when outputs are switched. TI's priority when designing the ABT bus-interface family was to insure signal integrity and eliminate the need for excess settling time of an output waveform. This section addresses the simultaneous switching performance of both the ABT octals and the Widebus functions.

Simultaneous-Switching Phenomenon

Figure 15 shows a simple model of an output pin, including the associated capacitance of the output load and the inherent inductance of the ground lead. The voltage drop across the GND inductor, V_L, is determined by the value of the inductance and the rate of change in current across the inductor. When multiple outputs are switched from high to low, the transient current (di/dt) through the GND inductor generates a difference in potential on the chip ground with respect to the system ground. This induced GND variation can be observed indirectly as shown in Figure 16. The voltage output low peak (V_{OLP}) is measured on one quiet output when all others are switched from high to low.

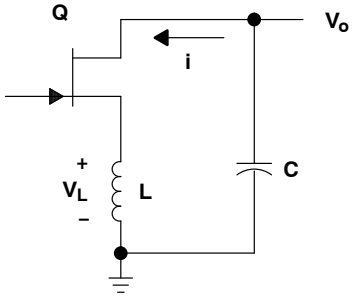
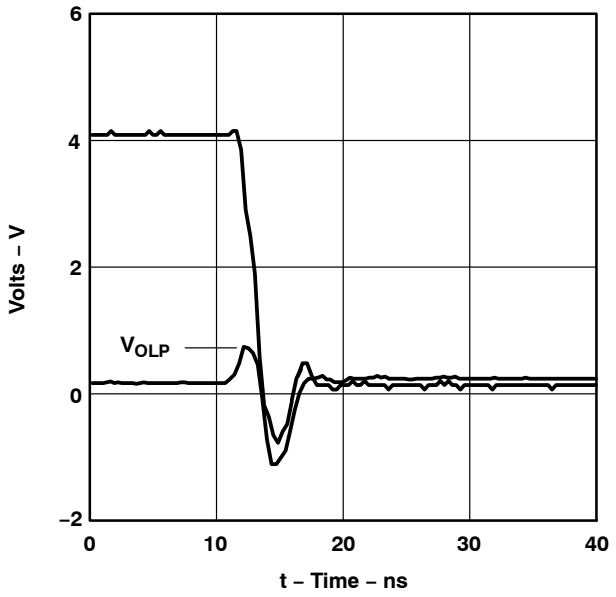


Figure 15. Simultaneous-Switching Output Model



NOTE: V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs

Figure 16. Simultaneous-Switching-Noise Waveform

A similar phenomena occurs with respect to the V_{CC} plane on a low-to-high transition, known as voltage output high valley (V_{OHV}). Most problems are associated with a large V_{OLP} because the range for a logic 0 is much less than the range for a logic 1, as shown in Figure 17. For a comprehensive discussion of simultaneous switching, see *Simultaneous Switching Evaluation and Testing*, Section 4.1, in the *Advanced CMOS Logic (ACL) Designer's Handbook*, literature number SCAA001B.

The impact of these voltage noise spikes on a system can be extreme. The noise can cause loss of stored data, severe speed degradation, false clocking, and/or reduction in system noise immunity. For an overview of how propagation delay is affected by the switching of multiple outputs, please refer to *ac Performance* in this document.

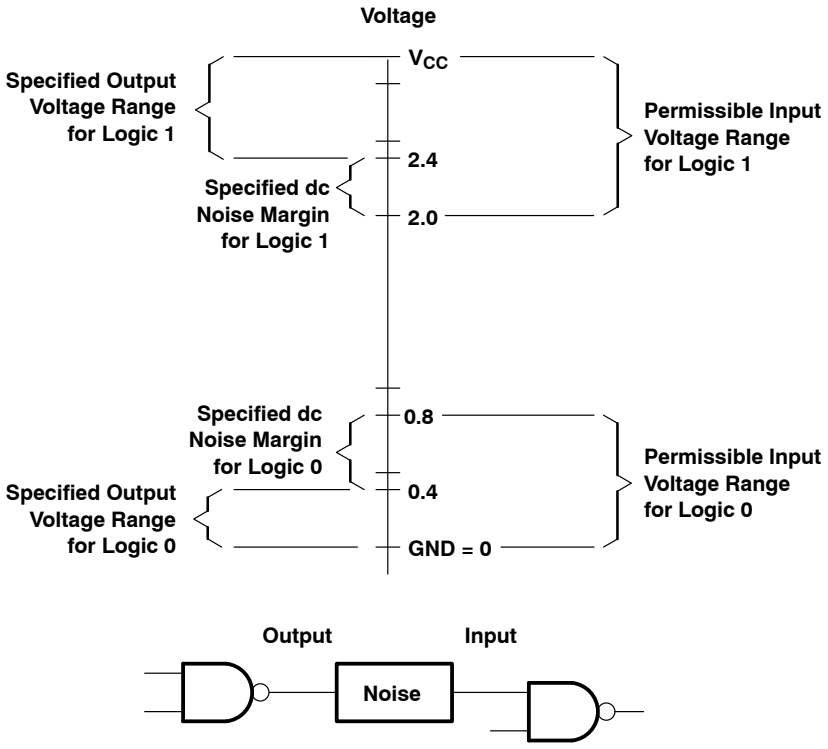


Figure 17. TTL DC Noise Margin

Simultaneous Switching Solutions

Some methods an IC manufacturer can use to reduce the effects of simultaneous switching include: reducing the inductance of the power pins, adding multiple power pins, and controlling the turn on of the output. These techniques are described in the *Advanced CMOS Logic (ACL) Designer's Handbook*, literature number SCAA001B.

Octal ABT devices employ the standard end-pin GND and V_{CC} configuration, while maintaining acceptable simultaneous switching performance, as shown in Figure 18. This is due to the TTL-level output swing (0.3−3 V) and a controlled feedback, which limits the base drive to the lower output.

The ABT Widebus series (16-, 18-, and 20-bit functions) are offered in an SSOP package (see *Packaging* in this document), which TI developed to save valuable board space and reduce simultaneous switching effects. One might expect an increase in noise with 16 outputs switching in a single package; however, the simultaneous switching performance is actually improved. There is a GND pin for every two outputs and a V_{CC} pin for every four. This allows the transient current to be distributed across multiple power pins and decreases the overall d_i/d_t effect. This results in a typical V_{OLP} value on the order of 500 mV for the ABT16500, as shown in Figure 19.

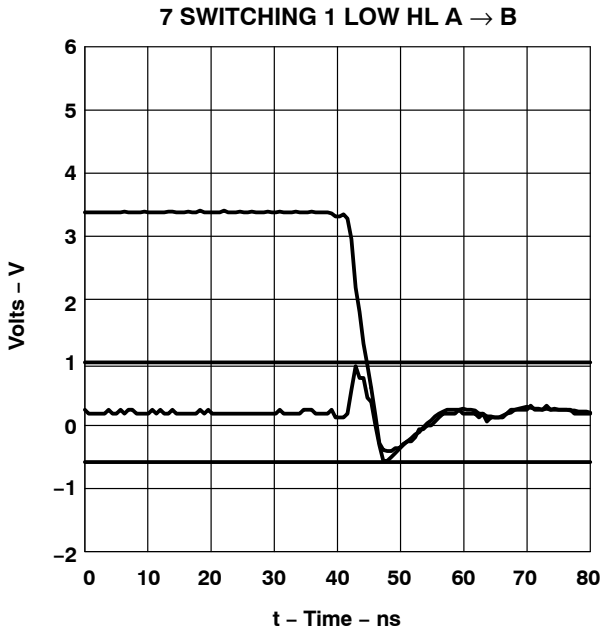


Figure 18. ABT646A Simultaneous-Switching Waveform

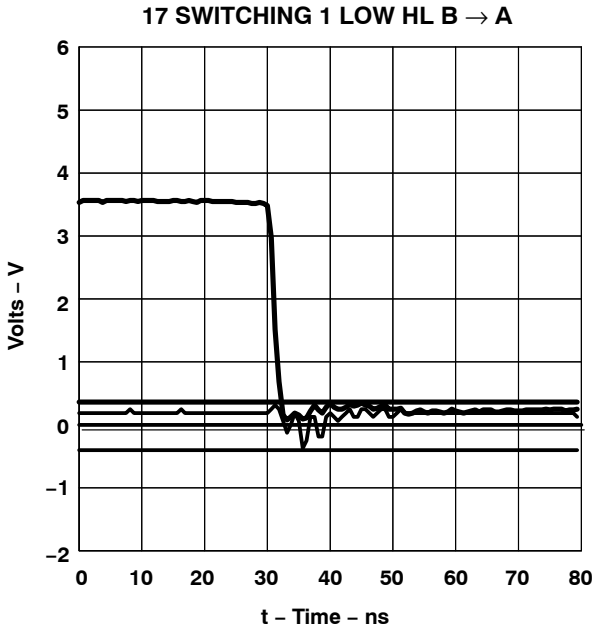


Figure 19. ABT16500B Simultaneous-Switching Waveform

Advanced Packaging

Along with a strong commitment to provide fast, low- power, high-drive ICs, TI is the leader in logic packaging advancements. The development of the shrink small-outline package (SSOP) in 1989 provided system designers the opportunity to reduce the amount of board space required for bus-interface devices by 50%. Several 24-pin solutions including the familiar SOIC, the SSOP, and the TSOP (thin small-outline package) are shown in Figure 20.

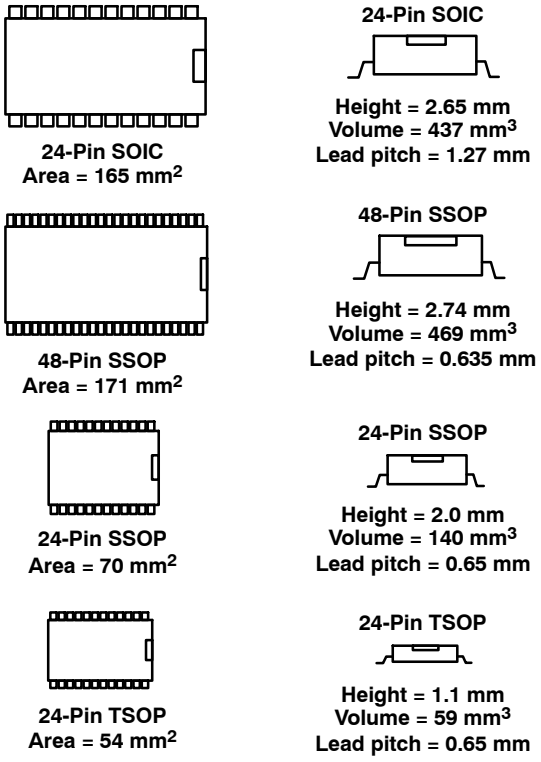


Figure 20. 24-Pin Surface-Mount Comparison

The 48/56-pin SSOP packages allow for twice the functionality (16-, 18-, and 20-bit functions) in approximately the same board area as a standard SOIC. This is accomplished by using a 25-mil (0.635 mm) lead pitch, as opposed to 50-mil (1.27 mm) in SOIC. Figure 21 shows a typical pinout structure for the 48-pin SSOP. The flow-through architecture is standard for all Widebus devices, making signal routing easier during board layout. Also note the distributed GND and V_{CC} pins, which improve simultaneous switching effects as discussed in *Signal Integrity* in this document.

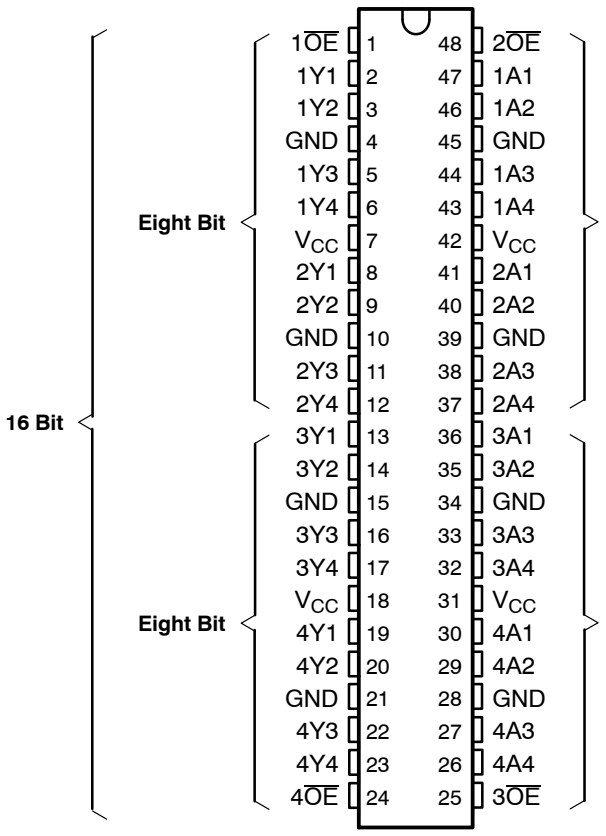


Figure 21. Distributed Pinout of ’ABT16244A

When using the small pin count SSOPs (8-, 9-, and 10-bit functions) the same functionality occupies less than half the board area of a SOIC (70 mm^2 vs 165 mm^2). There also is a height improvement over the SOIC, which is beneficial when the spacing between boards is a consideration. For very dense memory arrays the packaging evolution has been taken one step further with the TSOP. The TSOP thickness of 1.1 mm gives a 58% height improvement over the SOIC.

Table 4 provides a quick reference of the mechanical specifications of the various SSOP packages. For more information, see *Recent Advancements in Bus-Interface Packaging and Processing*, literature number SCZA001A, and *Thin Very Small-Outline Package (TVSOP)*, literature number SCBA009C.

Table 4. SSOP Metric Specifications†

PACKAGE SPECIFICATIONS						PIN SPECIFICATIONS	
PACKAGE TYPE	PINS	INDUSTRY STANDARD	THICKNESS (mm)	BODY WIDTH (mm)	STANDOFF HEIGHT (mm)‡	PIN PITCH (mm)	PIN WIDTH (mm)
SSOP	20	EIAJ	2.00	5.3	0.05	0.650	0.30
SSOP	24	EIAJ	2.00	5.3	0.05	0.650	0.30
SSOP	28	JEDEC	2.59	7.5	0.20	0.635	0.25
SSOP	48	JEDEC	2.59	7.5	0.20	0.635	0.25
SSOP	56	JEDEC	2.59	7.5	0.20	0.635	0.25

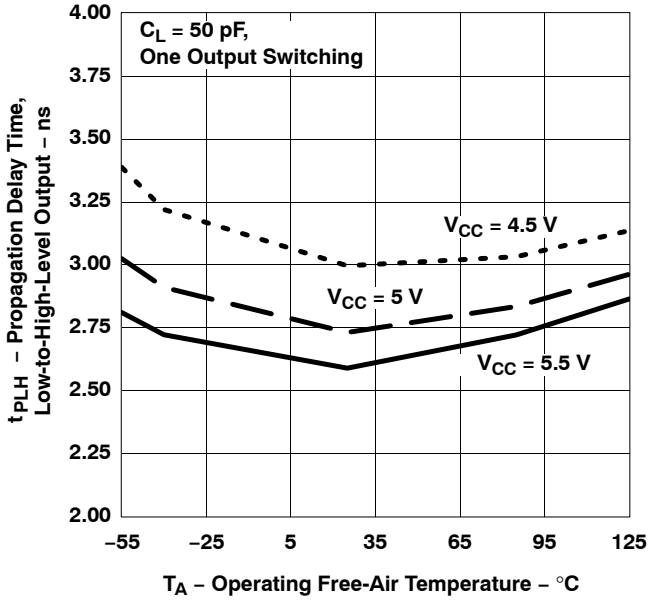
† All values are maximum typical values unless otherwise indicated.
‡ Minimum values

APPENDIX A
'ABT646A Characterization Data

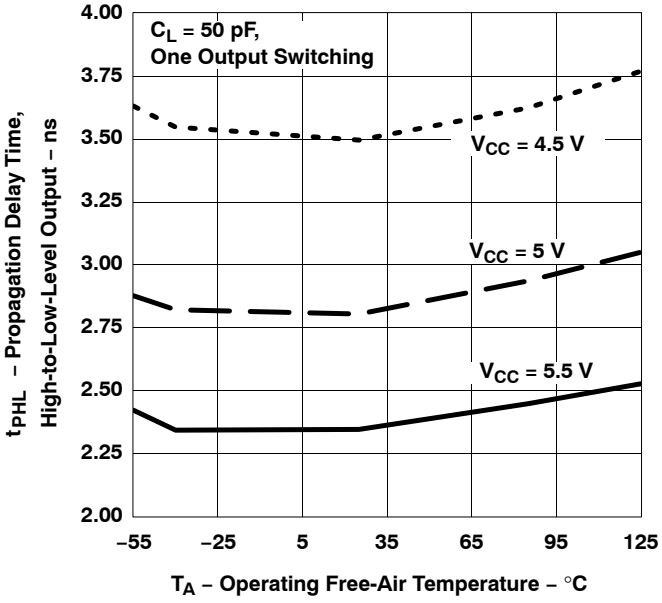
A

Propagation Delay Time vs Temperature

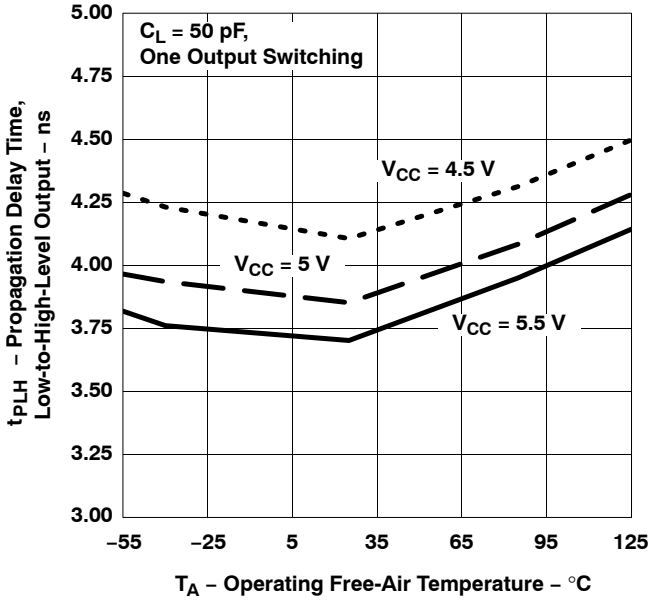
**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



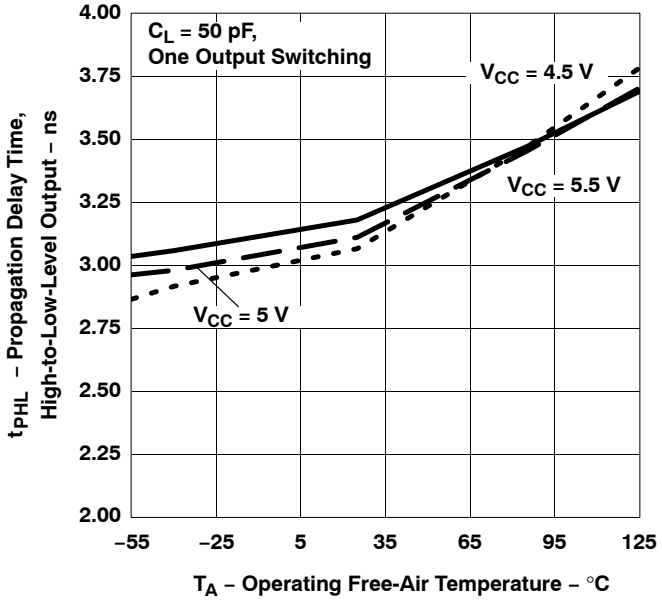
**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
CLKAB to B**

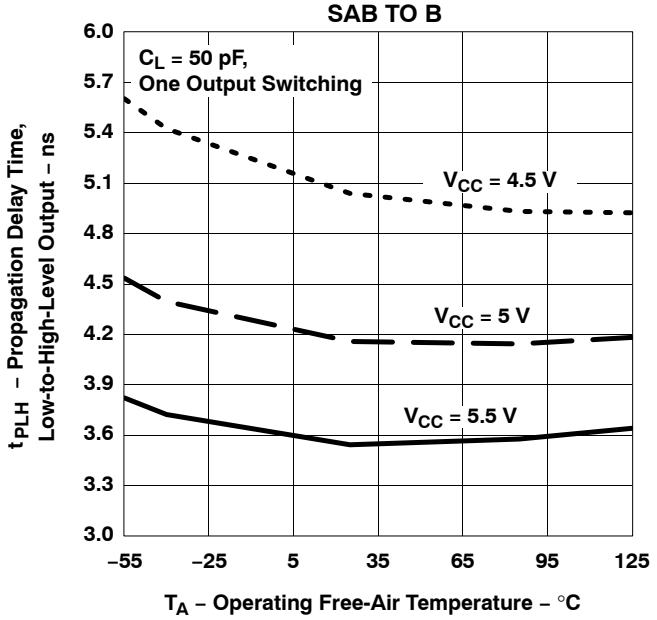


**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
CLKAB TO B**

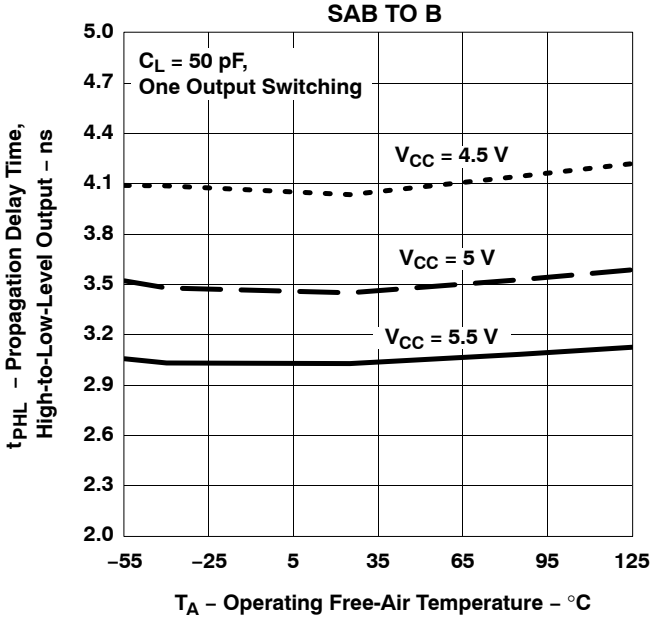


Propagation Delay Time vs Temperature

**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
SAB TO B**

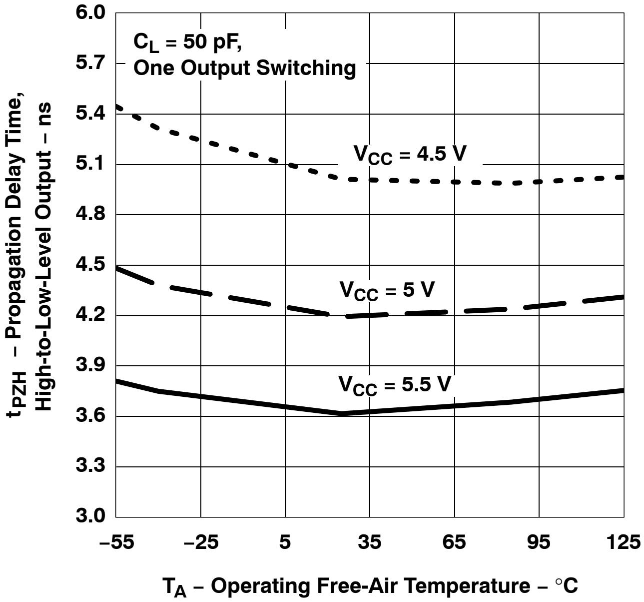


**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
SAB TO B**

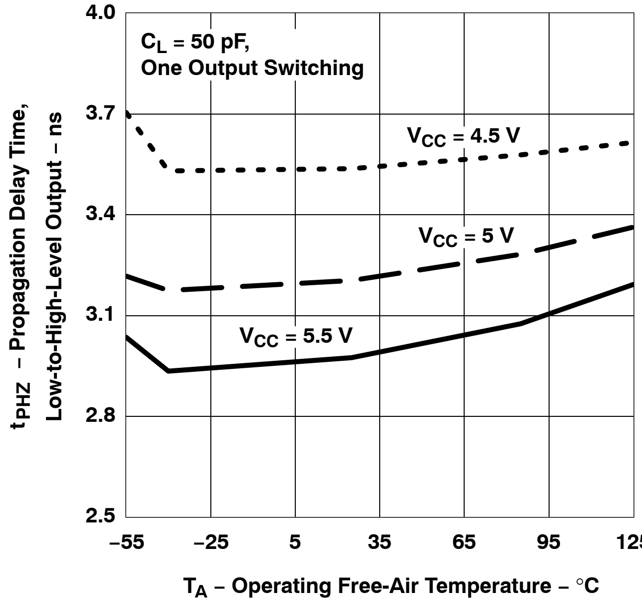


Propagation Delay Time vs Temperature

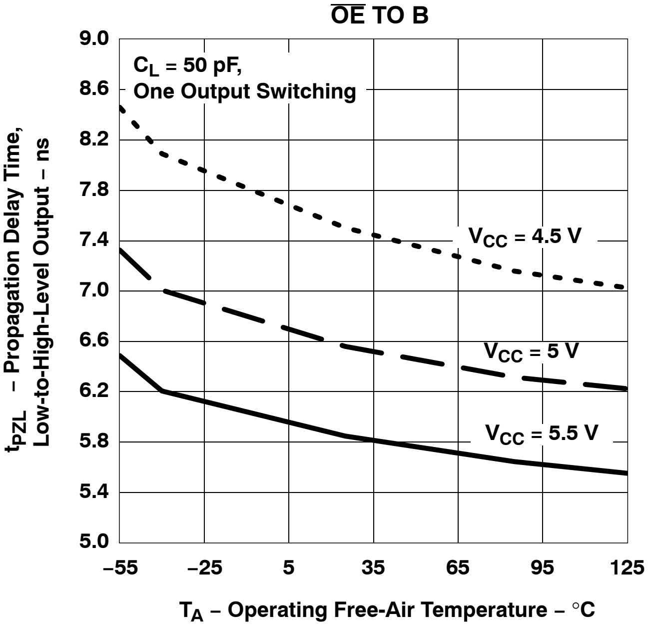
PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B



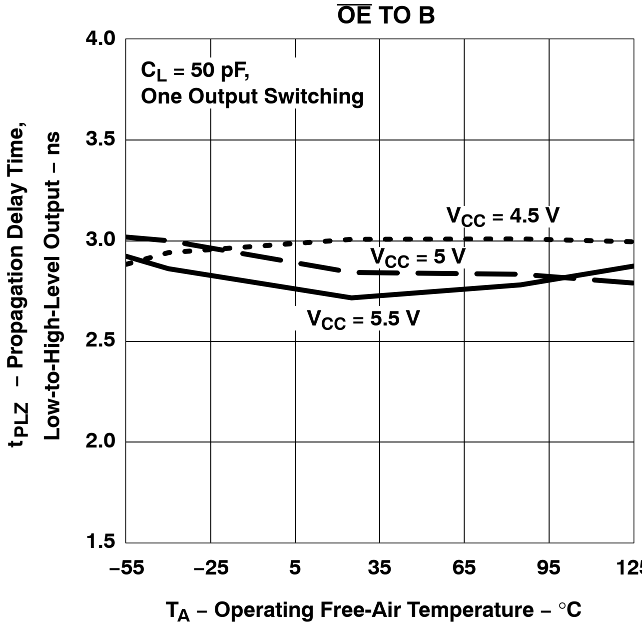
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B

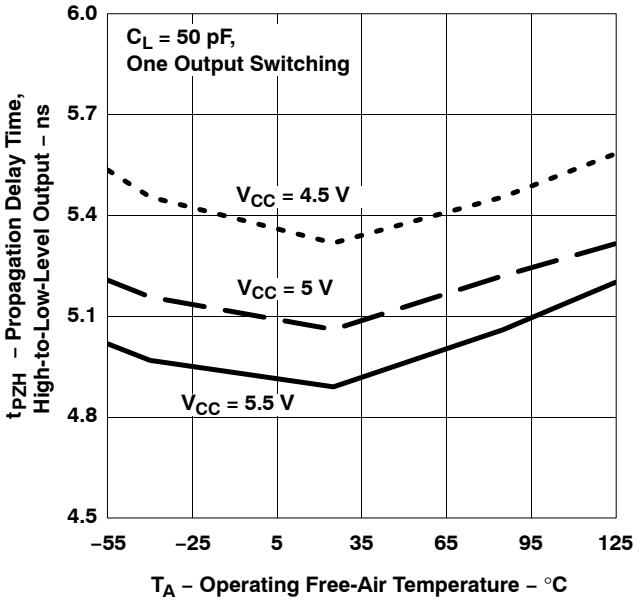


PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO B

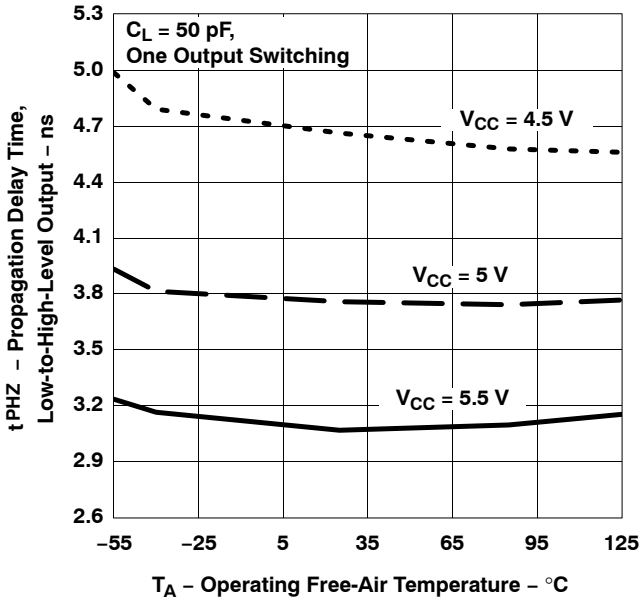


Propagation Delay Time vs Temperature

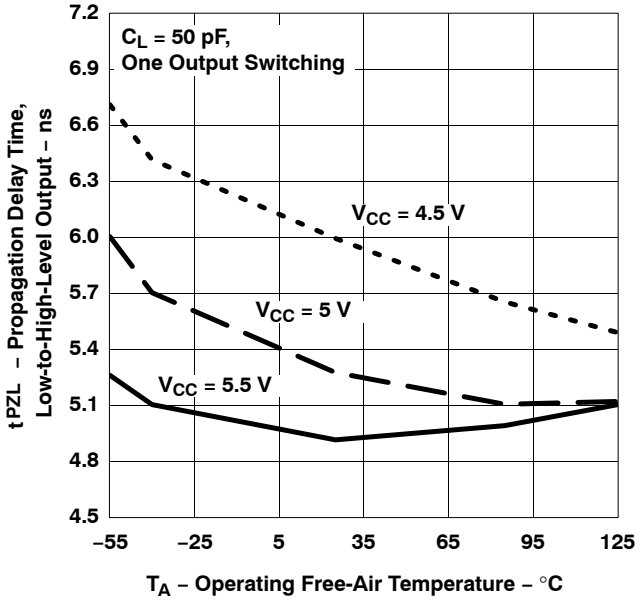
**PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**



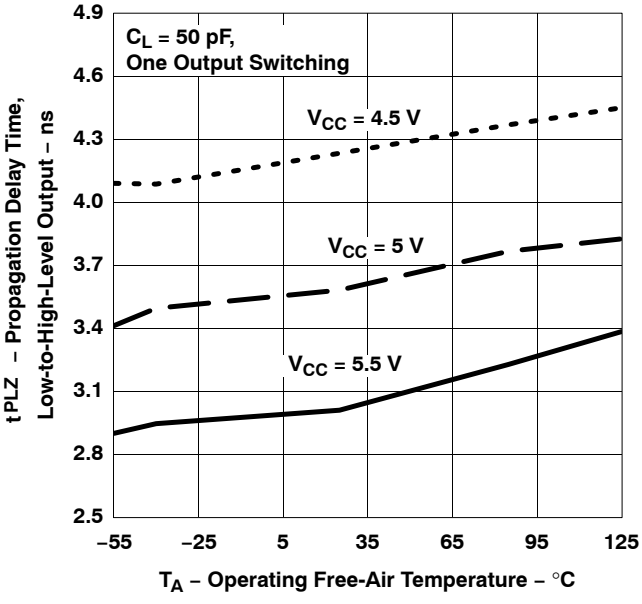
**PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**



**PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**

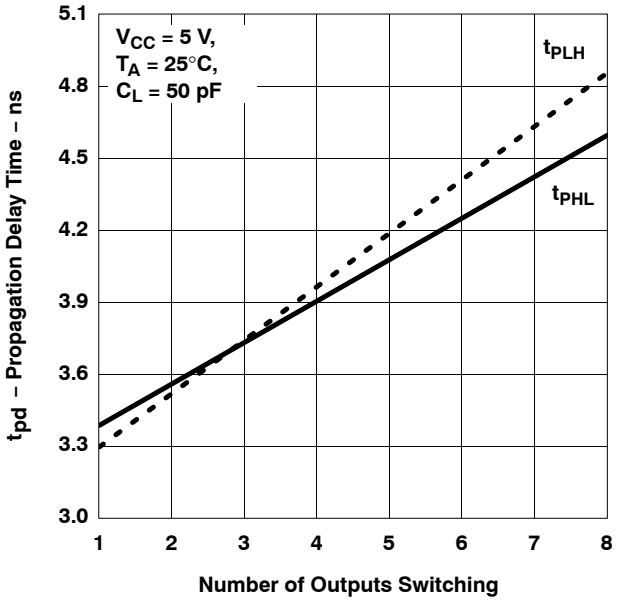


**PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
DIR TO B**

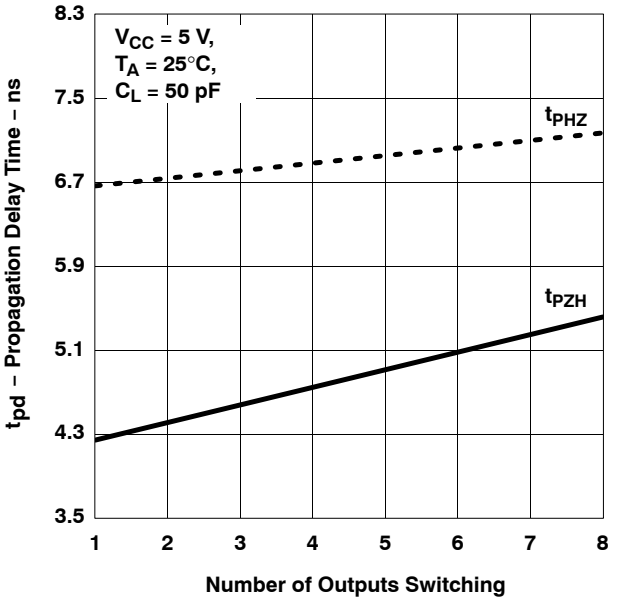


Propagation Delay Time vs Number of Outputs Switching

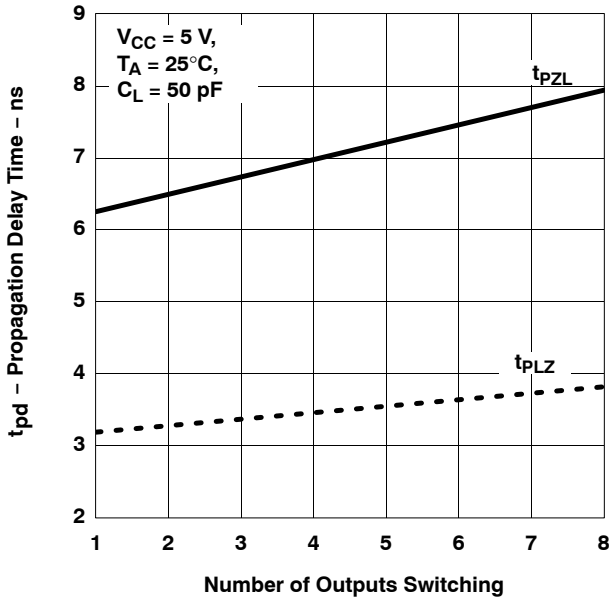
PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING A TO B



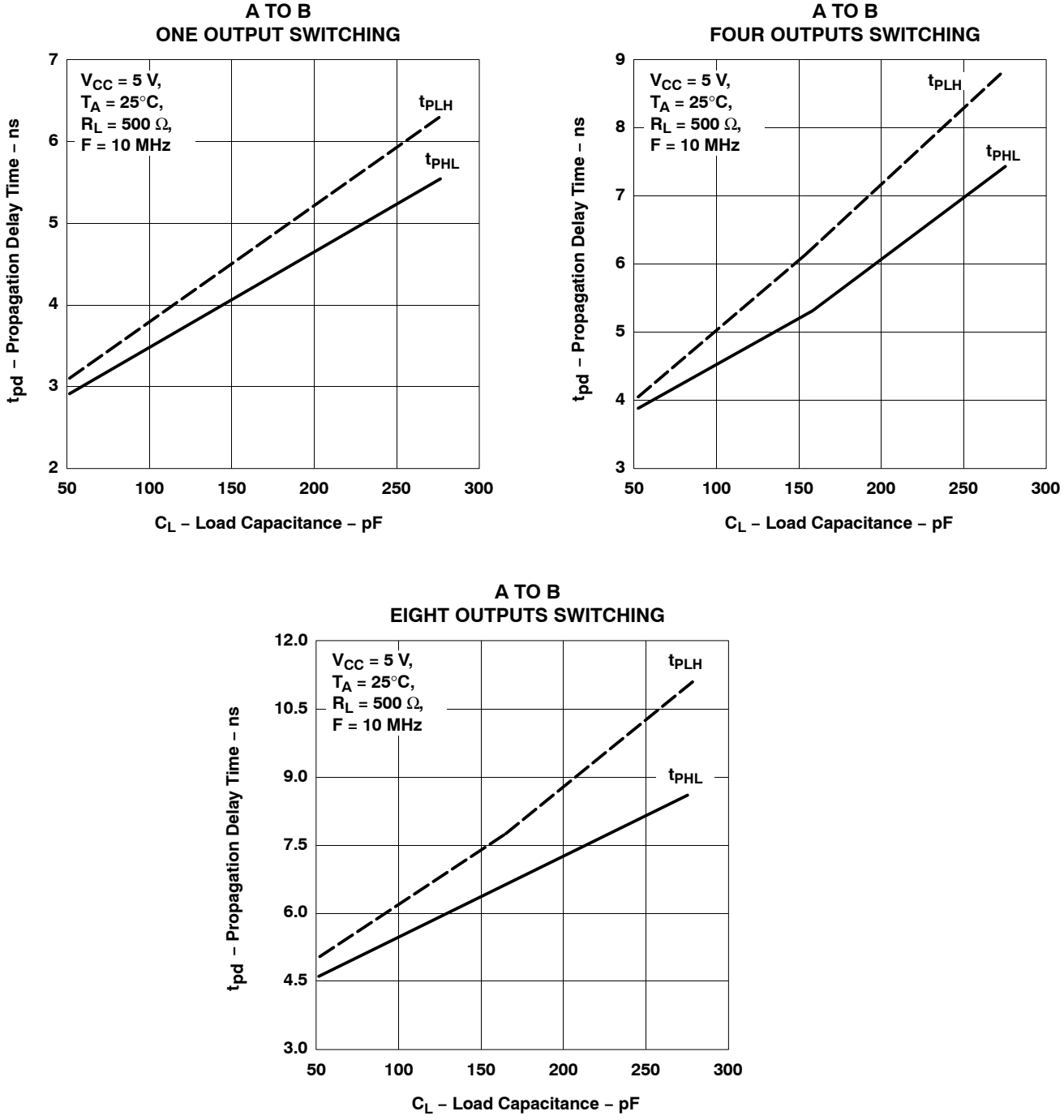
PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING A TO B



PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING A TO B

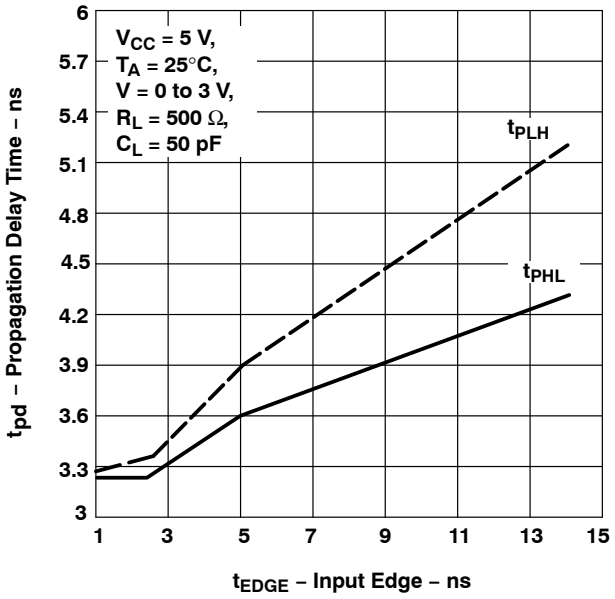


Propagation Delay Time vs Load Capacitance

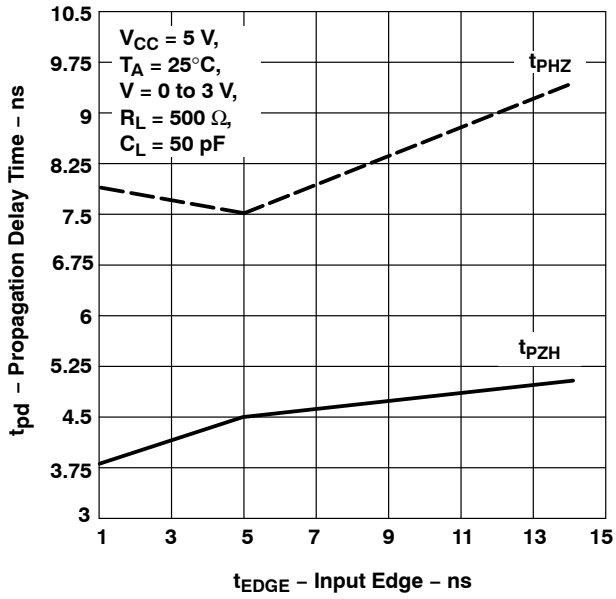


Propagation Delay Time vs Input Edge

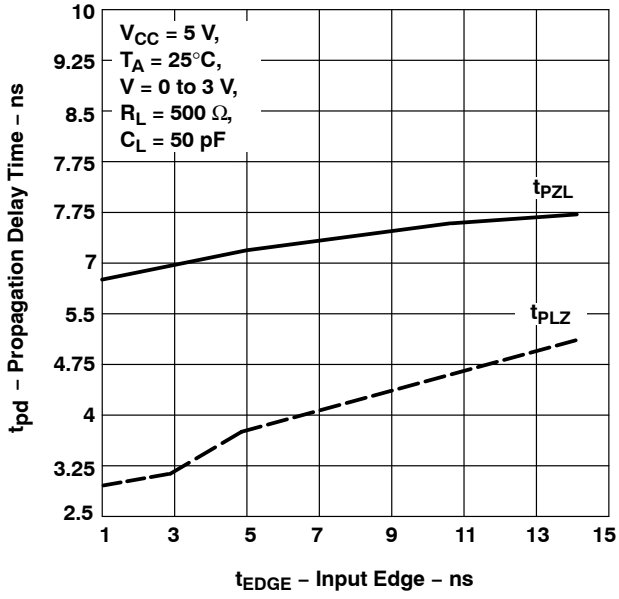
PROPAGATION DELAY TIME vs INPUT EDGE A TO B



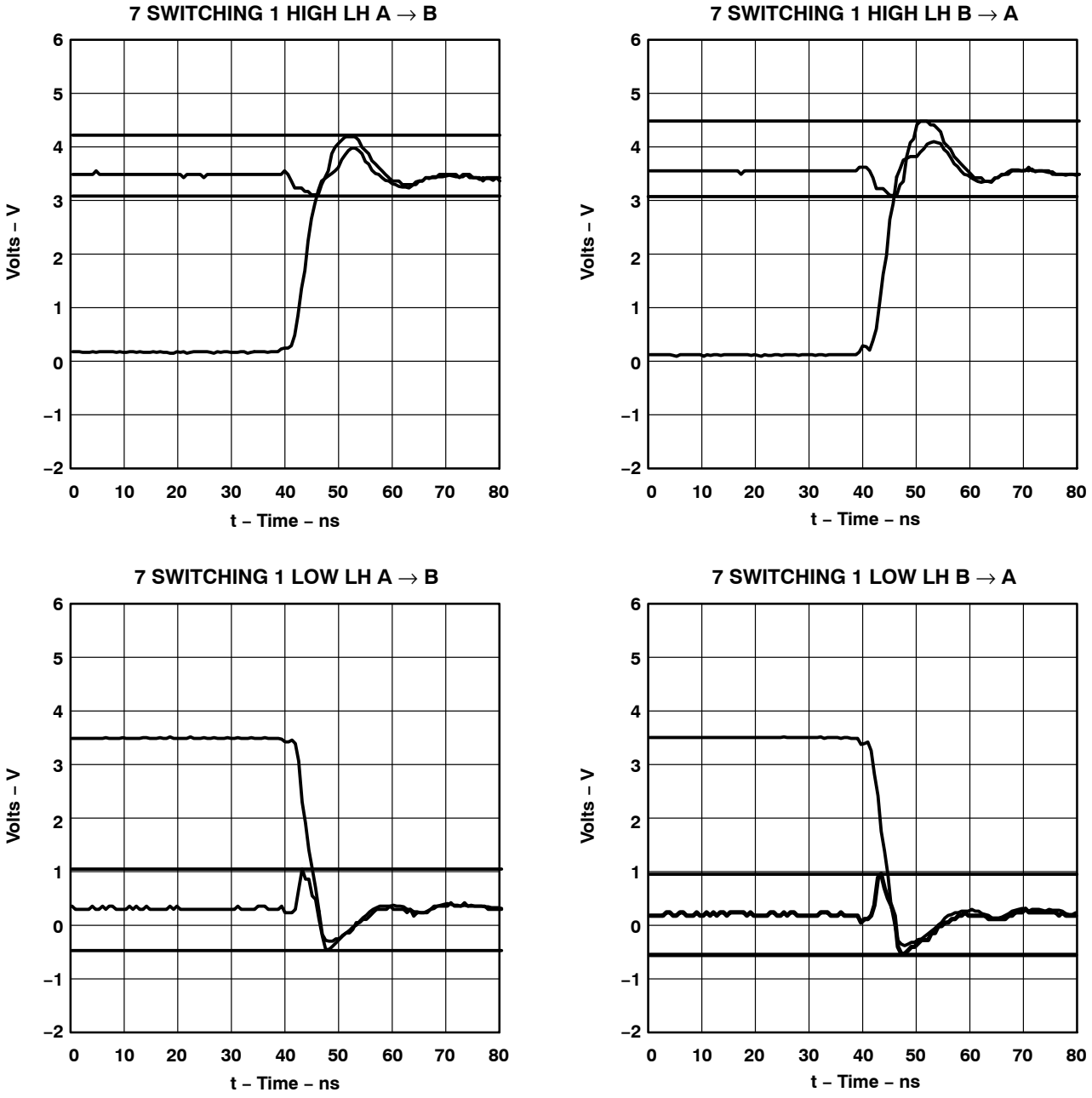
PROPAGATION DELAY TIME vs INPUT EDGE A TO B



PROPAGATION DELAY TIME vs INPUT EDGE A TO B



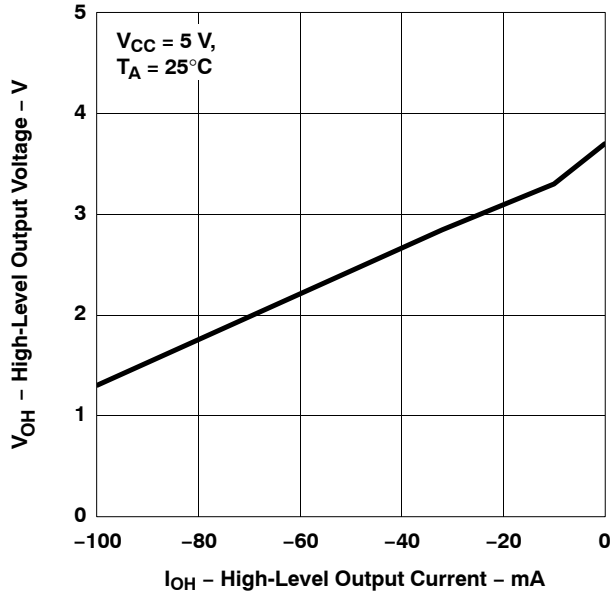
V_{OHV} and V_{OLP}



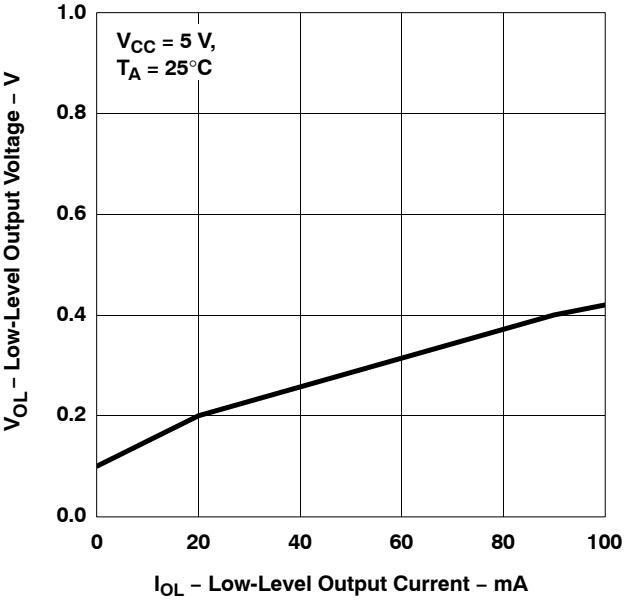
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

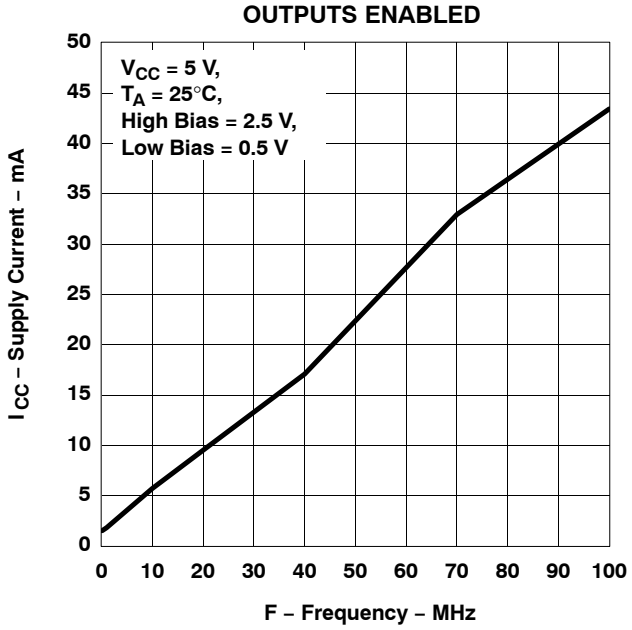
HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT

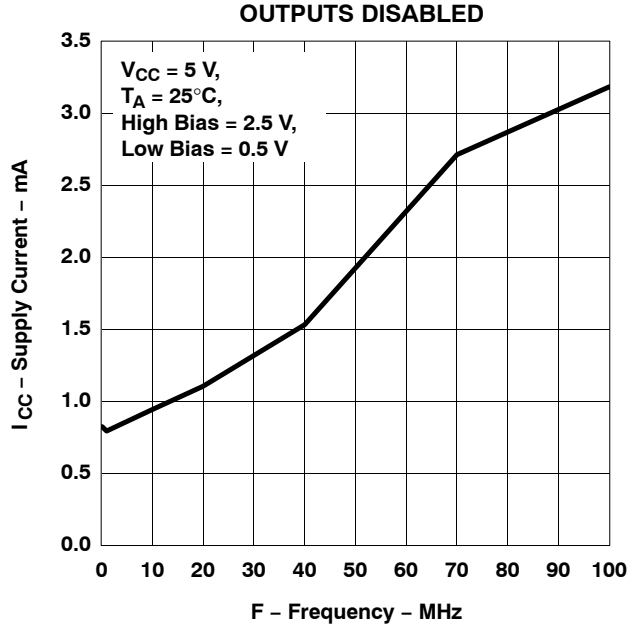


LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT



Supply Current vs Frequency



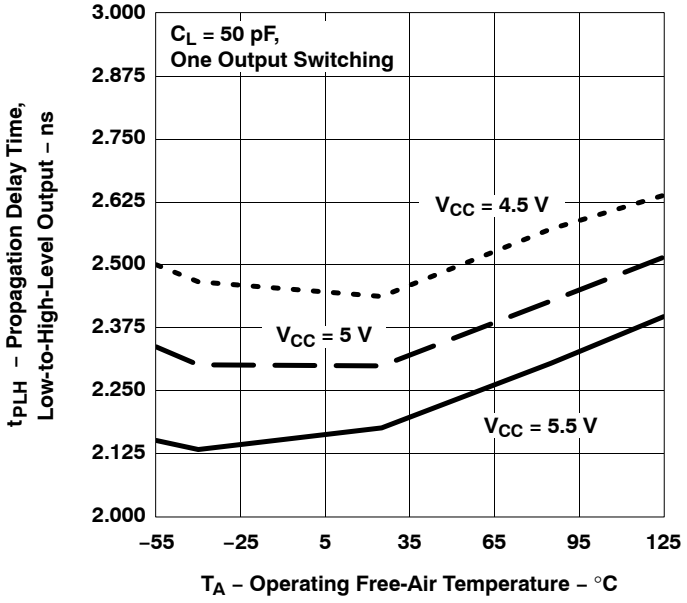


APPENDIX B
SN54ABT16244, SN74ABT16244A Characterization Data

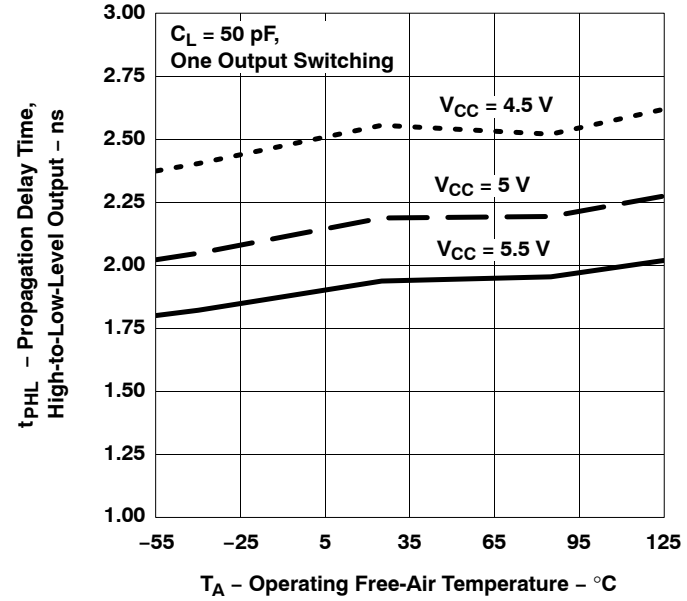
B

Propagation Delay Time vs Temperature

PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO Y

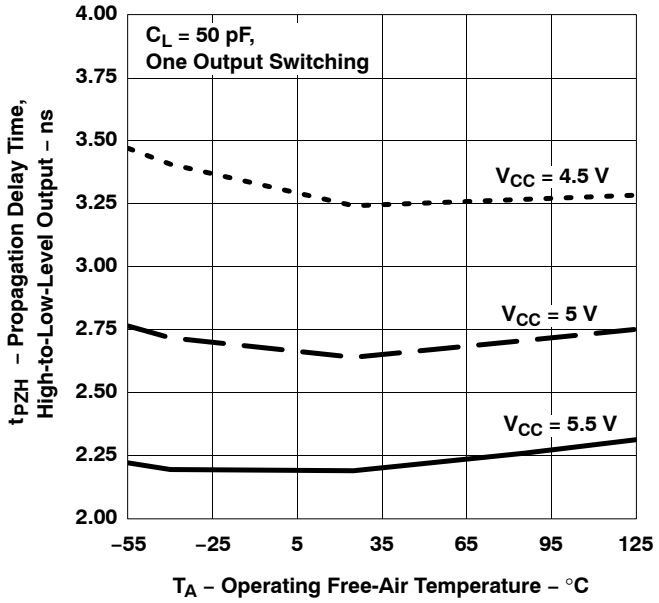


PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO Y

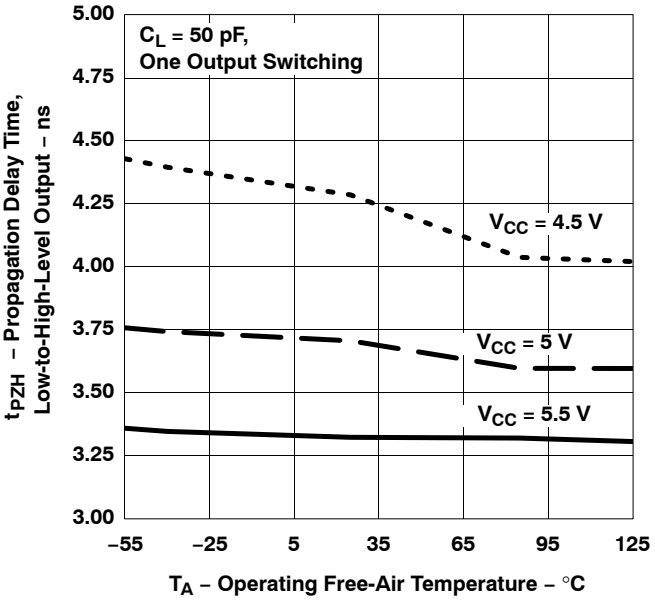


Propagation Delay Time vs Temperature

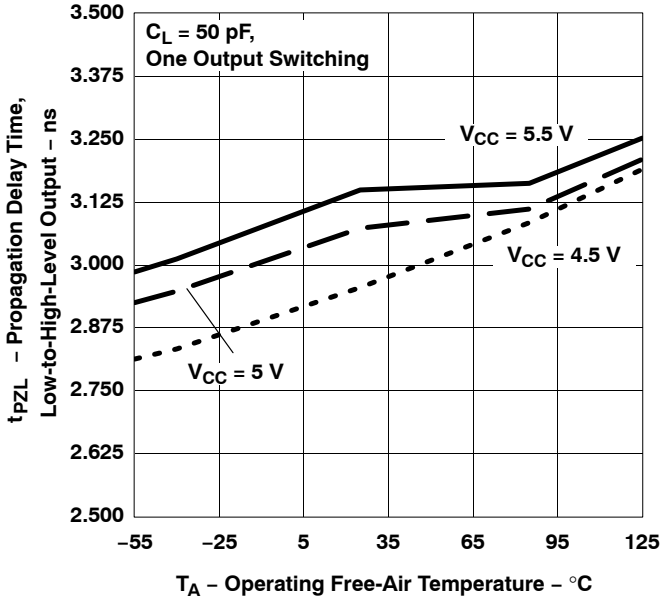
PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO Y



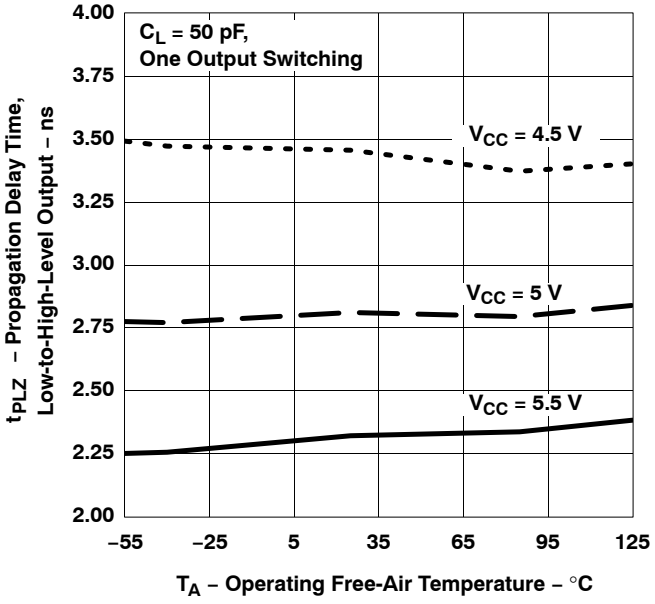
PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TOY



PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO Y

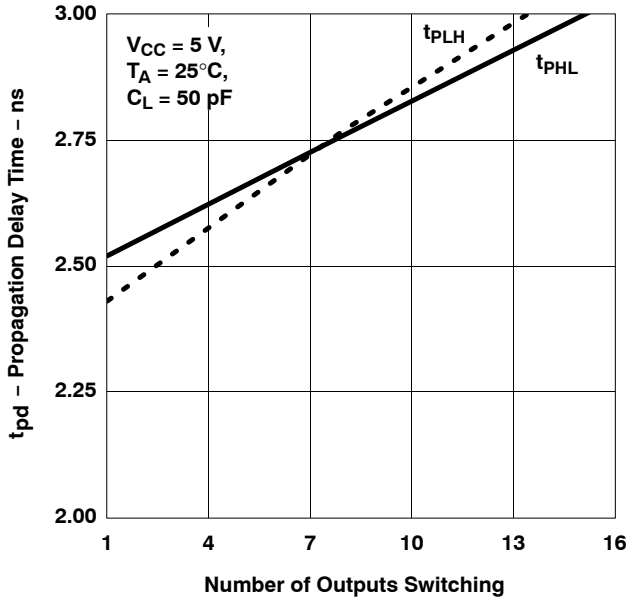


PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{OE}$ TO Y

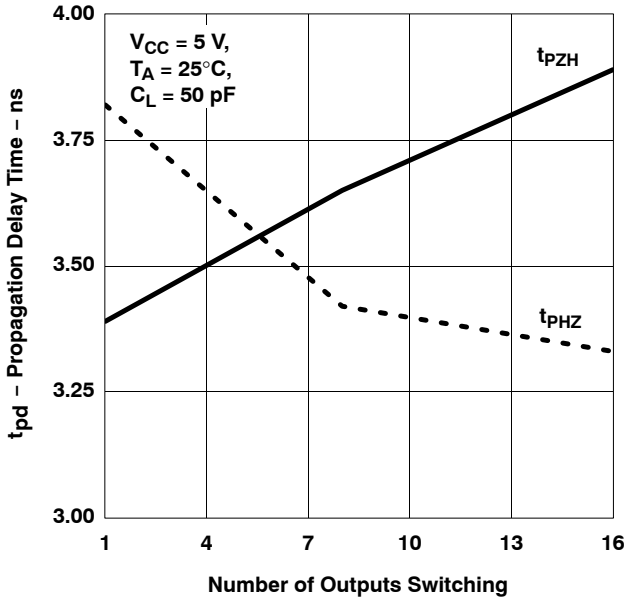


Propagation Delay Time vs Number of Outputs Switching

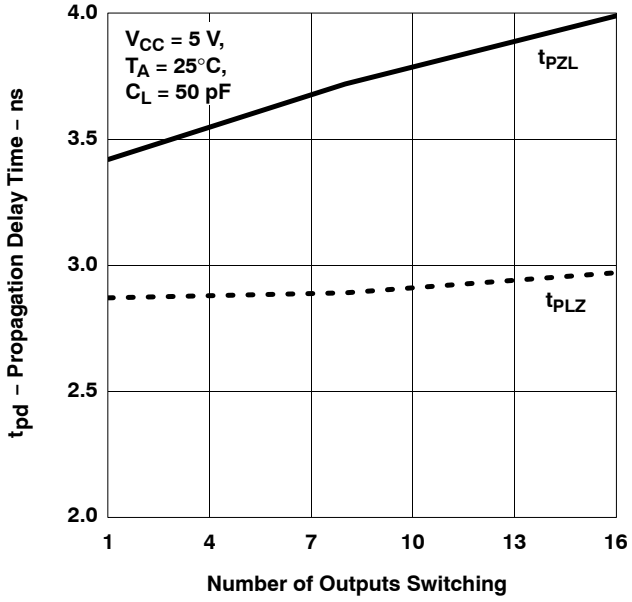
**PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A TO Y**



**PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
$\overline{OE}$ TO Y**

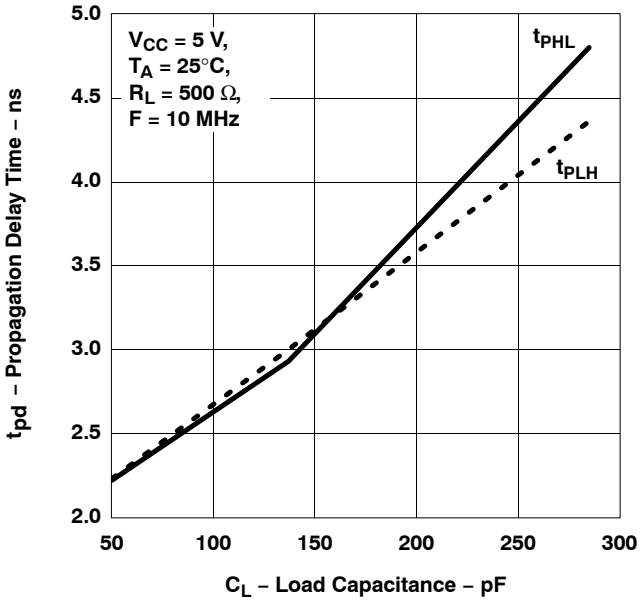


**PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
$\overline{OE}$ TO Y**

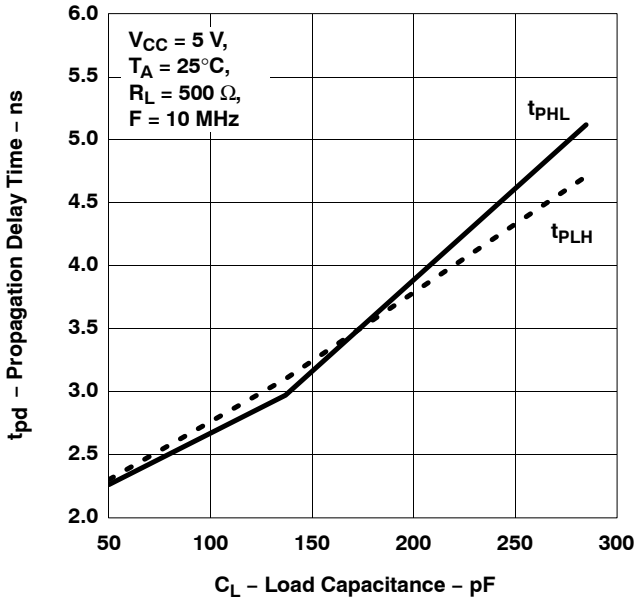


Propagation Delay Time vs Load Capacitance

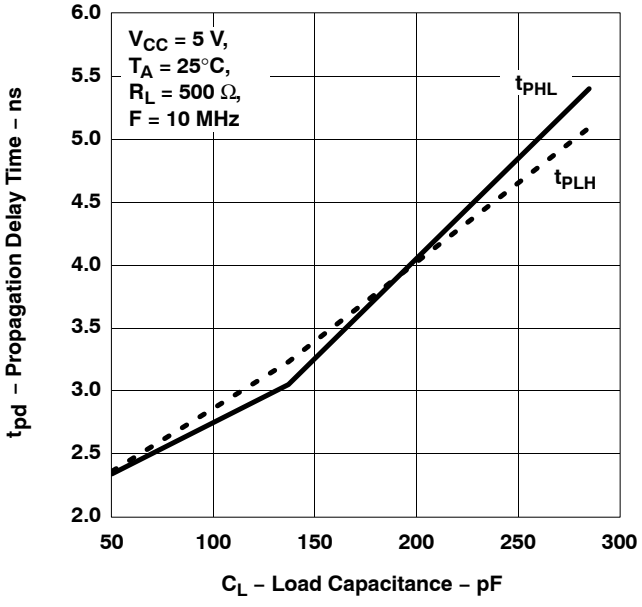
A TO Y
ONE OUTPUT SWITCHING



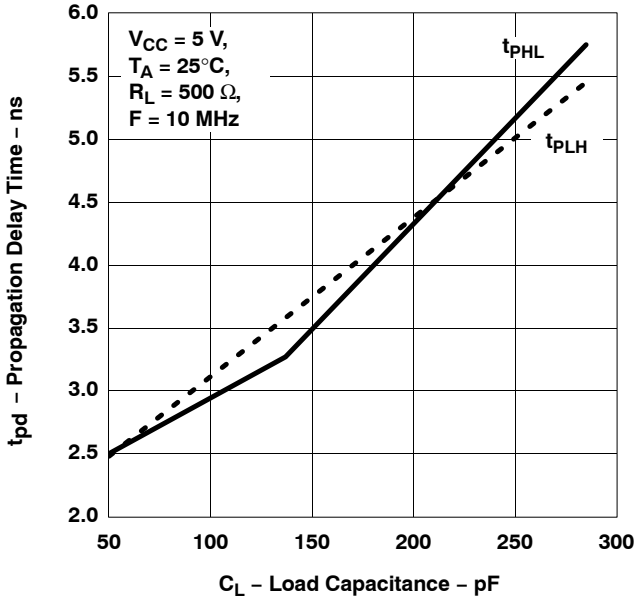
A TO Y
FOUR OUTPUTS SWITCHING



A TO Y
EIGHT OUTPUTS SWITCHING

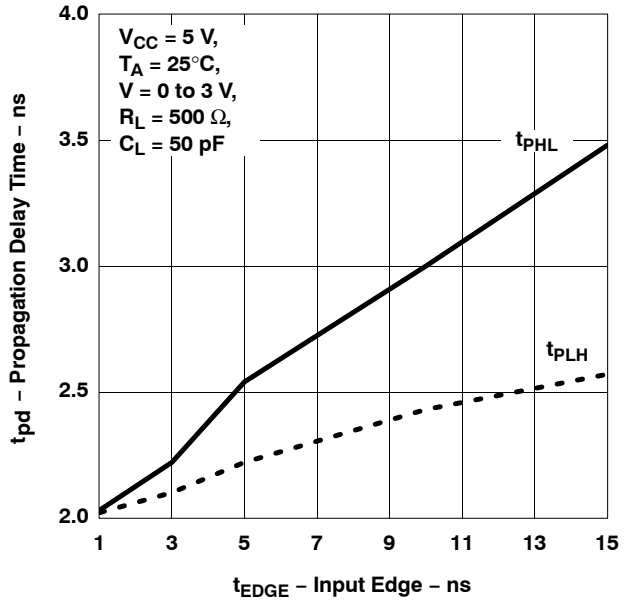


A TO Y
16 OUTPUTS SWITCHING

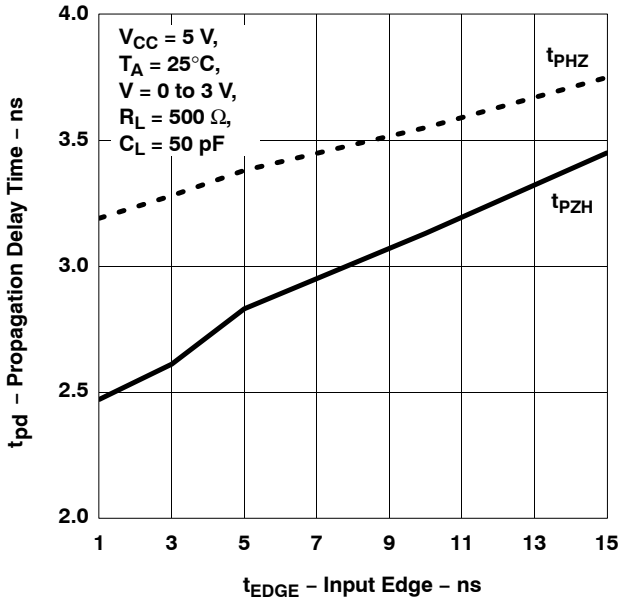


Propagation Delay Time vs Input Edge

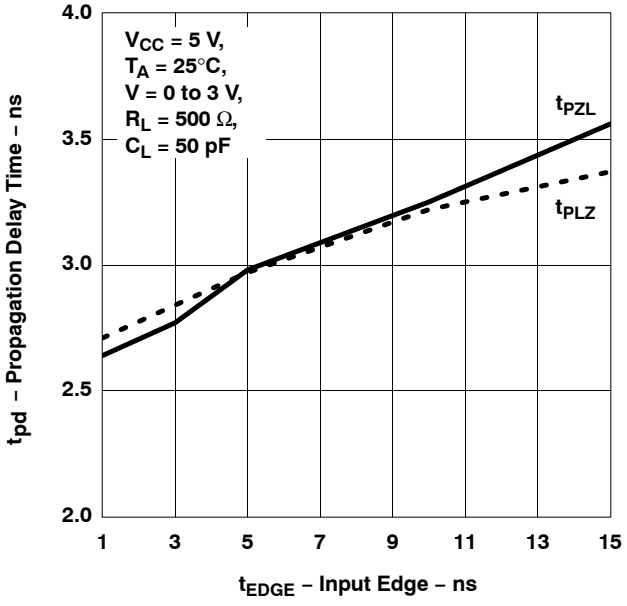
PROPAGATION DELAY TIME
vs
INPUT EDGE
A TO Y



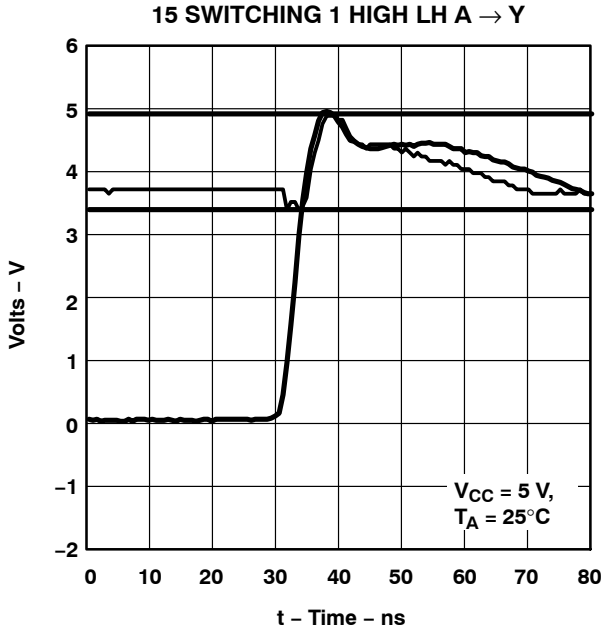
PROPAGATION DELAY TIME
vs
INPUT EDGE
$\overline{OE}$ TO Y

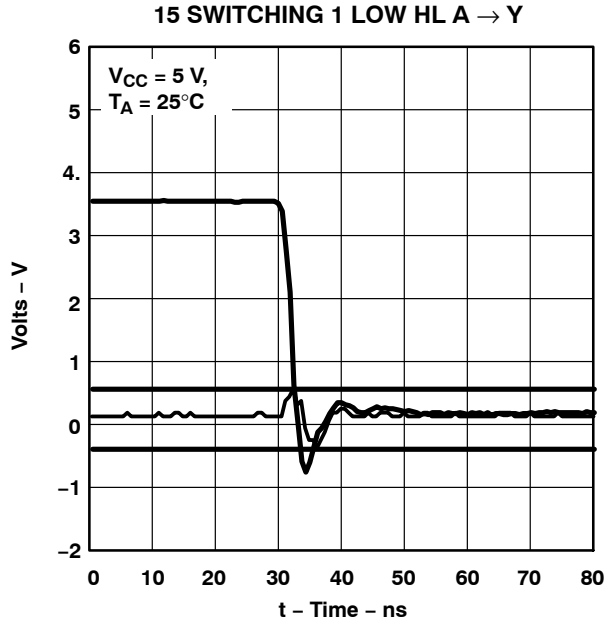


PROPAGATION DELAY TIME
vs
INPUT EDGE
$\overline{OE}$ TO Y



V_{OHV} and V_{OLP}

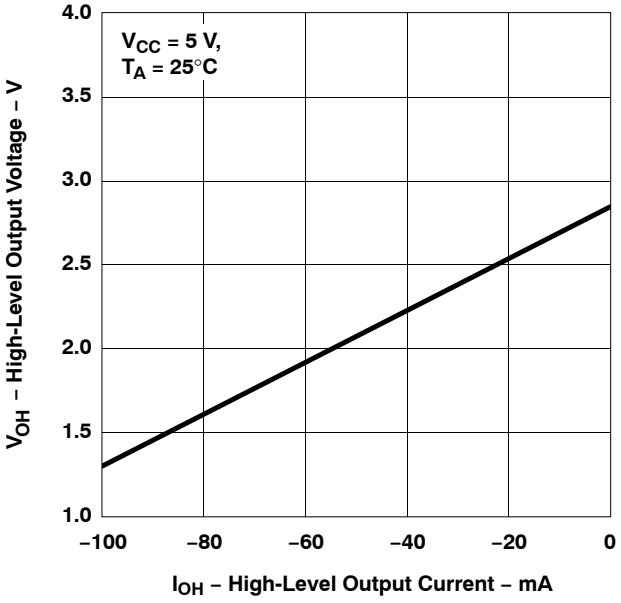




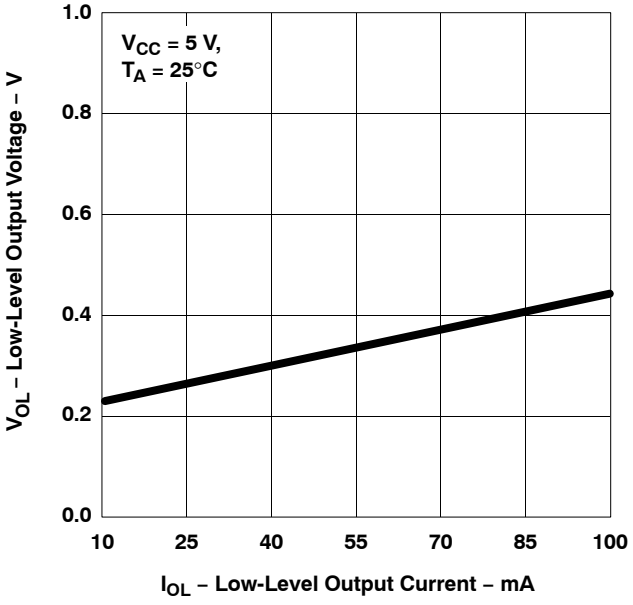
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

HIGH-LEVEL OUTPUT VOLTAGE
vs
HIGH-LEVEL OUTPUT CURRENT

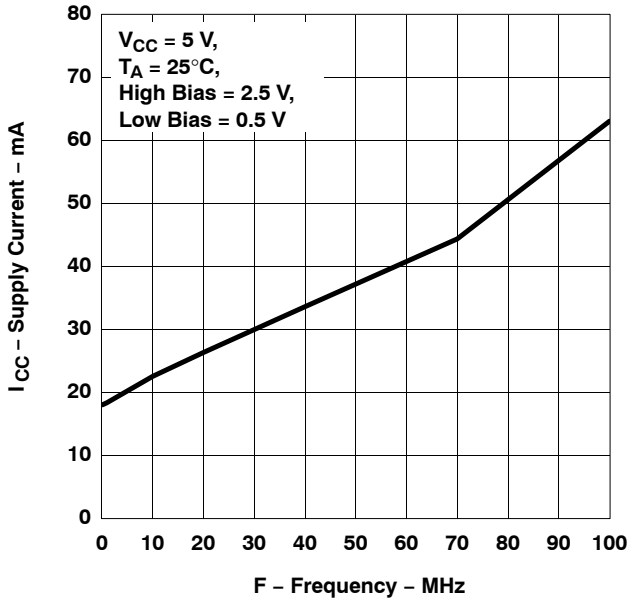


LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

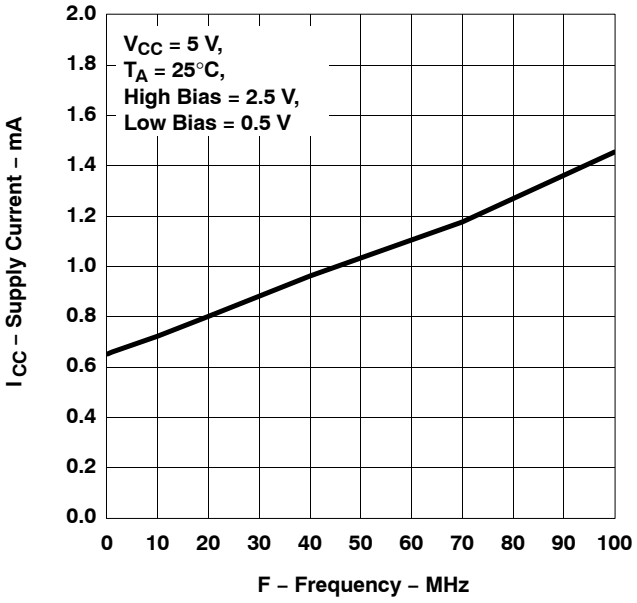


Supply Current vs Frequency

OUTPUTS ENABLED



OUTPUTS DISABLED

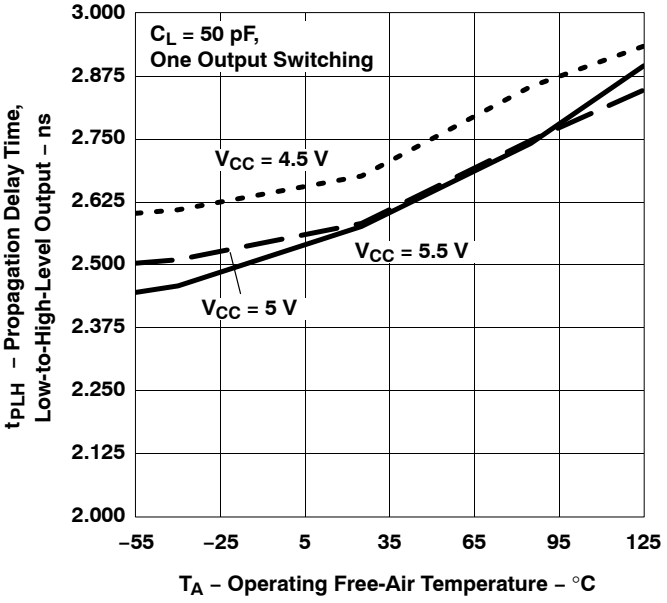


APPENDIX C
’ABT16500B Characterization Data

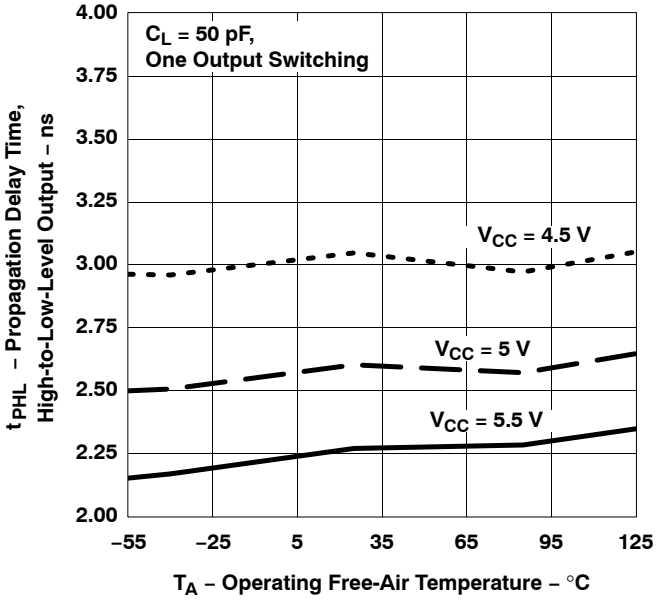
C

Propagation Delay Time vs Temperature

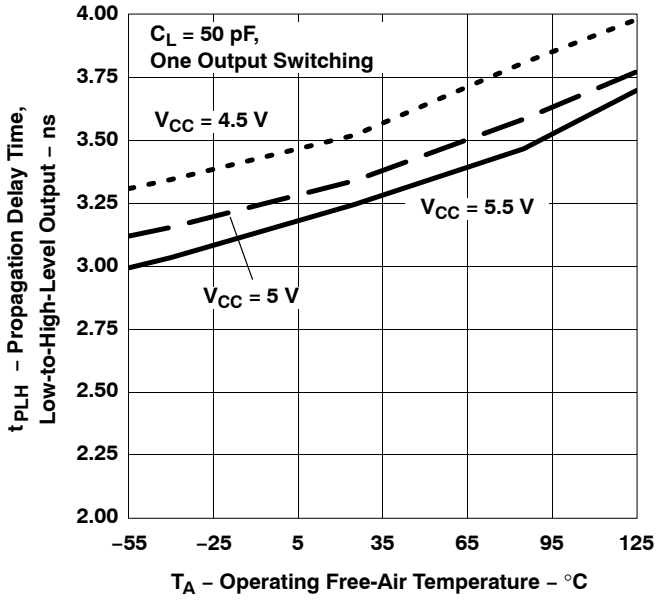
**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



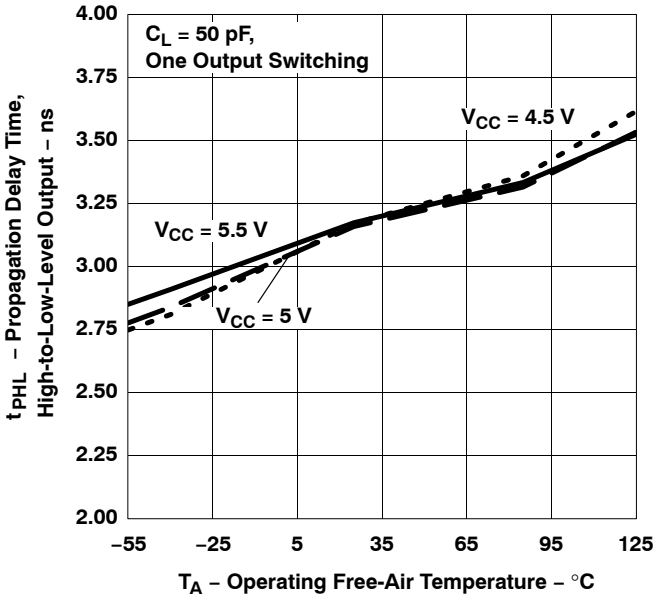
**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
A TO B**



**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
LEAB TO B**

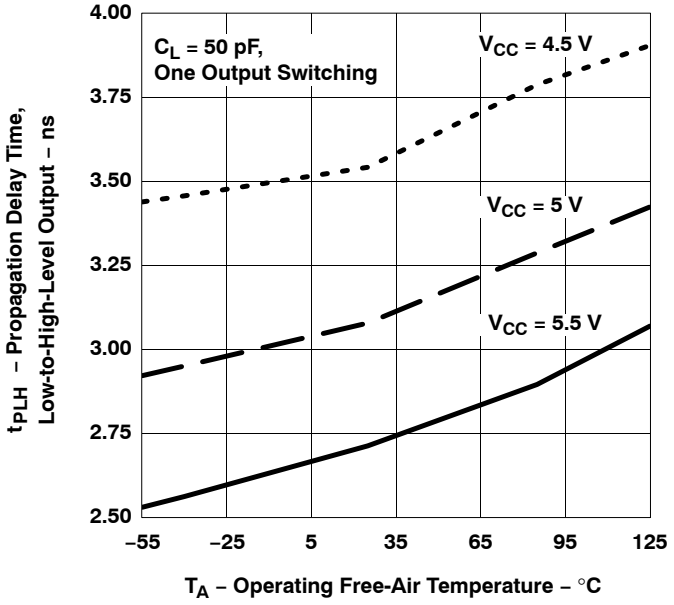


**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
LEAB TO B**

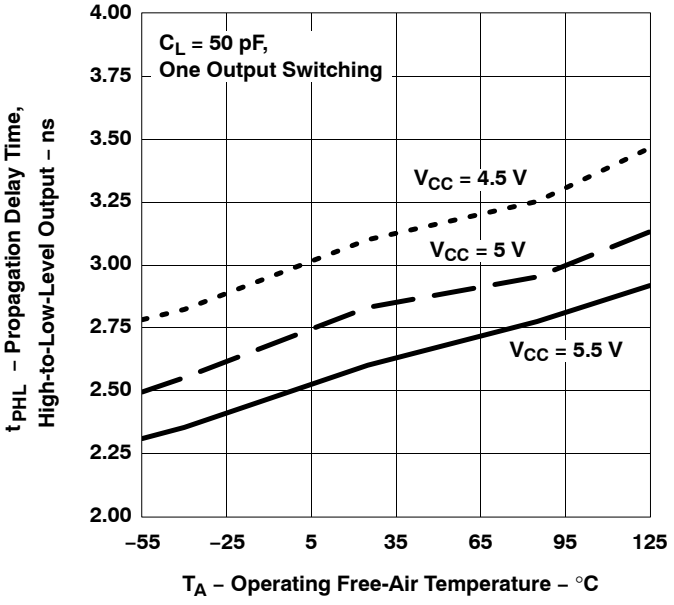


Propagation Delay Time vs Temperature

**PROPAGATION DELAY TIME
LOW-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{\text{CLKAB}}$ TO B**

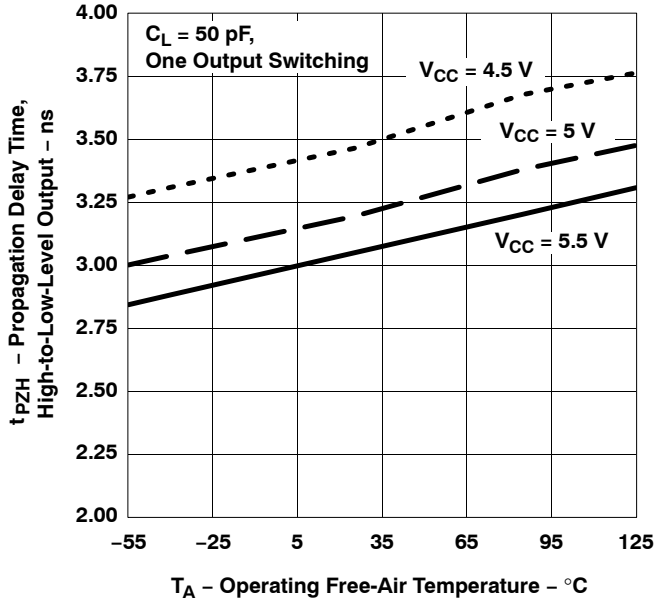


**PROPAGATION DELAY TIME
HIGH-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
$\overline{\text{CLKAB}}$ TO B**

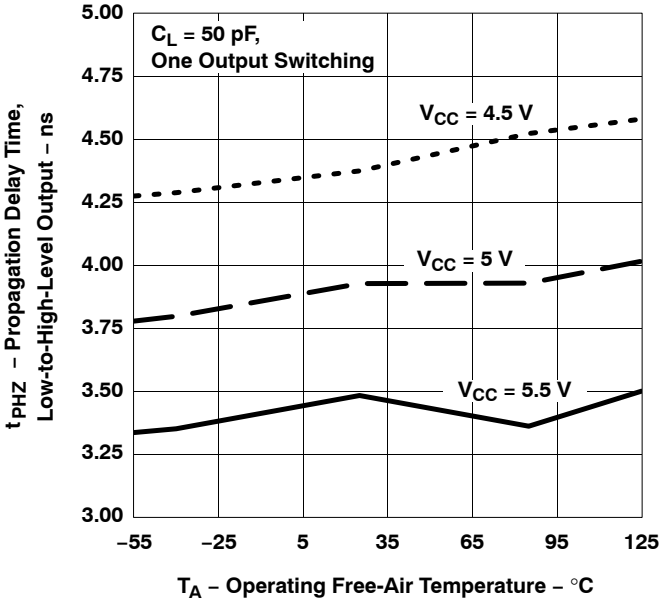


Propagation Delay Time vs Temperature

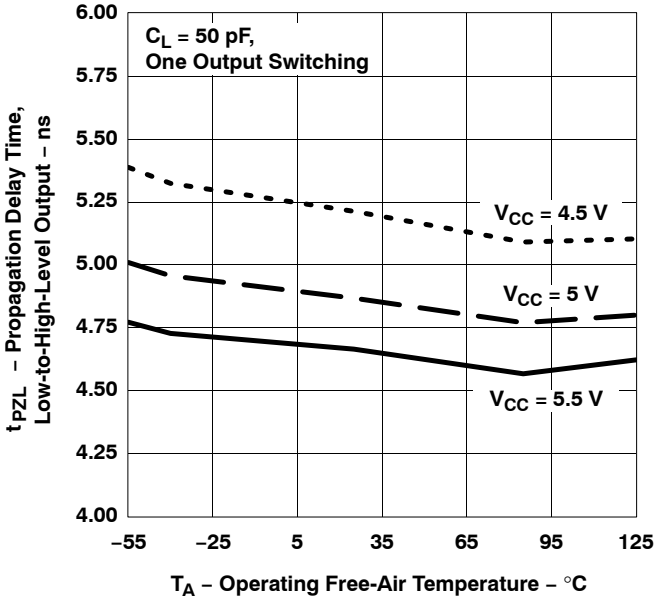
**PROPAGATION DELAY TIME
ENABLE-TO-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**



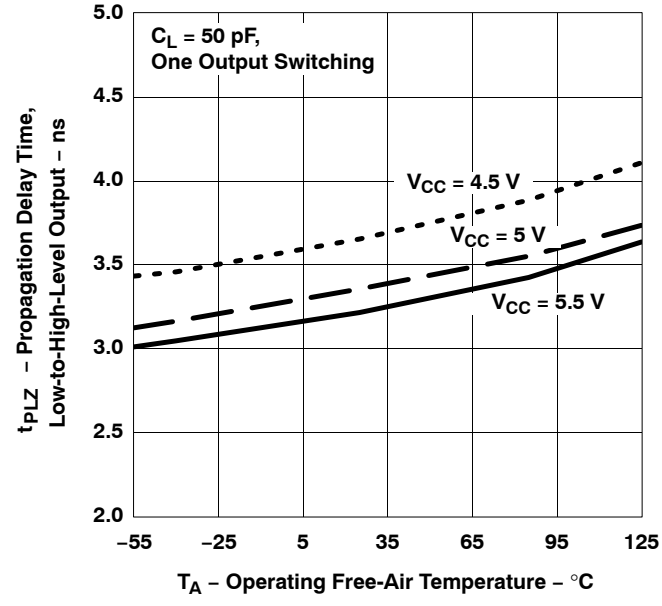
**PROPAGATION DELAY TIME
DISABLE-FROM-HIGH-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**



**PROPAGATION DELAY TIME
ENABLE-TO-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**

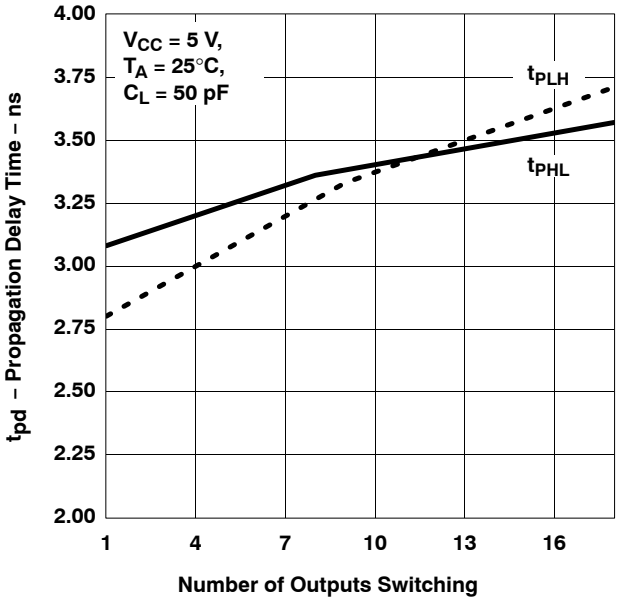


**PROPAGATION DELAY TIME
DISABLE-FROM-LOW-LEVEL OUTPUT
vs
OPERATING FREE-AIR TEMPERATURE
OEAB TO B**

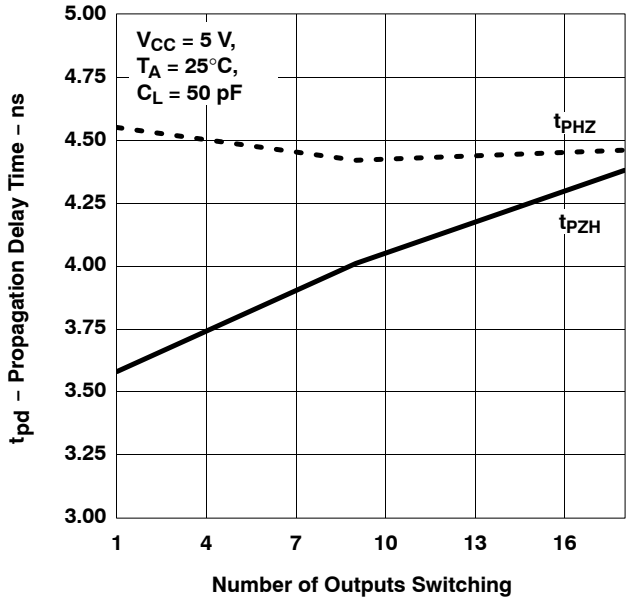


Propagation Delay Time vs Number of Outputs Switching

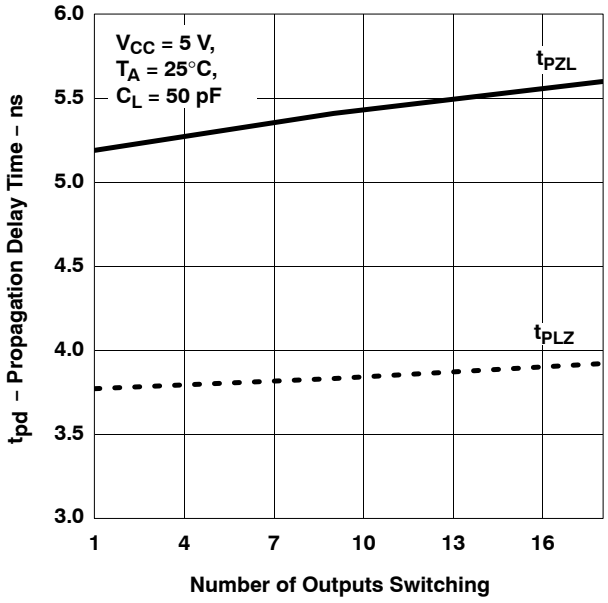
**PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
A TO B**



**PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
OEAB TO B**

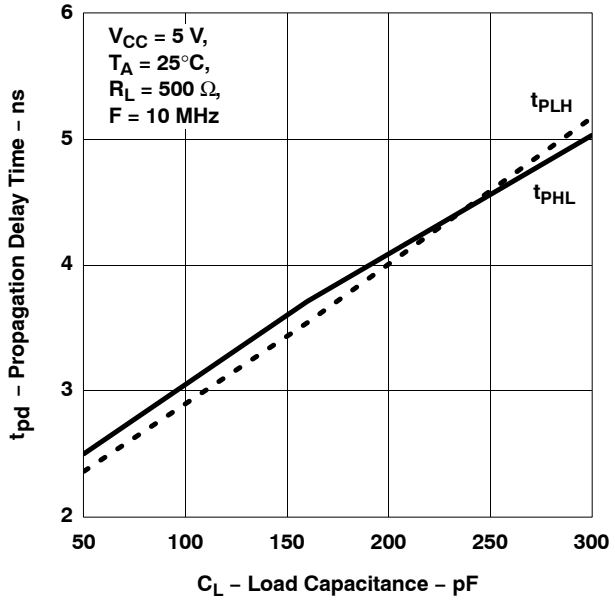


**PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING
OEAB TO B**

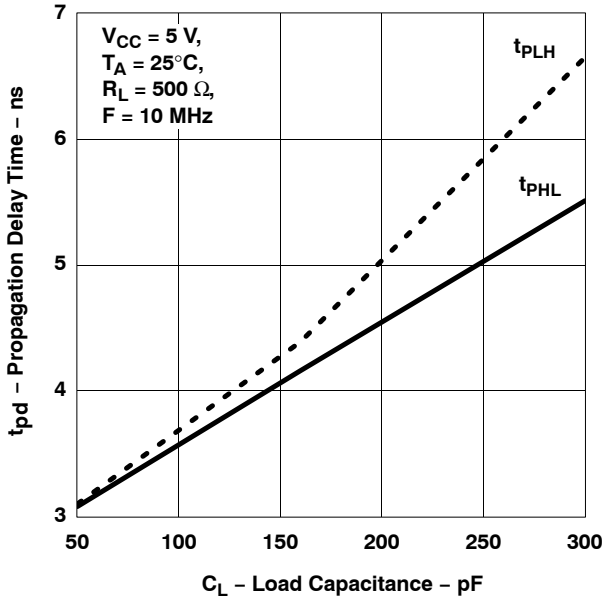


Propagation Delay Time vs Load Capacitance

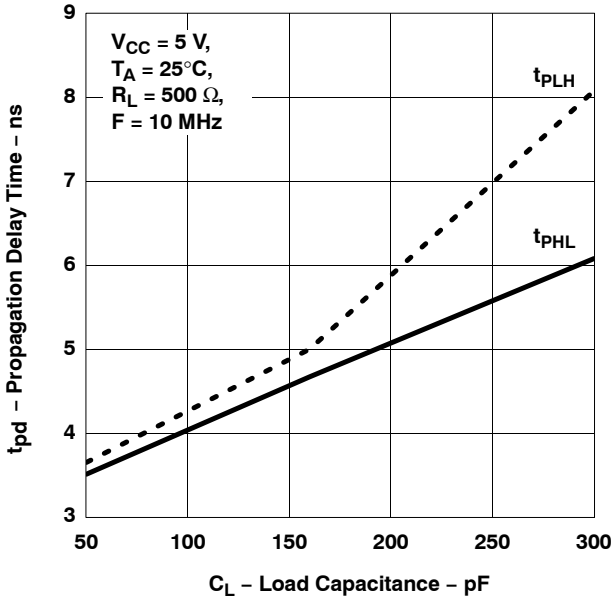
A TO B
ONE OUTPUT SWITCHING



A TO B
NINE OUTPUTS SWITCHING

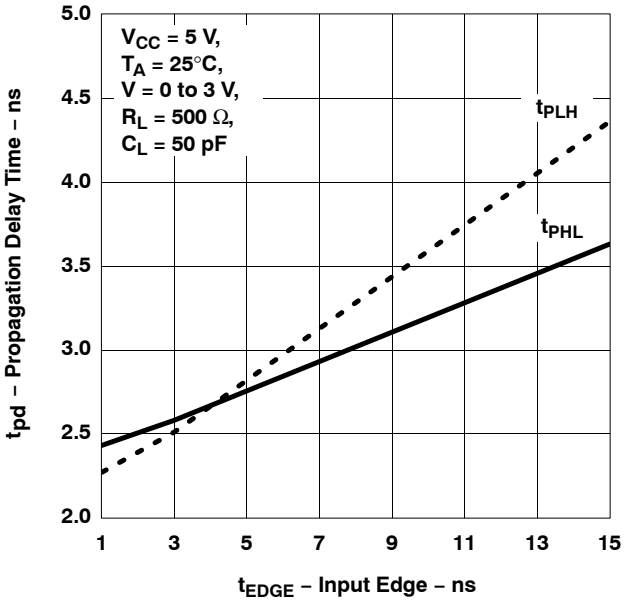


A TO B
18 OUTPUTS SWITCHING

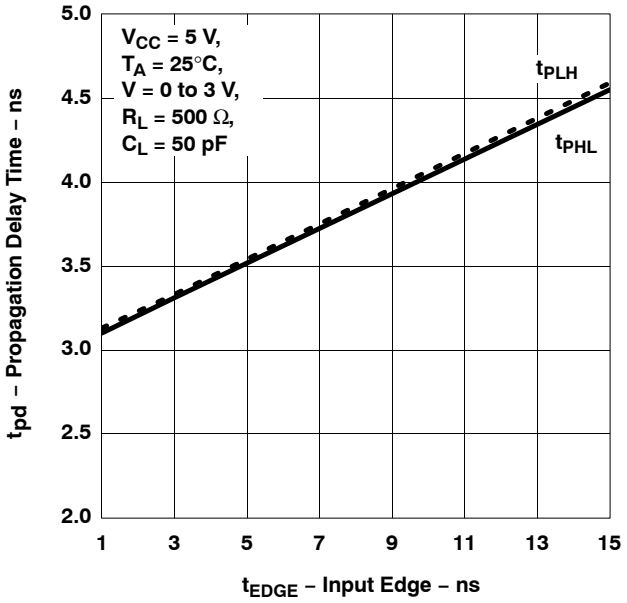


Propagation Delay Time vs Input Edge

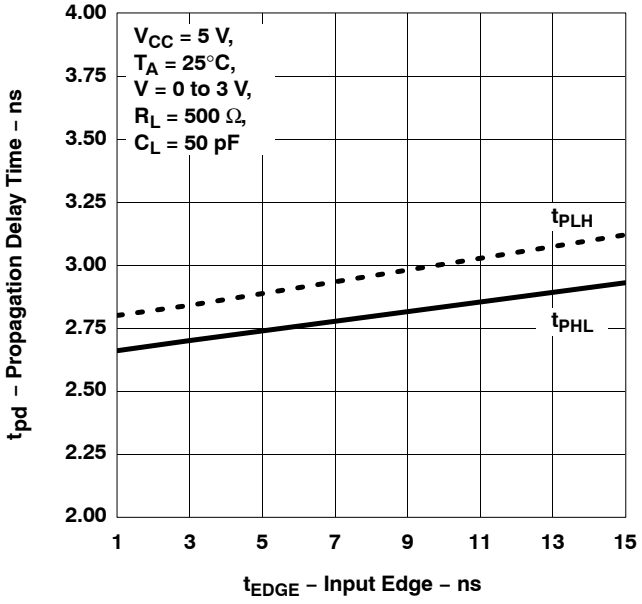
PROPAGATION DELAY TIME vs INPUT EDGE A TO B



PROPAGATION DELAY TIME vs INPUT EDGE LEAB TO B

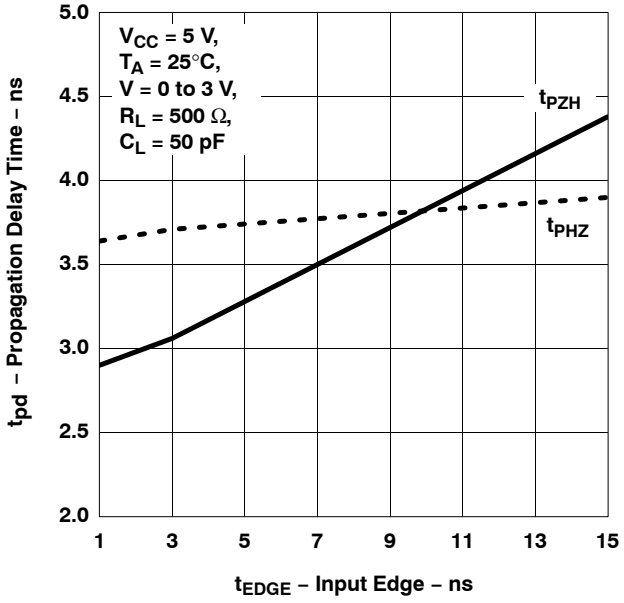


PROPAGATION DELAY TIME vs INPUT EDGE CLKAB TO B

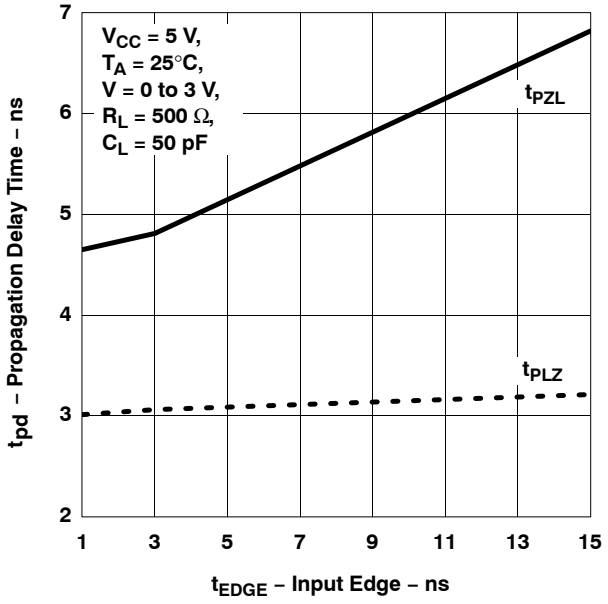


Propagation Delay Time vs Input Edge

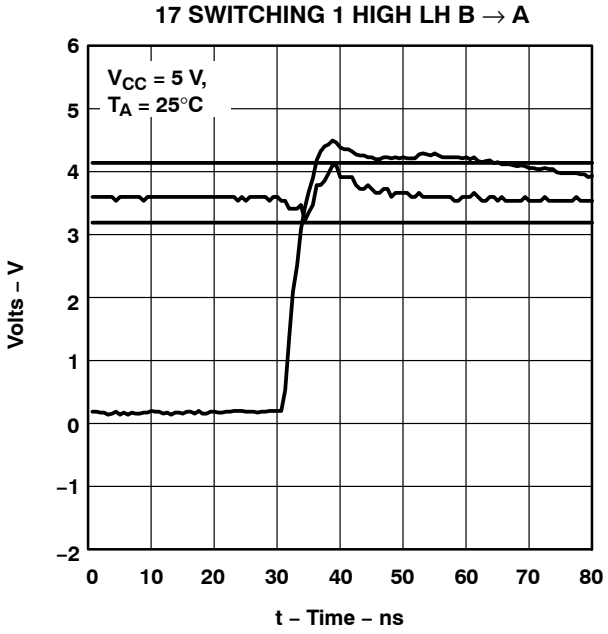
PROPAGATION DELAY TIME
vs
INPUT EDGE
OEAB TO B

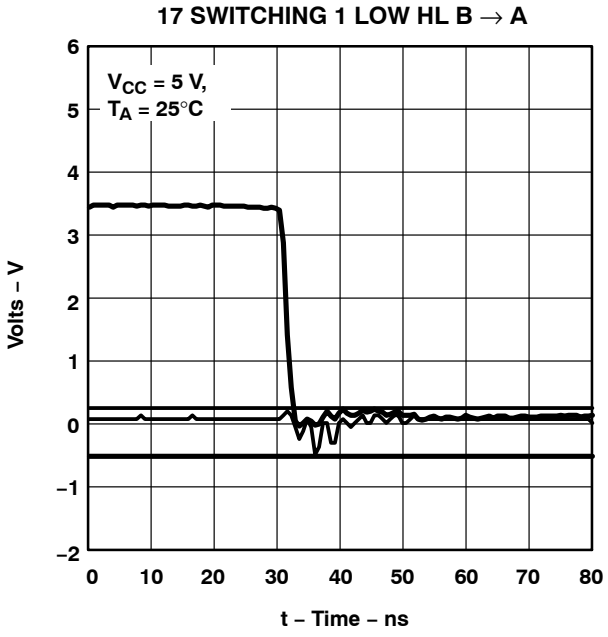


PROPAGATION DELAY TIME
vs
INPUT EDGE
OEAB TO B



V_{OHV} and V_{OLP}

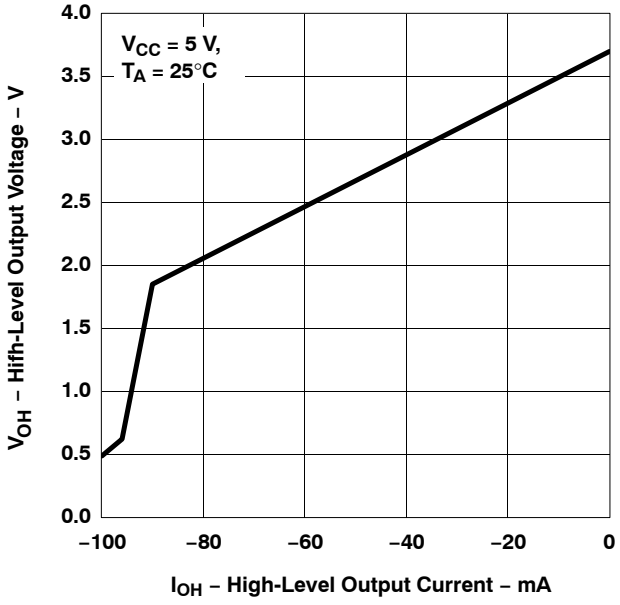




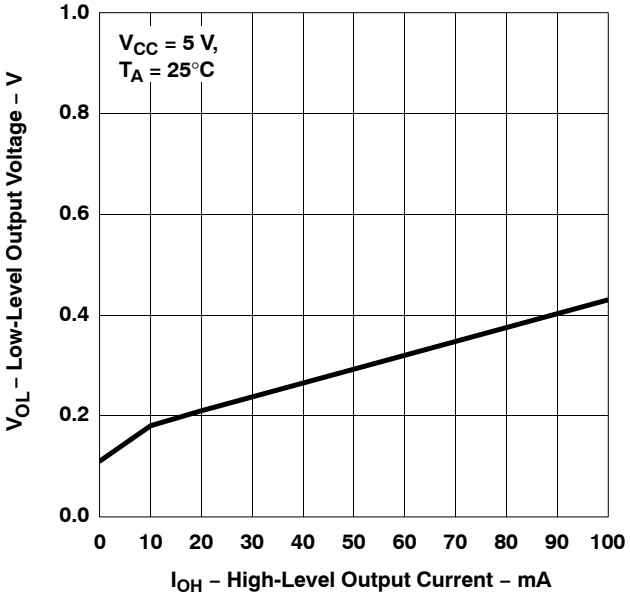
V_{OHV} = Minimum (valley) voltage induced on a quiescent high-level output during switching of other outputs.
V_{OLP} = Maximum (peak) voltage induced on a quiescent low-level output during switching of other outputs.

Typical Characteristics

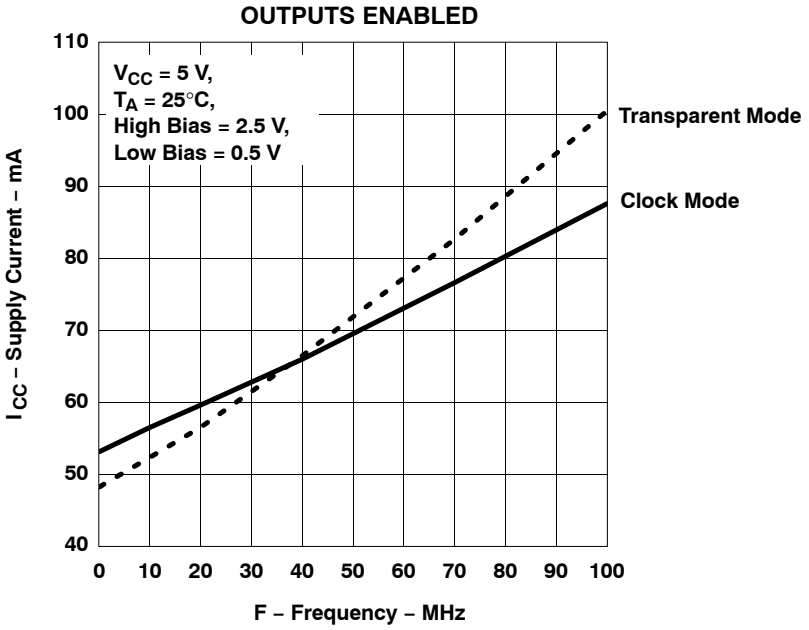
HIGH-LEVEL OUTPUT VOLTAGE vs HIGH-LEVEL OUTPUT CURRENT



LOW-LEVEL OUTPUT VOLTAGE vs LOW-LEVEL OUTPUT CURRENT

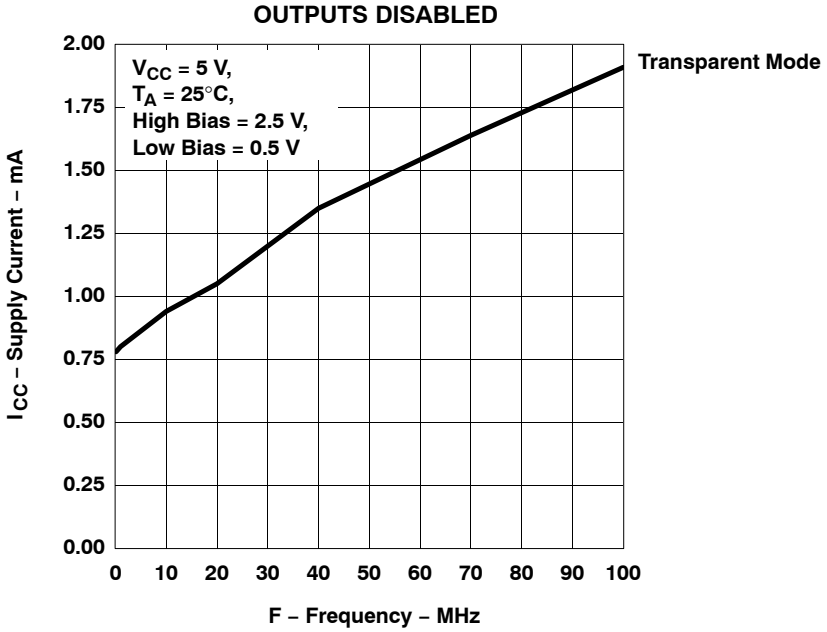


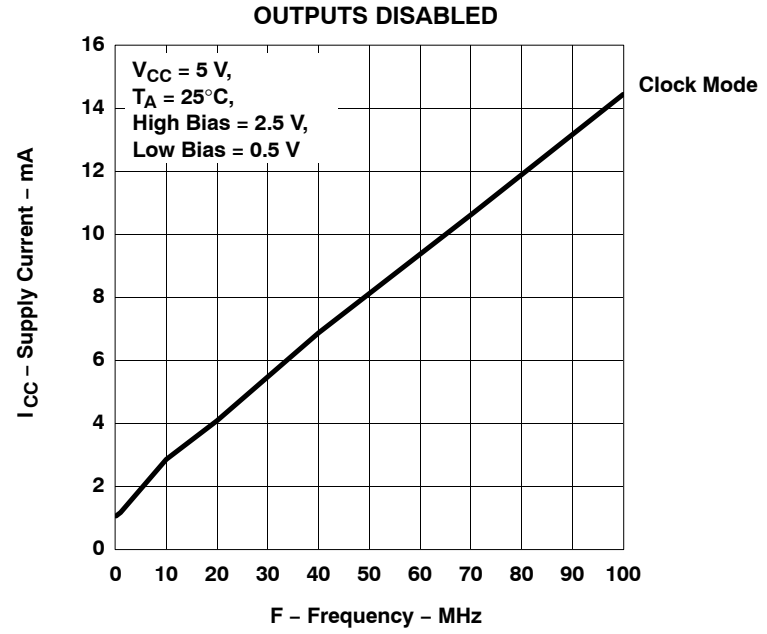
Supply Current vs Frequency



NOTE: Characteristics for latch mode are similar to those when in clock mode.

Supply Current vs Frequency





NOTE: Characteristics for latch mode are similar to those when in clock mode.

Advanced High-Speed CMOS (AHC) Logic Family

SCAA034B
January 1998

TEXAS INSTRUMENTS

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Introduction

The Texas Instruments (TI™) advanced high-speed CMOS (AHC) logic family provides a natural migration for high-speed CMOS (HCMOS) users who need more speed for low-power, and low-drive applications. Unlike many other advanced logic families, AHC does not have the drawbacks that come with higher speed, e.g., higher signal noise and power consumption. The AHC logic family consists of gates, medium-scale integrated circuits, and octal functions fabricated using the EPIC™ process that features higher performance than the HCMOS HC product family at comparable cost.

This application report introduces the AHC logic family characterization information to supplement the AHC/AHCT Logic Advanced High-Speed CMOS Data Book, literature number SCLD003A. The additional information is to aid design engineers in more accurately designing their digital logic systems. The focus is on the family's features and benefits, product characteristics, and design guidelines. This application report is divided into sections, each dealing with a specific characteristic of the AHC logic family. This application report focuses on the AHC logic family and compares it to the HC family.

The main topics discussed are:

- High-Speed CMOS (HC)
- Advanced High-Speed CMOS (AHC)
- Protection Circuitry
- AC Performance
- Power Considerations
- Input Characteristics
- Output Characteristics
- Signal Integrity
- AHC Versus HC
- Advanced Packaging
- Microgate Logic

For more information on TI's AHC logic products, please contact your local TI field sales office or an authorized distributor, or call TI at 1-800-336-5236.

High-Speed CMOS (HC)

HC has the following characteristics:

- The HC family covers a wide range of applications: low power drain for low-speed systems, and a slightly higher drain for higher-speed systems.
- The HC family has ac parameters ensured at supply voltages of 2 V, 4.5 V, and 6 V over the full operating temperature range into a 50-pF load. The TTL compatible version, HCT, is specified for a 4.5-V to 5.5-V V_{CC} range.
- In HC, only the gates that are switching contribute to the dynamic system power. This reduces the size of the power supply required, thus providing lower system cost and higher reliability through lower heat dissipation.
- HC devices are ideal for battery-operated systems, or systems requiring battery backup because there is virtually no static power dissipation.
- Improved noise immunity is due to the rail-to-rail (V_{CC}-to-ground) output voltage swings.
- HC devices are warranted for operation over an extended temperature range of −40°C to 85°C.

Advanced High-Speed CMOS (AHC)

AHC can be used for higher-speed applications. Some advantages of using AHC over HC are:

- The AHC logic family is almost three times faster than the HC family. The AHC logic family has a typical propagation delay of about 5.2 ns.
- The AHC logic family allows designers to combine the low-noise characteristics of HCMOS devices with today's performance levels without the overshoot/undershoot problems typical of higher-drive devices.
- The AHC family has lower power consumption than the HC family.
- The output drive is ±8 mA at 5-V V_{CC} and ±4 mA at 3.3-V V_{CC}.
- AHC devices are available in D and DW (SOIC), DB (SSOP), N (PDIP), PW (TSSOP), and DGV (TVSOP) packages. Selected AHC devices are available in military versions (SN54AHCxx).
- Microgate Logic (single-gate) versions that simplify routing are also available.

Protection Circuitry

Electrostatic discharge (ESD) and latchup are two traditional causes of CMOS device failure. To protect AHC devices from ESD and latchup, additional circuitry has been implemented at the inputs and outputs of each device.

Electrostatic Discharge

ESD occurs when a buildup of static charges on one surface arcs through a dielectric to another surface that has the opposite charge. The end effect is the ESD causes a short between the two surfaces. These damaged devices might pass normal data sheet tests, but eventually fail. The input and output protection circuitry designed by TI provides immunity to over 2000 V in the human-body-model test, over 200 V in the machine-model test, and over 1000 V in the charged-device model test.

Figure 1 shows the circuitry implemented to provide protection for the input gates against ESD. The primary protection device is a low-voltage-triggered silicon-controlled rectifier (LVTSCR). During an ESD event, most of the current is diverted through the LVTSCR. Additional protection is provided by the resistor and secondary clamp transistors, which break down during an ESD event and protect the gate oxides.

Figure 2 shows how the LVTSCR protects an output.

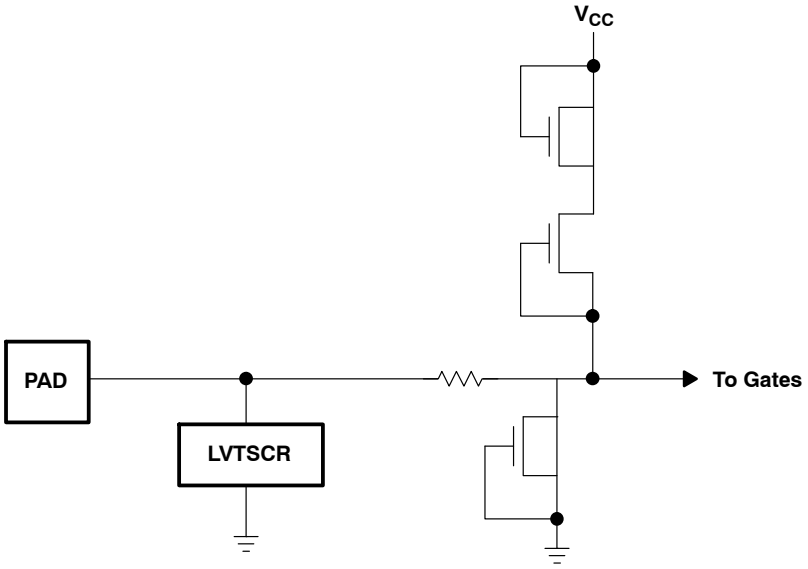

Figure 1. ESD Input Protection Circuitry

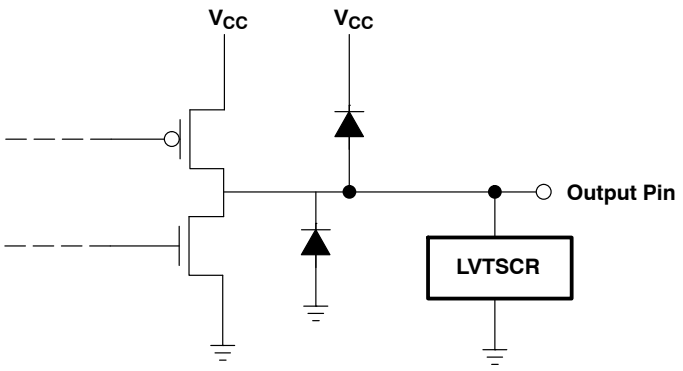

Figure 2. ESD Output Protection Circuitry

Latchup Protection

Internal to almost all CMOS devices are two parasitic bipolar transistors; one p-n-p and one n-p-n. Figure 3 shows the cross section of a typical CMOS inverter with the parasitic bipolar transistors. As shown in Figure 4, these parasitic bipolar transistors are naturally configured as a thyristor or a silicon-controlled rectifier (SCR). These transistors conduct when one or more of the p-n junctions become forward biased. When this happens, each parasitic transistor supplies the necessary base current for the other to remain in saturation. This is known as the latchup condition and could destroy the device if the supply current is not limited.

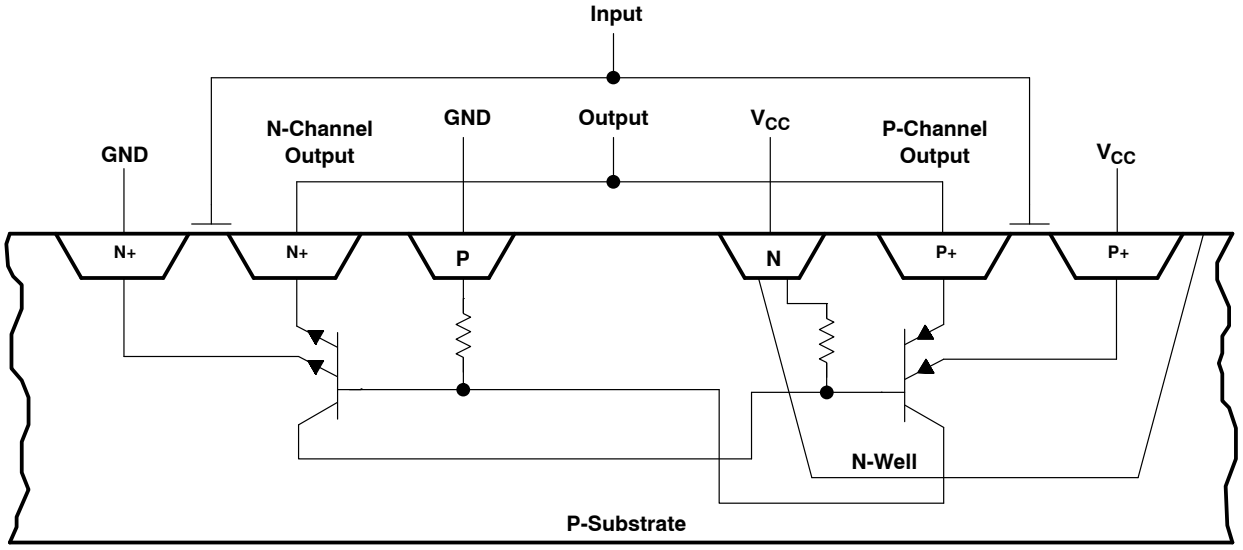

Figure 3. Parasitic Bipolar Transistors in CMOS

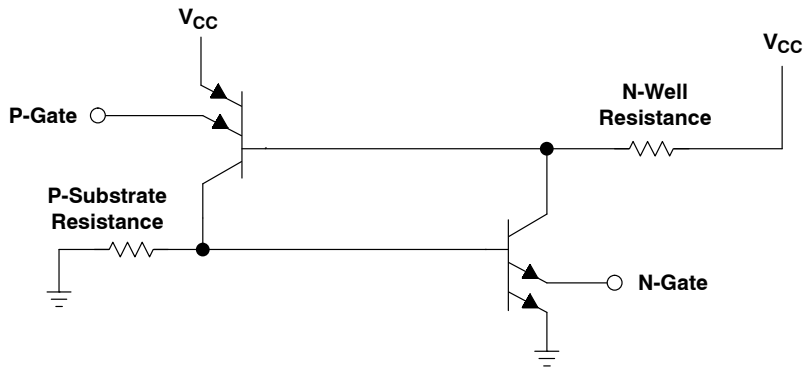

Figure 4. Schematic of Parasitic SCR Showing P-Gate and N-Gate Electrodes Connected

A conventional thyristor is fired (turned on) by applying a voltage to the base of the n-p-n transistor, but the parasitic CMOS thyristor is fired by applying a voltage to the emitter of either transistor. One emitter of the p-n-p transistor is connected to an emitter of the n-p-n transistor, which is also the output of the CMOS gate. The other two emitters of the p-n-p and the n-p-n transistors are connected to V_{CC} and ground, respectively. Therefore, to trigger the thyristor there must be a voltage greater than V_{CC} + 0.5 V or less than −0.5 V and there has to be sufficient current to cause the latchup condition.

Latchup cannot be completely eliminated. The alternative is to prevent the thyristor from triggering. TI has improved the circuit design by adding an additional diffusion or guard ring. The guard ring provides isolation between the device pins and any p-n junction that is not isolated by any transistor gate.

Switching Characteristics

The switching characteristics of the AHC are similar to those of the AHCT in terms of the operating conditions and limits, except for the AHCT input TTL compatibility. Table 1 gives the performance figures for the HC/HCT and the AHC/AHCT logic parts. Individual data sheets provide parameter values for the AHC and the AHCT devices for different values of operating free-air temperature, number of outputs switching, and load capacitance.

Table 1. HC and AHC Performance Comparison (Typical Values)

DEVICE	SN74HC	SN74HCT	SN74AHC	SN74AHCT
244 buffer	13 ns	15 ns	5.8 ns	5.4 ns
245 transceiver	15 ns	14 ns	5.8 ns	4.5 ns
373 latch	15 ns	20 ns	5 ns	5 ns
374 flip-flop	17 ns	25 ns	5.4 ns	5 ns

AHC is almost three times faster than HC.

Power Considerations

The power dissipation of CMOS devices can be divided into three components:

- Quiescent power dissipation, P_q
- Transient power dissipation, P_t
- Capacitive power dissipation, P_c

The quiescent power is the product of V_{CC} and the quiescent current, I_{CC}. The quiescent current is the reverse current through the diodes that are reverse biased. This reverse current is generally very small (a few nA), which makes the quiescent power insignificant. However, for circuits that are in static condition for long periods, the quiescent power must be considered.

The transient power is due to the current that flows only when the transistors are switching from one logic level to the other. During this time, both of the transistors are partially on, which produces a low-impedance path between V_{CC} and ground that results in a current spike. The rise (or fall) time of the input signal has a direct effect on the duration of the current spike. This is because the faster the input signal passes through the transition region, the less time both transistors are partially on. The transient power is dependent on the characteristics of the transistors, the switching frequency, and the rise and fall times of the input signal. The component can be calculated using the following equation:

$$P_t = C_{pd} \times V_{CC}^2 \times f_I \quad \textbf{(1)}$$

Where:

V_{CC} = Supply voltage (V)
f_I = Input frequency (Hz)
C_{pd} = Power dissipation capacitance (F)

Additional capacitive power dissipation is caused by the charging and discharging of external load capacitance and is dependent on the switching frequency. To calculate the power, the following equation can be used:

$$P_C = C_L \times V_{CC}^2 \times f_O \quad \textbf{(2)}$$

Where:

V_{CC} = Supply voltage (V)
f_O = Output frequency (Hz)
C_L = External load capacitance (F)

Power Dissipation

AHCT devices are used primarily to interface TTL output signals to CMOS inputs. To make the inputs of the AHCT devices TTL-voltage compatible, the input transistor geometries were changed. This increased the power consumption, as compared to the equivalent AHC device, if the input is kept at a level other than GND or V_{CC}. The increase in power consumption occurs because TTL input levels cause both transistors in the transistor pair to be partially turned on. Included in the tables for the AHCT devices is the parameter ΔI_{CC}, which enables the designer to compute how much additional current the AHCT device draws per input when at a TTL-voltage level.

Figure 5 shows the relation between the supply current and the frequency of operation for the AHC245 and the AHCT245. The increase in power consumption for the AHCT is relatively insignificant.

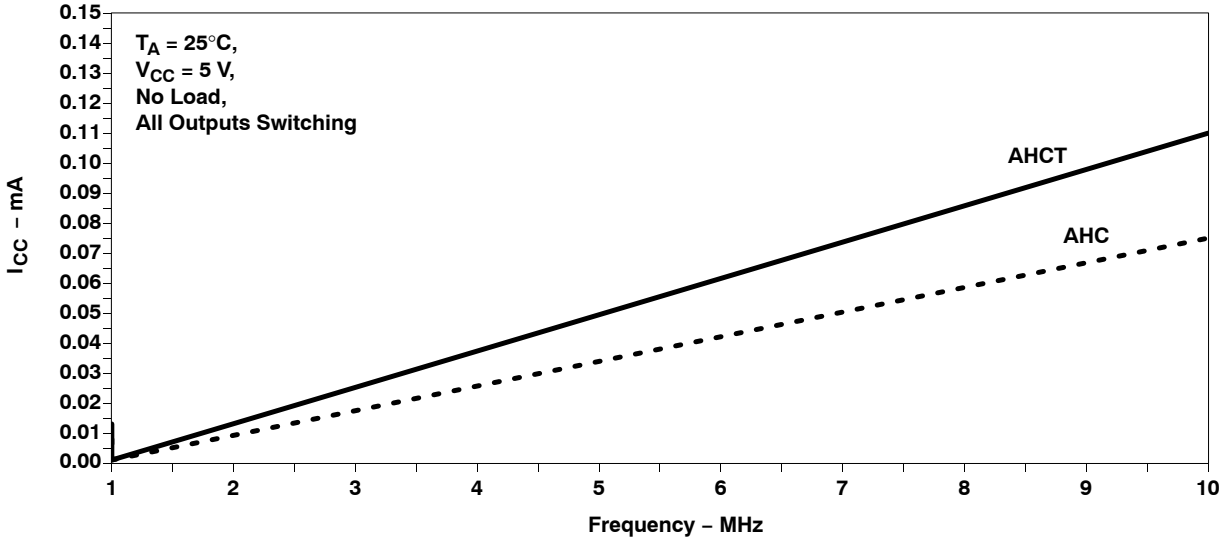

Figure 5. I_{CC} Versus Frequency

Input Characteristics

The AHC logic family input structure is such that the 5-V CMOS dc V_{IL} and V_{IH} fixed levels of 1.5 V and 3.5 V are ensured, meaning that, while the threshold voltage of 2.5 V is typically where the transition from a recognized low input to a recognized high input occurs, it is at 1.5 V and 3.5 V that the corresponding output levels are specified. For AHCT, V_{IL} and V_{IH} fixed levels of 0.8 V and 2 V are ensured, and the threshold voltage is 1.5 V. Figure 6 shows the characteristics for the AHC245 and the AHCT245.

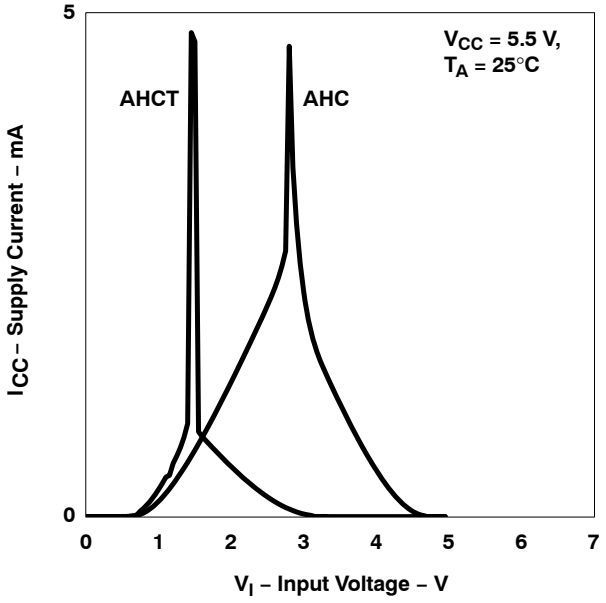

Figure 6. Supply Current Versus Input Voltage

AHC Input Circuitry

The simplified AHC input circuit shown in Figure 7 consists of two transistors, sized to achieve a threshold voltage of 2.5 V. Since V_{CC} is 5 V and the threshold voltage is commonly set to be centered around one-half of V_{CC} in a pure CMOS input, additional circuitry to reduce the voltage level is not required and the resulting simplified input structure consists of two transistors. When the input voltage V_I is low, the PMOS transistor (Q_p) turns on and the NMOS transistor (Q_n) turns off, causing current to flow through Q_p, resulting in the output voltage (of the input stage) to be pulled high. Conversely, when V_I is high, Q_n turns on and Q_p turns off, causing current to flow through Q_n, resulting in the output voltage (on the input stage) to be pulled low.

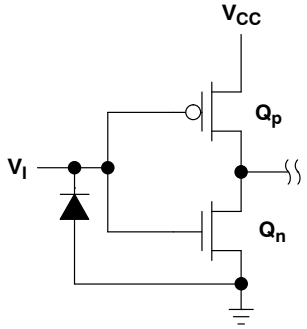

Figure 7. Simplified Input Stage of an AHC Circuit

Figures 8 and 9 show the graphs of V_O versus V_I for the AHC04 and the AHCT04. The recommended operating range for the AHC family is from 2 V to 5.5 V. For the AHCT the recommended range is from 4.5 V to 5.5 V. Input hysteresis of typically 150 mV is included in AHC devices (300 mV in AHCT devices), which ensures the devices are free from oscillations by increasing the noise margin around the threshold voltage during low-input transitions.

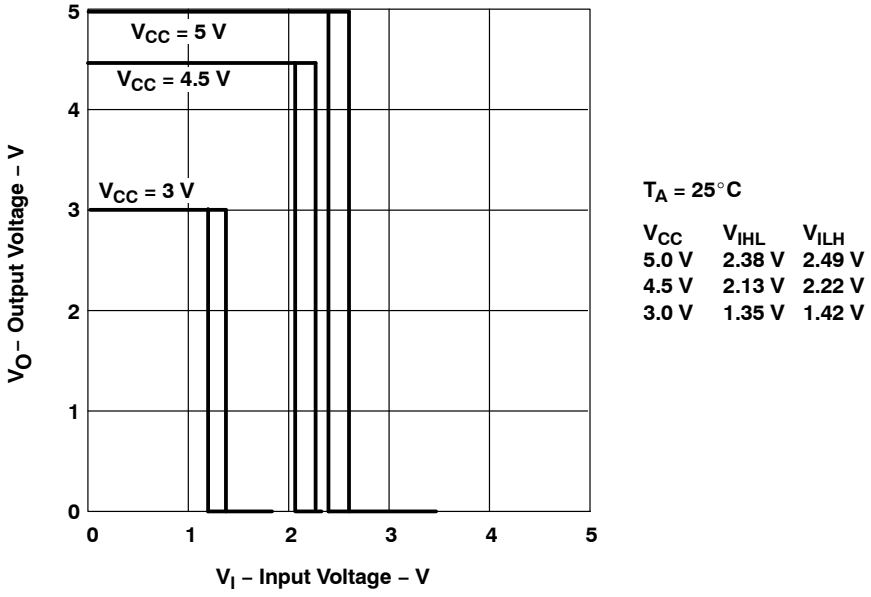

Figure 8. Output Voltage Versus Input Voltage (AHC04)

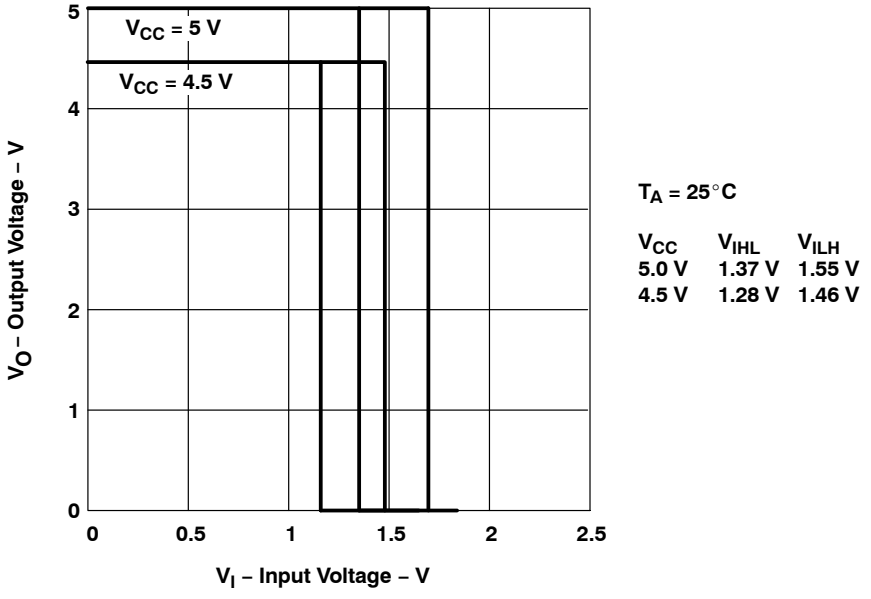

Figure 9. Output Voltage Versus Input Voltage (AHCT04)

Input Current Loading

Minimal loading of the system bus occurs when using the AHC family due to the EPIC process CMOS input structure; the only loading that occurs is caused by leakage current and capacitance. Input current is low, typically less than 1 μA (see Table 2). Capacitance for transceivers can be as low as 2.5 pF for C_i and 4 pF for C_{io}. Since both of the variables that can affect bus loading are relatively insignificant, the overall impact on bus loading on the input side using AHC devices is minimal and, depending on the logic family being used, bus loading can decrease as a result of using AHC parts.

Table 2. Input-Current Specification

PARAMETER	TEST CONDITIONS	SN74AHC245		UNIT
		MIN	MAX	
I_I	$V_I = V_{CC}$ or GND		±1	μA
I_{OZ}†	$V_O = V_{CC}$ or GND, $V_I = (\overline{OE}) = V_{IL}$ or V_{IH}		±2.5	μA

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

Supply Current Change (ΔI_{CC})

Because the input circuitry for AHC is CMOS, an additional specification, ΔI_{CC}, is provided to indicate the amount of input current present when both p- and n-channel transistors are conducting (see *Power Dissipation* in the application report). Although this situation exists when a low-to-high or high-to-low transition occurs, the transition usually occurs so quickly that the current flowing while both transistors are conducting is negligible. It is more of a concern, however, when a device with a TTL output drives the AHC part. Here, a dc voltage that is not at the rail is applied to the input of the AHC device. This results in both the n-channel transistor and the p-channel transistor conducting, and a path from V_{CC} to GND is established. This current is specified as ΔI_{CC} in the data sheet for each device and is measured one input at a time, with the input voltage set at V_{CC} – 0.6 V, while all other inputs are at V_{CC} or GND. Table 3 provides the ΔI_{CC} specification, which is contained in the data sheet for the SN74AHCT245.

Table 3. ΔI_{CC}-Current Specification

PARAMETER	TEST CONDITIONS	SN74AHCT245		UNIT
		MIN	MAX	
ΔI_{CC}	One input at 3.4 V, Other inputs at V_{CC} or GND, V_{CC} = 5.5 V		1.5	mA

Figure 10 is a graph of I_I versus V_I for the AHC245. An operating range from 0 V to 5.5 V is recommended.

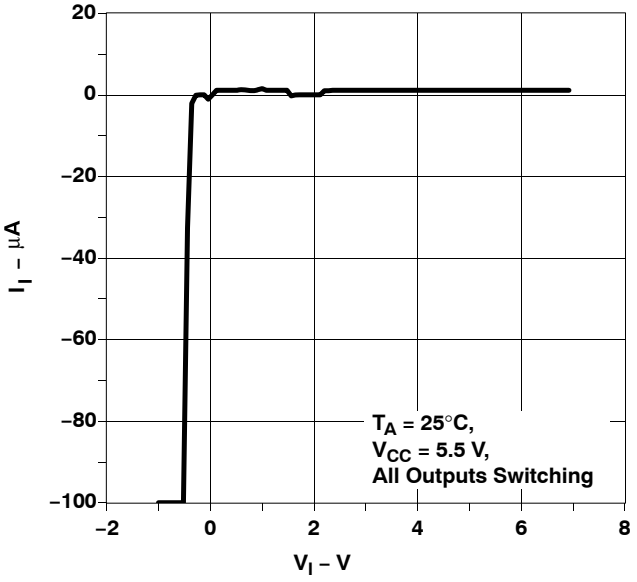

Figure 10. Input Current Versus Input Voltage (AHC245)

DC Characteristics

The AHC family uses a pure CMOS output structure. The AHC family has the dc characteristics shown in Table 4. The values are measured at $T_A = 25°C$.

Table 4. AHC DC Specifications

PARAMETER	TEST CONDITIONS		V_{CC}	SN74AHC245 $T_A = 25°C$			UNIT
				MIN	TYP	MAX	
V_{OH}	$I_{OH} = -50\ \mu A$		2 V	1.9	2		V
			3 V	2.9	3		
			4.5 V	4.4	4.5		
	$I_{OH} = -4$ mA		3 V	2.58			
	$I_{OH} = -8$ mA		4.5 V	3.94			
V_{OL}	$I_{OL} = 50\ \mu A$		2 V			0.1	V
			3 V			0.1	
			4.5 V			0.1	
	$I_{OL} = 4$ mA,		3 V			0.36	
	$I_{OL} = 8$ mA,		4.5 V			0.36	
I_I	$V_I = V_{CC}$ or GND		5.5 V			±0.1	μA
I_{OZ}†	$V_O = V_{CC}$ or GND,	V_I ($\overline{OE}$) = V_{IL} or V_{IH}	5.5 V			±0.25	μA
I_{CC}	$V_I = V_{CC}$ or GND,	$I_O = 0$	5.5 V			4	μA
C_i	$V_I = V_{CC}$ or GND		5 V		2.5		pF
C_{io}	$V_I = V_{CC}$ or GND		5 V		4		pF

† For I/O ports, the parameter I_{OZ} includes the input leakage current.

AHC/AHCT Output Circuitry

Figure 11 shows a simplified output stage of an AHC/AHCT circuit. When the NMOS transistor (Q_n) turns off and the PMOS transistor (Q_p) turns on and begins to conduct, the output voltage (V_O) is pulled high. Conversely, when Q_p turns off, Q_n begins to conduct and V_O is pulled low. The AHC/AHCT devices have a rail-to-rail output swing to make them compatible with the HC/HCT families.

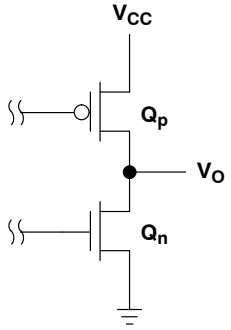

Figure 11. Simplified Output Stage of an AHC Circuit

Output Drive

Figure 12 shows values for V_{OL} vs $I_{OL,}$ and I_{OH} vs V_{OH} for the AHC/AHCT245.

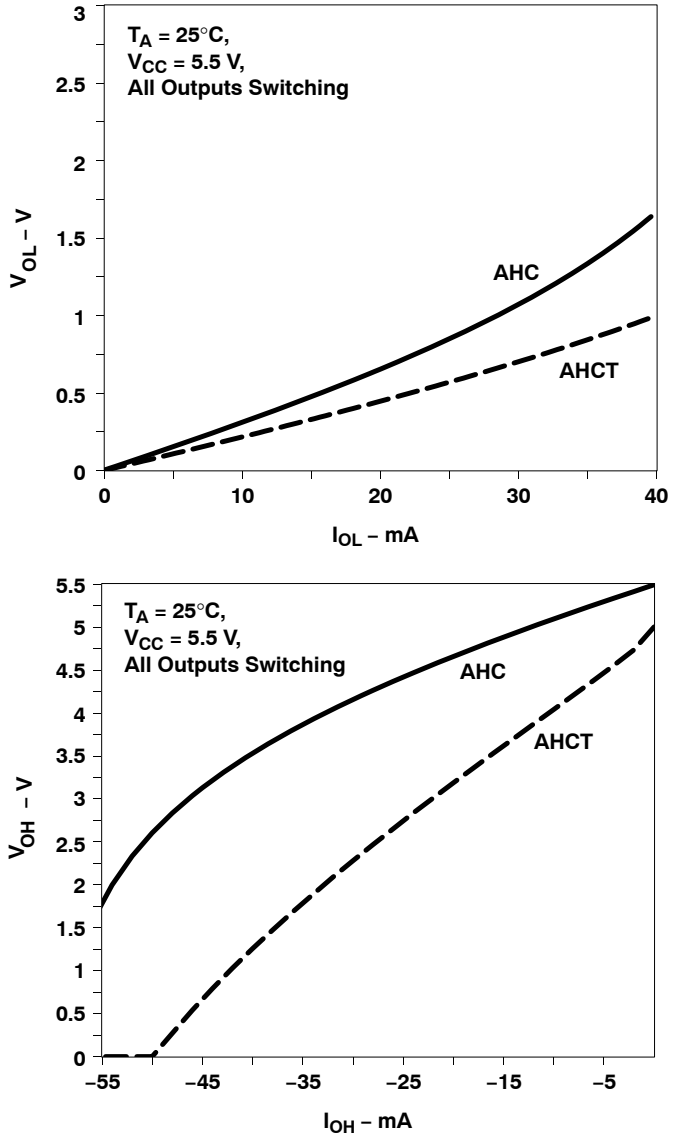

Figure 12. AHC Output Characteristics

Partial Power Down

All AHC devices are 5-V input tolerant when operated at 3.3 V. To partially power down a device, no paths from the input or output pins to V_{CC} exist. With the AHC family, there are no paths from the input pins to V_{CC}. The AHC/AHCT devices have rail-to-rail output swings to make them compatible with the HC/HCT family. The AHC/AHCT devices do not have a path from the output pins to V_{CC} and can be partially powered down.

Proper Termination of Outputs

Depending on the trace length, special consideration might need to be given to the termination of the outputs. As a general rule, if the trace length is less than four inches, no additional components are necessary to achieve proper termination. If the trace length is greater than four inches, reflections begin to appear on the line and the system might appear noisy and generate unreliable data. The solution to this is to terminate the outputs in an appropriate manner to minimize the reflections.

Common Termination Techniques

Most transmission-line termination techniques rely on impedance matching at either the source or receiver to reduce reflections and line noise (see Figure 13). Series, thevenin, and ac techniques commonly are used and are effective methods of line termination for high-speed logic. Shunt termination is educational, but has implementation problems. Diodes can be used as a solution, but, generally, this is not a good termination technique by itself.

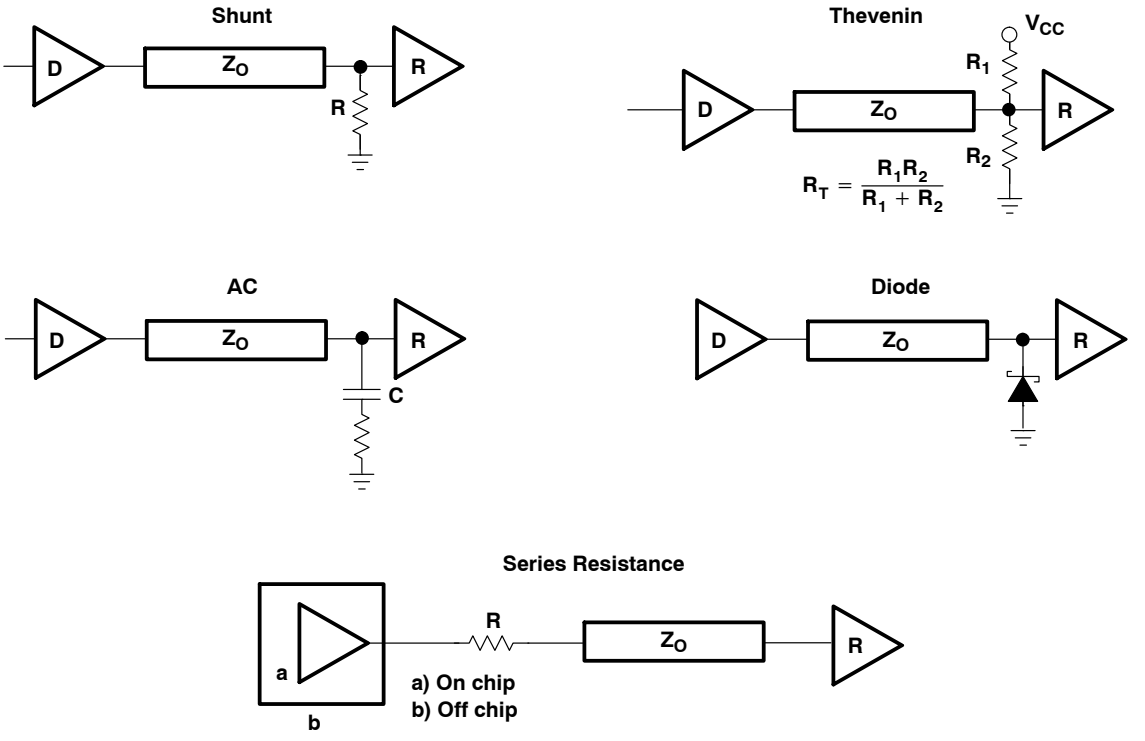

Figure 13. Termination Techniques

Shunt

Shunt termination (see Figure 13) is one of the simplest termination techniques to implement. The value of the termination resistor should match the line impedance for best performance. As the transmitted signal reaches the receiver, the shunt termination drains off the current with an impedance matching the transmission line. There is no reflection, thus, no noise is retransmitted down the transmission line.

There are several disadvantages to shunt termination. Usually the line impedance is fairly low (50 Ω to 70 Ω), which requires a resistor of similar value. This causes a heavy dc current drain on the source when in the logic high state and requires a strong line driver to source the current. With the low-impedance resistor pulling to GND, the V_{OH} of the transmission line is lower, reducing the noise immunity at the receiver. Additionally, having a strong pull down on the transmission line might unbalance the rising and falling edges of the signal, causing the falling edge to be faster than the rising edge, resulting in duty-cycle distortion of the signal.

AC

AC termination utilizes the same line-impedance-matching resistor as shunt termination, except it is ac coupled with a capacitor, making a simple high-pass filter. The capacitor appears to be a short circuit during signal transitions when termination is needed, but eliminates the dc component of the current drain.

AC termination (see Figure 13) has the precise termination advantages of shunt termination, but reduces the disadvantages of dc current drain and waveform distortion. At each transition of the signal, the capacitor charges up to the voltage level necessary to maintain zero volts across the resistor. During the arrival of the next input transition, the signal drives the full value of the resistor until the capacitor can again recharge.

It is recommended that the resistor value be equivalent to the line impedance. The ideal capacitor value varies with line impedance, edge rate, and desired signal quality. The values are not critical, but tests have shown that with TI logic, a value of 50 pF for the capacitor is a good compromise. Increasing the capacitance value to 200 pF improves signal quality, but sacrifices power dissipation. Reducing the value to 47 pF lowers the power dissipation, but sacrifices signal quality. Values below 47 pF give a very high frequency response to the filter and tend to be ineffective for line termination. Values above 200 pF add power dissipation without additional signal quality improvement. AC termination is excellent for use with clock drivers, cables, backplanes, distributed loads, and many other applications. The combined cost of the capacitor, resistor, and real estate for each line frequently precludes general use for on-board bus termination.

Thevenin

Thevenin termination (see Figure 13) attempts to correct the dc problems of shunt termination by reducing the dc load of the termination and pulling the signal closer to the center of the transition. For high-speed logic, it is best to center the dc level at a logic high (>2.0 V) to avoid holding the input at the input threshold (toggle point »1.5 V). Under this condition, if the driver shuts off (high Z), the input pulls up rather than causing oscillations from logic uncertainties.

A disadvantage of thevenin termination is the dc leakage from V_{CC} to GND through the terminator. Using thevenin termination to match a 50- or 70-Ω line requires a parallel resistance that is low enough to pass considerable current. Thevenin is commonly used on backplanes, cables, and other long transmission lines. Some applications, such as backplanes, might require termination at both ends of the transmission line.

Diode

Diode termination (see Figure 13) simply clips the undershoot of a high-to-low transitioning signal and thereby reduces the line reflection. Diode termination can be effective if the cause of the problem is undershoot and the frequency response of the diode is considerably higher than the transition frequency of the signal.

With very-high-speed logic families, such as TI's, the frequency response of the output-signal transition can reach 400 MHz and beyond. At these frequencies, the effectiveness of diode termination is limited due to the frequency response of the terminator. While some benefit might be realized with diode termination, the inductances, capacitances, and frequency response of the diode and diode connections probably make the termination scheme less effective when used at high frequencies.

The internal parasitic clamp diode to ground, found on the inputs and outputs of all CMOS logic, bleed off some of the overshoot current, but this parasitic clamp does not have the necessary frequency response to perform effective diode termination in high-speed applications. Diode termination frequently is used on backplanes and long cables, possibly in conjunction with another form of line termination.

Series (Source Terminated)

Series termination reduces the output edge rate of the driver, the switching amplitude of the signal, and the charge injected into the transmission line. This has significant benefits by reducing signal line noise and electromagnetic interference (EMI). Series termination adds a series resistor at the output of the line driver, effectively increasing the source impedance of the driver (see Figure 13). When using series termination with distributed loads, care must be taken that the combined output impedance of the driver and series resistor is small enough to allow first incident-wave switching. If the output impedance becomes too high, the step that is seen in the output transition does not toggle the components at the near end of the transmission line until the signal passes down the line and returns to the source, causing an unnecessary propagation delay. Series termination is the most commonly used form of termination and is found on circuit boards, cables, and in most other applications.

Table 5 provides a comparison of the five termination techniques.

Table 5. Termination Techniques Summary

TECHNIQUE	ADDITIONAL DEVICES	POWER INCREASE	DELAY	HOLDS DEFINED LEVEL	IDEAL VALUE†	COMMENTS
Shunt	1	Significant	No	Yes	$R = Z_O$	Low dc noise margin
Thevenin	2	Yes	No	Yes	$R_1 = R_2 = 2Z_O$	Good for backplanes due to maintaining drive current
AC	2	Yes	No	No	$R = Z_O$ $60 < C < 330$ pF	Increase in frequency and power
Series resistor on device	0	No	Small	No	$25 =< R =< 33\ \Omega$	Good undershoot clamping; useful for point-to-point driving
Diode	1	No	No	No	NA	Good undershoot clamping; useful for standard backplane terminations

† Symbols are defined in Figure 13.

Signal Integrity

System designers often are concerned with the performance of a device when the outputs are switched. The most common method of assessing this is by observing the impact on a single output when multiple outputs are switched.

Simultaneous Switching

In a digital circuit, when multiple outputs switch, the current through the ground or V_{CC} terminals changes rapidly. As this current flows through the ground (or V_{CC}) return path, it develops a voltage across the parasitic inductance of the bond wire and the package pin. The phenomenon is called simultaneous switching noise. Figure 14 shows the equivalent circuit of a typical CMOS output buffer stage with the package parasitics and the external load. The parasitic components that affect the ground bounce are inductance and resistance of the ground bond wire and pin, inductance and resistance of the output bond wire and pin, and load impedance. For the first-order analysis, the parasitics associated with the V_{CC} terminal can be ignored. Also, the external ground plane is assumed to be ideal.

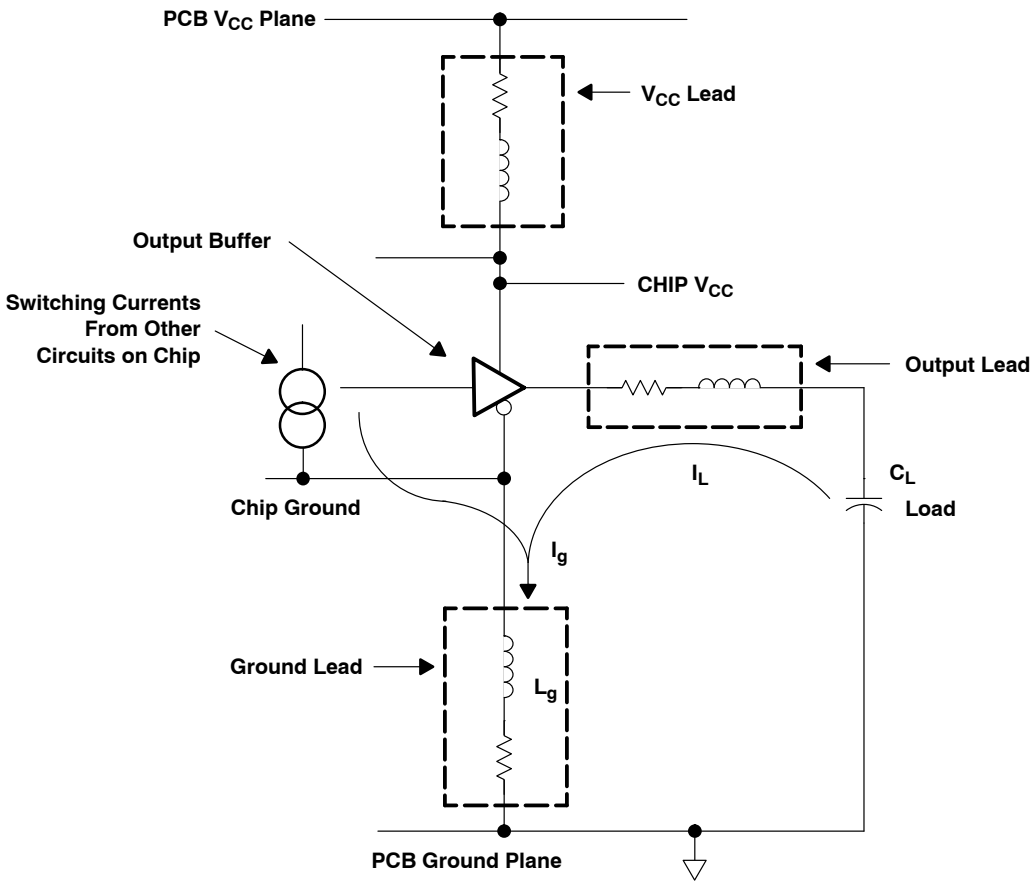

Figure 14. Output Buffer With External Parasitics

During the output high-to-low transition, the sum of the output load current and all switching current through the internal gates of the device flows through the ground lead. The rate of change of this current (di/dt) develops a voltage drop across the ground lead inductance and causes a positive ground bounce or an overshoot in an otherwise quiet ground. This positive ground bounce is normally followed by an undershoot coincident with the voltage waveform on the output terminal. The amplitudes of both the positive and the negative ground bounce are a function of $L_g * di/dt$ and of the number of outputs switching simultaneously (SS noise). The ground-bounce phenomenon can be clearly observed at an unswitched low output of a device by switching several other outputs simultaneously from logic high to low. Figure 15 shows the typical output voltage transition and the corresponding ground bounce, as observed at the unswitched low output. Positive ground bounce is primarily the result of the rate of change of current (di/dt) through the ground lead inductance. The rate is determined by the rate at which the gate-to-source voltage (V_{gs}) of the sink transistor changes. During the early part of the fall time, the ground voltage rises while the output voltage falls, forcing the sink transistor into the linear region. The transistor then behaves like a resistor R_{on} (the on-state resistance of the transistor in the linear region). For the remainder of the output voltage excursion, the equivalent circuit at the output can be treated like a resonant L-C-R circuit formed by the ground and the output lead inductance, load capacitance, and the total resistance in the loop, which includes R_{on}. The oscillation frequency is determined by the net values of L and C, while damping is determined by L and the total resistance in the loop. Ground bounce also is generated during the output low-to-high transition. However, the magnitude of this ground bounce is much smaller because of the absence of load current in the ground lead.

Ground and V_{CC} bounce cannot be eliminated, but they can be minimized by controlling edge rates and reducing output swing. Ground bounce depends on many factors, with device speed being one of the more important influences. As device speed goes up, the rate of change of current in the parasitic inductances increases and the related switching noise goes up. Due to this correlation between speed and ground bounce, high-speed logic families arouse increased concern over noise due to simultaneous switching of outputs.

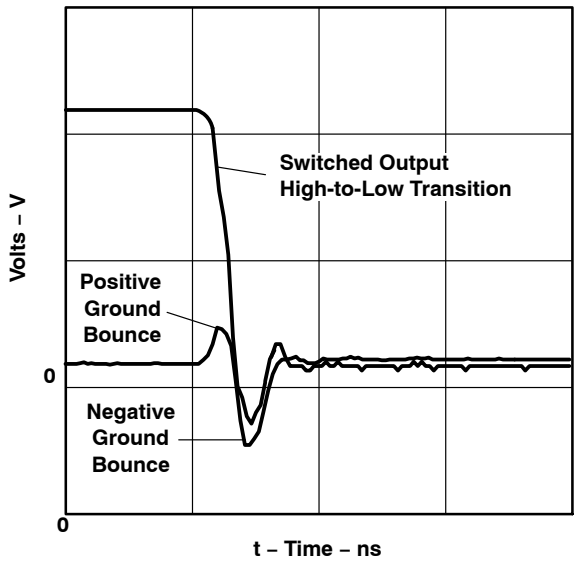

Figure 15. Simultaneous-Switching-Noise Waveform

Ground-Bounce Measurement

There is no industry standard for measuring ground bounce. However, the method most commonly used by IC vendors and customers is based on observing the disturbance of a logic-low level on an unswitched output of a multiple-output device while switching all other outputs from a high to a low state. Figure 16 shows the schematic for measuring ground bounce on a device such as the AHC244 octal buffer. One output is in the low state while the outputs are switched simultaneously. The load on each output consists of a 50-pF capacitor. Two outputs are connected to the oscilloscope: one for observing the high-to-low transition of a switched output and the other for observing the ground bounce on the quiet output.

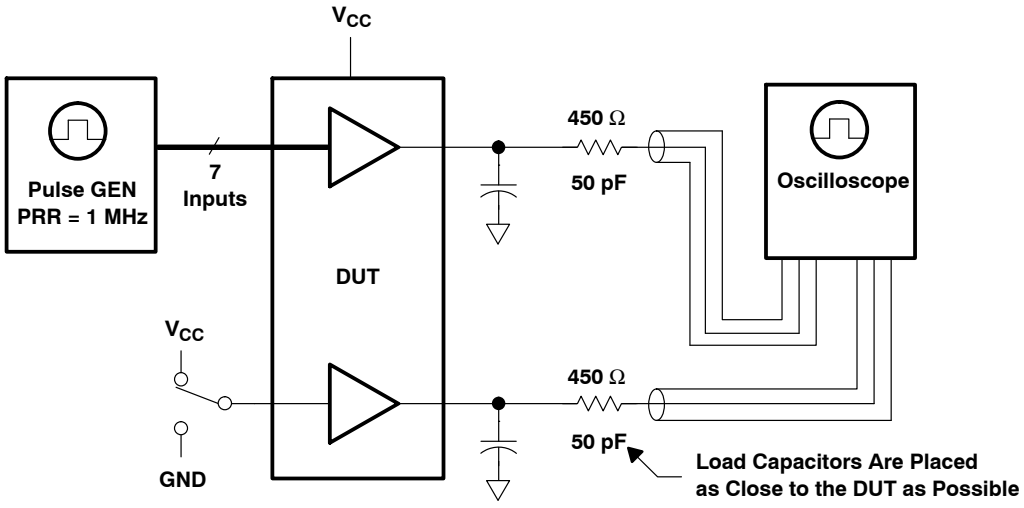

Figure 16. Ground-Bounce Test Circuit

With careful layout, proper bypassing to filter out high-frequency noise, and good oscilloscope probes, it is possible to observe the ground bounce on the internal ground of the chip by observing the voltage at the unswitched low output, whose sink transistor operates in the linear region and provides a Kelvin connection to the chip ground.

One technique to reduce the impact of simultaneous switching on a device is to increase the number of power and GND pins. The strategy is to disperse them throughout the chip (see the *Advanced Packaging* section of this application report). For a complete discussion of simultaneous switching, refer to TI's *Simultaneous Switching Evaluation and Testing,* in the *Advanced CMOS Logic Designer's Handbook*, literature number SCAA001B.

AHC Versus HC

A speed-versus-current-drive comparison between the AHC and HC families is shown in Figure 17. The speed for the AHC is much higher than the HC. Both these products support low-drive applications.

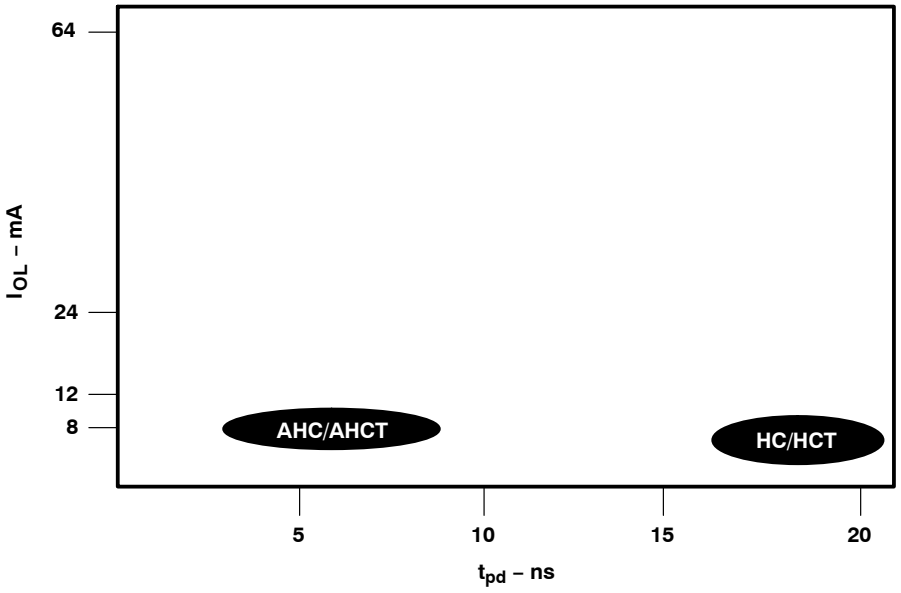

Figure 17. AHC/AHCT and HC Family Positioning

Table 6 shows the features of HC and AHC families. AHC provides much higher speeds with no noise penalty.

Table 6. AHC and HC Features (Typical Values)

PRODUCT FAMILY		AHC	HC
Technology		CMOS	CMOS
5-V tolerant†		Yes (inputs)	Yes (inputs)
Octals and gates		Yes	Yes
Widebus™ (16-bit products)		Yes	No
Bus hold		Yes	No
Damping resistors		No	No
I_{CC}	’245	40 μA	80 μA
DC output drive		–8 mA/8 mA	–8 mA/8 mA
t_{pd}	’245	5 ns	18 ns
C_i	’245	2.5 pF	3 pF
C_{io}	’245	8 pF	10 pF

† When operated at 3.3 V

Advanced Packaging

Figure 18 shows a comparison of packages in which AHC devices are available; for ease of analysis, 14-pin packages and 20-pin packages are included. Figure 19 is not an all-inclusive list of pin counts and corresponding packages, e.g., the TSSOP package is available in both 14-pin and 20-pin format. The TVSOP package, which has a lead pitch of 0.4 mm (16 mil) and a device height of 1.2 mm, is also available in the AHC family. Continued advancements in packaging are making more functionality possible with smaller space requirements.

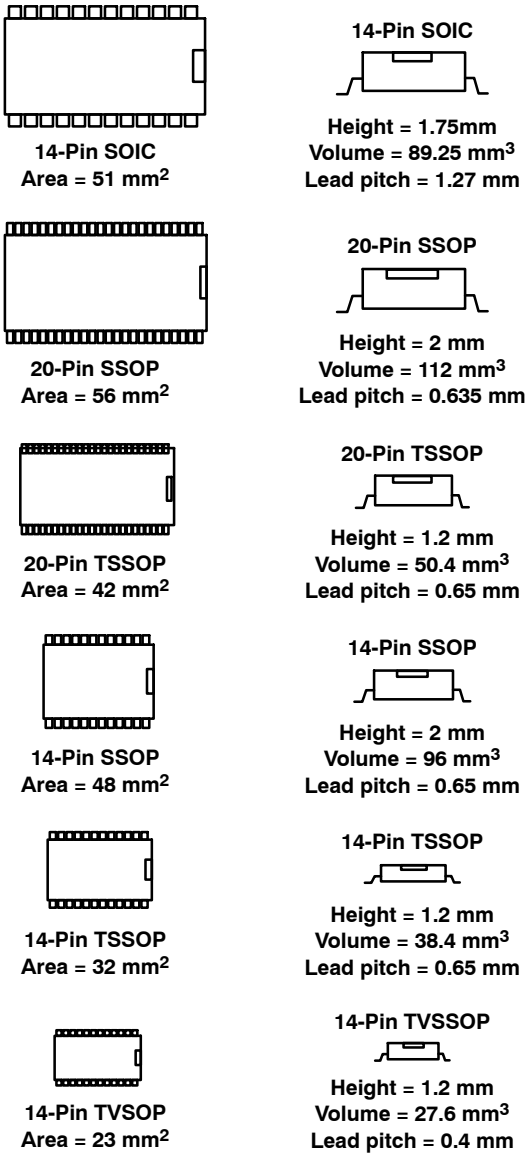

Figure 18. AHC Packages

Figure 19 shows a typical pinout structure for the 20-pin SSOP for the SN74AHC245. This provides for simultaneous switching improvements (see the *Signal Integrity* section of this application report).

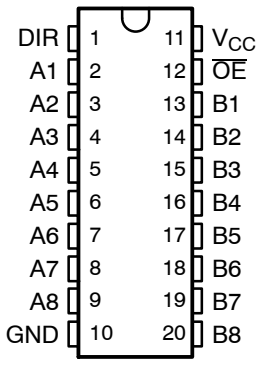

Figure 19. SN74AHC245 Pinout

For a comprehensive listing and explanation of TI's packaging options, consult the *Semiconductor Group Package Outlines Reference Guide*, literature number SSYU001C.

Microgate Logic

The Microgate Logic device is a single gate that is used instead of the two-, four-, or six-gate versions. The advantages of Microgate Logic are:

- Simplified circuit routing
- Help in ASIC modification
- 3.5-ns typical propagation delay

Microgate Logic is available in CMOS (AHC) and TTL (AHCT) versions. The AHC versions are compatible with Toshiba's TC7SHxx series. Figure 20 shows the pinout of the SN74AHC1G00.

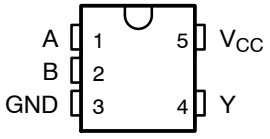

Figure 20. 5-Pin Microgate Logic Pinout

Acknowledgment

The author of this application report is Shankar Balasubramaniam.

AHC/AHCT
Designer's Guide

SCLA013B
June 1999

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INTRODUCTION

The Advanced High-Speed CMOS (AHC) logic family from Texas Instruments (TI™) provides an effortless migration path for HCMOS users who require higher speed and lower power without paying a noise or price premium. The AHC logic family also offers the broadest selection of logic choices, ranging from simple gates/MSI/octals (SN74AHCxxx) to single-gate (SN74AHC1Gxx) and Widebus™ (SN74AHC16xxx) devices. Add to that the ability to operate at both 3.3 V and 5 V, and you have a reliable migration path from HCMOS.

Performance characteristics of the AHC family are:

- **Low noise –** The AHC family allows designers to maintain the same low noise characteristics of HCMOS without the overshoot and undershoot typical of higher-drive devices usually required to achieve AHC speeds.
- **Low power –** The AHC family, by using CMOS technology, has low power consumption (40-µA maximum static current, one-half that of HCMOS).
- **Speed –** With typical propagation delays of 5.5 ns (’245), AHC offers three times the speed of HCMOS.
- **Drive –** Output-drive current is ±8 mA at 5-V V_{CC} and ±4-mA at 3.3-V V_{CC}.
- **5-V input tolerance at 3.3 V –** With the input diode to V_{CC} removed, AHC is specified for both 5-V and 3.3-V operation.
- **Pin-for-pin compatibility –** All AHC devices are pin-for-pin compatible with industry-standard functional pinouts.
- **Options –** With CMOS- (AHC) and TTL- (AHCT) compatible devices available in gates/MSI/octals, single gates, and Widebus, the AHC family offers the widest selection of logic choices on the market.
- **Packaging –** AHC devices are available in D and DW (SOIC), N (PDIP), DB and DL (SSOP), DGG and PW (TSSOP), DGV (TVSOP), and DBV and DCK (SOT) packages. Selected AHC devices are available in military versions (SN54AHCxx).

For more information on these or other TI products, please contact your local TI representative, authorized distributor, the TI technical support hotline at 972-644-5580, or visit the TI logic home page at http://www.ti.com/sc/logic.

For a complete listing of all TI logic products, please order our logic CD-ROM (literature number SCBC001) or Logic Selection Guide (literature number SDYU001) by calling our literature response center at 1-800-477-8924.

Contents

Contents (Continued)

Your Next Choice: Advanced High-Speed CMOS Logic (AHC)

Speed Up Your System With AHC/AHCT

Do you use HCMOS logic in telecom, computer, industrial, automotive, or consumer applications?

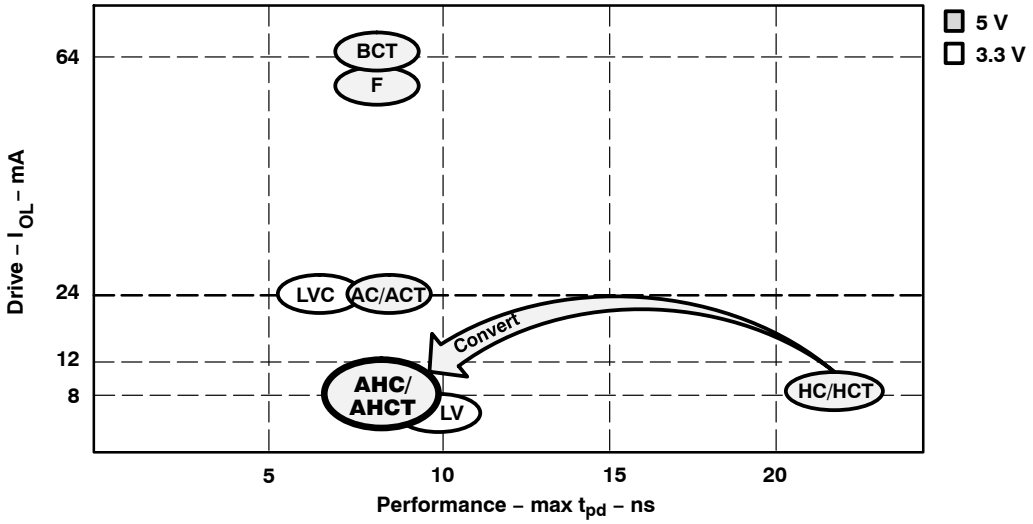
For the same price as HCMOS, would you like to plug in devices with:

- 3-times the speed of HCMOS
- Half the static power consumption of HCMOS
- The same low noise as HCMOS
- A wide supply-voltage range

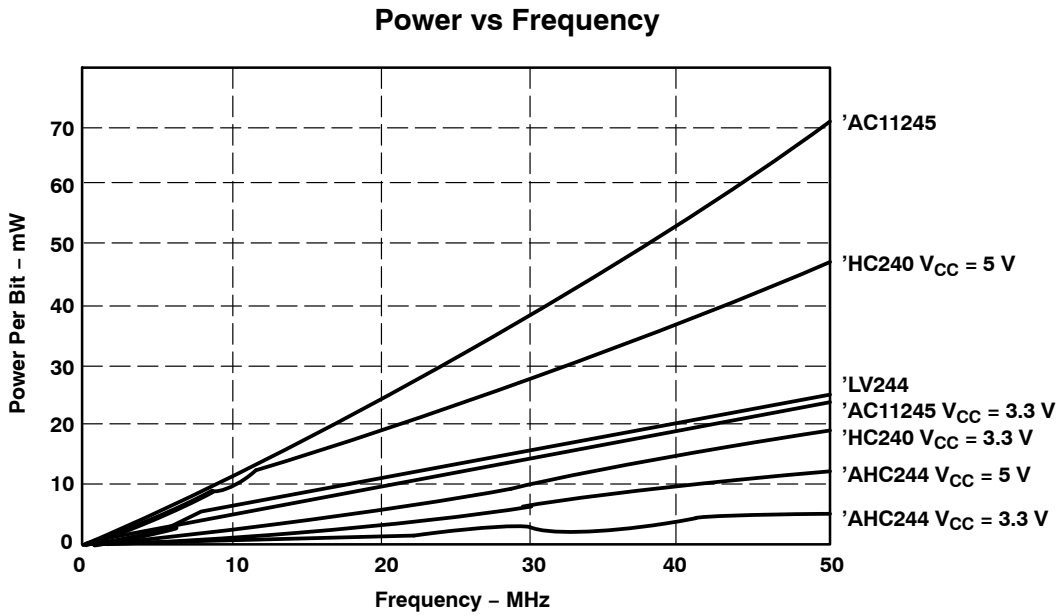
If so, this designer's guide is for you . . . and so is advanced high-speed CMOS (AHC).

Convert HC to AHC

Family Positioning



AC/ACT	Advanced CMOS	HC/HCT	High-Speed CMOS
AHC/AHCT	Advanced High-Speed CMOS	LV	Low Voltage CMOS
BCT	BiCMOS Technology	LVC	Low Voltage CMOS
F	74F Bipolar Technology		



Triple the Speed, Same Drive, But Less Power Consumption

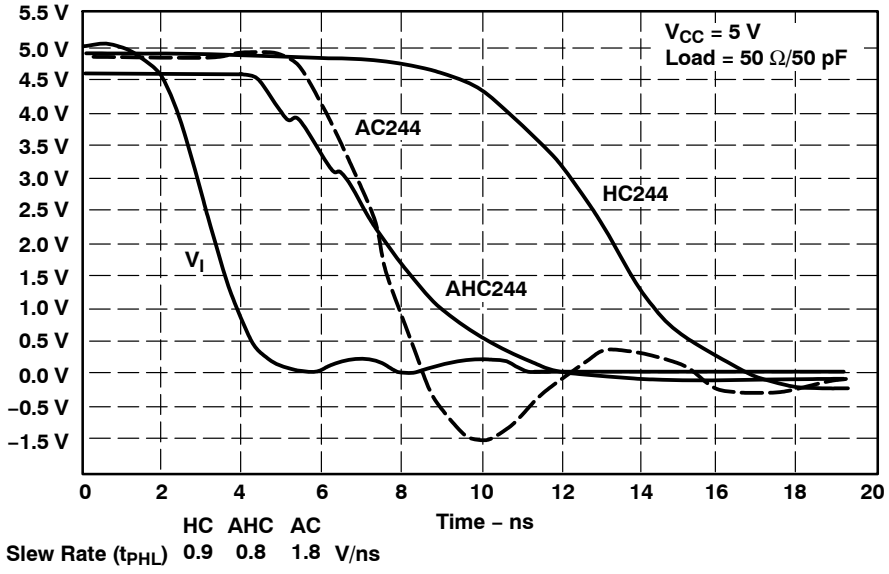
The AHC family typically replaces the slower 5-V HCMOS family, but is additionally specified at V_{CC} = 3.3 V.

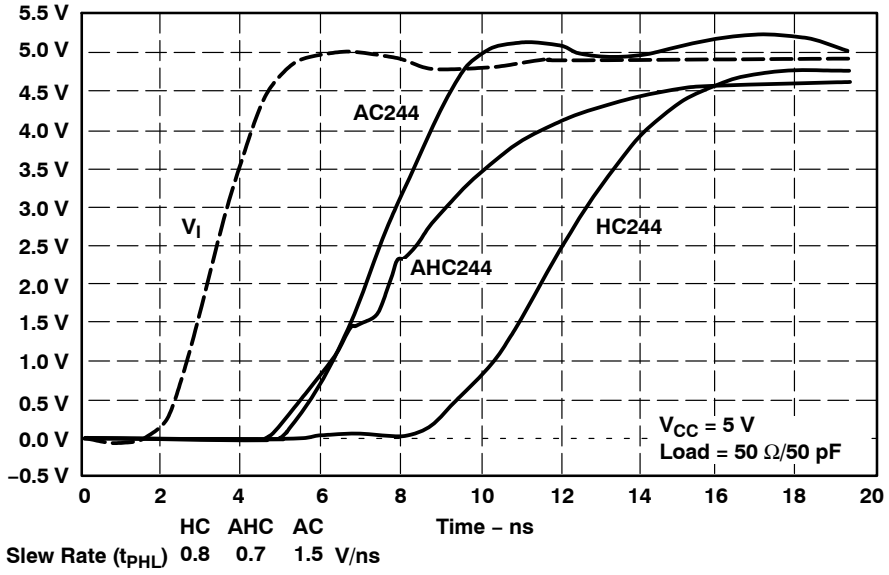
Drive capability is the same as for the HC/HCT family, while speed is comparable to that of the AC/ACT, BCT, and 74F families. For instance, the typical propagation delay time of octal transceiver SN74AHC245 at V_{CC} = 5 V is 5.5 ns (8.5 ns maximum) with drive capability of $I_{OH,OL}$ = ±8 mA. The CMOS-compatible AHC device can be used in low-voltage systems. However, when operated at V_{CC} = 3.3 V, t_{pd} slows to 8.5 ns (typically) at a drive of $I_{OH,OL}$ = ±4 mA.

The comparison of the power consumption between AC, HC, LV, and AHC families shows that for power-critical systems the use of AHC lengthens battery life.

Improve Switching Performance With AHC/AHCT

Switching Characteristics Comparison





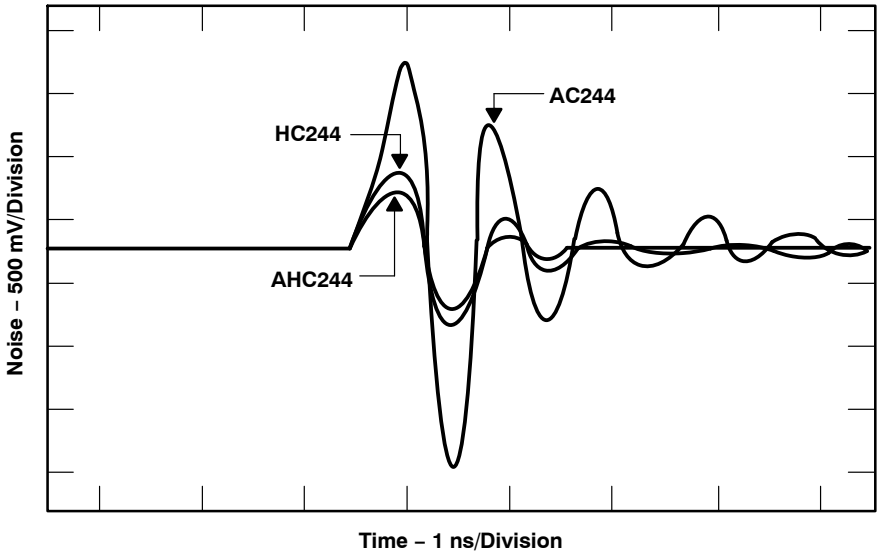
Low Switching Noise

The HCMOS family has very low switching noise, which is achieved primarily through a low slew rate, typically, 0.9 V/ns and the low drive capability of ±8 mA, resulting in low current spikes during switching. Though the speed of AHC/AHCT has been increased, the slew rate of AHC/AHCT is even lower than HCMOS. The ground bounce of AHC devices attributed to simultaneous switching is better than that of the standard HCMOS family. This is specified with the parameters $V_{OL(P)}$ and $V_{OL(V)}$. For example, SN74AHC244:

$V_{OL(P)}$ (typ) = 0.5 V

$V_{OL(V)}$) (typ) = –0.2 V

Ground-Bounce Comparison



Technical Comparison of AHC Versus Other CMOS Logic Families (’245 Function)

		AHC/AHCT		HC/HCT		AC/ACT	
V_{CC}		5 V	3.3 V	5 V	2 V	5 V	3.3 V
Drive		–8/8 mA	–4/4 mA	-8/8 mA	20 μA	–24/24 mA	–12/12 mA
Speed (typical)		5.5 ns	8.3 ns	18 ns	54 ns	3.5 ns	5 ns
Ground bounce		0.5 V (–0.2 V)	N/A	0.6 V (–0.3 V)	N/A	1.5 V (–1.8 V)	N/A
Power dissipation capacitance†		8.6 pF (at 1 MHz)	N/A	40 pF	N/A	45 pF	N/A
Quiescent power dissipation		40 μA		80 μA		40 μA	
Level conversion option	Input	3.3 V	5 V	3.3 V		3.3 V	
	Output	5 V	3.3 V	5 V		5 V	
Widebus package available		Yes	Yes	No	No	No	Yes

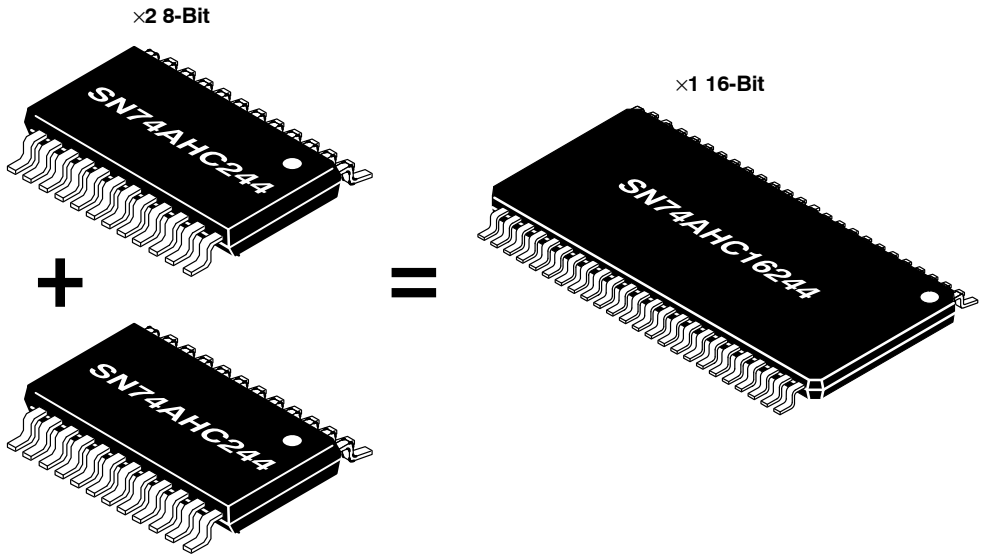
† C_L = 50 pF, f = 10 MHz unless otherwise specified

Widebus Minimizes Board Space (SN74AHC16xxx/SN74AHCT16xxx)

The trend toward 16-bit and 32-bit Widebus systems to increase data throughput continues unabated, requiring bus drivers that support these formats.

Many 16-bit bus systems can be supported easily by TI Widebus devices. These are designed to replace the commonly used 8-bit functions. A single 16-bit Widebus package replaces 2 × 8-bit packages. A typical Widebus example is the SN74AHC16244, which incorporates twice the functionality of an SN74AHC244.

Typical Widebus Example



Multiple Package Options

AHC Packages

	PDIP (N) DUAL-IN-LINE					SOIC (D/DW) SMALL OUTLINE			SOT-23 (DBV) SMALL OUTLINE	SOT-323 (DCK) SMALL OUTLINE
PIN COUNT	**14**	**16**	**18**	**20**	**28**	**16**	**20**	**28**	**5**	**5**
Width	6.60	6.60	6.60	6.60	14.22	7.59	7.59	7.59	1.80	1.35
Length	19.69	19.69	23.37	24.77	36.83	10.41	12.95	18.03	3.10	2.2
Pitch	2.54	2.54	2.54	2.54	2.54	1.27	1.27	1.27	0.95	0.65
Height	5.08	5.08	5.08	5.08	5.08	2.65	2.65	2.65	1.3	1.0

	SSOP (DB/DL) SMALL OUTLINE		TSSOP (DGG/PW) SMALL OUTLINE			TVSOP (DGV) SMALL OUTLINE				
PIN COUNT	**20**	**48**	**14**	**20**	**48**	**14**	**16**	**20**	**24**	**48**
Width	5.60	7.59	4.80	4.50	6.40	4.50	4.50	4.50	4.50	4.50
Length	7.50	16.00	5.10	6.60	12.60	3.70	3.70	5.10	5.10	9.80
Pitch	0.65	0.635	0.65	0.65	0.50	0.40	0.40	0.40	0.40	0.40
Height	2.00	2.79	1.20	1.20	1.20	1.20	1.20	1.20	1.20	1.20

All linear dimensions are maximums specified in millimeters.
All devices comprising gate, flip-flop, or bus functions are available with CMOS- and TTL-compatible I/Os, and are available in a broad range of package options.

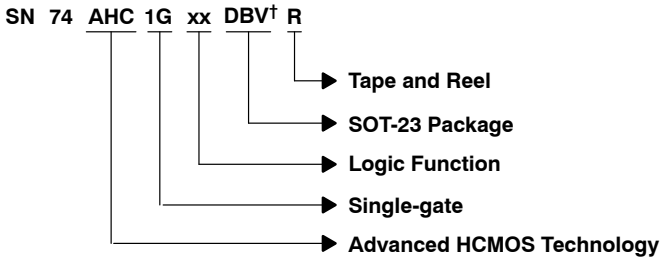
PACKAGES					
	TI NOMENCLATURE	**PHILIPS**	**MOTOROLA**	**FAIRCHILD**	**TOSHIBA**
SOT-23 (new)	DBV (5 pin)	N/A	N/A	M5X	F
SOT-323 (new)	DCK (5 pin)	N/A	N/A	P5X	FU
PDIP	N, NT (24 pin)	N	P	N	P
SOIC	D, DW (20 pin–>)	D	M	M	FN
SSOP	DB (24 pin–>), DL (48 pin–>)	DB, DL	SD	MSA, MEA	FS
TSSOP	PW (–>24 pin), DGG (48 pin–>)	PW, DGG	DT	MTC, MTD	ST
TVSOP (new)	DGV (≤ 56 pin)	N/A	N/A	N/A	N/A

Data sheets are available in the *AHC/AHCT Logic Advanced High-Speed CMOS Data Book*, literature number SCLD003A, or at http://www.ti.com/sc/logic.

Single-gate Logic
(SN74AHC1Gxxx/SN74AHCT1Gxxx)

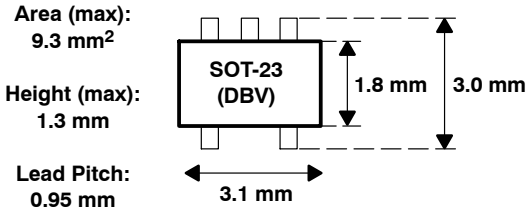
TI's Single-gate Logic helps designers of handheld systems, such as portable computers, remote control units, and cellular telephones, to reduce the size and weight of their designs. The extremely small logic devices simplify the layout of printed circuit boards, and can be used to make simple functional modifications of ASICs without the cost and delay of redesigning.

Nomenclature



† Also available in SOT-323 (DCK). Refer to Figure 43.

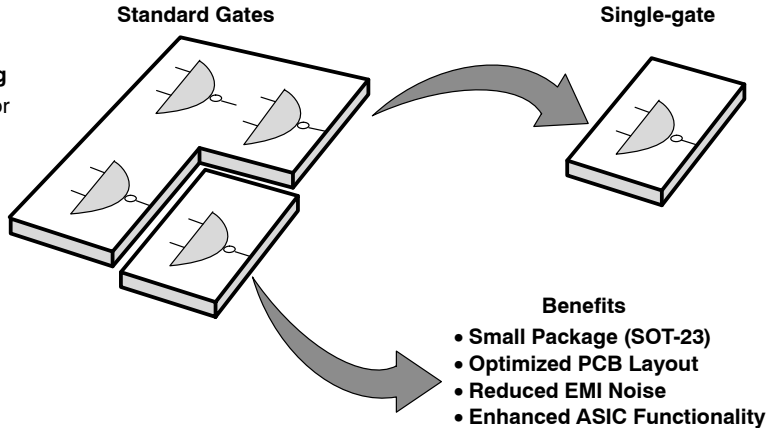
Package



The Principle

Board Space Comparison

Quad Gate	Single-gate	Area Saving
TSSOP 14 Pin 33.66 mm^2	SOT-23 5 Pin 9.3 mm^2	24.36 mm^2 or 72.7%



Performance

- 3.5-ns typical propagation delay
- ±8-mA output drive
- 20-μA static current
- CMOS (AHC)- and TTL (AHCT)-compatible versions

Cross-Reference Examples

TEXAS INSTRUMENTS	TOSHIBA
SN74AHC1G00DBV	TC7SH00F
SN74AHCT1G00DBV	TC7ST00F
SN74AHCU1G04DBV	TC7SHU04F

Abstract

With the advanced high-speed CMOS family of logic devices, TI has brought to market a series of components that fully meets today's requirements for increased speed, that is, reduced signal delay time, and for operation from supply voltages of 5 V and 3.3 V. This document first addresses the electrical characteristics of these new devices. A detailed investigation of dc parameters, input/output characteristics, and dynamic behavior follows. Power consumption, cross talk between signal lines, and electromagnetic compatibility also are discussed.

1. Introduction

The introduction of the high-speed CMOS family SN74HC device at the beginning of the 1980s provided the system designer with a sensible and logical alternative to bipolar logic devices, which, until then had been so widely used. These CMOS devices featured delay times approximately comparable to those of the low-power Schottky family. The output currents that these components could deliver were also comparable to those of their bipolar predecessors. An advantage of the CMOS devices is the wide range of supply voltages (2 V to 6 V) with which these components could be operated. It allowed their effective application in battery-operated equipment. However, as with all other CMOS devices, lowering the supply voltage meant that increased delay times had to be tolerated. A few years later, improvements in semiconductor technology made possible the introduction of the advanced CMOS (AHC) devices. In addition to the advantage of a wide range of supply voltage, these devices featured significant improvements in drive capability and delay time. As a result, CMOS devices were for the first time able to penetrate a domain that had been the reserve of fast bipolar logic devices from the SN74F and SN74AS series. Also, whereas CMOS devices were seldom used in applications with extreme requirements of drive capability and speed, such as backplane wiring in large computer systems, advanced CMOS devices established a firm position in all applications. Examples include applications in personal computers and workstations.

With the introduction of notebook computers at the beginning of the 1990s, new requirements were placed on logic devices to perform well at the supply voltage of 3.3 V, which is usual in battery-operated equipment. The HC and AC devices performed inadequately with regard to drive capability and delay time at this low supply voltage. As fast logic circuits, the LVC and ALVC devices were acceptable successors to the AC devices. In drive capability and delay time, these new logic families operating at a supply voltage of only 3.3 V provided the same results as the well-known AC devices using a supply voltage of 5 V. In 3.3-V applications, a useable successor to the HC devices was still missing. In many applications, the outstanding characteristics of the LVC and ALVC devices are not required. In fact, the interference resulting from the steep-edges characteristic of such devices is a disadvantage. They require additional circuit-design precautions, such as multilayer circuit boards, which, in turn, increase equipment costs unnecessarily. With the introduction of the LV series, the attempt was made to create quickly an appropriate logic family. Clever modifications of the process steps in semiconductor manufacturing allowed better performance at a lower supply voltage, but the long-term result was inadequate. Consequently, a new logic family, which, at a supply voltage of 3.3 V, would have the same, or better characteristics as its well-known predecessor was needed. Also, several problems associated with interfaces of circuits operating at 3.3 V and 5 V needed to be addressed. For various reasons, future systems are expected to use both supply voltages.

The logical answer to all these questions is the series of advanced high-speed CMOS devices manufactured in a process that permits gate lengths of 1 µm. The result is typical delay times of 6 ns at 3-V V_{CC} that, in the past, were measured on ALS circuits. This document acquaints the system designer with the characteristics of these advanced components. In addition, a large number of questions with which the designer is often confronted are discussed. Many application problems that can be solved elegantly with this new logic family are shown.

2. DC Characteristics

2.1 Input Circuit

As in all CMOS devices, the input stage consists of a p-channel and an n-channel transistor (see Figure 1) connected in series. With a high logic level at the input ($V_I = V_{CC}$), the n-channel transistor Q2 is conducting and the p-channel transistor Q1 is turned off. A low logic level is created at the output of this inverter. The corresponding complementary state applies with a low logic level at the input ($V_I = 0$ V). In both cases, no current flows through the two transistors. This property is responsible for the low current drain of CMOS devices in the quiescent state.

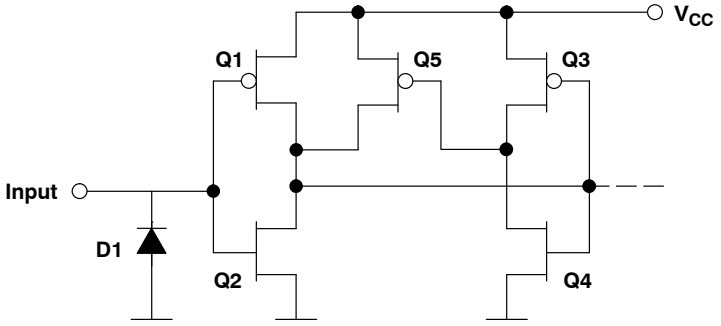


Figure 1. Simplified Input of an AHC Device

Transistors Q1 and Q2 are chosen to have the same transfer characteristics to ensure that the switching threshold of a circuit of this kind is at 50% of V_{CC} (see Figure 2). If the two input transistors Q1 and Q2 have the same characteristics, behavior of the circuit is ensured over a wide range of supply voltage. For CMOS devices, an optimum noise margin is possible in this way. Such devices often are used with interfaces when the other sides deliver only TTL-compatible signals with a high logic level of >2.4 V. To process such signals reliably, a TTL-compatible version with the designation AHCT is available in addition to the AHC family. To shift the switching threshold to lower values, transistors Q1 and Q2 are made so different in their characteristics that the switching threshold becomes about 30% of V_{CC}. Using a supply voltage of 4.5 V to 5.5 V, as is usual with TTL circuits, TTL-compatible threshold voltages for the input stage are achieved (see Figure 3). Such a circuit basically operates with other supply voltages. In this case as well, the threshold voltage has a specific relationship to the input voltage. However, under these conditions the threshold voltage is shifted to values that cannot allow an adequate noise margin in the system. Thus, the TTL-compatible AHCT devices should operate over a range of supply voltage from 4.5 V to 5.5 V.

When a device of this kind is controlled by signals coming from similar devices, and its rise and fall times are only a few nanoseconds, reliable operation can be expected. However, in many cases, for example, at the interfaces with other parts of an equipment, this reliability may not be possible. When there are slowly rising edges at the input, oscillation within the device can occur as a result of high voltage amplification, high cutoff frequency of the transistors, and parasitic components coming mostly from the package (see *Package Construction*). To suppress this oscillator, a kind of Schmitt-trigger circuit has been integrated into the input stage. In addition, the inverted input signal is inverted again with inverter Q3/Q4, and then fed back through transistor Q5 to the output of the input inverter. The switching thresholds on the positive and negative edges at the input differ by about 200 mV and the input circuit has the hysteresis characteristic that is typical of Schmitt-trigger circuits. Transfer characteristics of AHC devices are shown in Figure 2 and those of TTL-compatible AHCT devices are shown in Figure 3.

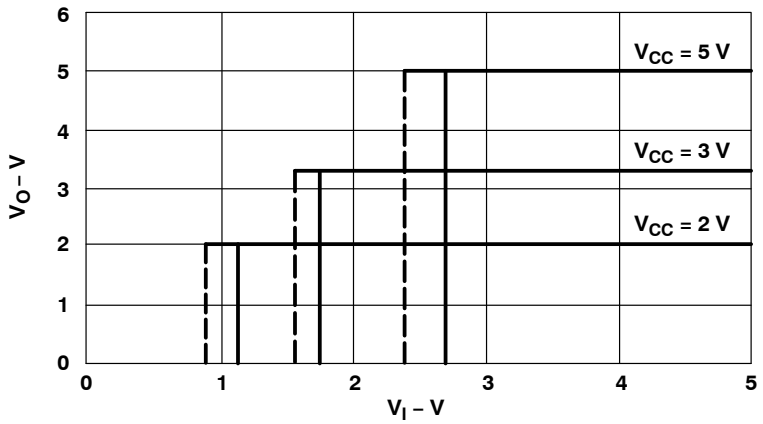


Figure 2. Transfer Characteristics of AHC Devices

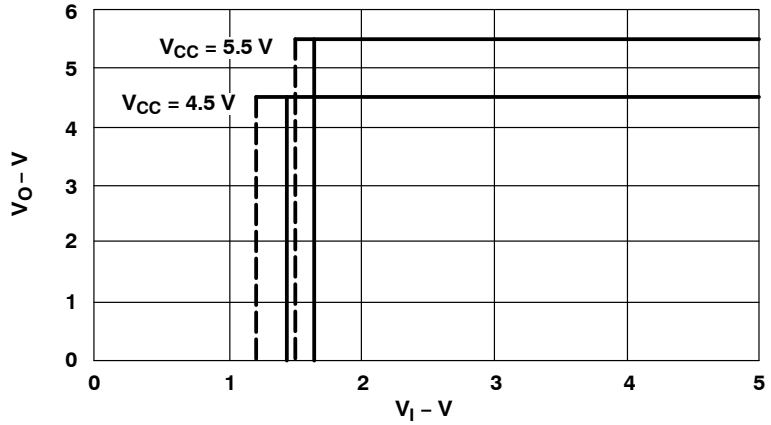


Figure 3. Transfer Characteristics of AHCT Devices

Hysteresis in the input circuit is intended only to process reliably signals that have a slew rate of <10 ns/V. With a signal swing of 5 V, this corresponds to rise and fall times of about 50 ns. If signals with considerably longer rise and fall times are processed, the specially developed Schmitt triggers, such as the SN74AHC(T)14, should be used. These components have a considerably larger hysteresis of about 800 mV at V_{CC} = 5 V and, therefore, allow processing of very slow edges without any problems. When the supply voltage changes, switching thresholds and hysteresis change approximately in proportion to the supply voltage (see Figure 4).

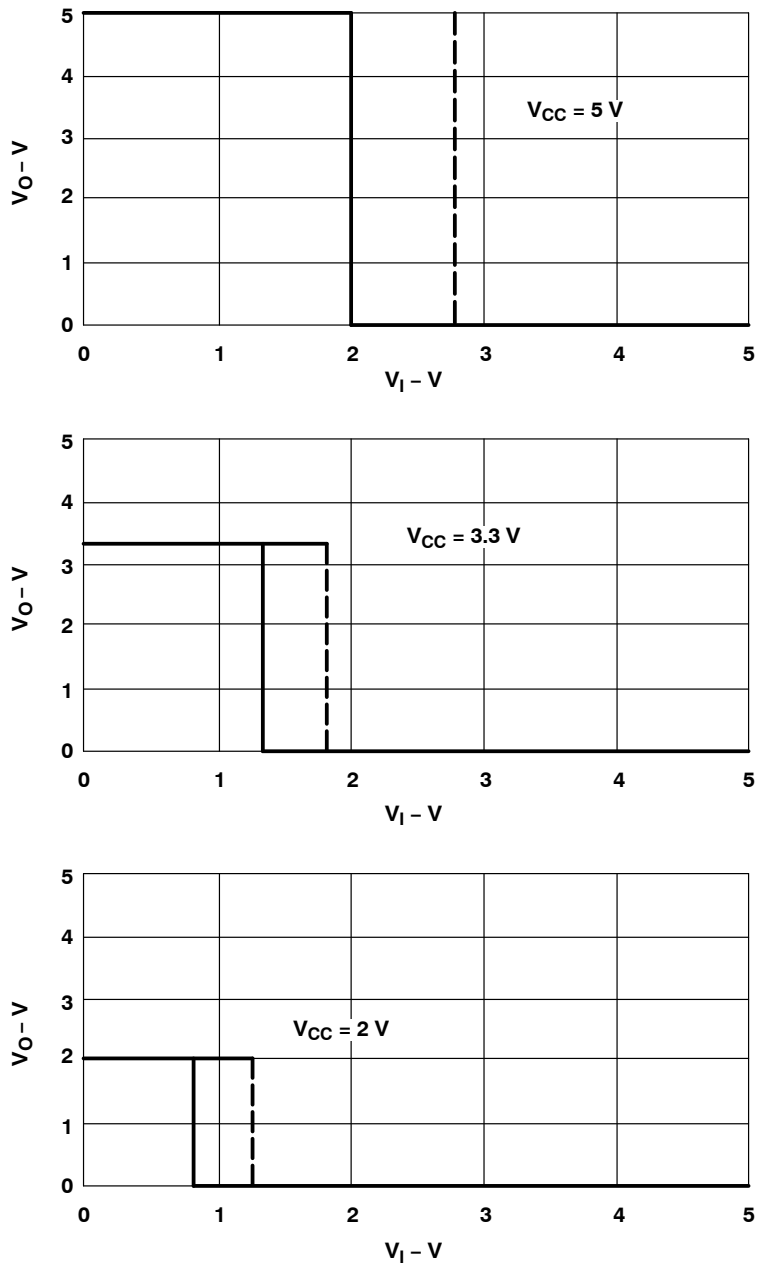


Figure 4. Transfer Characteristics of the SN74AHC14 Schmitt Trigger

To process signals having a swing of only about 3 V in a system with a supply voltage of 5 V, the TTL-compatible SN74AHCT14 Schmitt trigger is available. This device has the same switching characteristics as the previously described Schmitt trigger, except that appropriate circuitry shifts the switching thresholds into the region of the commonly used TTL-voltage levels. Figure 5 shows the transfer function of such components.

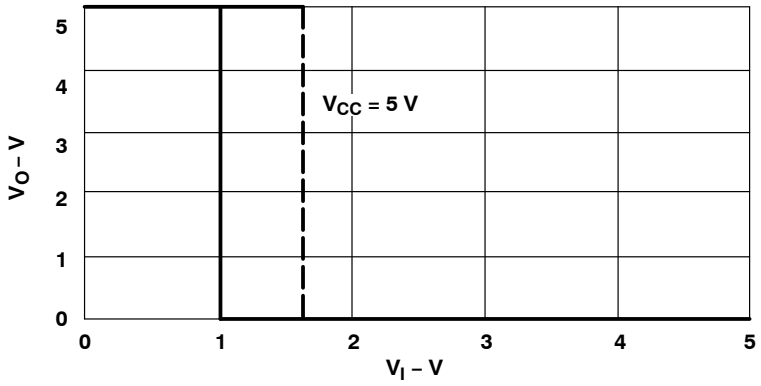


Figure 5. Transfer Characteristics of a TTL-Compatible SN74AHCT Schmitt Trigger

Due to the very low current consumption of CMOS devices in normal operation, only one of the two complementary transistors connected in series conducts. However, this is true only if the input voltage is more negative than the threshold voltage (V_{tn}) of the n-channel transistor or more positive than the supply voltage minus the threshold voltage ($V_{CC} - V_{tp}$) of the p-channel transistor. The threshold voltages V_t of the transistors are, in this case, about 1 V. Over a range of input voltage from $V_{tn} < V_i < (V_{CC} - V_{tp})$, both transistors simultaneously conduct, such that current flows in the input stage that cannot be neglected, and that must be added to the supply current I_{CC} of the circuit. Figure 6 shows the current consumption of AHC and AHCT devices as a function of the input voltage. With both varieties of circuit, the supply current, with the input threshold voltage which is involved, reaches a maximum of about 1 mA to 2 mA. The effective operation of the Schmitt trigger is demonstrated by the transfer characteristics of the AHCT device, as well as in the very rapid change in current that arises after the input voltage exceeds the threshold voltage of ≈1.5 V.

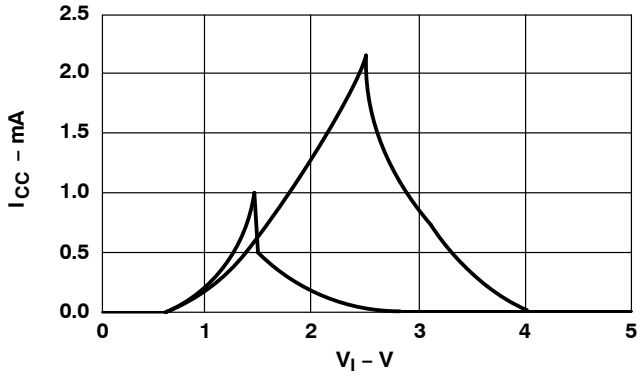


Figure 6. Supply Current as a Function of Input Voltage

In normal operation of a CMOS device, the effect previously described is not relevant, because the high and low logic levels supplied by the outputs of another CMOS device always ensure that the transistor in question turns off. However, if such devices are, for example, controlled by bipolar circuits, results are different. With a high logic level at the output, these supply a voltage that can only be >2.4 V. TTL-compatible CMOS devices, such as those from the SN74AHCT series, recognize such a level as being a high logic state. However, for previously stated reasons, under these conditions a supply current flows in the input stage (see Figure 6), which is significant, particularly with battery-operated equipment. To give system designers specific information about these phenomena, TTL-compatible CMOS-device data sheets have values for the ΔI_{CC} parameter (see Table 1). ΔI_{CC} specifies how much the supply current increases when the high logic level that is typically supplied by a TTL device is applied to one of its inputs. Data sheets show a considerably higher value than that given in Figure 6, but Figure 6 shows only the typical behavior of an AHC or AHCT device. As a result of process and parameter variations and to account for the worst case, values in the data sheets must be used.

Table 1. Specification of ΔI_{CC}

PARAMETER	TEST CONDITIONS		V_{cc}	SN74AHCT245		UNIT
				MIN	MAX	
ΔI_{CC}	One input at 3.4 V,	Other inputs at V_{CC} or GND	5.5 V		1.5	mA

Input characteristics of an AHC device depend on the input of the inverter with a diode connected in parallel (see Figure 1) that is part of the electrostatic discharge (ESD) protection circuit for the input. In addition, the diode limits negative-going overshoots caused by line reflections and improves the quality of the signal. Over a voltage range of $0 \leq V_I \leq 7$ V, the circuit has an extremely high resistance, as indicated by the value of I_I in Table 2. When a device's output that is in an inactive high-impedance state is connected internally in parallel with an input, as in bidirectional circuits, for example, SN74AHC245, I_{OZ} should be used as the effective input current (see Table 2). The value of I_{OZ} is the sum of the leakage currents of the input and output circuits.

Table 2. Specification of the Input Current

PARAMETER	TEST CONDITIONS		SN74AHC245		UNIT
			MIN	MAX	
I_I	$V_I = V_{CC}$ or GND			±1	μA
I_{OZ}†	$V_O = V_{CC}$ or GND,	$V_{I(OE)} = V_{IL}$ or V_{IH}		±2.5	μA

† The parameter I_{OZ} includes the input leakage current.

Input voltages greater than 7 V must be avoided to preclude damage to the gate oxide of the input stage. This damage is not necessarily permanent, but will adversely affect the expected lifetime of the circuit. The gate oxide of AHC devices is only 200 Å thick. An input voltage of 7 V corresponds to a field strength over the gate oxide of 350 kV/cm. Although breakdown of the oxide is expected only at input voltages above 10 V, electrons tunnel increasingly into the gate oxide at field strengths greater than 350 kV/cm, influencing characteristics of the transistors and causing failure.

In practice, negative input voltages are of greater interest. These voltages result from negative-going overshoots generated by line reflections. To limit these negative overshoots and improve the quality of the signal, an effective clamping diode (D1 in Figure 1) is used. Figure 7 shows a typical input characteristic of an AHC device. The input is at a high resistance with positive input voltages ($0 \text{ V} \leq V_I \leq 7$ V). With negative input voltages, the clamping diode conducts. It also limits negative-going overshoots at higher currents to voltages of about −1 V (see Figure 7).

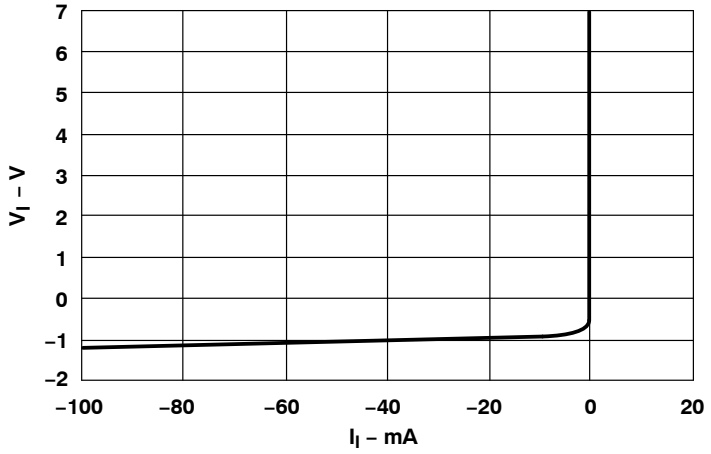


Figure 7. Input Characteristic of an AHC Device

2.2 Output Circuit

The simplified output circuit of an AHC device is shown in Figure 8. Only those components necessary to understand the behavior of the circuit are shown.

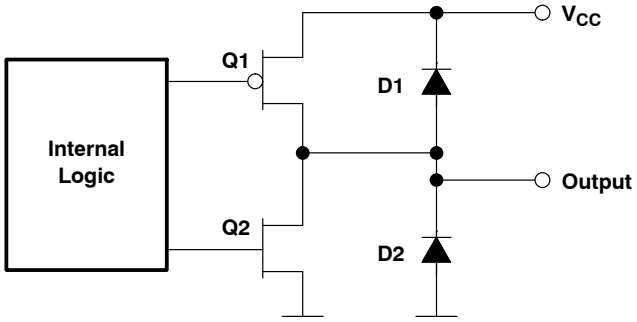


Figure 8. Output of an AHC Device

The internal circuit of the device that drives the load consists of two complementary MOS transistors, Q1 and Q2, connected in series to deliver the necessary output currents. Diodes D1 and D2 are parts of the ESD protection circuit. These diodes, which are created as parasitics during the manufacture of the device, also are intentionally integrated into the internal device circuit. Currents shown in Table 3, which are extracted from the data sheet, are measured under test conditions that produce correct operation of these devices. These values ensure the operation without problems of several logic devices connected together, but give only limited information about their actual behavior.

Table 3. DC Voltage Specifications of the AHC Outputs

PARAMETER	TEST CONDITIONS	V_{CC}	SN74AHC245			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH} = –50 μA	2 V	1.9	2		V
		3 V	2.9	3		
		4.5 V	4.4	4.5		
	I_{OH} = –4 mA	3 V	2.58			
	I_{OH} = –8 mA	4.5 V	3.94			
V_{OL}	I_{OL} = 50 μA	2 V			0.1	V
		3 V			0.1	
		4.5 V			0.1	
	I_{OL} = 4 mA	3 V			0.36	
	I_{OL} = 8 mA	4.5 V			0.36	
I_{OZ}†	V_O = V_{CC} or GND, $V_{I(OE)}$ = V_{IL} or V_{IH}	5.5 V			±0.25	μA

† The parameter I_{OZ} includes the input leakage current.

Figure 9 shows the high- and low-logic output characteristics of AHC devices for various supply voltages. Figure 10 shows the capacitive loading effect on AHC devices.

Output characteristics of AHC devices with 3-state outputs in the inactive high-impedance state are shown in Figure 11. The output data are based on the simplified circuit of the output stage in Figure 8. In the operating state discussed here, output transistors Q1 and Q2 are nonconducting. Over a range of output voltage from $0 V \le V_O \le V_{CC}$, the circuit is, accordingly, at a high resistance. If the output voltage is raised to a value above V_{CC} + 0.7 V, or reduced to below –0.7 V, diode D1 or D2, respectively, conducts and will limit the output voltage. The output characteristic with V_{CC} = 0 V is shown in Figure 11. At this supply voltage, the output transistors do not conduct. The circuit then behaves like two diodes connected in parallel but with opposite polarities. These curves apply to circuits with 3-state outputs and to those with the push-pull output stage, which is usual with all CMOS devices.

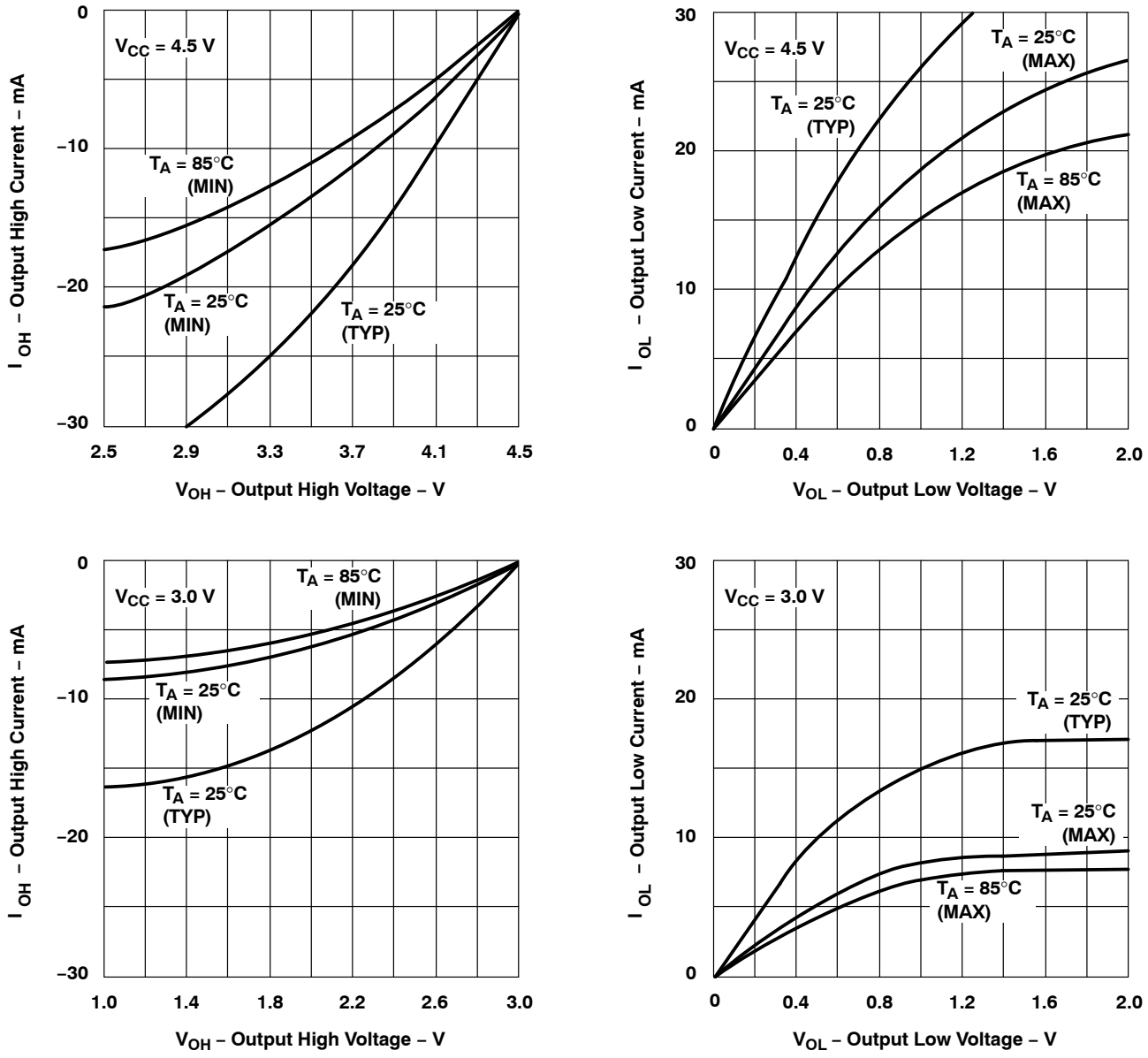


Figure 9. Output Characteristics of an AHC Device

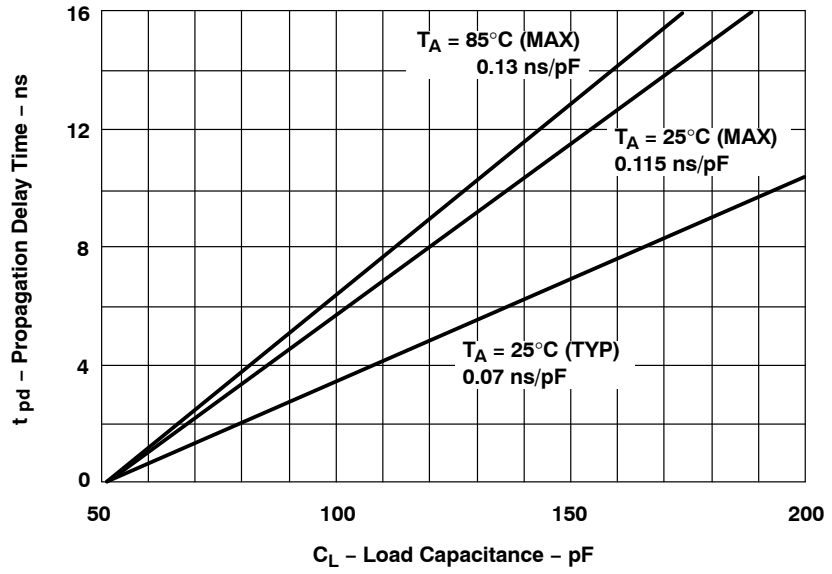


Figure 10. Capacitive Loading Effect on AHC Devices

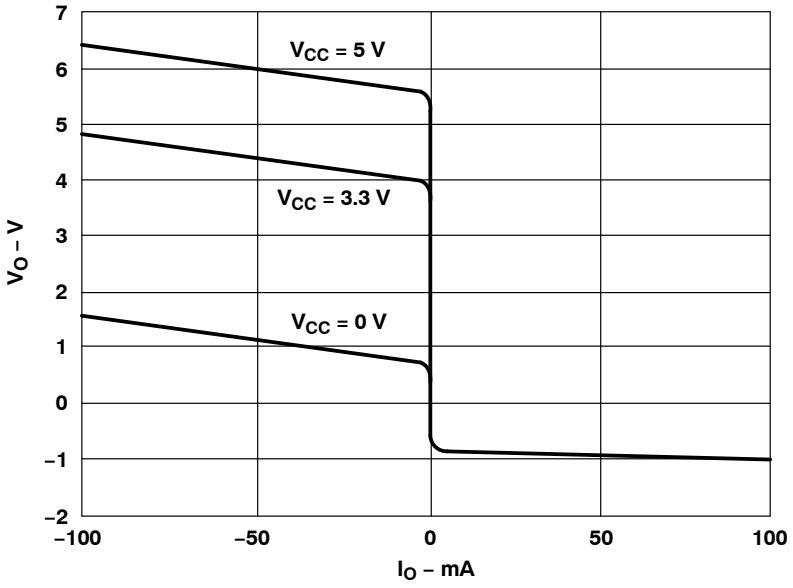


Figure 11. Output Characteristics in High-Impedance State With Supply Voltage Switched Off

2.3 Protection Circuits

Because of their small internal structures, all integrated circuits are susceptible to ESD. An additional problem arises with complementary MOS circuits whose internal structures form parasitic thyristors, which under certain conditions, can be fired and cause a short circuit. Destruction of the device usually is the unavoidable consequence. Therefore, when developing and manufacturing integrated circuits, semiconductor manufacturers must take precautions to protect them from ESD.

2.3.1 Electrostatic Discharge (ESD)

ESD occurs when two bodies with different charges are brought together and an equalization of their charges takes place. This effect is well-known from the situation in which someone walks on a carpet and becomes charged, then touches a metallic object, such as a door handle or water tap. The current that flows as the charge is equalized can be felt as a tingle, or even an unpleasant shock, at the point of body contact. As a result of high charging voltages of several kilovolts and the high currents that result, semiconductors can be destroyed in these circumstances. In practice, three established test procedures reflect the various situations that can arise:

Human-Body Model

This model simulates the situation in which the energy stored in the human body is discharged into the device under test. In this case, a 100-pF capacitor is charged to ±2000 V, then discharged through a resistor of 1.5 kΩ into the device under test. The rise time of the discharge current must be less than a nanosecond.

Machine Model

In this model, immunity to disturbances that contain considerably more energy but have a significantly longer current rise time is tested. For this purpose, a 200-pF capacitor is charged to ±200 V, then discharged without any series resistor into the device under test. The inductances of the lines in the measurement setup (L > 500 nH) reduce the rate of rise of the discharge current sufficiently.

Charged-Device Model

This test simulates the situation in which an integrated circuit is charged, for example, by sliding along a plastic transport rail before insertion by an automatic insertion machine, then is discharged when it touches the printed circuit board. The capacitance of the integrated circuit including package, in which the energy is stored, is then only a few picofarads, but at the instant of the discharge extremely short rise times can be expected. With integrated circuits as currently used, withstanding ±1000 V can be regarded as sufficient in this test.

The engineer who designs integrated circuits must provide protection circuits that will withstand the stresses of the tests described above. A distinction must be made between two destructive processes. High energy levels with relatively long rise times (machine model) in which the protection circuit must be designed with sufficient ability to conduct current away. With the two other test methods, the danger is that, because of the extremely short rise times, the protection circuit will only partially conduct and is overloaded in this region.

Conventional protection circuits consist of diodes or zener diodes that conduct away the currents and limit the voltages. Resistors in series with the circuit to be protected limit the current. Besides reliably diverting the current, whereby the circuit must be protected against thermal overload, the device also must be protected against excessive voltages, for example, to avoid a breakdown of the gate oxide of an MOS transistor. In general, a combination of various methods is used to obtain optimum results.

Figure 12 shows protective circuits used for advanced high-speed CMOS devices. To meet the requirements outlined previously, the protective circuit is constructed in two stages. The input is first protected by a thyristor consisting of transistors Q2 and Q3. This provides coarse protection. If the input voltage rises above about 15 V, transistor Q1 breaks down and fires the thyristor. The latter then short circuits the high currents. Resistors R1 and R2 have values of only a few ohms. Therefore, the holding current of the thyristor is several tens of mA. When the current is reduced again at the end of the discharge, the thyristor is extinguished. Transistors Q4, Q5, and Q6 operate as fine protection and are intended principally to protect the input from excessive voltages. When there are overvoltages at the input, these transistors are driven into breakdown and limit the voltage, while resistor R3 limits the current.

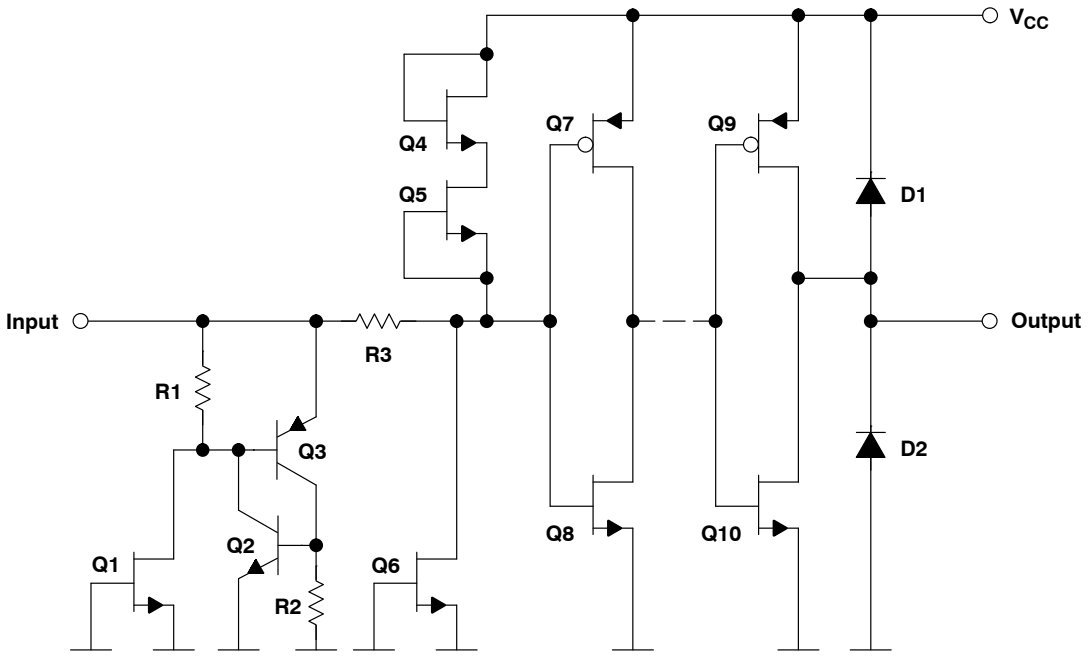


Figure 12. ESD Protection Circuits

A two-stage protection circuit also is to be found at the output of the circuit. The previously mentioned thyristor (Q11, Q12, and Q13) provides coarse protection. Diodes D1 and D2 limit the voltages at the output to tolerable levels.

2.3.2 Latch-Up Protection

When manufacturing complementary MOS circuits, p-n-p-n structures are created internally as a result of the various differently doped regions (see Figure 13). Such structures are thyristors because the anodes and the cathodes are connected to the V_{CC} and GND, respectively, of the integrated circuit, and inputs and outputs of the circuit form the gates of these thyristors. If a sufficiently high current is injected into a termination of this kind, the thyristor fires. A short circuit is produced between the supply-voltage rails, resulting in a high probability that the component will be destroyed.

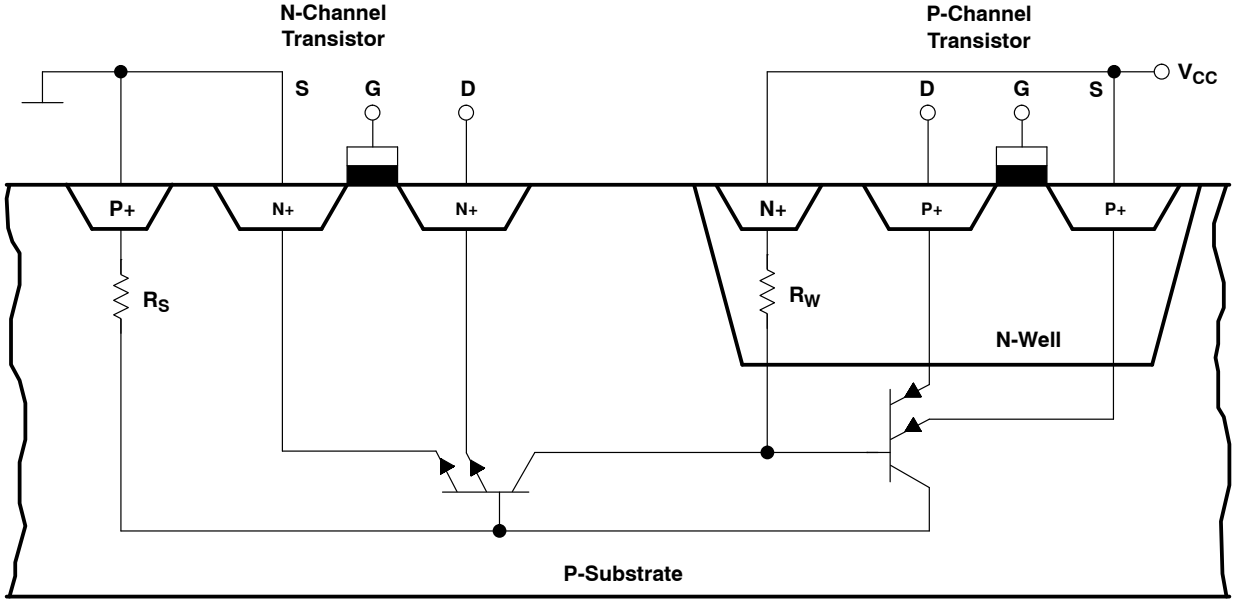


Figure 13. Parasitic Transistors in a CMOS Device

In the early days of CMOS technology, the latch-up effect was a major problem for system designers. Often, many additional precautions had to be taken in a system to avoid excessive currents in the connections to integrated-circuit devices. This inevitably increased the cost of the complete equipment. To counteract the disadvantage of CMOS devices at that time, precautions were taken later when designing the device to prevent latch-up from occurring. This began with the choice of a high-resistance substrate to prevent the spreading of undesired currents. In addition, n- or p-doped guard rings (see Figure 14) were placed around critical parts of the circuit that were connected to the corresponding supply-voltage rails. These guard rings function as additional collectors of the parasitic transistors. Since these collectors are considerably closer to the corresponding base-emitter areas than the bases of the complementary transistors, they take the major part of the current that wanders about in the substrate. In this way, the thyristor is not completely eliminated. However, its sensitivity is reduced to such an extent that, under normal operating conditions, triggering the thyristor is not expected. During the characterization of a new component (type testing), its resistance to latch-up also is checked. With AHC circuits, a current of ±300 mA is applied to all relevant pins of the device under test. At an ambient temperature of 125°C and V_{CC} = 7 V, latch-up must not occur. At room temperature, currents of more than 1 A typically are necessary to cause latch-up.

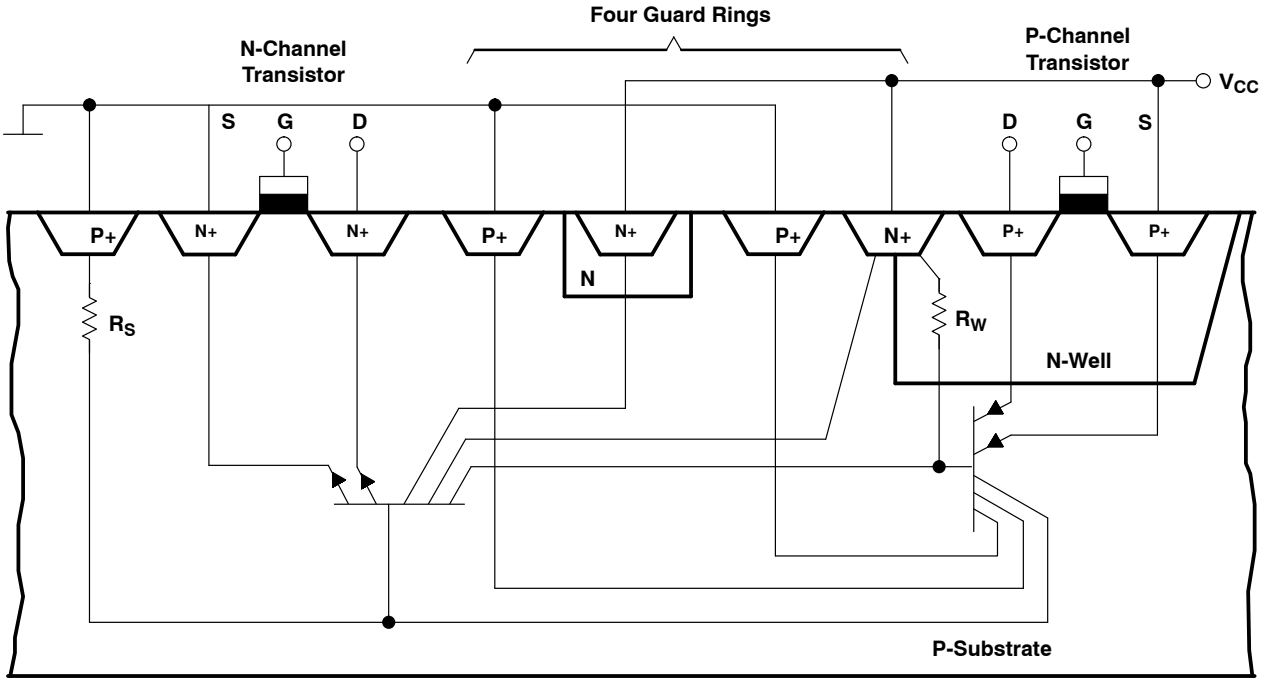


Figure 14. Guard Rings in a CMOS Device

3. Dynamic Behavior

An important parameter when choosing a device is the delay time. Table 4 gives a comparison between HC/HCT and AC/ACT devices. Advanced high-speed CMOS devices are about three times faster than comparable HC devices; AHC and the TTL-compatible AHCT devices have only minor differences with regard to their dynamic characteristics.

Table 4. Comparison of the Delay Times of HC and AHC Devices

DEVICE	SN74HC	SN74HCT	SN74AHC	SN74AHCT
’244 buffer	13 ns	15 ns	5.8 ns	5.4 ns
’245 transceiver	15 ns	14 ns	5.8 ns	4.5 ns
’373 latch	15 ns	20 ns	5 ns	5 ns
’374 flip-flop	17 ns	25 ns	5.4 ns	5 ns

3.1 Power Dissipation

The power dissipation of a CMOS circuit is made up of three distinct components:

- Quiescent power dissipation, P_r
- Internal switching losses, P_s
- Losses P_l, that result from the load connected to the output

The following expression thus applies:

$$P_{ges} = P_r + P_s + P_l \quad (1)$$

The quiescent power dissipation, P_r, is calculated as the product of the supply voltage, V_{CC}, and the quiescent current, I_{CC}, as given in the data sheet. This quiescent current results primarily from the leakage currents of the reverse-biased p-n junctions in the integrated circuit. At room temperature, it is only a few nanoamperes. This current usually can be neglected, but leakage currents in depletion layers typically double with a temperature increase of 10°C. In equipment that is operated at high temperatures, this leakage current can be significant.

The switching loss, P_s, results from charging, discharging, and switching processes inside the device. The charge and discharge of the internal capacitances of the circuit make up a minor part of the total. The major part comes from the current spikes that occur when switching every CMOS stage and which, in this case, primarily affect the output stage. If a CMOS output stage (shown in Figure 8) is switched from a high to low logic level or vice versa, the control voltage on the gate of the transistor within the device only rises (or falls) in a finite time from low to high. The complementary transistor also is being driven in this finite time. Thus, at the moment of switchover, both transistors conduct simultaneously for several nanoseconds. Therefore, a considerable current flows for a short time (see Figure 15) in the circuit. When measuring this current, care must be taken not to capacitively load the output being measured.

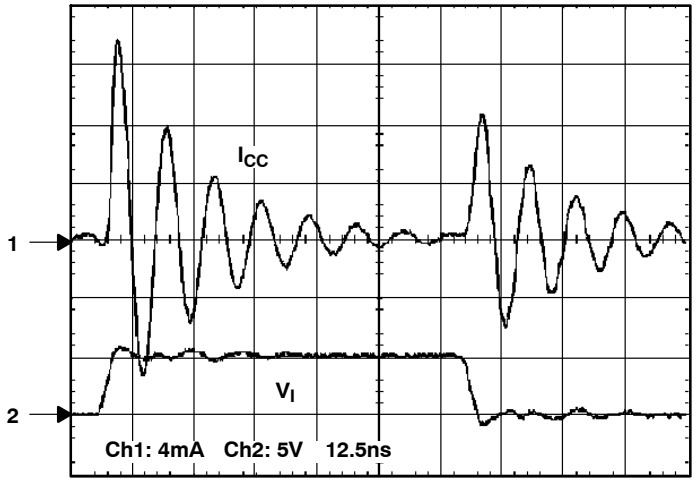


Figure 15. Current Spikes When Switching an AHC Output

The charge, Q, and the energy consumed can be calculated at every switching cycle from the amplitude of the current and its waveform over a period of time. In this way, switching loss, P_s, can be calculated. In practice, a simpler process is used. The supply current, I_{CCS}, of the circuit being considered is measured at a specific input frequency, f_I, but the output must not be loaded. This current consumption can be thought of as generated by an equivalent power-dissipation capacitance, C_{pd}, at the output of the circuit. The following expression then applies:

$$I_{CCS} = C_{pd} \cdot V_{CC} \cdot f_I \quad \textbf{(2)}$$

or

$$C_{pd} = \frac{I_{CCS}}{V_{CC} \cdot f_I} \quad \textbf{(3)}$$

This power-dissipation capacitance, C_{pd}, is given in the data sheet. In a particular application, the following formula can be used to calculate the switching loss P_s:

$$P_s = C_{pd} \cdot V_{CC}^2 \cdot f_I \quad \textbf{(4)}$$

Where:

V_{CC} = Supply voltage (V)
f_I = Input frequency (Hz)
C_{pd} = Power-dissipation capacitance (F)

For circuits with 3-state outputs, such as the SN74AHC244, two C_{pd} values are given. One is for the case in which the output is active, and the other for the case in which the output is in the inactive high-impedance state.

The third component of the total power dissipation, P_{ges}, is contributed by the charging and discharging of the load connected to the output. The simplified assumption is that the load connected consists of a capacitor, C_L. The power dissipation, P_l, resulting from this load can be calculated as follows:

$$P_I = C_L \cdot V_{CC}^2 \cdot f_O \quad \textbf{(5)}$$

Neglecting the quiescent power dissipation, P_r, the following expression gives total power dissipation:

$$P_{ges} = \left(C_{pd} \cdot f_I + C_L \cdot f_O\right) V_{CC}^2 \quad \textbf{(6)}$$

For a SN74AHC244, the data sheet gives a power-dissipation capacitance, C_{pd}, of 8.6 pF. With a capacitive load, C_L, of 50 pF and V_{CC} = 5 V, the following then applies:

$$P_{ges} = (8.6\ \text{pF} \cdot f_I + 50\ \text{pF} \cdot f_O)5^2 \quad \textbf{(7)}$$

With a buffer such as the SN74AHC244, the input and output frequencies are the same ($f_I = f_O$). In this case, the resulting power dissipation per output becomes:

$$P_{ges} = 1.47\ \text{mW/MHz} \quad \textbf{(8)}$$

Figure 16 provides a comparison between the theoretical power dissipation calculated from the formula above and the dissipation actually measured. There is good correlation between the theoretical result and the measurements made. Figure 17 shows the measurement results at a supply voltage V_{CC} = 3.3 V and load of 50 pF or with no load at the output.

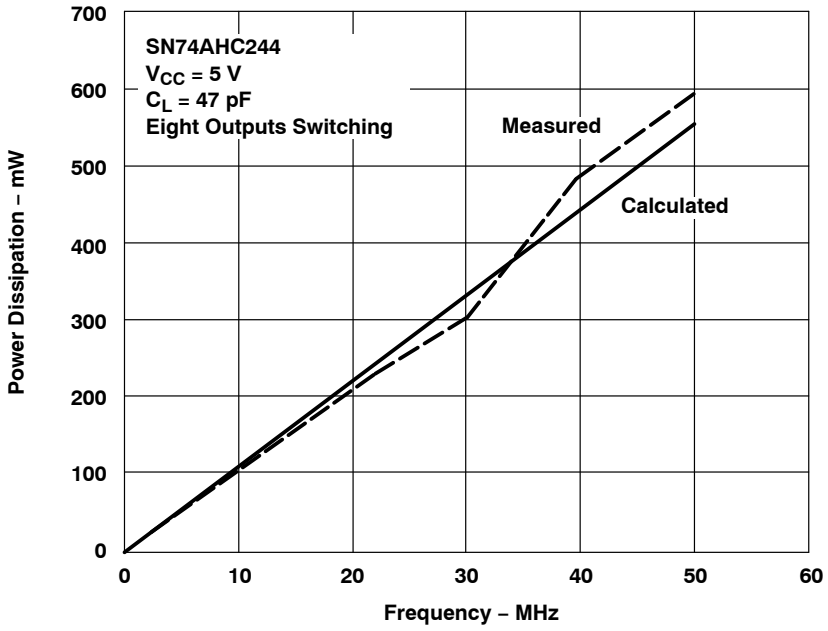


Figure 16. Power Dissipation of SN74AHC244 Bus-Interface Device (V_{CC} = 5 V)

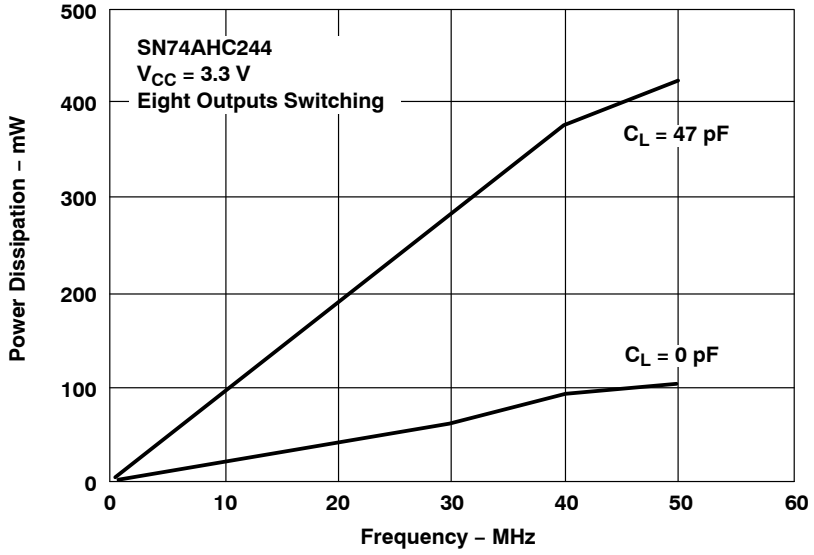


Figure 17. Power Dissipation of SN74AHC244 Bus-Interface Device (V_{CC} = 3.3 V)

3.2 Quality of the Waveforms

An important parameter that significantly affects a circuit or system is the quality of the waveforms. The signals transmitted by the output of an integrated circuit are influenced in many ways en route to the receiver. One form of interference is cross talk, which is coupled from nearby lines to the line where the transmission is occurring. With fast logic circuits, additional interference is generated within the circuits themselves, which can be traced back to the voltage drops across the inductances of the package. Last, waveform distortions occur as a result of reflections along the line.

3.2.1 Cross Talk

The cross talk between adjacent signal lines results from the undesirable inductive and capacitive coupling between them. A precise mathematical treatment of this phenomenon is very complicated, particularly because the precise electrical characteristics of the lines, such as the line inductance and capacitance and the line mutual inductance and mutual capacitance, must be known. For the system designer, it usually is sufficient to know the behavior of typical configurations to draw conclusions about similar situations in other applications. Typical line configurations are illustrated in Figure 18.

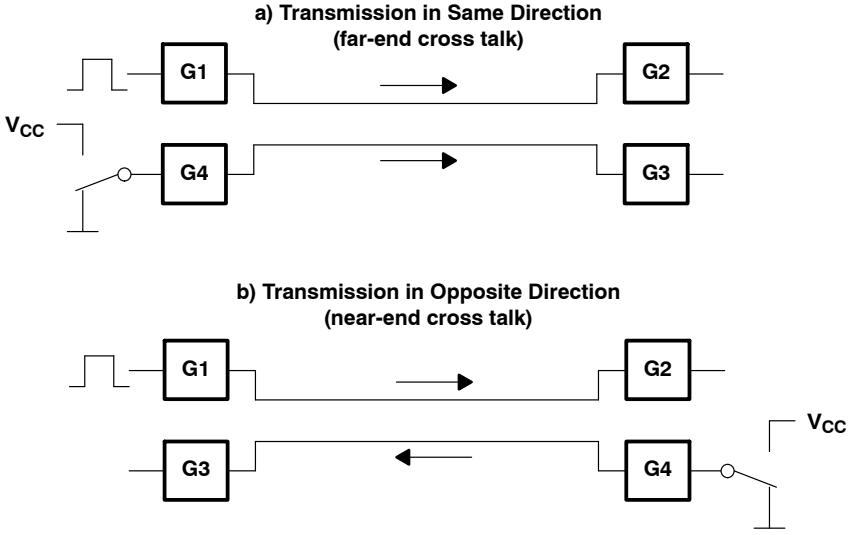


Figure 18. Power Transmission in Same and Opposite Directions

For the following measurements, a measurement setup was used in which on a circuit board two 0.6-mm wide, conductors with a spacing of 0.6 mm were run parallel over a distance of 25 cm. Experience has shown that significantly different results are not obtained with a narrower conductor width, provided the ratio of conductor width to conductor spacing is 1:1.

If gate G1 is switched to have transmission in the same direction (see Figure 18a), the change of voltage is coupled inductively and capacitively into the line running parallel with it. The interfering signal first encounters the low resistance output of gate G4, where it is largely short circuited. After the waveform arrives at the end of the line subjected to this interference, only a low level of interference voltage will be measurable at the input of gate G3 (see Figure 19). With respect to cross talk, this configuration, known as far-end cross talk, is not critical.

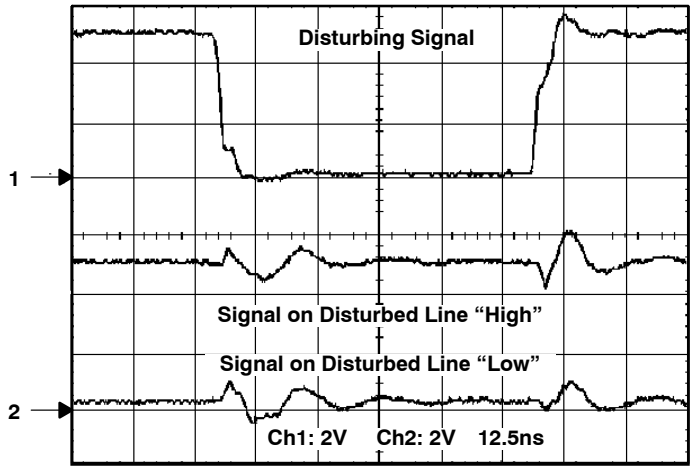


Figure 19. Far-End Cross Talk With Line Length of 25 cm

The behavior is different with transmission in opposite directions (see Figure 18b). The interfering signal, which is coupled into the disturbed line when gate G1 is switched, encounters the high-resistance input of G3 and has significant effects. The disturbance then runs to the end of line G3–G4 (output at G4). Because the output impedance of this gate typically is significantly lower than the line impedance, the interfering waveform is reflected with reversed polarity. After its return, the disturbance will arrive at the input of gate G3. At this point, an interfering pulse can be expected, the length of which is determined as a result of its doubled signal propagation time on this line. Line length directly influences the magnitude of the interference. This considerably more critical manifestation of cross talk is known as near-end cross talk. In the example shown, AHC devices should not have been disturbed. Their switching threshold is typically about 2.5 V, providing an adequate noise margin. In contrast, the situation is different when G3 (see Figure 18b) has a TTL-compatible input stage with a threshold voltage of 1.5 V. In this case, the switching threshold of the circuit that is disturbed is clearly exceeded and experience has shown that this can lead to false triggering. As mentioned previously, the length of the interference pulse, t_w, is in accordance with the doubled signal propagation time on the line in question. With a line having a length of 25 cm and a typical signal propagation time of 6 ns/m (see Figure 20), the width of the resulting interference pulse is:

$$t_w = 2 \cdot t_p \cdot l = 2 \cdot 6\frac{ns}{m} \cdot 25\ cm = 3\ ns \quad (9)$$

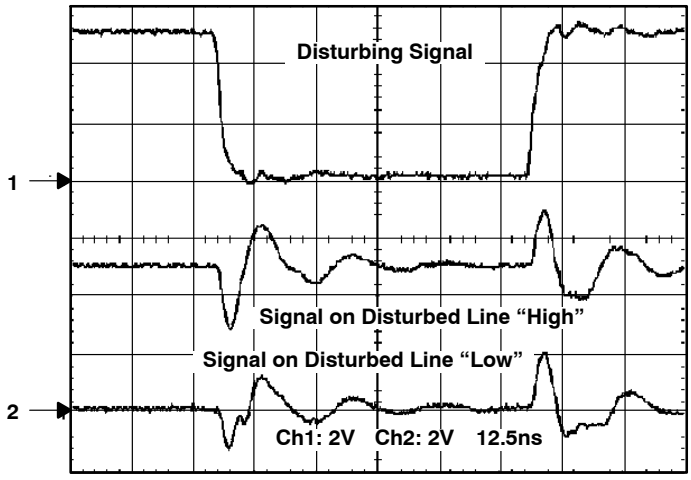


Figure 20. Near-End Cross Talk With Line Length of 25 cm

There are various ways to reduce cross talk between signal lines. One method is to shorten the length of signal paths. In most cases, this will solve the problem because most connecting paths on circuit boards are significantly shorter than 25 cm. With a line length of 12 cm, which covers the majority of connections on circuit boards, signal propagation time, t_p, is 0.75 ns; thus, the width of the interference impulses, t_w, that can be expected is 1.5 ns. Under these conditions, at least as far as cross talk is concerned, there should be no more problems. Also, with appropriate construction of the circuit board, the coupling between the signal lines can be reduced. One precaution consists of incorporating a continuous ground plane under the signal lines. This usually is achieved by correct construction of multilayer circuit boards. With these boards, supply voltage layers (V_{CC} and ground), which lie directly over one another, reduce disturbances on the supply voltage rails and produce significantly less cross talk.

As shown in Figure 21, screening between critical lines provides a significant improvement in every case. For these measurements, an additional ground line having a width of 0.6 mm was placed between the signal lines. As a result of the reduction of the undesired coupling, the amplitude of the coupled signal was reduced. With construction of this kind, transmission over considerably greater distances also is possible. Having a ground layer under the signal lines and a signal-return ground line beside the signal line significantly improves the electromagnetic compatibility of the circuit. Both precautions reduce the area of the effective antenna. In this way, the danger of undesirable radiation of electromagnetic energy and the sensitivity of the circuit to radiation from outside is reduced.

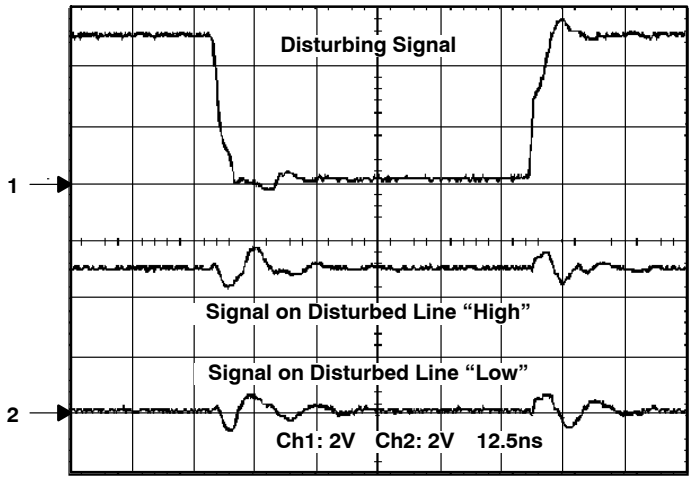


Figure 21. Near-End Cross Talk With Screening Between the Lines and Line Length of 25 cm

3.2.2 Ground Bounce

Shifts of the ground potential (ground bounce) can have various causes. They can result from voltage drops across the ohmic resistance of the ground connections of a circuit. These dc voltage drops can be neglected in most cases. The situation is different with voltage drops that result from rapid current changes in the inductances of the lines. The inductances of the connections within an integrated circuit have significant implications for proper operation of the device. If one or more outputs in an integrated circuit are switched simultaneously, voltage drops on the supply voltage connections can influence the potential at an output that is not involved. The expression used in this case is simultaneous switching noise interference as a result of switching several outputs at the same time.

This behavior can be explained in more detail by referring to the circuit in Figure 22. The input of inverter Q1/Q2 is switched from a low to a high logic level while the input of inverter Q3/Q4 is at a high logic level. The current that flows when discharging capacitor C1 results in a voltage drop across inductances, L_g, of the connections within the package, in this case, primarily the inductance of the ground connections. This raises the internal ground potential of the integrated circuit. This change of voltage can be calculated using the following formula:

$$\mu = L \cdot \frac{di}{dt} \tag{10}$$

It is this change of voltage that appears with undiminished amplitude at the output of inverter Q3/Q4, and the output potential should remain constant. Circuits connected to its output may be influenced by this disturbance. The same effect, but with opposite polarity, occurs when the output in question is at a high logic level and the other outputs of the circuit are switched from a low to a high logic level.

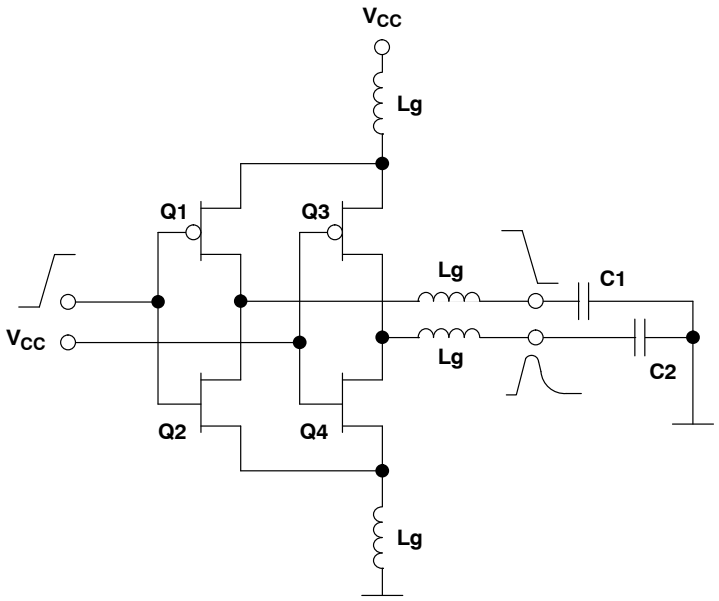


Figure 22. Formation of Shifts of Ground Potential

The interference voltage that can be expected at an output that is in a quiescent state is proportionately higher as the number of outputs that switched simultaneously is increased. These disturbances commonly are known as simultaneous-switching noise, and only devices that can switch several outputs simultaneously are affected. Of principal interest are bus-interface circuits with 4, 8, 16, and even 20 outputs. To evaluate these effects, the measurement setup in Figure 23 has proven to be most effective. With an n-channel circuit, n − 1 outputs are driven simultaneously, while the remaining outputs stay in a quiescent state. All outputs have a 50-pF load (load capacitance includes probe and jig capacitance). This capacitance has proven to be a good choice. Smaller capacitors are not recommended because they would be charged and discharged so rapidly during the switching process that the current could not reach its maximum value. Conversely, capacitors larger than 50 pF do not give rise to any higher currents because currents are limited by the drive capability of the circuit under investigation.

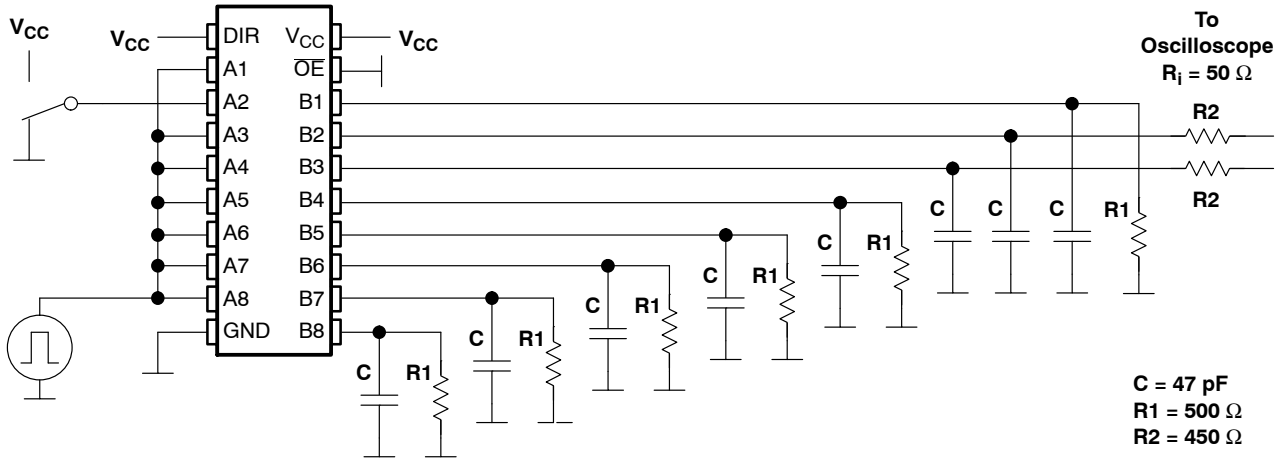


Figure 23. Circuit for Evaluating Simultaneous-Switching Noise (8-Bit SN74AHC245, V_{CC} = 5 V)

Figure 24 shows the interference voltage that arises when simultaneously switching several outputs as measured on an SN74AHC245 bus-interface device in a dual-in-line (N) package. The measured output B2 (see Figure 23) is at a low logic level, while seven other outputs are switched simultaneously from high to low.

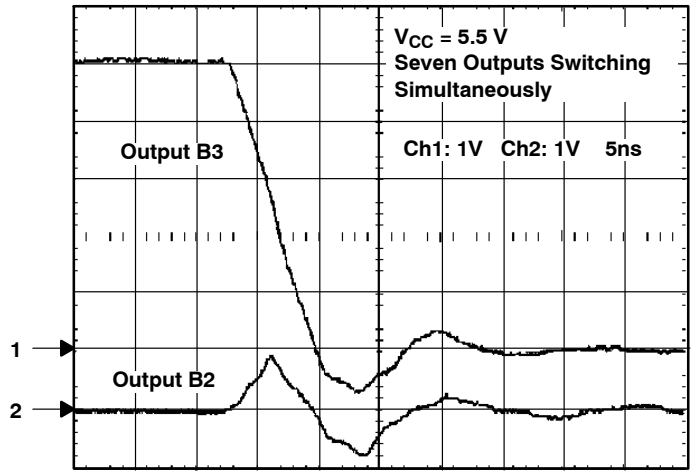


Figure 24. Simultaneous-Switching Noise of SN74AHC245 (V_{CC} = 5.5 V)

With a reduction of the supply voltage, the output current supplied by the circuit is also reduced. The simultaneous-switching noise (see Figure 25) also is reduced.

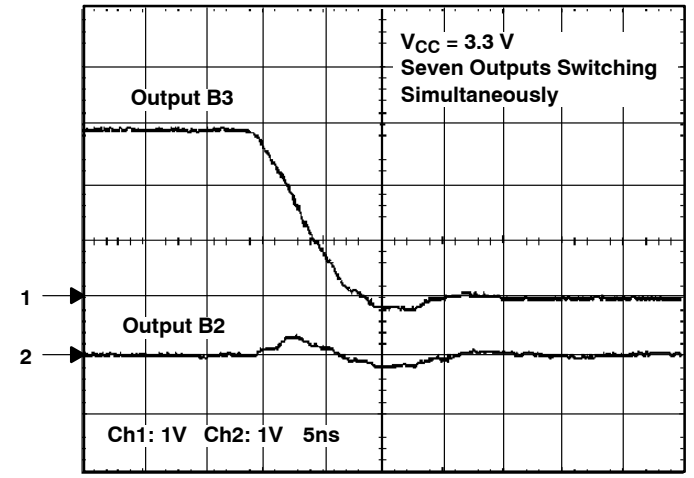


Figure 25. Simultaneous-Switching Noise of SN74AHC245 (V_{CC} = 3.3 V)

A general conclusion can be drawn from the considerations detailed previously that packages intended for surface mounting (for example, the SO package) should show significantly better behavior than packages that are considerably larger and are intended for through-hole mounting (DIL package), because their smaller mechanical dimensions should lead to lower values for the inductances of the internal connections. These conclusions are basically correct, as shown in Table 5. However, if the inductances of the supply pins of a circuit are reduced, the primary result will be an increase in speed because of improved voltage response, which is, for example, evidenced by a significantly shorter delay time. For this reason, the interference voltages measured on SO packages typically are only about 10% to 20% smaller than with DIL packages. Only when critical inductances are reduced to below about 2 nH will the interference become smaller in proportion to the reduction of the inductances. Below this value, experience has shown that the speed of the circuit is determined by the limits imposed by the semiconductor technology.

Table 5. Inductances of a 20-Pin Package

PACKAGE	PIN INDUCTANCE AT THE ENDS OF THE PACKAGE (PINS 1, 10, 11, 20)	PIN INDUCTANCE IN THE MIDDLE OF THE PACKAGE (PINS 5, 6, 15, 16)
DIL	13,7 nH	3,4 nH
SO	4,2 nH	2,4 nH

Besides the effect of the voltage drop across the inductances of the supply lines, the amplitude of the noise voltage also is determined by the cross talk between the pins of the package. One of the consequences is that the measured interference voltage is at a maximum at those pins that have simultaneously switching outputs on both sides. Conversely, interference voltages at the ends of the package are significantly lower. When low distortion of the signal is particularly important in specific applications, the latter situation can be attained by appropriate routing of the signals. As a result of the many supply voltage connections distributed around the perimeter of Widebus packages (see Figure 26), harmful inductance is reduced in accordance with the number of parallel electrical connections. Also, supply lines between the signal lines reduce the coupling between signal lines, further contributing to the low level of interference voltage.

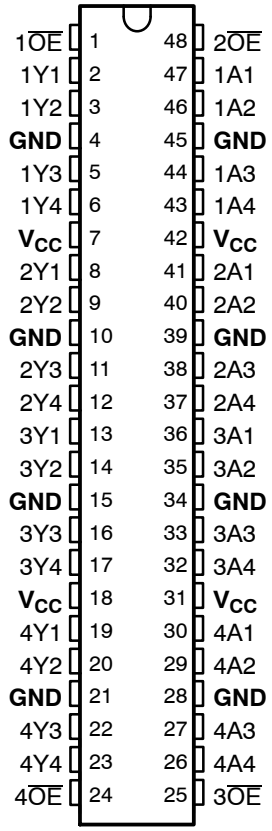


Figure 26. Pin Layout of an SN74AHC16244 Widebus Device

3.3 Signal Transmission

The principal purpose of digital devices (besides implementing logic functions) is driving other digital circuits. In some cases, the devices can be connected on a printed circuit board by printed wires that are only a few millimeters long or in other cases, a bus line connects several other transmitters and receivers (transceivers). The behavior of AHC circuits under a variety of operating conditions is discussed in the following paragraphs.

3.3.1 Point-to-Point Connections

For point-to-point connections (see Figure 27), line impedances of 70 Ω to 100 Ω for the conductors on circuit boards can be assumed. The line is terminated at its end by a circuit that essentially is as shown in Figure 27. For positive voltages, this line termination has a high resistance and negative-going overshoots are limited by clamping diode D1. Under these conditions, AHC circuits will have no problem driving the loads connected to them.

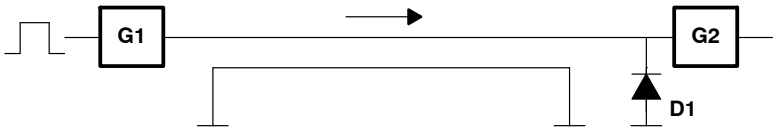


Figure 27. Typical Point-to-Point Connection

Figure 28 shows the waveform at the beginning and at the end of a line having an impedance, Z_O, of about 100 Ω. Because output impedance of the circuit is about 35 Ω, overshoots and undershoots at the end of the line are sufficiently limited. The clamping diode at the input of the receiver circuit limits negative voltages to acceptable values.

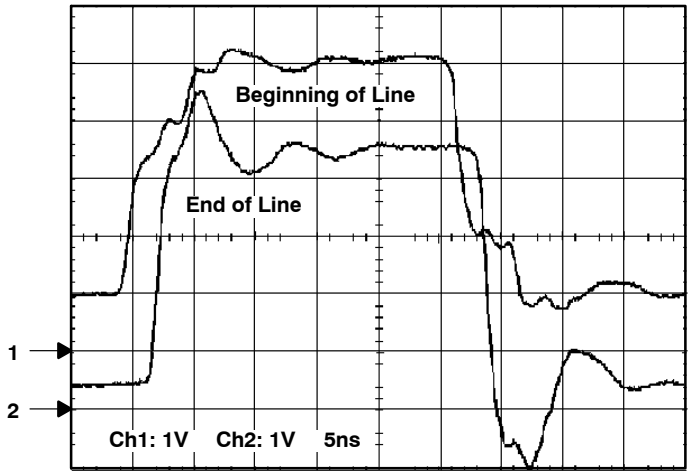


Figure 28. Waveform in a Point-to-Point Connection

In some cases it may be necessary to take additional precautions to reduce distortion resulting from reflections at the line ends. The options are to provide an appropriate termination at the end of the line or a matching circuit at the beginning of the line.

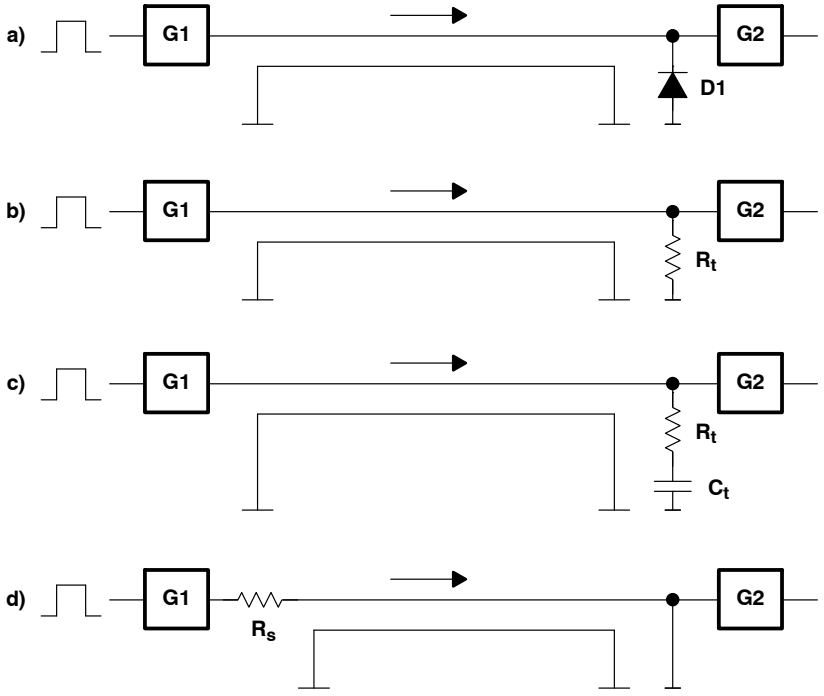


Figure 29. Line Termination and Matching

The use of clamping diodes (D1 in Figure 29a) is the most effective method of termination, especially when the protection diodes already incorporated in the input circuits of AHC devices can take on this job. In some cases, limiting positive overshoots may also be advisable. In this case, additional diodes should be connected between the input and the positive supply-voltage connection terminal.

The use of termination resistors of the proper value at the end of the line (R_t in Figure 29b) produce ideal waveforms. However, the higher power dissipation in the termination resistors, which results from this arrangement, usually outweighs the advantage of the low distortion of the signal.

If a termination at the end of the line cannot be avoided, connecting a termination resistor and a capacitor in series is recommended. This blocks dc from the terminating network and reduces power consumption of the circuit. Capacitor C_t in Figure 29c is chosen so that the time constant $R_t \times C_t$ is approximately four times the signal propagation time along the line.

A more elegant method of preventing undershoots and overshoots at the end of the line consists of matching the output impedance of the line driver with a series resistor (R_s in Figure 29d) to the line impedance. This makes optimum matching possible, without adversely affecting the balancing of the line.

3.3.2 Bus Lines

In addition to point-to-point connections previously mentioned, bus lines have great importance in computer systems. In this application several transmitter and receiver circuits, or combinations of them as transceivers, are situated along a line (see Figure 30). Each of these circuits loads the system with its input capacitance, which leads to a significantly longer signal propagation time ($t_p \approx 20$ ns/m) and to line impedances, Z_O, of about 30 Ω.

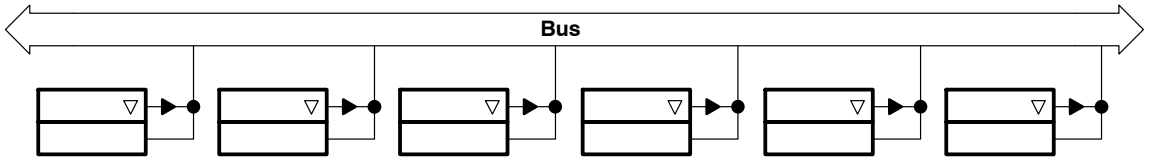


Figure 30. Bus Line

Because line impedances are now the same as, or smaller than, the output impedances of the AHC circuits, no more undershoots or overshoots occur at the end of the line (see Figure 31). Thus, in general, it is possible to dispense completely with line terminations. However, because of the unfavorable impedance relationships, four to six signal-propagation time periods will have passed before the desired logic level is reached. In smaller systems, and with bus lines having a length of only a few centimeters, this disadvantage is acceptable. The possibility of being able to dispense almost entirely with precautions to prevent reflections along the line usually completely outweighs the disadvantage of the longer settling time. With longer bus lines and their resultant longer settling times, voltage levels will exist for a longer time at the inputs of the receivers connected to the bus, which do not conform to the nominal voltage of the input signal. Figure 31 shows that with the incident wave at the end of the line, a level has been reached that is only very close to the threshold voltage of the receivers that are connected. In these circumstances, operation of the circuit without problems cannot be ensured. With longer bus lines and when shorter settling times are needed, components with better drive capability, such as those from the series SN74LVC and SN74ALVC, should be used.

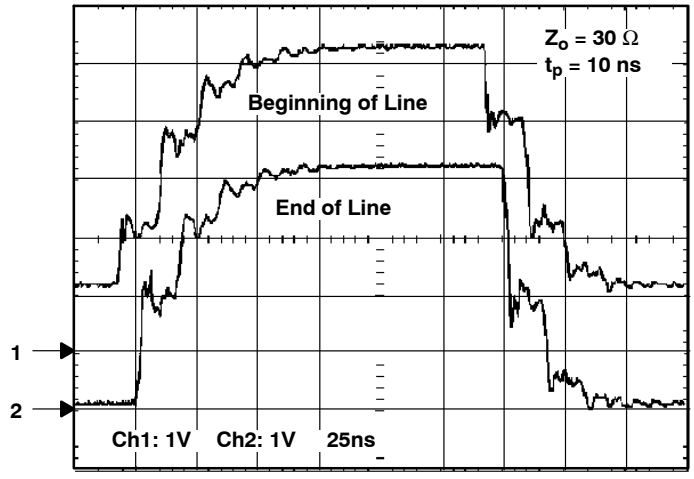


Figure 31. Waveform on a Bus Line

3.4 Behavior With Slow Signal Edges

During the development of the AHC devices, precautions were taken to prevent the internal circuit of the devices from oscillating with input signals having slow edges. The hysteresis built into the input stages provides for operation without problems only with signals that are usually delivered by logic circuits. The permissible transition time of the input signal is given in the data sheet as t_B = 10 ns/V. With a signal swing of 5 V, this corresponds to a rise and fall time $t_{r/t}$ < 45 ns. If a typical rise time of the output signals of AHC circuits of $t_{r/f}$ < 5 ns is assumed, there is a sufficient margin available within the circuit. In practice, input circuits also can typically process signals with significantly slower edges. Figure 32 shows the behavior of SN74AHC244 bus-interface device when it is controlled by extremely slow signals ($t_f \approx$ 100 ns). Even under these conditions, the device shows no tendency to oscillate. However, this example should not tempt the system designer generally to allow signals with such slow edges. If rise times of the input signal that lie outside the previously given specification can be expected, the Schmitt trigger, which has been specially developed for this application, always should be used.

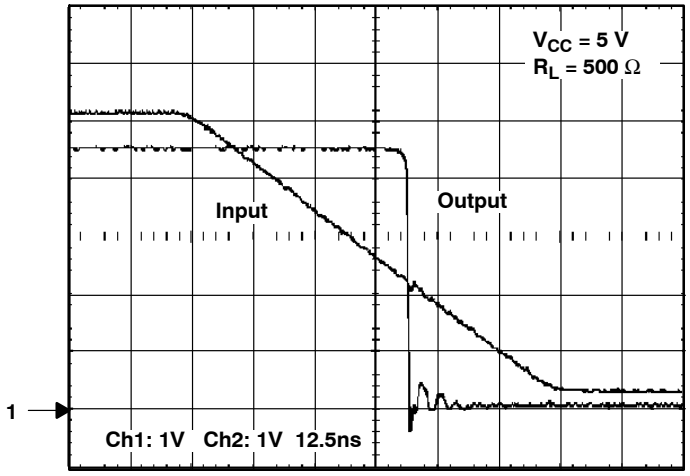


Figure 32. Behavior With Extremely Slow Input Signals

4. Special Application Problems

For several years, systems have been designed and manufactured to use two or more supply voltages, 3.3 V and 5 V. The reason is that, with the introduction of the so-called low-voltage logic circuits, all components needed were not available and, in some cases, still are not. Therefore, often there was no alternative but to use integrated circuits requiring a supply voltage of 5 V in systems conceived for a supply voltage of 3.3 V. Special circuit techniques are then required at the interfaces. The problems involving the use of several supply voltages can be expected to increase in the future. With components having structures of <0.5 µm being manufactured, still lower operating voltages will be needed, and the problem mentioned above will appear again in another form. Level conversion and matching will remain an applications problem.

4.1 Level Matching and Conversion

Level matching between parts of circuits that operate with different supply voltages, for example, 3.3 V and 5 V, is very simple if AHC and AHCT circuits are used (see Figure 33). Protection circuits at the inputs of these components do not contain any diodes between the input and the supply-voltage connection. The problem of feedback from a part of the circuit that is switched off does not exist.

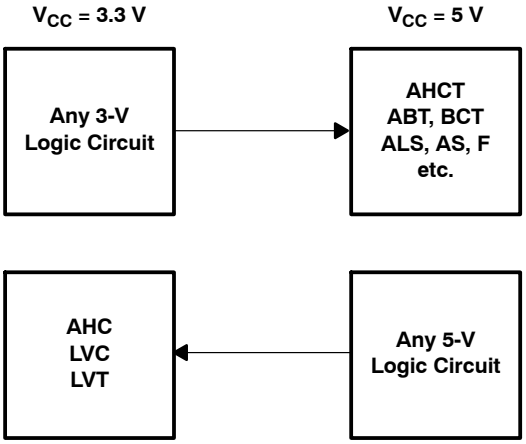


Figure 33. Level Conversion

All circuits designed for V_{CC} = 3.3 V deliver TTL-compatible signal levels at their outputs. When controlling parts of the circuit that operate at V_{CC} = 5 V, TTL-compatible devices must be used on the 5-V side. Also, these integrated circuits must not have any of the clamping diodes mentioned above. For this purpose, AHCT devices, as well as all bipolar and BiCMOS circuits are suitable. HCT and ACT devices should not be used. Level problems should not be expected when choosing suitable interface circuits for level converters from 5 V to 3 V. With few exceptions, for example, ALVC, devices that have been designed for V_{CC} = 3.3 V can be controlled with a signal swing of up to 5 V. Also, in this case, care must be taken that only components are used on the 3.3-V side that do not contain the clamping diodes mentioned above. Circuits from the series SN74HC, SN74AC, and SN74LV are not suitable for this purpose.

Table 6. Level Converters, 5 V to 3.3 V

FROM V_{CC} = 5 V	TO V_{CC} = 3 V							
	LV	LVC	ALVC	HC	AC	AHC	LVT	ALVT
Bipolar TTL	No	Yes	No	No	No	Yes	Yes	Yes
BiCMOS (ABT, BCT)	No	Yes	No	No	No	Yes	Yes	Yes
CMOS	No	Yes	No	No	No	Yes	Yes	Yes

Table 7. Level Converters, 3.3 V to 5 V

FROM V_{CC} = 3.3 V	TO V_{CC} = 5 V				
	BIPOLAR TTL	BiCMOS (ABT, BCT)	AHCT	HC	AC
Any circuit	Yes	Yes	Yes	No	No

4.2 Partial Switching Off of Parts of a System

Partial switching off of parts of a system occurs when part of an equipment or installation is switched off (without supply voltage) while other parts of the equipment remain in normal operation. This operating situation occurs regularly at the interfaces with other equipment. The same state can be observed frequently within a module that operates with several supply voltages, for example, 3.3 V and 5 V. Since the individual power supplies are not switched on and off simultaneously and in coordination, the case in which one or other power supply does not deliver the required voltage must be considered. The simplified output circuit of an AHC/AHCT device is shown in Figure 8. Diode D1 short circuits the output to ground when the supply voltage is switched off (V_{CC} = 0 V). Since this diode has a very low resistance (see Figure 11), this operating state is a defined low-logic level. To this extent, such a circuit provides a defined level. This behavior has disadvantages in bus systems. If the supply voltage of one of the subscribers connected to the bus is switched off, its output short circuits the complete bus line. A solution in such a case can be provided only by using bipolar and BiCMOS circuits, which do not have the diodes shown in Figure 8 in their output stages. In this connection, special mention should be made of the circuits from the SN74ABT and SN74LVT series.

Many of the interface problems discussed here can be solved very easily using integrated circuits specially developed for this purpose, such as the bidirectional 8-bit Widebus transceiver SN74LVC4245 (see Figure 34), or its 16-bit Widebus version SN74ALVC164245. These components have two separate supply-voltage connections [V_{CCA} (5 V) and V_{CCB} (3.3 V)]. In this way it is possible to solve the problems previously discussed by means of appropriate circuitry within the component. The engineer developing a system will no longer be concerned with these problems.

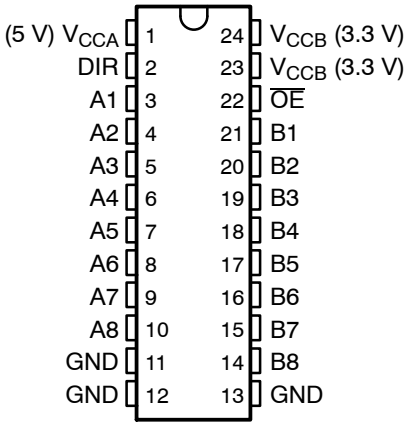


Figure 34. Pin Layout of SN74LVC4245 Transceiver

5. Comparison of AHC and HC Circuits

High-speed CMOS and advanced CMOS circuits have been used for more than a decade in many diverse applications. The HC circuits feature comparatively simple application rules, and this has encouraged their widespread use. AC circuits are found in applications in which high speed (i.e., short delay times) and high drive capability are required. The latter advantages must be weighed against the considerable internal noise (ground bounce, cross talk, etc.) that these circuits generate.

The ideal situation was a combination of the advantages of both logic families. Maintaining the moderate drive capability of HC circuits, which ensures a low internal-noise level, and incorporating the technical advantages offered by a modern manufacturing process with structures of 1 μm, the creation of the advanced high-speed CMOS family became a reality. In addition, particular attention was paid to the increasing trend toward applications operating with supply voltages of only 3.3 V. A number of improvements were also incorporated that facilitate applications with these components: changes to the input circuits, and improved ESD protection. The most important parameters are summarized in Table 8.

Table 8. Comparison of the Logic Families

	PRODUCT FAMILY				
	AHC		HC	LVC	AC
Technology	CMOS		CMOS	CMOS	CMOS
Structure (gate length)	1 μm		2–3 μm	0.8 μm	1 μm
5-V tolerant?	Yes		No	Yes	No
Gate and bus-interface circuits available?	Yes		Yes	Yes	Yes
Widebus circuits (16 bit) available?	Yes		No	Yes	Yes
Bus-hold circuit?	No		No	Yes	No
	V_{CC} = 5 V	V_{CC} = 3.3 V	V_{CC} = 5 V	V_{CC} = 3.3 V	V_{CC} = 5 V
Supply current, I_{CC} ('245)	40 μA	40 μA	80 μA	10 μA	40 μA
Output current	–8/8 mA	–4/4 mA	–6/6 mA	–24/24 mA	–24/24 mA
Delay time, $t_{pd(max)}$ ('245)	6.5 ns	10 ns	26 ns	7.5 ns	9 ns
Input capacitance, C_i ('245)	2.5 pF		4.6 pF	3.3 pF	4.5 pF
Input/output capacitance, C_{io} ('245)	8 pF		16 pF	5.4 pF	15 pF

6. Package Construction

The trend toward further miniaturization of equipment and appliances is continuing, as indicated by the huge range of portable battery-operated equipment now available. Manufacturers of semiconductors are making a major contribution to this trend, because miniaturization can be realized only with smaller packages and corresponding progress in manufacturing technology. System designers always should remain aware of the problems involved in the use of modern packages.

Special manufacturing techniques when encapsulating the integrated circuits (chips) in their packages are employed to overcome problems that can occur. Everything possible must be done to eliminate humidity inside the package. This humidity has less to do with possible corrosion of the integrated circuits because, for the last 20 years, surfaces of all chips have been passivated with a glass layer (nitride), and possible corrosion has lost its significance. Any humidity trapped in the package shows up as a problem with the soldering techniques, for example, flow-soldering baths, now used for surface-mounted components. During the soldering process, humidity can vaporize and cause the package to burst (the “popcorn” effect). Immediately after manufacture, the devices must be stored in a special packing (Dry Pack) and, in some cases, in air-conditioned rooms.

The handling of ever-smaller packages presents a problem for the manufacturing engineer. With a pin spacing of only 0.4 mm, such as that attained with the thin shrink small-outline packages (TSSOP), exceptional demands are placed on soldering techniques, such as the accuracy with which the components are placed in assembly and the precise control of the soldering process. In the past, difficulty in controlling the soldering process often has been responsible for delaying the introduction of smaller packages.

Although maximum permissible power dissipation of the small packages is of secondary significance only for the AHC circuits, miniaturization of components obviously has reduced their ability dissipate heat. The relationships are explained in Table 9. With AHC circuits in the middle-speed class, thermal impedance usually is of little importance; these devices have an extremely low quiescent current drain. Also, in the frequency range up to about 10 MHz, in which these components should be used, the dynamic power dissipation is kept within reasonable limits. In individual cases, for example, at high clock frequencies or with the use of Widebus circuits, the system designer should calculate the power dissipation that can be expected to prevent overloading of these components.

Table 9. Thermal Impedance of 20-Pin Packages

PARAMETER	PACKAGE					UNIT
	DIL	SOP	SSOP	TSSOP	TVSOP	
Thermal impedance, θ_{JA}	67	96.6	104.2	148.9	179.5	°C/W

Figure 35 provides mechanical dimensions of the various packages in which AHC/AHCT families are available. This table is not all inclusive because the many variants of different numbers of package pins from 14 to 56 cannot be shown in the space available. The spectrum of available packages extends from the very well-known and much-used dual-in-line package (DIL), through the well-established small outline package (SO) and up to the thin very small-outline package (TVSOP). With a pin spacing of only 0.4 mm (16 mil) and a height of 1.2 mm, this package is ideal for use in chip cards.

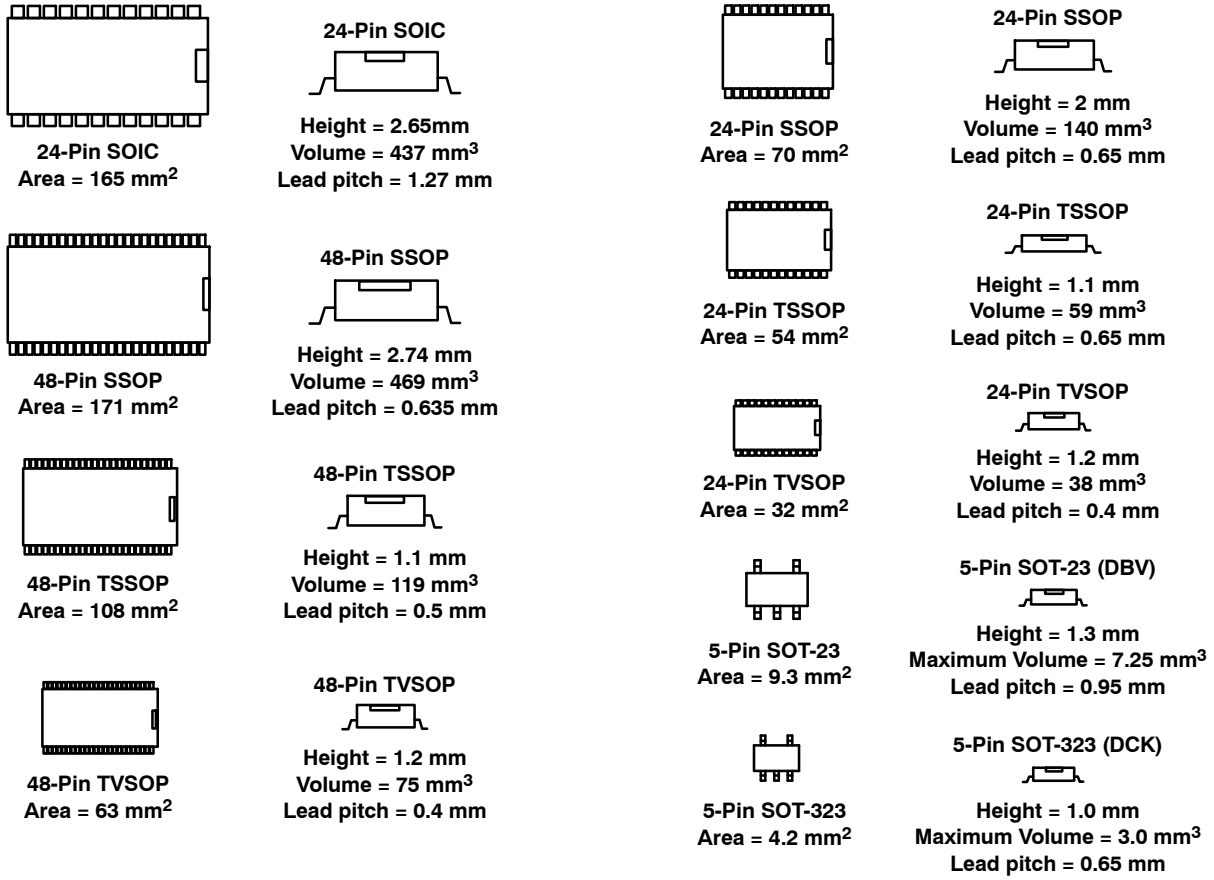


Figure 35. Selected Package Dimensions

6.1 Single-gate Logic

System designers often are confronted with the need for another gate or inverter to complete the design. The reason for this additional component may be, for example, that a signal from one circuit can supply the logic level needed by the subsequent circuit only after inversion. Or, at the last moment, it may be realized that the logical combination of two signals (AND, OR) is needed to implement the required function. Finally, it can be determined that the input signal needs to be amplified or that a Schmitt trigger is required to make an edge steeper so that a following circuit will operate properly.

In the past when this situation arose, it was necessary to incorporate an additional 14- or 16-pin package, which might have been only 25% utilized. Besides the cost of this additional component, the space required becomes of great importance when equipment and systems need to be miniaturized. To meet this need, the Microgate Logic and Picogate Logic packages have been developed. The Microgate Logic circuits are supplied in a 5-pin SOT-23 package, and the Picogate Logic circuits in the still smaller SOT-323 package (Figure 35). The dimensions of Microgate Logic conform to those of the SOT-23, which has long been used for small-signal transistors and has been extended with two additional pins. It should be emphasized that the 5-pin SOT-23 package originally was introduced for use with analog circuits. In analog circuit practice there are far fewer opportunities to construct circuits (such as amplifiers) with standardized components than is the case in digital circuitry where all circuits are basically derived from gates or inverters. Because amplifiers or comparators are chosen for specific functions in the application, the SOT-23 package containing the required function is the logical choice.

Because the SOT-23 package has only five pins, of which two need to be reserved for the supply voltage, the functions that can be integrated into them are limited: AND, NAND, OR, NOR, EXOR gates, and inverters. Other functions, such as the Schmitt trigger, are available that are particularly needed in interfaces. An available often-used function is the unbuffered inverter, designated as ’04U (U = unbuffered). This device has applications in oscillators, and can be used as an analog wideband amplifier.

7. Summary

With their advanced high-speed CMOS logic family, TI has created a series of components that combines the advantages of many integrated circuits that are already well known, without having to accept many of their disadvantages:

- All CMOS circuits have low power requirements in common.
- Delay times have been much improved in comparison with HC devices.
- Values have been reached that were previously possible only with AC devices.

The high driveability of the latter family has not been incorporated – this is reserved for the AC, LVC, and ALVC families – but instead they have been limited in this respect to values that are usual for high-speed CMOS. From the point of view of interference that integrated circuits themselves generate, these components are easy to use. This ease of use extends from their dynamic-power dissipation and low cross talk between signal lines to the precautions necessary to ensure the electromagnetic compatibility of a circuit or system.

8. References

1. Texas Instruments, *AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book*, literature number SCLD004.
2. Texas Instruments, *Semiconductor Group Package Outlines Reference Guide,* literature number SSYU001.
3. *Fachverband Bauelemente der Elektronik: Messung der EME von integrierten Schaltungen* (Professional Association for Electronic Components: Measuring the EME of Integrated Circuits).
4. Texas Instruments, *Digital Design Seminar,* literature number SDYDE01A.

Appendix A

Product Portfolio

ADDITIONAL LITERATURE

For more information on the AHC product line, please visit http://www.ti.com/sc/docs/asl/families/ahct.htm and http://www.ti.com/sc/docs/asl/sin_gate.htm.

If you would like additional AHC literature, please call 1-800-477-8924 and ask for the following items:

TITLE	LITERATURE NUMBER
Logic Selection Guide and Data Book CD-ROM (February 1998)	SCBC001B
Logic Selection Guide	SDYU001
Logic Solutions Overview Brochure (1998)	SCAB003
AHC Sample Kit (1997)	SCLP002
AHC/AHCT Brochure (1998)	SCAB002
AHC/AHCT Logic Advanced High-Speed CMOS Data Book (1997)	SCLD003A
Design Considerations for Logic Products Application Book (1997)	SDYA002

PRODUCT AVAILABILITY

Refer to the following codes for column entries on the following pages.

military package description and availability

CDIP (ceramic dual-in-line package)
J = 14/16/20 pins
JT = 24/28 pins

CFP (ceramic flat package)
WA = 14 pins (small outline)
W = 14/16/20 pins
WD = 48/56 pins

CPGA (ceramic pin grid array)
GB = 68/84/120 pins

CQFP (ceramic quad flat package)
HV = 68 pins
HT = 84 pins
HS = 100 pins
HFP = 132 pins

LCCC (leadless ceramic chip carrier)
FK = 20/28 pins

schedule

✔ = Now
✣ = Planned
★ = Please see the corresponding device data sheet for correct military nomenclature or visit http://www.ti.com/sc/docs/military for TI military product information.

APPENDIX
PRODUCT AVAILABILITY
AHC

DEVICE	NO. OF PINS	FUNCTION	AVAILABILITY						LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	BOT	
SN74AHC1G00	5	Single 2-Input Positive-NAND Gate							✔	SCLS313E
SN74AHC1G02	5	Single 2-Input Positive-NOR Gate							✔	SCLS342D
SN74AHC1G04	5	Single Inverter Gate							✔	SCLS318G
SN74AHC1GU04	5	Unbuffered Single Inverter Gate							✔	SCLS343H
SN74AHC1G08	5	Single 2-Input Positive-AND Gate							✔	SCLS314E
SN74AHC1G14	5	Single Schmitt-Trigger Inverter Gate							✔	SCLS321F
SN74AHC1G32	5	Single 2-Input Positive-OR Gate							✔	SCLS317F
SN74AHC1G86	5	Single 2-Input Exclusive-OR Gate							✔	SCLS323E
SN74AHC1G125	5	Single Bus Buffer Gate With 3-State Outputs							✣	SCLS377B
SN74AHC1G126	5	Single Bus Buffer Gate With 3-State Outputs							✣	SCLS379B
SN74AHC00	14	Quad 2-Input NAND Gate	✔	✔	✔	✔	✔	✔		SCLS227D
SN74AHC02	14	Quad 2-Input NOR Gate	✔	✔	✔	✔	✔	✣		SCLS254E
SN74AHC04	14	Hex Inverter	✔	✔	✔	✔	✔	✔		SCLS231H
SN74AHCU04	14	Unbuffered Hex Inverter	✔	✔	✔	✔	✔	✔		SCLS234F
SN74AHC05	14	Hex Inverter	✣	✣	✣	✣	✣	✣		SCLS357B
SN74AHC08	14	Quad 2-Input AND Gate	✔	✔	✔	✔	✔	✣		SCLS236C
SN74AHC14	14	Hex Inverter With Schmitt Trigger	✔	✔	✔	✔	✔	✣		SCLS238D
SN74AHC32	14	Quad 2-Input OR Gate	✔	✔	✔	✔	✔	✣		SCLS247C
SN74AHC74	14	Dual D-Type Flip-Flop With Preset and Clear	✔	✔	✔	✔	✔	✣		SCLS255D
SN74AHC86	14	Quad Exclusive-OR Gate	✔	✔	✔	✔	✔	✣		SCLS249C
SN74AHC123A	16	Dual Monostable Vibrator	✣	✣	✣	✣	✣	✣		SCLS352A
SN74AHC125	14	Quad Bus Buffer Gate ($\overline{OE}$)	✔	✔	✔	✔	✔	✣		SCLS256E
SN74AHC126	14	Quad Bus Buffer Gate (OE)	✔	✔	✔	✔	✔	✣		SCLS257F
SN74AHC132	14	Quad NAND Gate With Schmitt-Trigger Inputs	✣	✣	✣	✣	✣	✣		SCLS365B
SN74AHC138	16	3-to-8 Decoder/Demultiplexer	✔	✔	✔	✔	✔	✔		SCLS258F
SN74AHC139	16	Dual 2-to-4 Line Decoder/Demultiplexer		✔	✔	✔	✔	✔		SCLS259F
SN74AHC157	16	Quad 2-to-1 Data Selector/Multiplexer	✔	✔	✔	✔	✔	✔		SCLS345D

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✔ = Now ★ = See page A–3
✣ = Planned

MIL See page A–3 for military package description and availability

TEXAS INSTRUMENTS

DEVICE	NO. OF PINS	FUNCTION	AVAILABILITY						LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	BOT
SN74AHC158	16	Quad 2-to-1 Data Selector/Multiplexer		✔	✔	✔	✔	✔	SCLS346C
SN74AHC174	16	Hex D-Type Flip-Flop With Clear	✣	✣	✣	✣	✣	✣	SCLS425
SN74AHC240	20	Octal Buffer/Driver	✔	✔	✔	✔	✔	✣	SCLS251D
SN74AHC244	20	Octal Buffer/Driver	✔	✔	✔	✔	✔	✔	SCLS226F
SN74AHC245	20	Octal Bus Transceiver	✔	✔	✔	✔	✔	✔	SCLS230E
SN74AHC257	20	Quad 2-to-1 Data Selector/Multiplexer		✣	✣	✣	✣	✣	SCLS349C
SN74AHC258	20	Quad 2-to-1 Data Selector/Multiplexer		✣	✣	✣	✣	✣	SCLS350C
SN74AHC273	20	Octal D-Type Flip-Flop With Clear	✔	✔	✔	✔	✔	✔	SCLS376C
SN74AHC367	16	Hex Buffer and Line Driver With 3-State Outputs	✣	✣	✣	✣	✣	✣	SCLS424
SN74AHC373	20	Octal D-Type Transparent Latch	✔	✔	✔	✔	✔	✣	SCLS235E
SN74AHC374	20	Octal D-Type Flip-Flop	✔	✔	✔	✔	✔	✣	SCLS240E
SN74AHC540	20	Inverting Octal Buffer/Driver	✔	✔	✔	✔	✔	✣	SCLS260E
SN74AHC541	20	Octal Buffer/Driver	✔	✔	✔	✔	✔	✣	SCLS261I
SN74AHC573	20	Octal D-Type Transparent Latch	✔	✔	✔	✔	✔	✣	SCLS242F
SN74AHC574	20	Octal D-Type Flip-Flop	✔	✔	✔	✔	✔	✣	SCLS244D
SN74AHC594	16	8-Bit Shift Register With Output Registers	✣	✣	✣	✣	✣	✣	SCLS423
SN74AHC595	16	8-Bit Shift Register With 3-State Output Registers	✣	✣	✣	✣	✣	✣	SCLS373B
SN74AHC4040	16	12-Bit Asynchronous Binary Counter	✣	✣	✣	✣	✣	✣	SCLS422
SN74AHC4051	16	Analog Multiplexer/Demultiplexer	✣	✣	✣	✣	✣	✣	SCLS415
SN74AHC4053	16	Analog Multiplexer/Demultiplexer	✣	✣	✣	✣	✣	✣	SCLS416
SN74AHC4066	14	Quad Bilateral Analog Switch		✣	✣	✣	✣	✣	SCLS421
SN74AHC16240	48	16-Bit Buffer/Driver	✣			✔	✔	✔	SCLS326D
SN74AHC16244	48	16-Bit Buffer/Driver	✣			✔	✔	✔	SCLS327D
SN74AHC16245	48	16-Bit Bus Transceiver	✣			✣	✣	✣	SCLS328B
SN74AHC16373	48	16-Bit D-Type Transparent Latch	✣			✔	✔	✔	SCLS329C
SN74AHC16374	48	16-Bit D-Type Flip-Flop	✣			✔	✔	✔	SCLS330D
SN74AHC16540	48	16-Bit Inverting Buffer/Driver	✣			✔	✔	✔	SCLS331C
SN74AHC16541	48	16-Bit Buffer/Driver	✣			✔	✔	✔	SCLS332C

commercial package description and availability

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DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
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schedule

✔ = Now ★ = See page A–3
✣ = Planned

MIL See page A–3 for military package description and availability

TEXAS INSTRUMENTS

APPENDIX
PRODUCT AVAILABILITY
AHCT

DEVICE	NO. OF PINS	FUNCTION	AVAILABILITY						LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	BOT	
SN74AHCT1G00	5	Single 2-Input Positive-NAND Gate							✔	SCLS316F
SN74AHCT1G02	5	Single 2-Input Positive-NOR Gate							✔	SCLS341E
SN74AHCT1G04	5	Single Inverter Gate							✔	SCLS319G
SN74AHCT1G08	5	Single 2-Input Positive-AND Gate							✔	SCLS315F
SN74AHCT1G14	5	Single Schmitt-Trigger Inverter Gate							✔	SCLS322H
SN74AHCT1G32	5	Single 2-Input Positive-OR Gate							✔	SCLS320F
SN74AHCT1G86	5	Single 2-Input Exclusive-OR Gate							✔	SCLS324F
SN74AHCT1G125	5	Single Bus Buffer Gate With 3-State Outputs							✣	SCLS378B
SN74AHCT1G126	5	Single Bus Buffer Gate With 3-State Outputs							✣	SCLS380B
SN74AHCT00	14	Quad 2-Input NAND Gate	✔	✔	✔	✔	✔	✔		SCLS229E
SN74AHCT02	14	Quad 2-Input NOR Gate	✔	✔	✔	✔	✔	✔		SCLS262E
SN74AHCT04	14	Hex Inverter	✔	✔	✔	✔	✔	✔		SCLS232H
SN74AHCT08	14	Quad 2-Input AND Gate	✔	✔	✔	✔	✔	✔		SCLS237F
SN74AHCT14	14	Hex Inverter With Schmitt Trigger	✔	✔	✔	✔	✔	✔		SCLS246I
SN74AHCT32	14	Quad 2-Input OR Gate	✔	✔	✔	✔	✔	✔		SCLS248F
SN74AHCT74	14	Dual D-Type Flip-Flop With Preset and Clear	✔	✔	✔	✔	✔	✔		SCLS263H
SN74AHCT86	14	Quad Exclusive-OR Gate	✔	✔	✔	✔	✔	✔		SCLS250G
SN74AHCT123A	16	Dual Retriggerable Monostable Vibrator	✣	✣	✣	✣	✣	✣		SCLS420
SN74AHCT125	14	Quad Bus Buffer Gate ($\overline{OE}$)	✔	✔	✔	✔	✔	✔		SCLS264I
SN74AHCT126	14	Quad Bus Buffer Gate (OE)	✔	✔	✔	✔	✔	✔		SCLS265J
SN74AHCT132	14	Quad NAND Gate With Schmitt-Trigger Inputs	✣	✣	✣	✣	✣	✣		SCLS366B
SN74AHCT138	16	3-to-8 Decoder/Demultiplexer	✔	✔	✔	✔	✔	✔		SCLS266G
SN74AHCT139	16	Dual 2-to-4 Line Decoder/Demultiplexer		✔	✔	✔	✔	✔		SCLS267G
SN74AHCT157	16	Quad 2-to-1 Data Selector/Multiplexer		✔	✔	✔	✔	✔		SCLS347F
SN74AHCT158	16	Quad 2-to-1 Data Selector/Multiplexer		✔	✔	✔	✔	✔		SCLS348E
SN74AHCT174	16	Hex D-Type Flip-Flop With Clear	✣	✣	✣	✣	✣	✣		SCLS419
SN74AHCT240	20	Octal Buffer/Driver	✔	✔	✔	✔	✔	✔		SCLS252F

commercial package description and availability

For the latest product availability, visit http://www.ti.com/sc/docs/asl/news.htm

PDIP (plastic dual-in-line package)
P = 8 pins
N = 14/16/20 pins
NT = 24/28 pins

PLCC (plastic leaded chip carrier)
FN = 20/28/44/52/68/84 pins

QFP (quad flat package)
RC = 52 pins (FB only)
PH = 80 pins (FIFO only)
PQ = 100/132 pins (FIFO only)

SOT (small-outline transistor)
DBV = 5 pins
DCK = 5 pins

SSOP (shrink small-outline package)
DB = 14/16/20/24/28/30/38 pins
DBQ = 16/20/24
DL = 28/48/56 pins

QSOP (quarter-size outline package)
DBQ = 16/20/24 pins

SOIC (small-outline integrated circuit)
D = 8/14/16 pins
DW = 16/20/24/28 pins

TSSOP (thin shrink small-outline package)
PW = 8/14/16/20/24/28 pins
DGG = 48/56/64 pins

TVSOP (thin very small-outline package)
DGV = 14/16/20/24/48/56 pins
DBB = 80 pins

TQFP (plastic thin quad flat package)
PAH = 52 pins
PAG = 64 pins (FB only)
PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✔ = Now ★ = See page A–3
✣ = Planned

MIL See page A–3 for military package description and availability

TEXAS INSTRUMENTS

DEVICE	NO. OF PINS	FUNCTION	AVAILABILITY						LITERATURE REFERENCE
			MIL	PDIP	SOIC	SSOP	TSSOP	TVSOP	
SN74AHCT244	20	Octal Buffer/Driver	✔	✔	✔	✔	✔	✔	SCLS228G
SN74AHCT245	20	Octal Bus Transceiver	✔	✔	✔	✔	✔	✔	SCLS233F
SN74AHCT257	20	Quad 2-to-1 Data Selector/Multiplexer		✢	✢	✢	✢	✢	SCLS351D
SN74AHCT258	20	Quad 2-to-1 Data Selector/Multiplexer		✢	✢	✢	✢	✢	SCLS344D
SN74AHCT273	20	Octal D-Type Flip-Flop With Clear	✢	✢	✢	✢	✢	✢	SCLS375A
SN74AHCT367	16	Hex Buffer and Line Driver With 3-State Outputs	✢	✢	✢	✢	✢	✢	SCLS418
SN74AHCT373	20	Octal D-Type Transparent Latch	✔	✔	✔	✔	✔	✔	SCLS239H
SN74AHCT374	20	Octal D-Type Flip-Flop	✔	✔	✔	✔	✔	✔	SCLS241G
SN74AHCT540	20	Inverting Octal Buffer/Driver	✔	✔	✔	✔	✔	✔	SCLS268G
SN74AHCT541	20	Octal Buffer/Driver	✔	✔	✔	✔	✔	✔	SCLS269J
SN74AHCT573	20	Octal D-Type Transparent Latch	✔	✔	✔	✔	✔	✔	SCLS243H
SN74AHCT574	20	Octal D-Type Flip-Flop	✔	✔	✔	✔	✔	✔	SCLS245F
SN74AHCT594	16	8-Bit Shift Register With Output Registers	✢	✢	✢	✢	✢	✢	SCLS417
SN74AHCT595	16	8-Bit Shift Register With 3-State Output Registers	✢	✢	✢	✢	✢	✢	SCLS374B
SN74AHCT16240	48	16-Bit Buffer/Driver	✢			✔	✔	✔	SCLS333E
SN74AHCT16244	48	16-Bit Buffer/Driver	✢			✔	✔	✔	SCLS334E
SN74AHCT16245	48	16-Bit Bus Transceiver	✢			✔	✔	✔	SCLS335E
SN74AHCT16373	48	16-Bit D-Type Transparent Latch	✢			✔	✔	✔	SCLS336D
SN74AHCT16374	48	16-Bit D-Type Flip-Flop	✢			✔	✔	✔	SCLS337D
SN74AHCT16540	48	16-Bit Inverting Buffer/Driver	✢			✔	✔	✔	SCLS338D
SN74AHCT16541	48	16-Bit Buffer/Driver	✢			✔	✔	✔	SCLS339D

commercial package description and availability

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TSSOP (thin shrink small-outline package)
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PM = 64 pins
PN = 80 pins
PCA, PZ = 100 pins (FB only)
PCB = 120 pins (FIFO only)

schedule

✔ = Now ★ = See page A–3
✢ = Planned

MIL See page A–3 for military package description and availability

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Insert Tab Here

LVT Family Characteristics

Ken Ristow
Advanced System Logic – Semiconductor Group

SCEA002A
March 1998

TEXAS INSTRUMENTS

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Contents

List of Illustrations

Introduction

To address the need for a complete low-voltage interface solution, Texas Instruments has developed a new generation of logic devices capable of mixed-mode operation. The LVT series relies on a state-of-the-art submicron BiCMOS process to provide up to a 90% reduction in static power dissipation over ABT, as well as the following family characteristics:

5.5-V maximum input voltage

Specified 2.7-V to 3.6-V supply voltage

I/O structures that support live insertion

Standard TTL output drives of:
V_{OH} = 2 V at I_{OH} = −32 mA
V_{OL} = 0.55 V at I_{OL} = 64 mA

Rail-to-rail switching for driving CMOS

Maximum supply currents of:
$I_{CCL} \leq 15$ mA
$I_{CCH} \leq 200$ µA
$I_{CCZ} \leq 200$ µA

Propagation delays of:
$t_{pd} < 4.6$ ns
t_{pd} (LE to Q) < 5.1 ns
t_{pd} (CLK to Q) < 6.3 ns

Surface-mount packaging support including fine-pitch packages:
48-/56-pin SSOP and TSSOP for LVT Widebus™
20-/24-pin SOIC and TSSOP for standard LVT

LVT Input/Output Characteristics

Figure 1 shows a simplified LVT output and illustrates the mixed-mode-signal drive designed into the output stage. This combination of a high-drive TTL stage along with the rail-to-rail CMOS switching gives the LVT series of products extreme application flexibility. These parts have the same drive characteristics as 5-V ABT devices (see Figure 2), and provide the dc drive needed for existing 5-V backplanes. This allows for a simple solution to reduce system power via the migration to 3.3-V operation.

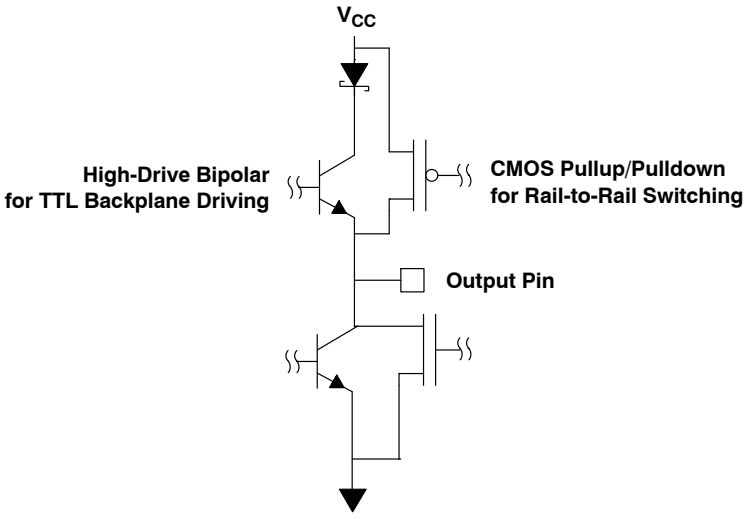


Figure 1. Simplified LVT Output Structure

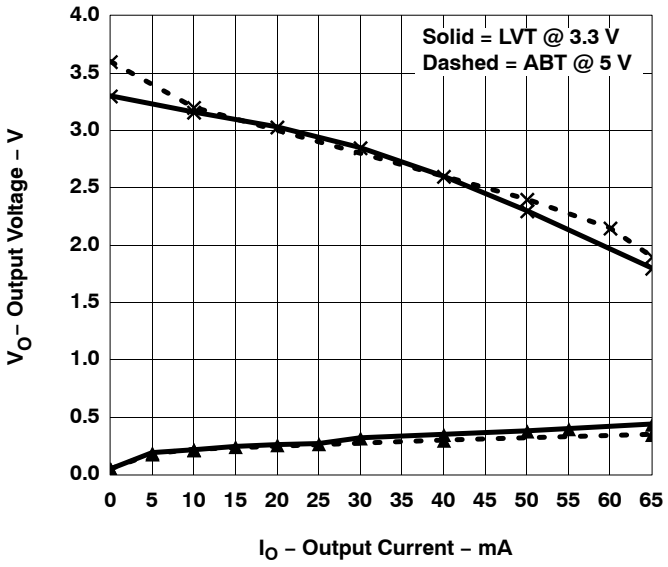


Figure 2. ABT Versus LVT Output-Drive Comparison

Not only can LVT devices operate as 3-V to 5-V level translators by supporting input or I/O voltages of 5.5 V with V_{CC} = 2.7 V to 3.6 V, the inputs can withstand 5.5 V even when V_{CC} = 0 V. This allows for the devices to be used under partial system power-down applications or those that require live insertion.

Bus Hold

Many times, devices are used in applications that do not provide a pullup or pulldown voltage to the input or I/O pin when the driving device goes into a high-impedance state, as in the case of CMOS buses or nonbused lines. To prevent application problems or oscillations, a large pullup resistor typically is used, but this consumes board area and contributes to driver loading. The LVT series of devices incorporates active circuitry that holds unused or floating inputs or I/Os at a valid logic level. This circuitry provides for a typical holding current, ± 100 μA, that is sufficient enough to overcome any CMOS-type leakages. Since this is an active circuit, it does take current, approximately ± 500 μA, to toggle the state of the input. This current is trivial when compared to the current that is needed to charge a capacitive load, thereby not affecting the propagation delay of the driving output.

Conclusion

LVT devices solve the system need for a transparent seam between the low-voltage and 5-V sections by providing for mixed-signal operation. The devices support live-insertion or partial-power applications, while providing for low-input leakage currents. The outputs can drive today's 5-V backplanes, with a considerable reduction in device power consumption, as well as being packaged in state-of-the-art, fine-pitch surface-mount packages.

’LVT244 Characteristics

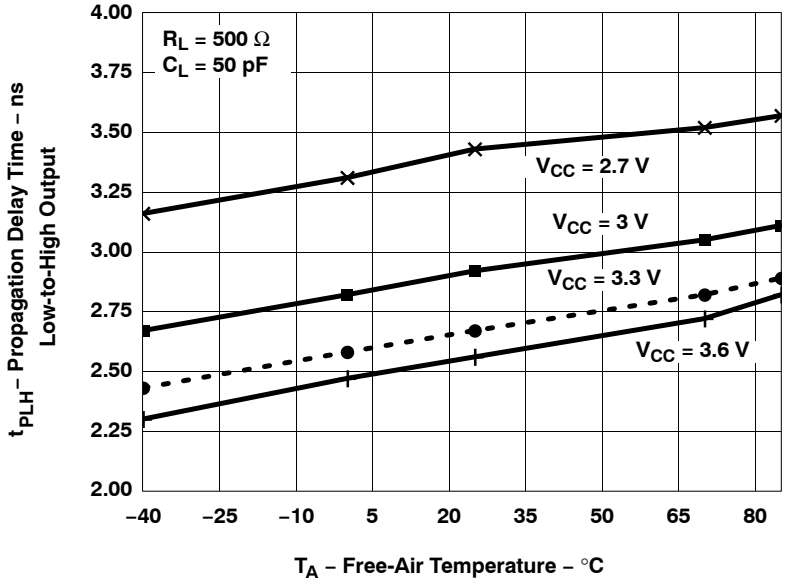


Figure 3. Propagation Delay (t_{PLH}) Versus Free-Air Temperature

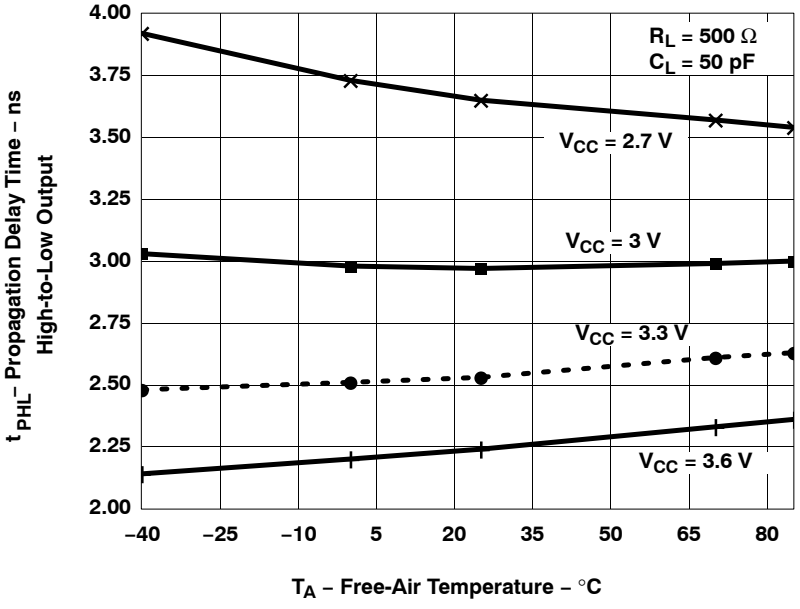


Figure 4. Propagation Delay (t_{PLH}) Versus Free-Air Temperature

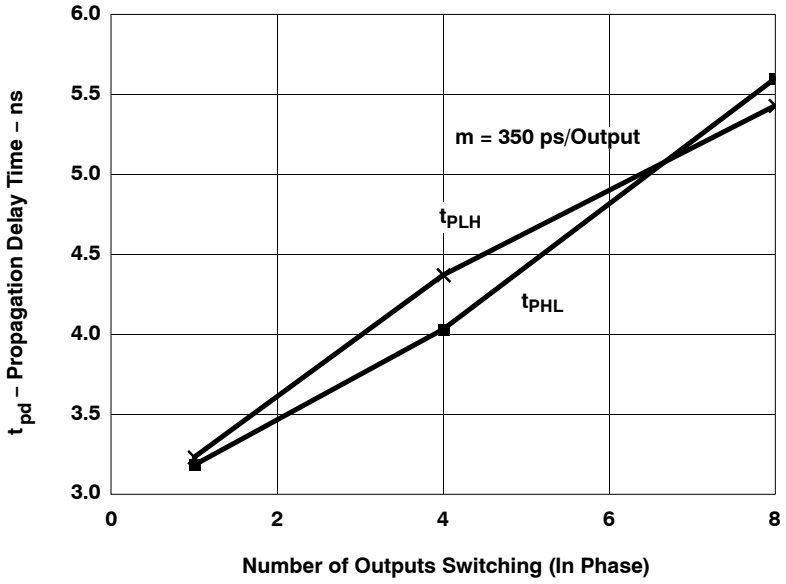


Figure 5. Propagation Delay Versus Outputs Switching

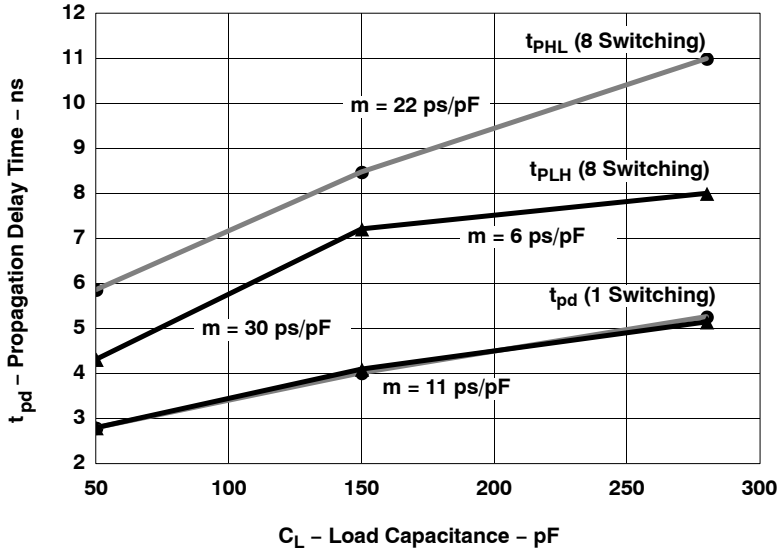


Figure 6. Propagation Delay Versus Load Capacitance

’LVT244 Typical dc Characteristics

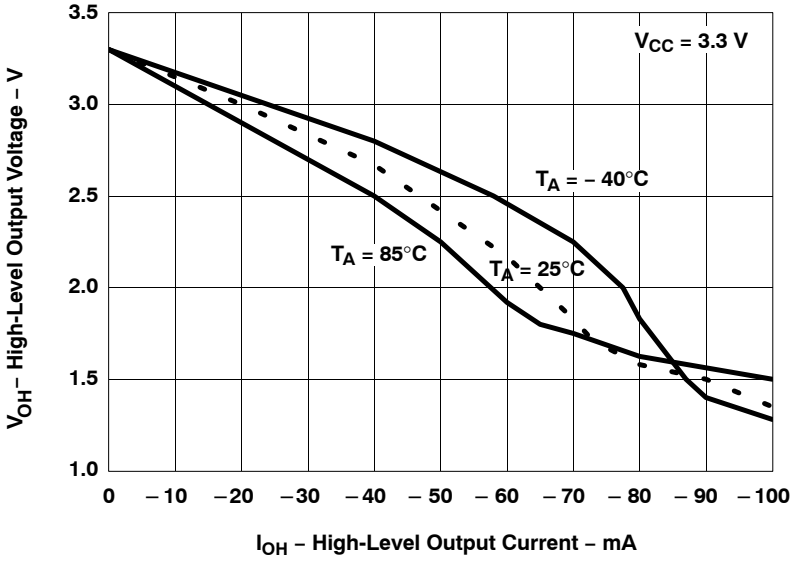


Figure 7. High-Level Output Voltage Versus High-Level Output Current, V_{CC} = 3.3 V

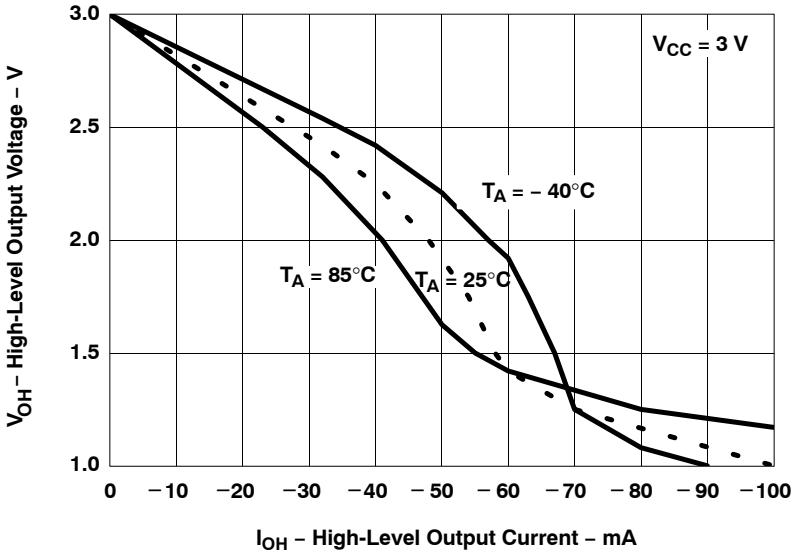


Figure 8. High-Level Output Voltage Versus High-Level Output Current, V_{CC} = 3 V

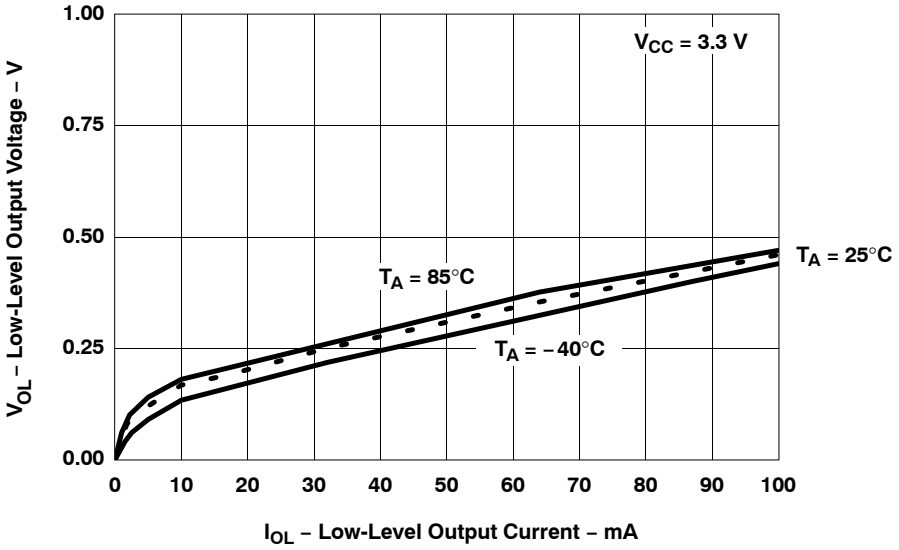


Figure 9. Low-Level Output Voltage Versus Low-Level Output Current

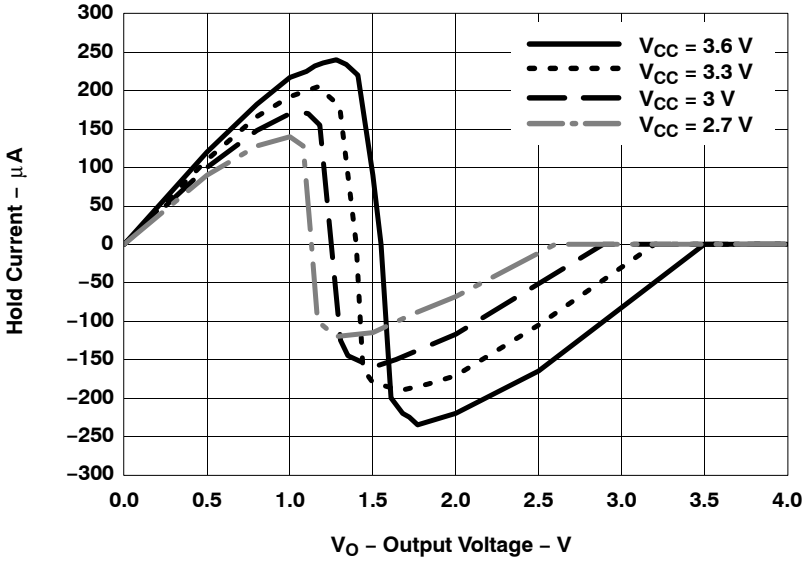


Figure 10. Hold Current Versus Output Voltage

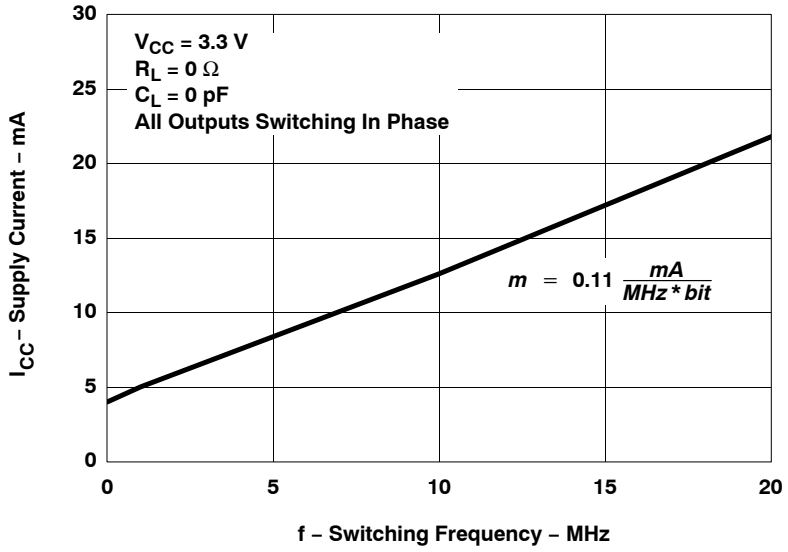


Figure 11. Supply Current Versus Switching Frequency

Unloaded t_r and t_f Rates

The circuit shown in Figure 12 was used to measure the unloaded transition rates of the output.

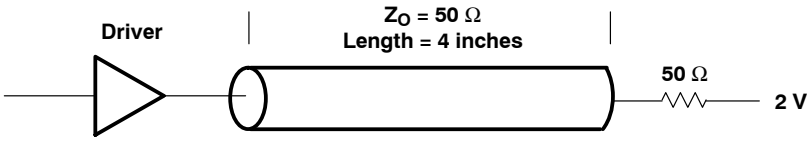


Figure 12. Load Circuit

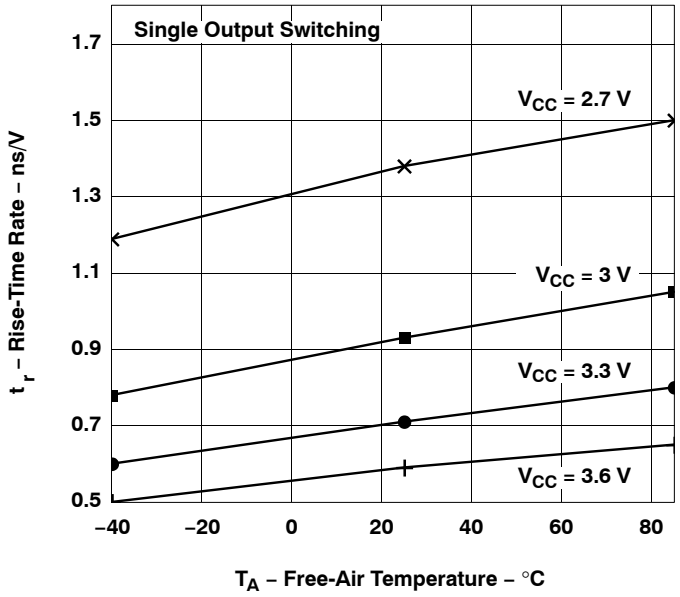


Figure 13. Rise-Time Rate Versus Free-Air Temperature, Single Output Switching

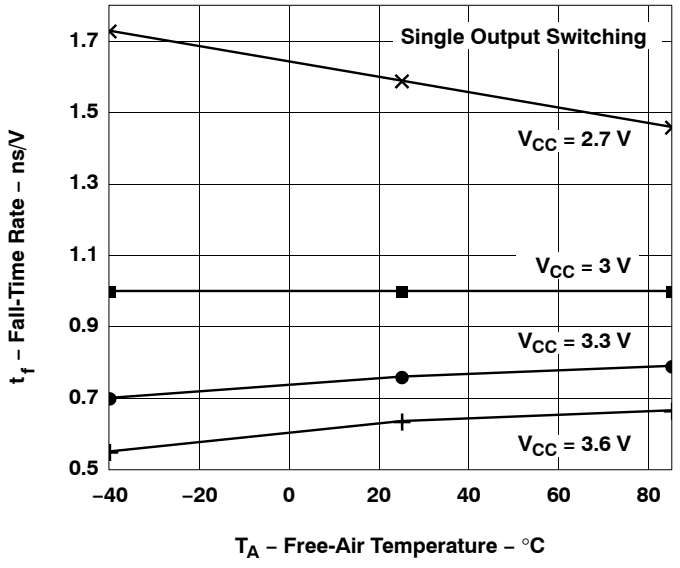


Figure 14. Fall-Time Rate Versus Free-Air Temperature, Single Output Switching

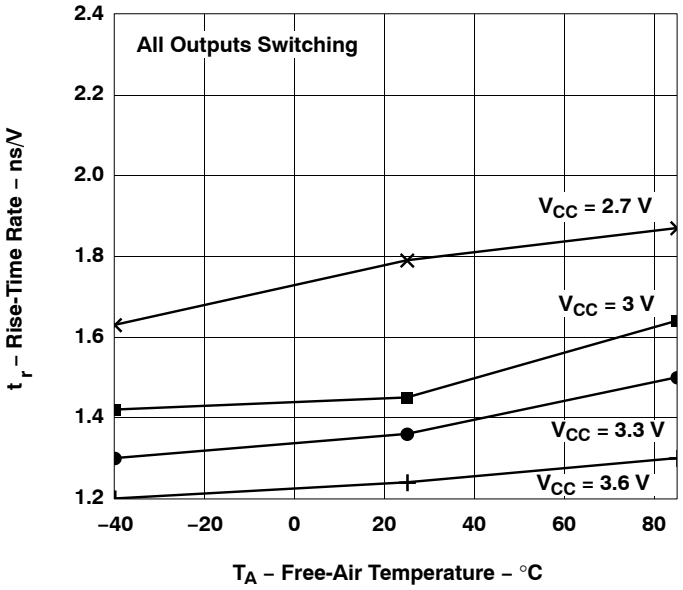


Figure 15. Rise-Time Rate Versus Free-Air Temperature, All Outputs Switching

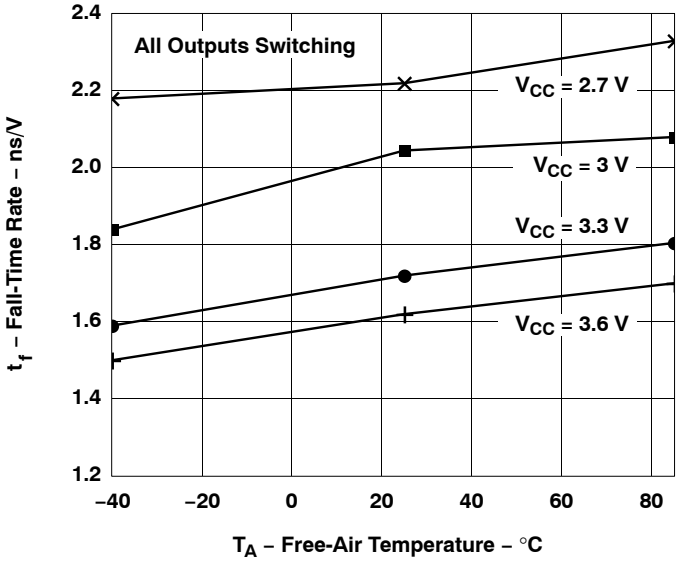


Figure 16. Fall-Time Rate Versus Free-Air Temperature, All Outputs Switching

’LVT646 Characteristics

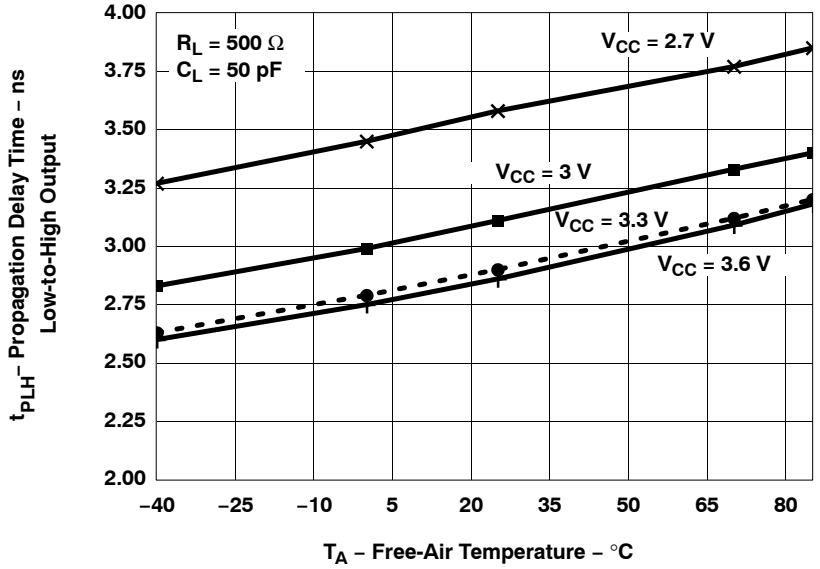


Figure 17. Through-Mode Propagation Delay (t_{PLH}) Versus Free-Air Temperature

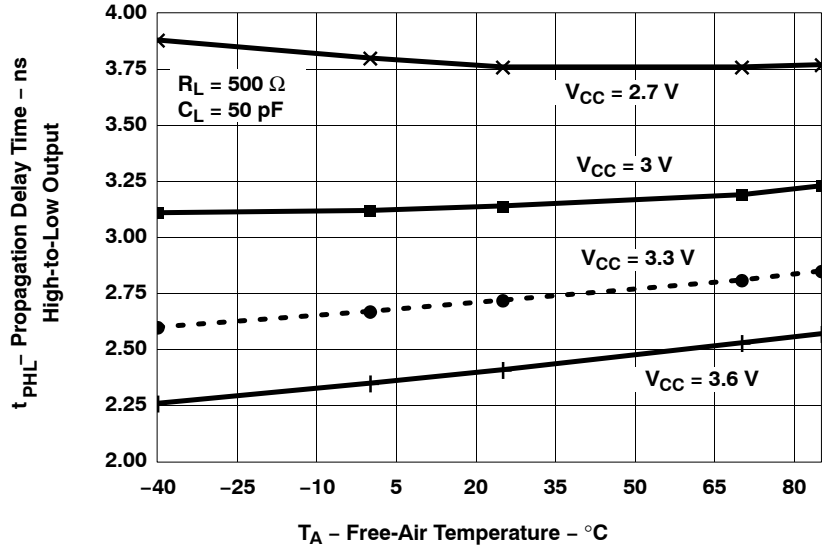


Figure 18. Through-Mode Propagation Delay (t_{PHL}) Versus Free-Air Temperature

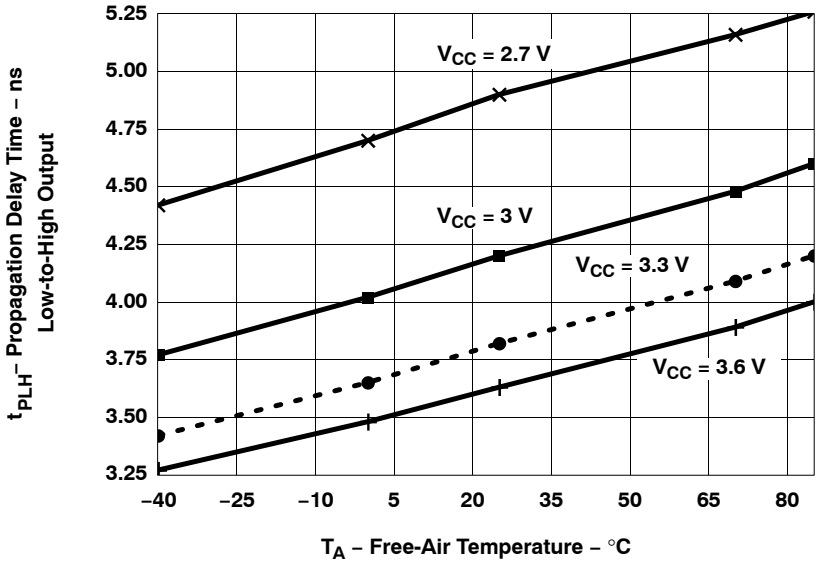


Figure 19. Clock-to-Q Propagation Delay (t_{PLH}) Versus Free-Air Temperature

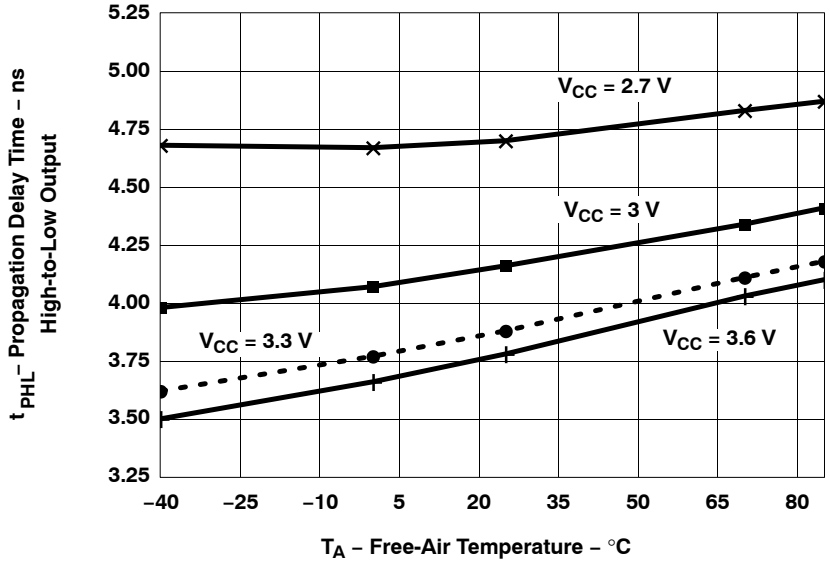


Figure 20. Clock-to-Q Propagation Delay (t_{PHL}) Versus Free-Air Temperature

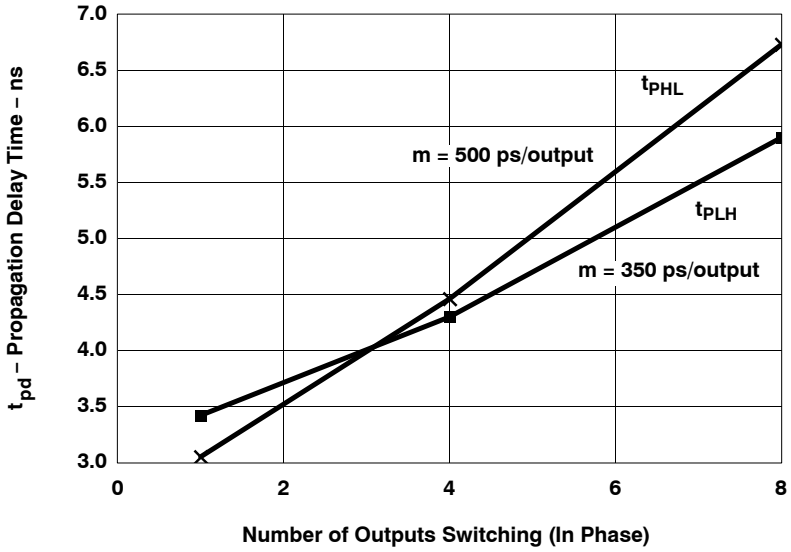


Figure 21. Propagation Delay Versus Outputs Switching

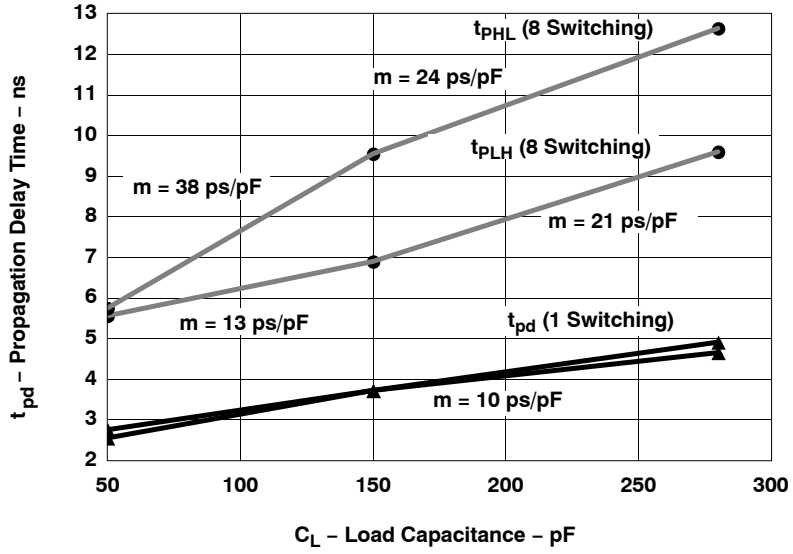
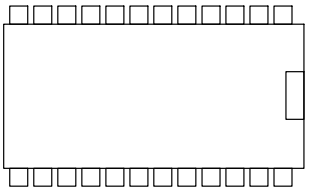


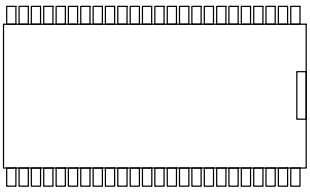
Figure 22. Propagation Delay Versus Load Capacitance

Packaging Options

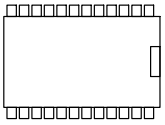


24-Pin SOIC (DW)†
Area = 165 mm²
Height = 2.65 mm
Lead pitch = 1.27 mm

Widebus™

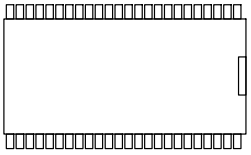


48-Pin SSOP (DL)†
Area = 171 mm²
Height = 2.74 mm
Lead pitch = 0.635 mm



24-Pin TSSOP (PW)†
Area = 54 mm²
Height = 1.1 mm
Lead Pitch = 0.65 mm

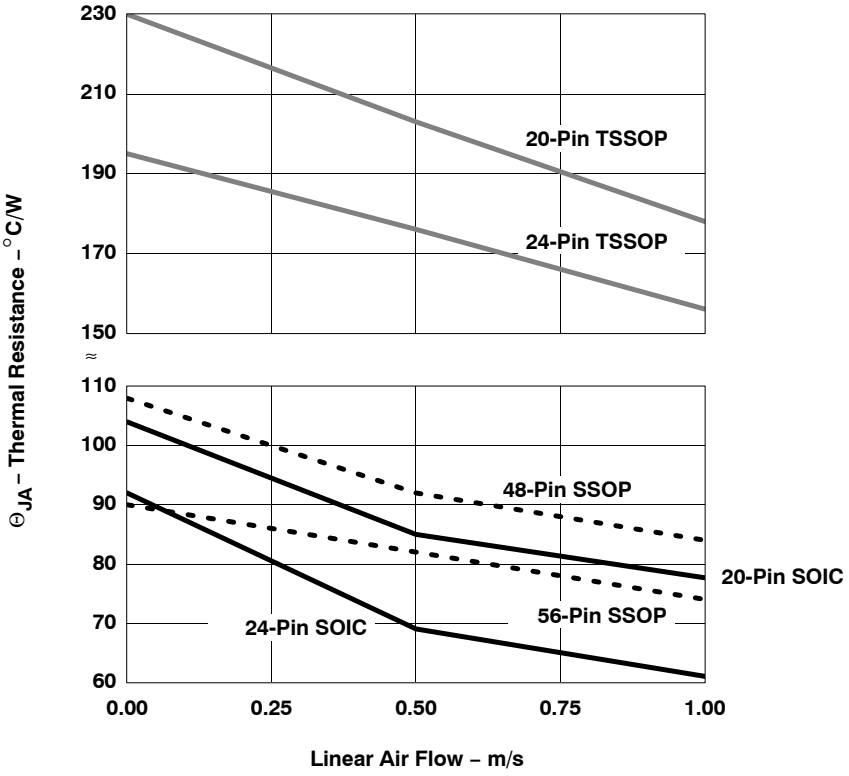
Shrink Widebus™



48-Pin TSSOP (DGG)†
Area = 108 mm²
Height = 1.1 mm
Lead Pitch = 0.5 mm

† TI package designators

Thermal Characteristics



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LVT-to-LVTH Conversion

SCEA010
January 1999

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Abstract

Original LVT devices that have bus hold have been redesigned to add the High-Impedance State During Power Up and Power Down feature. Additional devices with and without bus hold have been added to the LVT product line. Design guidelines and issues related to the bus-hold features, switching characteristics, and timing requirements are discussed.

Introduction

In 1992, Texas Instruments (TI™) introduced the LVT low-voltage BiCMOS logic family. All of the devices in the LVT family had bus hold as a feature. In 1996, in response to market demands, redesign of the LVT family began to enhance performance. As part of this redesign, all devices were renamed to LVTH to denote the bus-hold feature explicitly in the device name, and to standardize the bus-hold naming convention used on all TI logic families.

With this redesign, switching performance generally improved, timing requirements changed, and the High-Impedance State During Power Up and Power Down feature was added to all devices in this family. To facilitate the conversion of applications from LVT devices to their LVTH replacements, a device conversion guide, an explanation of the High-Impedance State During Power Up and Power Down feature, changes in bus-hold requirements, and a discussion of the changes to switching and timing requirements are included in this application report.

Conversion Guide

The original LVT devices had the bus-hold feature. The LVTH replacements for these devices not only have bus hold, but also have the High-Impedance State During Power Up and Power Down feature. Table 1 shows the LVTH replacement device for every LVT octal device. Table 2 shows the LVTH replacement device for every LVT Widebus™ device.

Table 1. Octal-Function Conversion

LVT OCTAL FUNCTION	REPLACEMENT LVTH OCTAL FUNCTION
LVT125	LVTH125
LVT240	LVTH240
LVT241	LVTH241
LVT244/LVT244A	LVTH244A
LVT245/LVT245A	LVTH245
LVT273	LVTH273
LVT543	LVTH543
LVT573	LVTH573
LVT574	LVTH574
LVT646	LVTH646
LVT652	LVTH652
LVT2952	LVTH2952

Table 2. Widebus-Function Conversion

LVT WIDEBUS FUNCTION	REPLACEMENT LVTH WIDEBUS FUNCTION
LVT16244/LVT16244A	LVTH16244A
LVT162244	LVTH162244
LVT16245/LVT16245A	LVTH16245A
LVT162245	LVTH162245
LVT16373	LVTH16373
LVT16374	LVTH16374
LVT16500	LVTH16500
LVT16501	LVTH16501
LVT16543	LVTH16543
LVT16646	LVTH16646
LVT16835	LVTH16835
LVTH16952	LVTH16952

The original LVTZ products had the High-Impedance State During Power Up and Power Down feature. These devices also had bus hold, as did the original LVT devices. The LVTH device is a direct feature-for-feature replacement for LVTZ. Table 3 shows the LVTH replacement device for every LVTZ device.

Table 3. LVTZ-Function Conversion

LVTZ OCTAL FUNCTION	REPLACEMENT LVTH OCTAL FUNCTION
LVTZ240	LVTH240
LVTZ244	LVTH244A
LVTZ245	LVTH245A

Also, 14 devices with bus hold that were not available in the original LVT product line were added in the redesigned LVT product line. These devices are shown in Table 4.

Table 4. New Functions With Bus Hold in the Redesigned LVT Product Line

LVTH2245
LVTH373
LVTH374
LVTH540
LVTH541
LVTH16240
LVTH162240
LVTH16241
LVTH162241
LVTH162373
LVTH162374
LVTH16541
LVTH162541
LVTH16652

Also, three octal functions without bus hold are new to the LVT product line. These devices are shown in Table 5. Care should be taken not to confuse these with the replacements for the original LVT240, LVT244A, and LVT245A devices, which had bus hold and for which LVTH replacements are shown in Table 1.

Table 5. New Functions Without Bus Hold in the Redesigned LVT Product Line

LVT240A
LVT244B
LVT245B

High-Impedance State During Power Up and Power Down

High-Impedance State During Power Up and Power Down is one of the features that has been added with the redesign of LVT devices. This feature enables the LVTH replacement devices to better support insertion into or removal from systems that are powered on.

Device capability for supporting live insertion is noted by the specification of output-pin current (I_{OZPU} and I_{OZPD}) while V_{CC} is suboperational. Typically, I_{OZPU} and I_{OZPD} are tested at pin voltages that approximate valid logic low and high levels for that pin (0.5V, 3V). The I_{OZPU} and I_{OZPD} currents at each level are specified in the range of ±50 μA and are tested for V_{CC} in the range below a level at which the circuit is expected to be functionally operational (1.5 V for LVT and LVTH devices).

Figures 1 through 4 demonstrate the effect of the High-Impedance State During Power Up and Power Down feature on the V_{CC} level at which the LVTH device outputs become active, in comparison to the LVT device outputs that lack this feature. In the I_{OZL} plots, the output is pulled to ground through a 500-Ω resistor so that, while the output is in the high-impedance state, the output will be low. The input is biased so that the output will drive to a valid logic-high state when active. In the I_{OZH} plots, the output is pulled to a valid high state through a 500-Ω pullup resistor, so that while the output is in the high-impedance state, the output will be high. The input is biased such that the output will drive to a valid logic-low state when active.

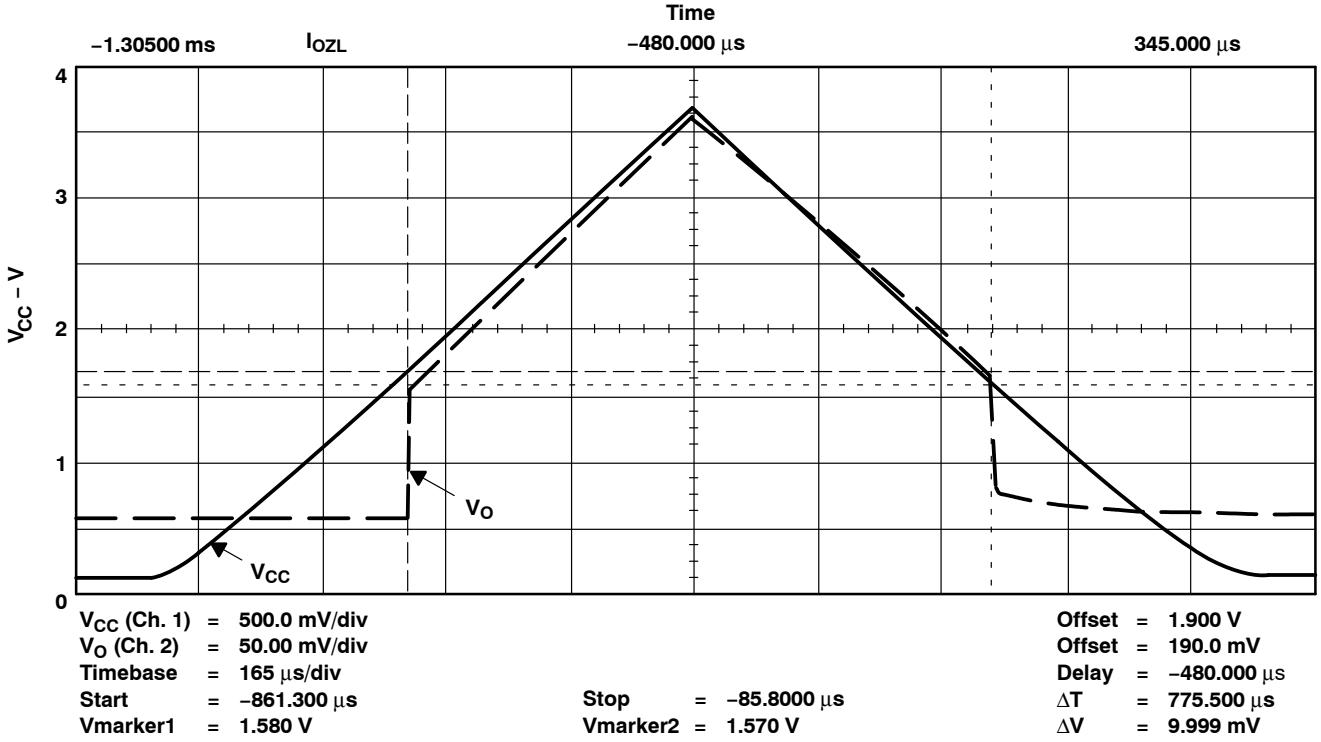

Figure 1. LVT16244A at 85°C With Input Biased to Drive Output High When Active

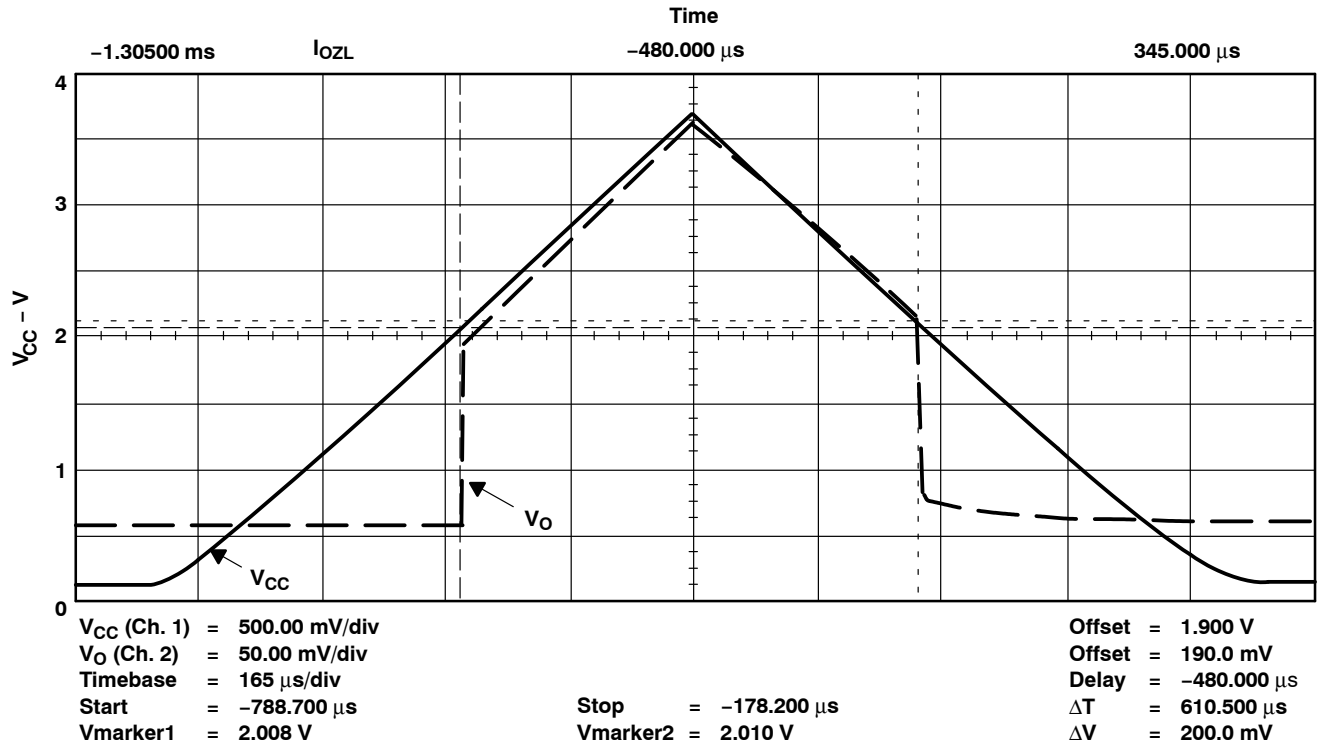

Figure 2. LVTH16244A at 85°C With Input Biased to Drive Output High When Active

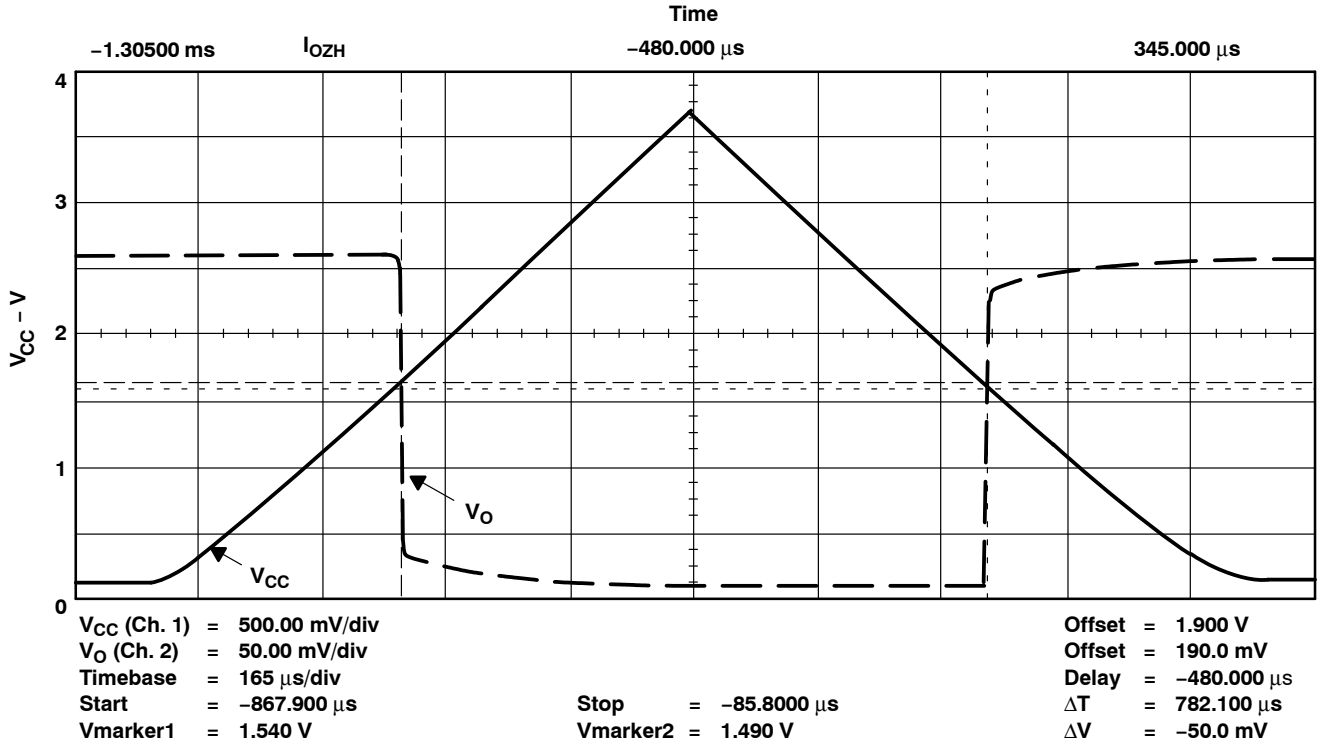

Figure 3. LVT16244A at 85°C With Input Biased to Drive Output Low When Active

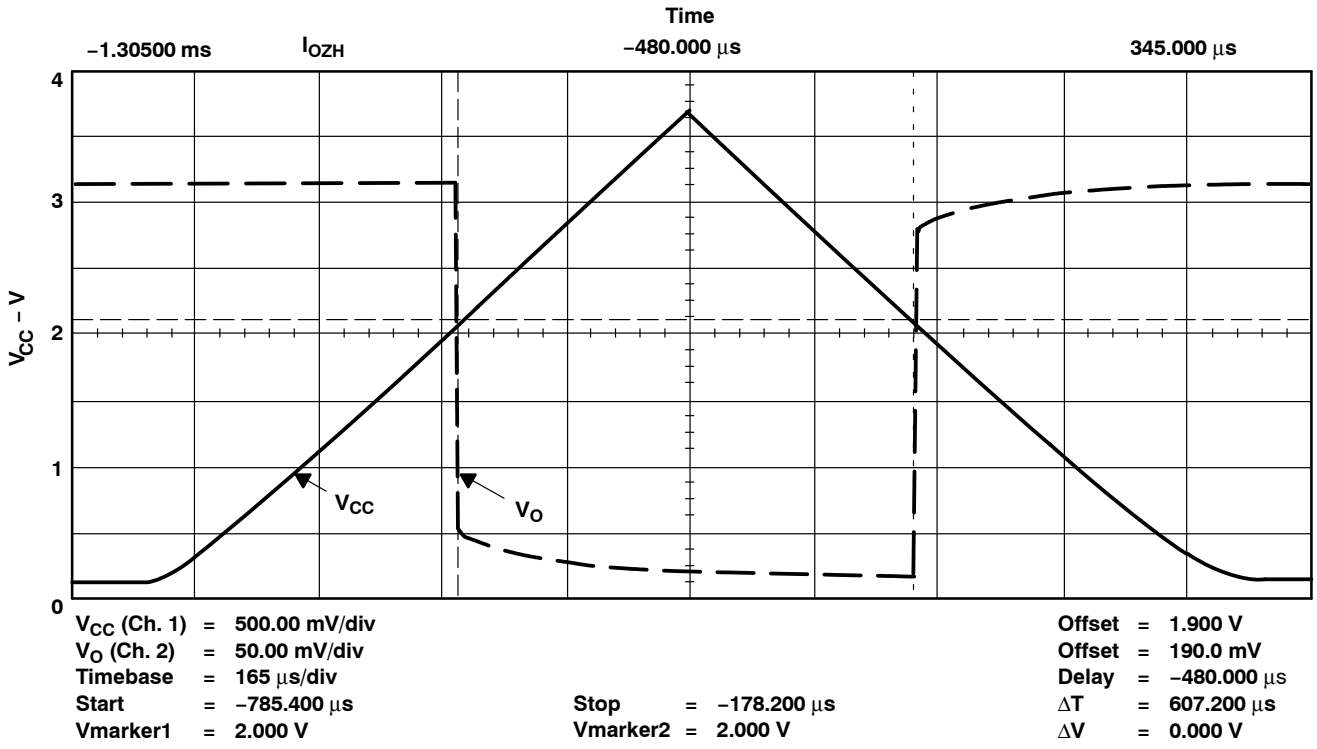

Figure 4. LVTH16244A at 85°C With Input Biased to Drive Output Low When Active

Figures 1 and 3 show that, once the V_{CC} of the LVT16244A exceeds about 1.5 V on power up or that the V_{CC} drops below about 1.5 V on power down, the outputs become active or enter the high-impedance state, respectively. Figures 2 and 4 show that once the V_{CC} of LVTH16244A exceeds about 2 V on power up or that V_{CC} drops below about 2 V on power down, the outputs become active or enter the high-impedance state, respectively.

These figures demonstrate that, while the original LVT devices do exhibit a high-impedance characteristic during the initial phase of power up and final phase of power down, they do so only below V_{CC} levels that are too low to provide adequate margin versus the I_{OZPU} and I_{OZPD} specifications. The new LVTH devices, with the deliberately designed High-Impedance State During Power Up and Power Down feature, do provide adequate margin to the specifications.

Finally, when the device is fully powered, the High-Impedance State During Power Up and Power Down feature does not affect operation or any other specifications of the device. This feature is active and affects device operation only during power up and power down.

Design Guidelines and Issues Concerning the Bus-Hold Feature

The original LVT product line had the bus-hold feature on all data inputs. When the LVT product line was redesigned, the names were changed to match TI standard naming conventions for bus hold. There have been some issues concerning the bus-hold feature on the replacement LVTH devices versus the original LVT devices. Among the issues are the differences in bus-hold current requirements between some LVTH devices and the LVT devices they replace: overdrive current required to ensure switching of an input from one state to the other and tie-off of bus-hold data inputs.

Bus hold is intended to remove the requirement to tie-off unused data inputs. The bus-hold feature is only on the data inputs and data I/O pins of the LVTH devices. Unused control pins still must be tied off to ensure that the input does not float.

LVTH devices in the redesigned product line have one of two versions of the bus-hold circuit. The devices with Type-A circuits have a recommended overdrive current of 750 μA. The devices with Type-B circuits have a recommended overdrive current of 500 μA. The original LVT family had a recommended overdrive current of 500 μA. See Table 6 for a list of LVTH devices that have the Type-A circuit and those that have the Type-B circuit. Overdrive current is the current required to ensure that a bus-hold input is switched from one logic state to the other. Devices with the Type-B circuit are not significantly different from the LVT devices they replace. However, devices with the Type-A circuit require more overdrive current than the LVT devices they replace. This increase in overdrive current on devices with a Type-A circuit must be comprehended when converting an application to use the LVTH device, especially if pullup or pulldown resistors are used at the inputs. Figure 5 shows a comparison of the V-I characteristics of a bus-hold data input on the LVT16244A and the replacement LVTH16244A.

Table 6. LVTH Devices by Bus-Hold Circuit Type

CIRCUIT TYPE	DEVICES
Type A (750 μA)	LVTH240, LVTH241, LVTH244A, LVTH245A, LVTH2245, LVTH273, LVTH373, LVTH374, LVTH16240, LVTH162240, LVTH16241, LVTH162241, LVTH16244A, LVTH162244, LVTH16245A, LVTH162245, LVTH16373, LVTH162373, LVTH16374, LVTH162374, LVTH16541, LVTH162541
Type B (500 μA)	LVTH125, LVTH540, LVTH541, LVTH543, LVTH573, LVTH574, LVTH646, LVTH652, LVTH2952, LVTH16500, LVTH16501, LVTH16543, LVTH16646, LVTH16652, LVTH16835, LVTH16952

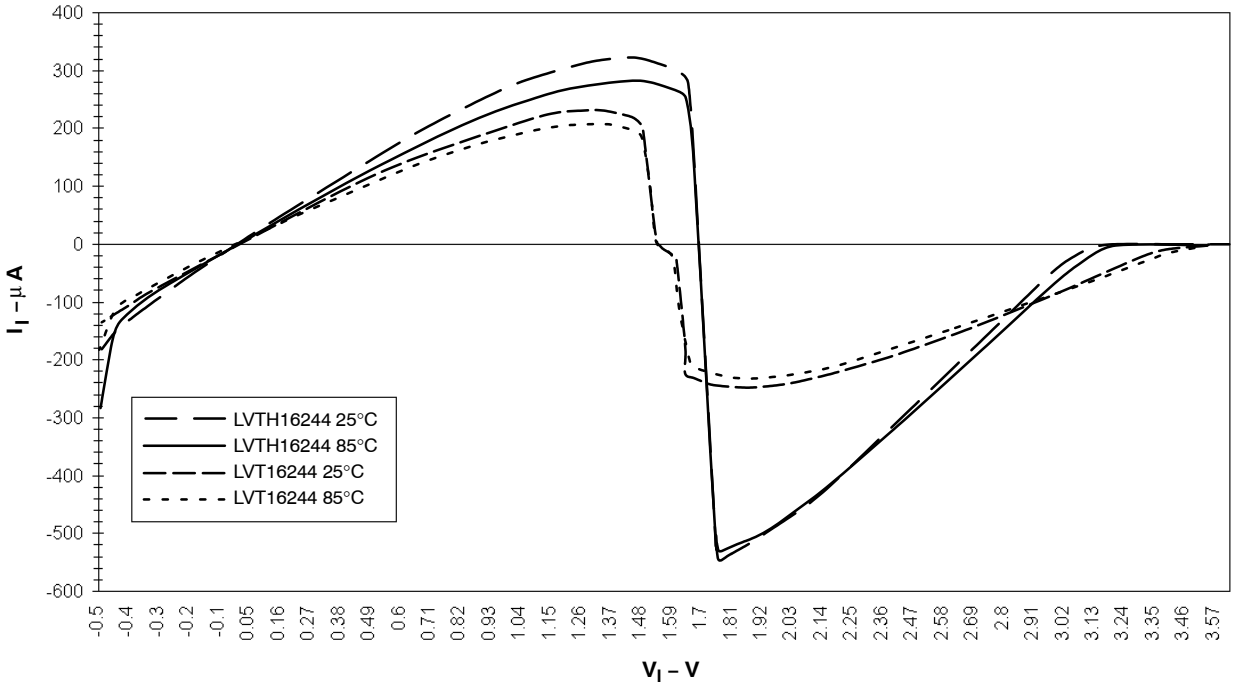

Figure 5. V-I Characteristics for LVT16244A and LVTH16244A Bus-Hold Inputs

Although bus hold eliminates the need to tie-off unused data inputs, there are other situations that require tie-off. When tie-off of inputs is required, the pullup or pulldown mechanism must be able to sink or source the recommended overdrive current to ensure that the input will be pulled to the desired state. See Table 7 for the recommended resistor size for the most common tie-off voltages.

Table 7. Recommended Resistor Values for Tie-Off

BUS-HOLD CIRCUIT TYPE	TIE-OFF VOLTAGE					
	0 V	2.7 V	3.0 V	3.3 V	3.6 V	5.0 V
Type A (750 uA)	<1.35 kΩ	<1.08 kΩ	<1.48 kΩ	<1.88 kΩ	<2.28 kΩ	<4.15 kΩ
Type B (500 uA)	<2.02 kΩ	<1.62 kΩ	<2.22 kΩ	<2.82 kΩ	<3.42 kΩ	<6.22 kΩ

Another consideration for bus-hold inputs is that multiple bus-hold data inputs on a node increase the overdrive-current requirements for that node. The current requirement is a parallel condition. For example, if the bus-hold inputs of an LVTH244A device and an LVTH574 device were connected on the same node, the node would require 1.25 mA of overdrive current to ensure that the inputs are driven to the correct logic state. This is extensible for three or more devices as well; the total overdrive current for a node is the sum of the individual overdrive currents of each connected device pin.

Switching Characteristics and Timing Requirements

As a result of the redesign of the original LVT product line, switching characteristics and timing requirements of most LVTH replacement devices have changed.

Table 8 shows an example of the switching-characteristics and timing-requirements specification-change summary for all devices that are moving from LVT to LVTH. The specification-change summaries are provided in the Product Change Notifications (PCN) for the devices in question. See Table 8 to determine which PCN has this information for a given original LVT device. Any specifications from the data sheet that are not listed have not changed with the LVTH replacement. In Table 9, for specifications that are listed, only items that are in bold underlined italics are changed from the original LVT device.

Table 8. PCN-to-Device Cross-Reference

PCN NUMBER	DEVICES
PCN 5287	LVT240, LVT244A, LVTZ244, LVT245A, LVT273, LVT16244A, LVT162244, LVT16373, LVT16374
PCN 5287A	LVTZ240, LVT241, LVTZ245, LVT543, LVT573, LVT574, LVT646, LVT652, LVT2952, LVT16245A, LVT162245
PCN 5287B	LVT16543, LVT16646, LVT16952
PCN 5287C	LVT125
PCN 5287D	LVT16500, LVT16501, LVT16835

In the case of the LVT16835 versus LVTH16835, as shown in Table 9, setup times for data before LE, and hold times for data after CLK and data after LE have improved. Also, maximum propagation delays have been improved significantly. However, because all design features are tradeoffs, minimum propagation delays are lower and the setup time of data before CLK has increased slightly. See device data sheets for all specifications and parameter values.

Generally, the switching characteristics and timing requirements have improved. These specification changes should be considered when converting an application from an original LVT device to an LVTH replacement.

Table 9. Comparison of LVT16835 and LVTH16835 Timing Requirements and Propagation Delays

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 3.3 V ± 0.3 V						V_{CC} = 2.7 V				UNIT
			OLD			NEW			OLD		NEW		
			74LVT16835			74LVTH16835			74LVT16835		74LVTH16835		
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{clock}	Clock frequency		0		150			150	0	125		***150***	MHz
t_{su}	Data before CLK↑		1.6			***2.1***			2.1		***2.4***		ns
t_{su}	Data before LE↑, CLK high		2.6			***2.3***			1.9		***1.5***		ns
t_{su}	Data before LE↑, CLK low		2			***1.5***			1.3		***0.5***		ns
t_h	Data after CLK↑		2			***1.0***			2.1		***0.0***		ns
t_h	Data after LE↑		0.9			***0.8***			1.2		***0.8***		ns
f_{max}			150			150			125		***150***		MHz
t_{PLH}	A	Y	1.7	3	5.4	***1.3***	***2.6***	***3.7***		6.8		***4***	ns
t_{PHL}	A	Y	1.6	3.2	5.9	***1.3***	***2.4***	***3.7***		7.7		***4***	ns
t_{PLH}	LE	Y	2.3	4	7	***1.5***	***3.2***	***5.1***		8.5		***5.7***	ns
t_{PHL}	LE	Y	2.7	4.3	7.9	***1.5***	***3.3***	***5.1***		9.7		***5.7***	ns
t_{PLH}	CLK	Y	2.5	4.1	7.9	***1.5***	***3.5***	***5.1***		9.2		***5.7***	ns
t_{PHL}	CLK	Y	3.5	5.4	8.9	***1.5***	***3.4***	***5.1***		10.4		***5.7***	ns
t_{PZH}	$\overline{OE}$	Y	1.2	3	5	***1.3***	***2.9***	***4.6***		5.9		***5.5***	ns
t_{PZL}	$\overline{OE}$	Y	1.5	3	5.8	***1.3***	3	***4.6***		6.9		***5.5***	ns
t_{PHZ}	$\overline{OE}$	Y	2.7	4.6	7.4	***1.7***	***4.2***	***5.8***		8.3		***6.3***	ns
t_{PLZ}	$\overline{OE}$	Y	2.8	4.7	6.7	***1.7***	***3.7***	***5.8***		7.2		***6.3***	ns

Summary

The LVTH devices are offered as replacements for the original LVT devices. The LVTH devices, with enhanced performance and added High-Impedance State during Power Up and Power Down feature, are drop-in replacements for the original LVT devices if the changes in bus hold, switching characteristics, and timing requirements are addressed.

Acknowledgment

The authors of this report are Gordon Holton and George Mourad. The authors acknowledge John Harrison for the laboratory data used in this report and Adam Ley for technical inputs and suggestions.

References

LVT Logic Low-Voltage Technology Data Book, 1998, literature number SCBD154.

The following Product Change Notifications are available on the TI web page at http://www.ti.com/sc/docs/asl/pcns.htm.

PCN5287
PCN5287A
PCN5287B
PCN5287C
PCN5287D

Insert Tab Here

AVC Logic Family Technology and Applications

SCEA006A
August 1998

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Abstract

Texas Instruments (TI™) announces the industry's first logic family to achieve maximum propagation delays of less than 2 ns at 2.5 V. TI's next-generation logic is the Advanced Very-low-voltage CMOS (AVC) family. Although optimized for 2.5-V systems, AVC logic supports mixed-voltage systems because it is compatible with 3.3-V and 1.8-V devices. The AVC family features TI's Dynamic Output Control (DOC™) circuit (patent pending). The DOC circuit provides enough current to achieve high signaling speeds, but automatically lowers the output impedance of the circuit during a signal transition and subsequently increases the impedance to reduce the overshoot and undershoot noise that is often found in high-speed logic. This feature of AVC logic eliminates the need for series damping resistors. AVC logic also has a power-off feature that disables outputs from the device when no power is applied.

Introduction

Current trends in advanced digital electronics design continue to include lower power consumption, lower supply voltages, faster operating speeds, smaller timing budgets, and heavier loads. Many designs are making the transition from 3.3 V to 2.5 V, and bus speeds are increasing beyond 100 MHz. Encompassing all these goals makes the requirement of signal integrity more difficult to achieve. For designs that require very-low-voltage logic and bus-interface functions, TI produces a new logic family that designers of next-generation high-performance workstations, PCs, networking, and telecommunications equipment find particularly useful.

AVC Family

TI's next-generation logic family is AVC (see Figure 1). As part of TI's Widebus™ and Widebus+™ families, these devices give designers an easy migration path to higher performance and lower voltages. Also offered in the AVC family are a broad line of logic gates and octal bus-interface functions. The devices in TI's AVC family are available in multiple JEDEC-standard advanced packages to provide maximum flexibility in board layout and cost.

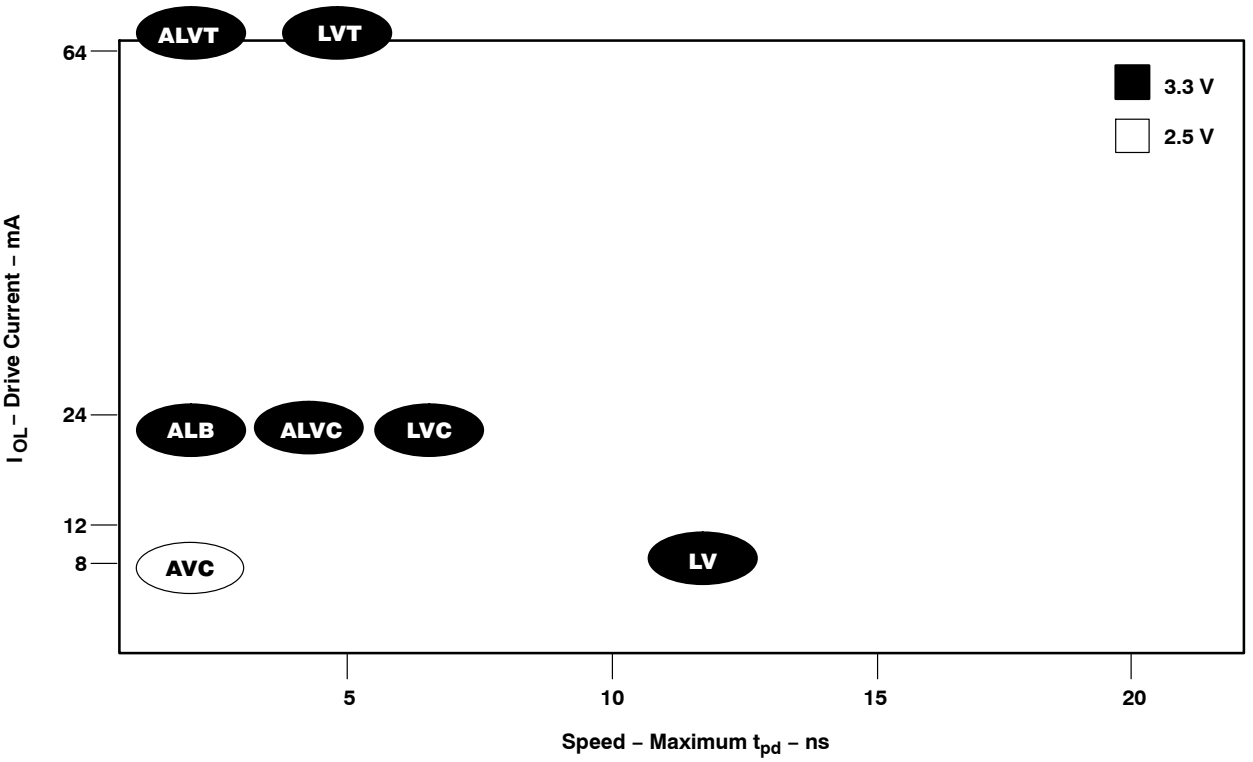

Figure 1. Low-Voltage Logic Family Performance Positioning

Unparalleled Performance

TI's AVC family is the industry's first logic family to achieve maximum propagation delays of less than 2 ns at 2.5 V. This premier performance is achieved through a combination of advances. The family was designed for high performance, incorporating several novel circuit structures and changes to conventional logic-circuit designs. TI's advanced 0.5-micron Enhanced-Performance Implanted CMOS (EPIC™) fabrication process is used to produce the new devices.

Novel Output Structure

The AVC family features TI's DOC circuit, which changes output impedance during switching (see Figure 2). The DOC circuit allows a single device to have the desirable characteristics of reduced noise, similar to damping-resistor outputs during static conditions, and high drive similar to a low-impedance output during dynamic conditions. The DOC circuit controls overshoots and undershoots and limits noise, which are inherent in high-speed, high-current devices.

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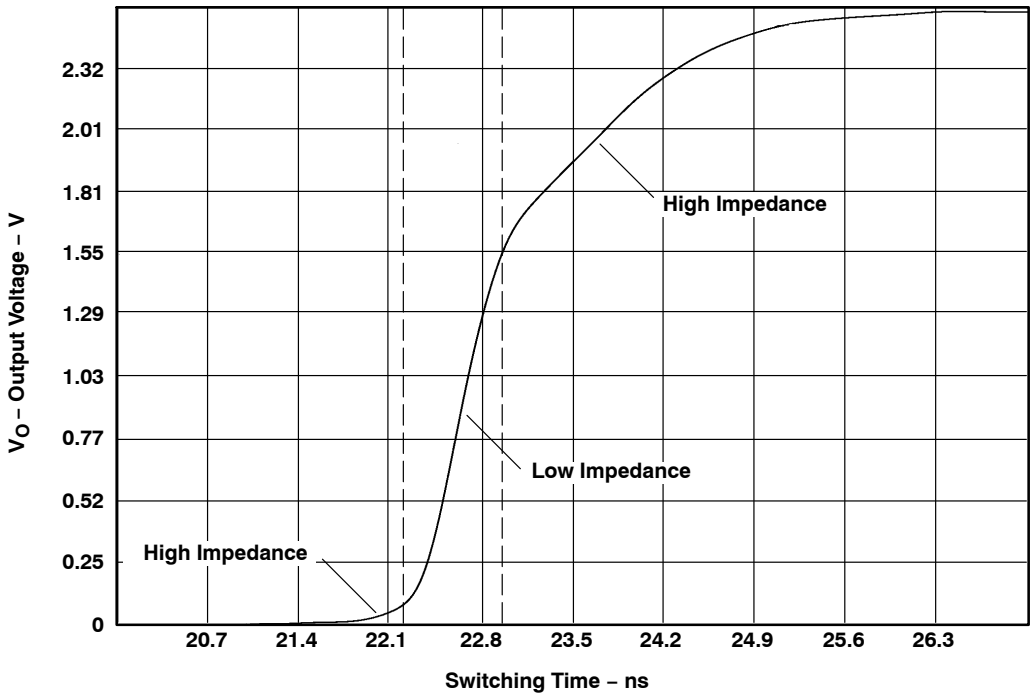


Figure 2. Impedance Changes Through Switching Transitions

Mixed-Voltage Mode and Power Off

The AVC family is optimized for low-power 2.5-V systems and effectively supports mixed-voltage systems because it is compatible with 3.3-V and 1.8-V devices. AVC device inputs and outputs are 3.6-V tolerant at 2.5-V and 1.8-V V_{CC}. This provides a bidirectional data path between 3.3-V LVTTL and 2.5-V CMOS, and a one-way data path from 3.3-V LVTTL or 2.5-V CMOS to 1.8-V CMOS. AVC logic also has a power-off isolation feature that disables outputs from the device during system partial power down.

Design Issues and AVC Family Solutions

Low Power (Optimized for 2.5 V)

Perhaps one of the most pervasive trends in advanced digital-electronics design is lower power consumption. Lower power consumption is especially important to extend battery life of portable equipment. Reduced heat dissipation from lower power consumption simplifies the measures necessary to remove heat and decrease the necessary packaging area, leading to production of smaller and less expensive products. One of the most effective ways to reduce power dissipation is to decrease integrated-circuit operating voltages. The AVC family, designed to operate at 2.5-V V_{CC}, enables high-performance, low-power, and advanced designs. Not simply a scaled-down 3.3-V family, AVC is the first logic family conceived and designed for optimized performance at 2.5 V.

Unused and Undriven Inputs (Bus Hold)

A circuit element that must be addressed when designing with a CMOS family, such as AVC, is circuit inputs. With the totem-pole structure (see Figure 3) that characterizes the inputs of CMOS devices, the input node must be held as close to the V_{CC} or GND rails as possible.

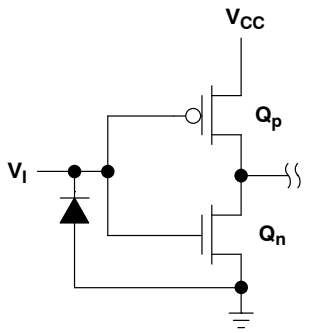


Figure 3. Totem-Pole Input Structure

Precautions should be taken to prevent the input voltage from floating near the threshold voltage because this biases both input transistors on and creates undesirably high I_{CC} currents at the V_{CC} pin of the device. Under certain conditions, this can damage the device. One way to address this concern is to place external pullup resistors at any input that might be in a high-impedance, undriven state. This is costly in terms of component count, reliability, and board area. An alternative solution is to employ the devices in the AVC family that utilize the optional bus-hold circuit at the inputs (see Figure 4). AVC devices with bus-hold circuitry are designated as AVCH.

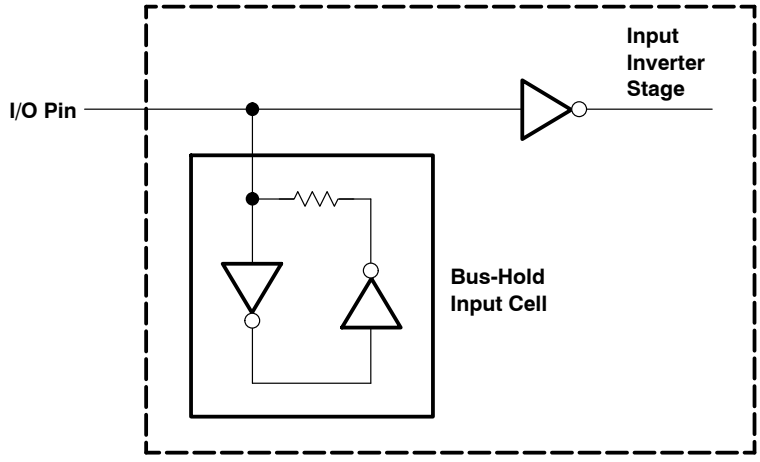


Figure 4. Typical Bus-Hold Cell

The bus-hold circuit consists of two series inverters with the output fed back to the input through a resistor. This provides a weak positive feedback by sinking or sourcing current to the input node. The bus-hold cell holds the input at its last-known valid logic state until forcibly changed by a driving circuit. Figure 5 shows the input characteristics of bus hold as the input voltage is swept from 0 V to 2.5 V. These characteristics are similar to a weak bistable latch. The bus-hold cell sinks current when the input is low, and sources current when the input is high. When the input voltage is near the threshold, the circuit sinks or sources maximum current to force the input node toward either the V_{CC} or GND rail.

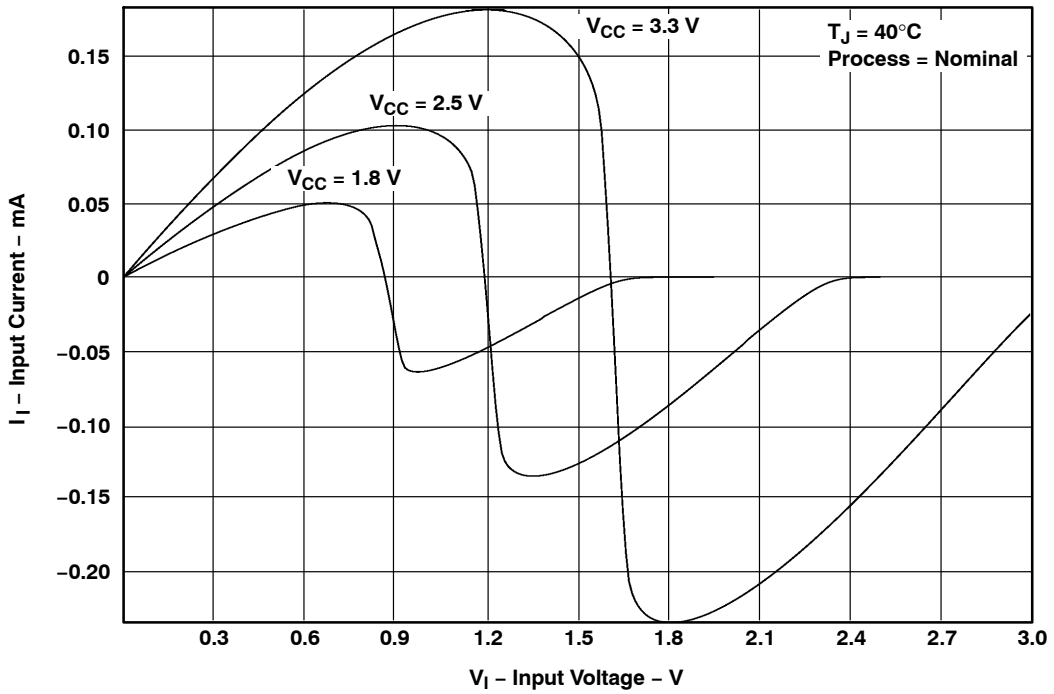


Figure 5. Bus Hold Across V_{CC}

Generally, pullup and pulldown resistors should not be used on the inputs of devices with bus hold. In applications that require pullup or pulldown resistors to hold the inputs at a specific logic level, the $I_{I(hold)}$ maximum specification should be considered. The resistor value should be chosen to overcome bus hold under worst-case conditions. The resistor must supply enough current so that the input is pulled through the threshold to the desired logic level. If the current supplied is too weak, the input node could be held near the threshold, causing a high I_{CC} that could damage the part.

Partial Power-Down and Mixed-Voltage-Mode Data Communication

The inputs and outputs of the AVC family have been designed with all reverse-current paths to V_{CC} blocked. This low I_{OFF} current feature allows the device to remain electrically connected to a bus during partial power down without loading the remaining live circuits. This feature also allows the use of this family in a mixed-voltage environment. If the inputs or outputs are at a voltage greater than the V_{CC} of the device, there is no current sourcing back through the device from the higher voltage node to the lower-voltage V_{CC} supply.

With a bidirectional AVC transceiver powered with 2.5-V V_{CC}, two-way data communication between 3.3-V LVTTL devices and 2.5-V CMOS devices can occur (see Figure 6). The inputs of the AVC part are 3.6-V tolerant and accept the LVTTL switching levels. The outputs of the AVC part, when powered at 2.5-V V_{CC} under worst-case conditions, are accepted as valid switching levels at the input of a 3.3-V LVTTL device.

With a unidirectional AVC driver powered with 1.8-V V_{CC}, data communication from 2.5-V or 3.3-V signal levels to 1.8-V devices can occur (see Figure 7). The inputs of the AVC part are tolerant of the higher voltages and accept the higher switching levels. The outputs of the AVC driver are valid 1.8-V signal levels.

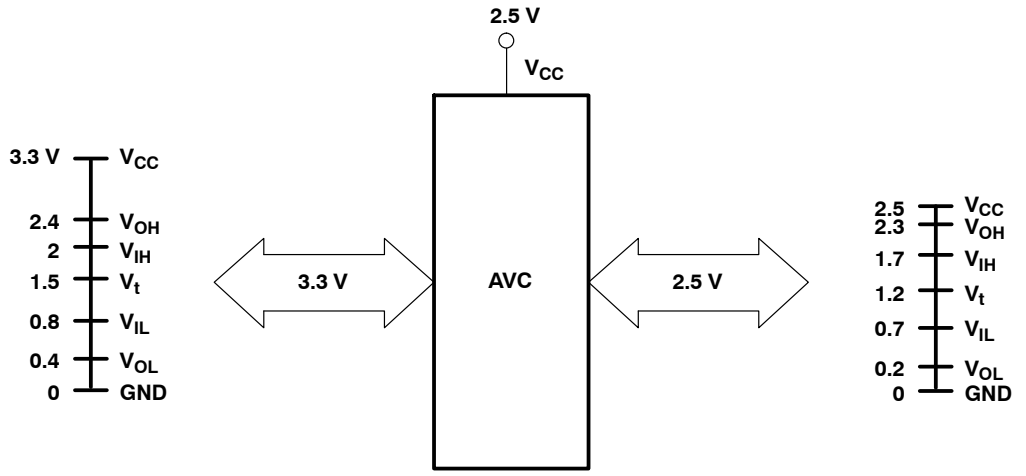


Figure 6. Device at 2.5-V V_{CC} With 3.3-V I/Os on One Side and 2.5-V I/Os on the Other, Showing Switching Levels

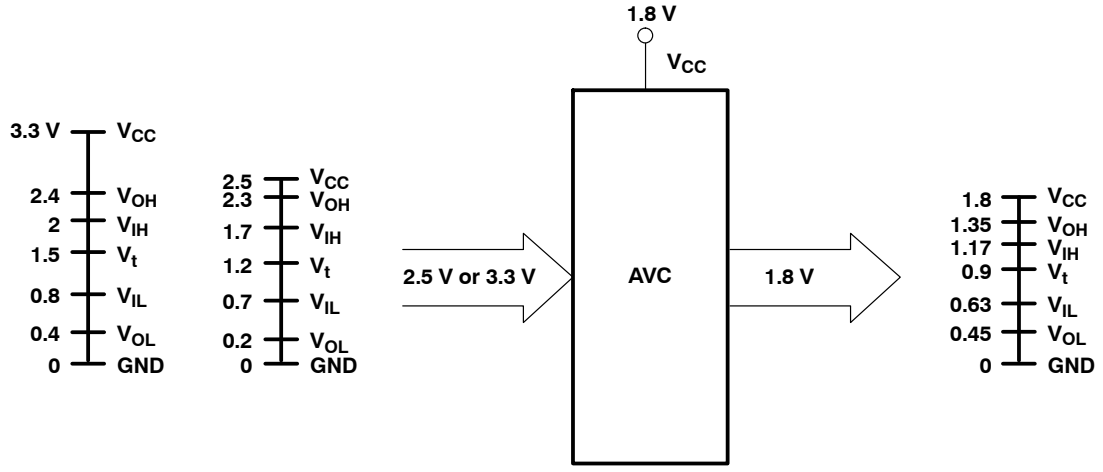


Figure 7. Device at 1.8-V V_{CC} With 2.5-V Inputs or 3.3-V Inputs, Showing Switching Levels

Device Characteristics

To facilitate a preliminary analysis of the characteristics of the AVC family, SPICE analysis graphs from TI's initial AVC-family device, the SN74AVC16245 16-bit bus transceiver with 3-state outputs are shown in Figures 8 through 22. These analyses are the outputs of SPICE simulations using standard loads specified in the parameter measurement information illustrations in Appendix A, unless otherwise noted.

Power Consumption

Figure 8 presents SPICE information about the device dynamic power consumption across the operating frequencies. Table 1 shows modeled values of power dissipation capacitance (C_{pd}). The C_{pd} data were obtained using an input edge rate of 1 ns (0%–100%), open-circuit load on the output, and one output switching with a 48-pin TSSOP (DGG) package.

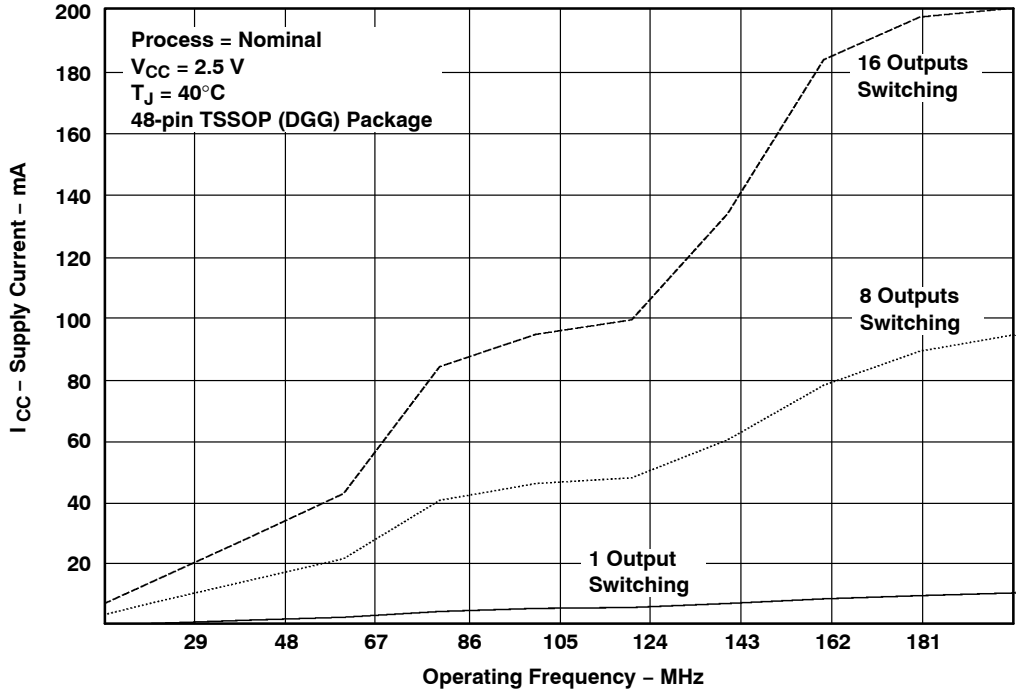


Figure 8. I_{CC} vs Frequency With 1, 8, or 16 Outputs Switching

Table 1. C_{pd} for Various Conditions, One Output Switching

PARAMETER	TEST CONDITIONS C_L = 0, f = 10 MHz	V_{CC} = 1.8 V ± 0.15 V TYP	V_{CC} = 2.5 V ± 0.2 V TYP	V_{CC} = 3.3 V ± 0.3 V TYP
C_{pd}	Outputs enabled	15.9 pF	18.1 pF	21.1 pF
C_{pd}	Outputs disabled	~1 pF	~1 pF	~1 pF

Input Characteristics

Figures 9 and 10 present SPICE information about the device static behavior. Figure 9 shows the device supply-current requirements across input voltage and Figure 10 shows the output-voltage versus input-voltage transfer curves.

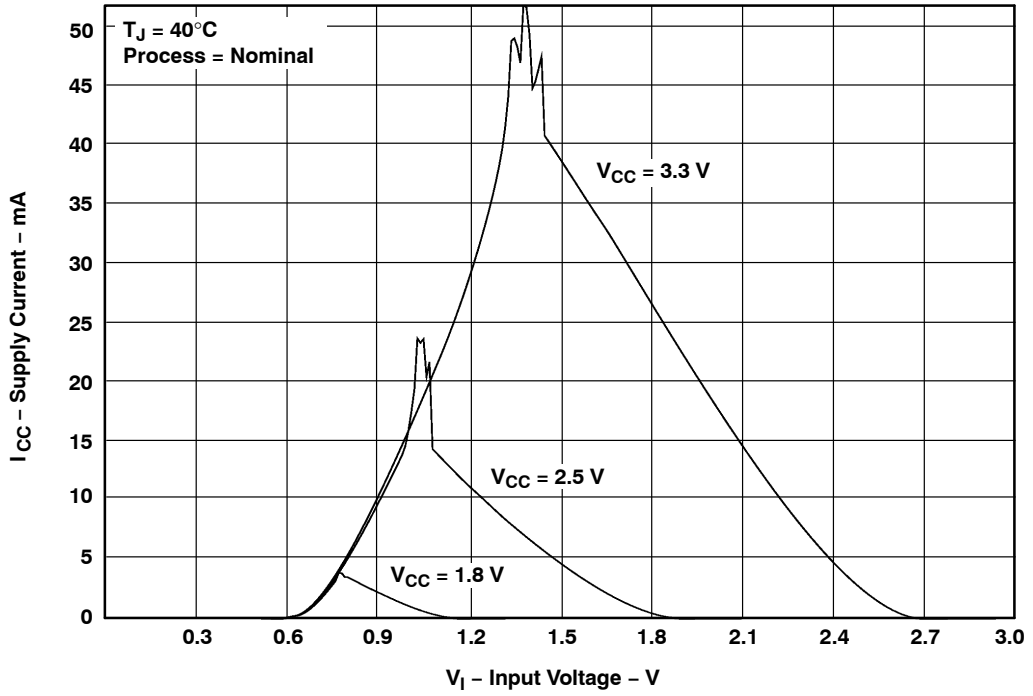


Figure 9. I_{CC} vs V_I

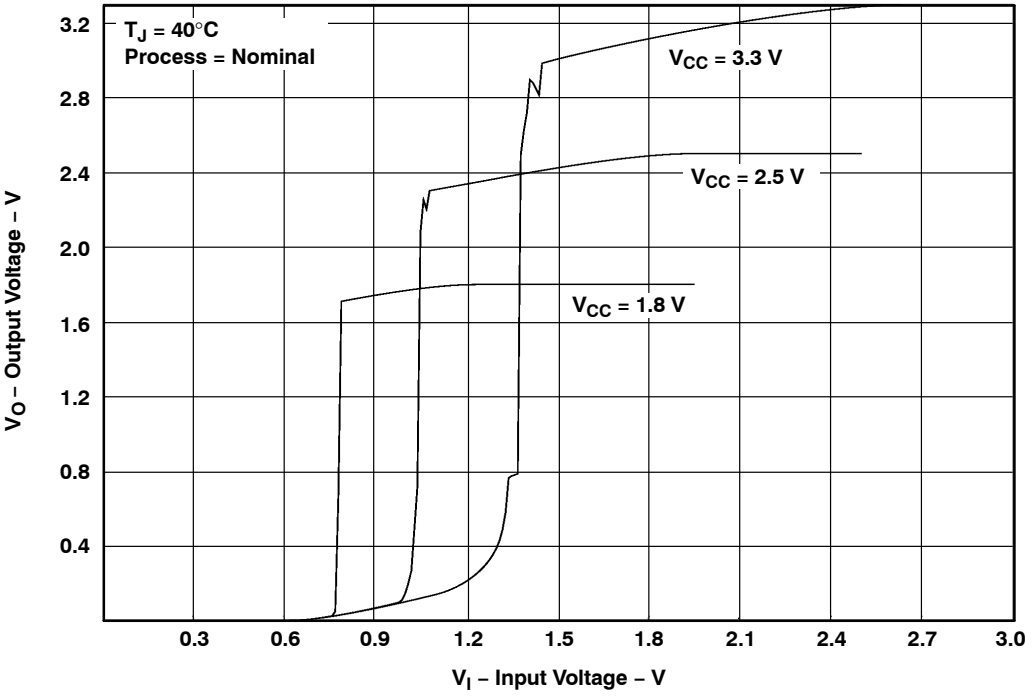


Figure 10. V_O vs V_I

Switching Performance

Figures 11 through 16 present SPICE models of the device dynamic behavior. Propagation delay times across various conditions of ambient temperature, load capacitance with one output switching, and load capacitance with 16 outputs switching are shown.

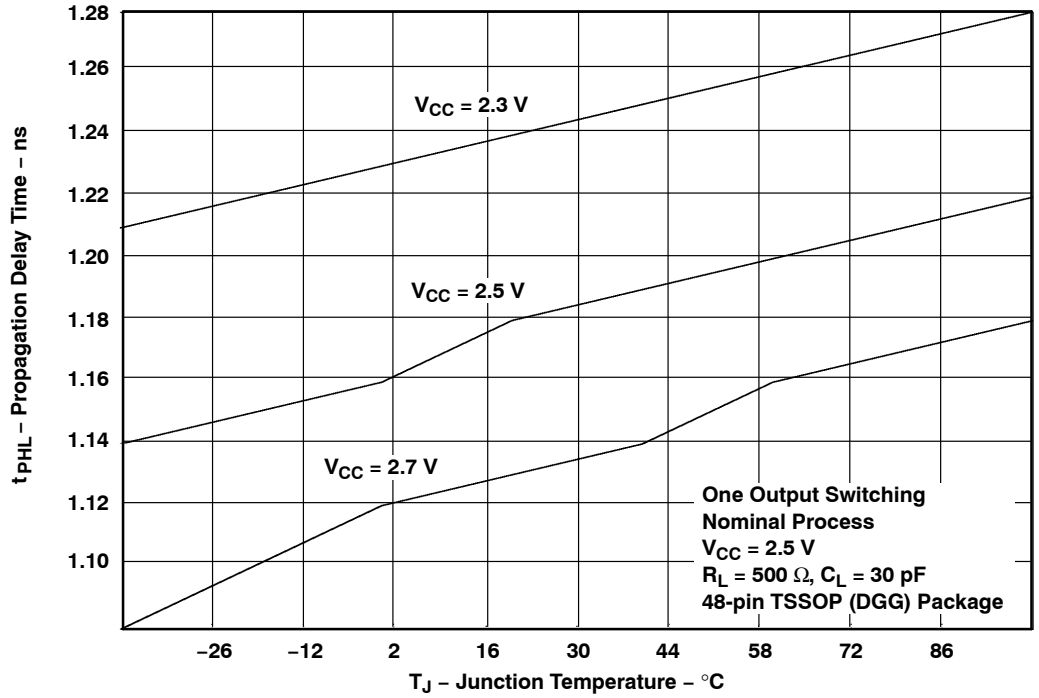


Figure 11. t_{PHL} vs T_J

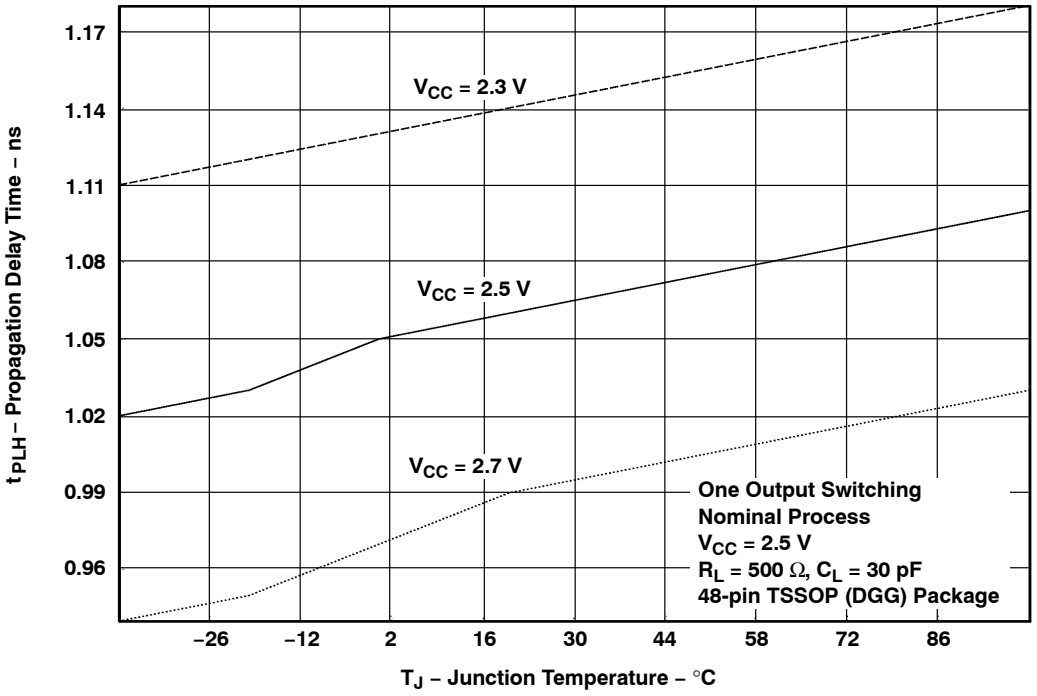


Figure 12. t_{PLH} vs T_J

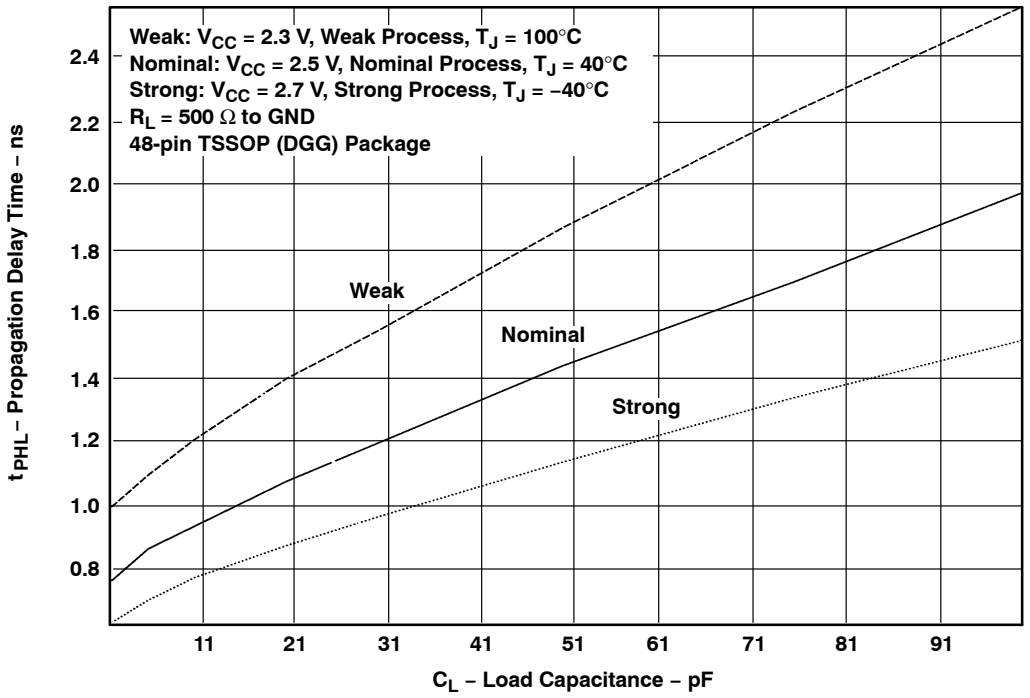


Figure 13. t_{PHL} vs Load Capacitance, One Output Switching

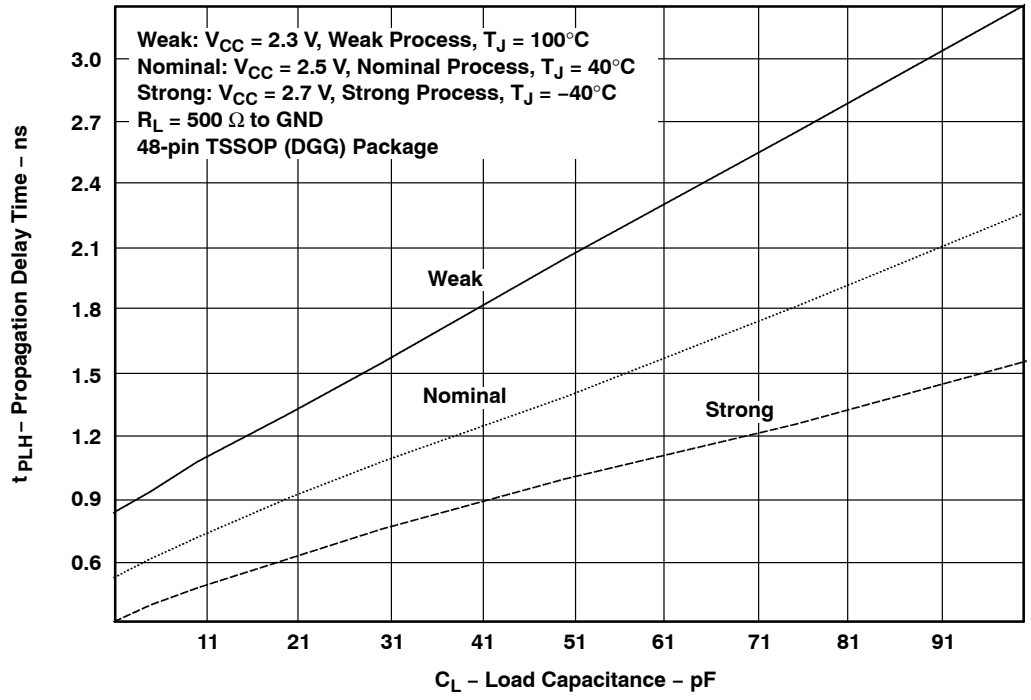


Figure 14. t_{PLH} vs Load Capacitance, One Output Switching

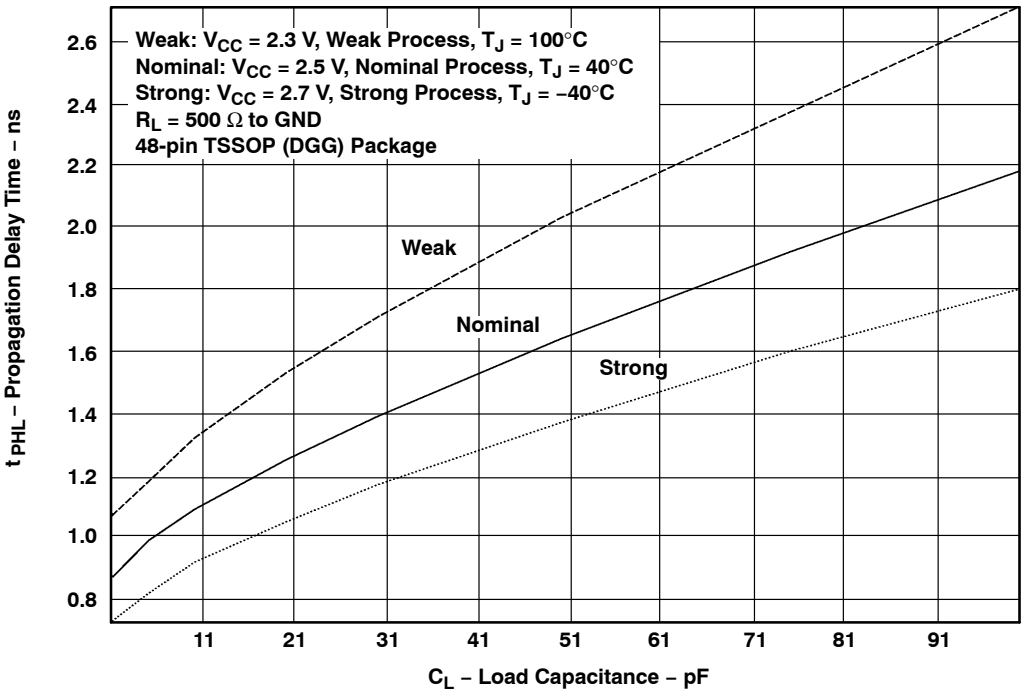


Figure 15. t_{PHL} vs Load Capacitance, 16 Outputs Switching

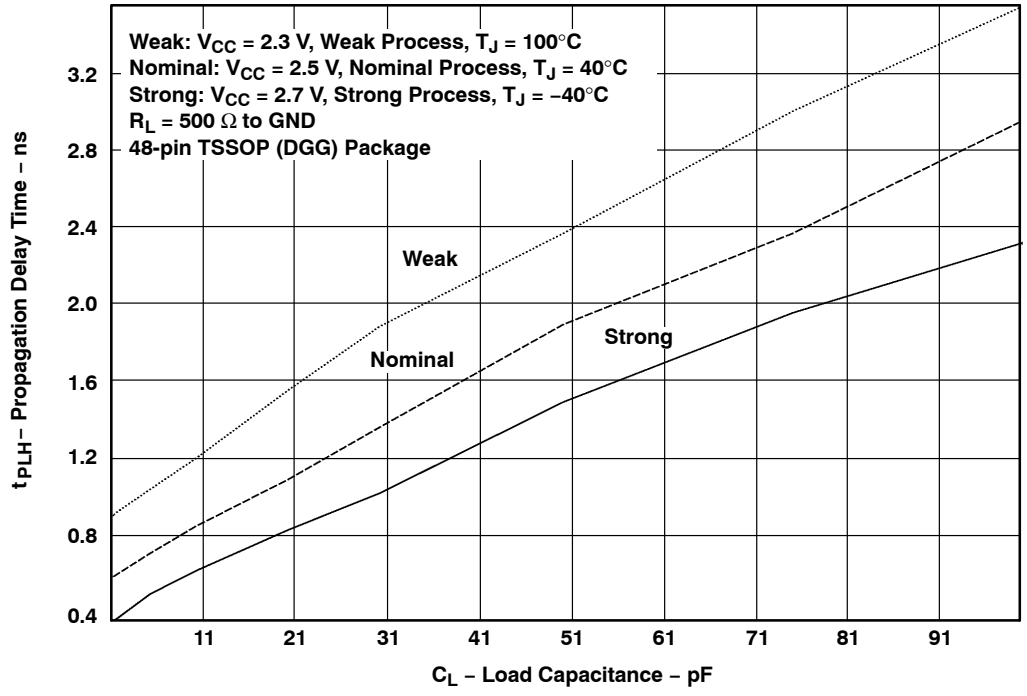


Figure 16. t_{PLH} vs Load Capacitance, 16 Outputs Switching

Signal Integrity

Perhaps the most important measure of a device's performance in the dynamic domain is the effect of varying conditions upon signal integrity. Figures 17 through 20 show SPICE simulations of the device dynamic behavior. The effect of multiple outputs switching simultaneously on one that is held at a valid logic level is shown (see Figures 17 and 18). The effects of slow input-transition time (see Figure 19), and pin-to-pin skew (see Figure 20) are shown.

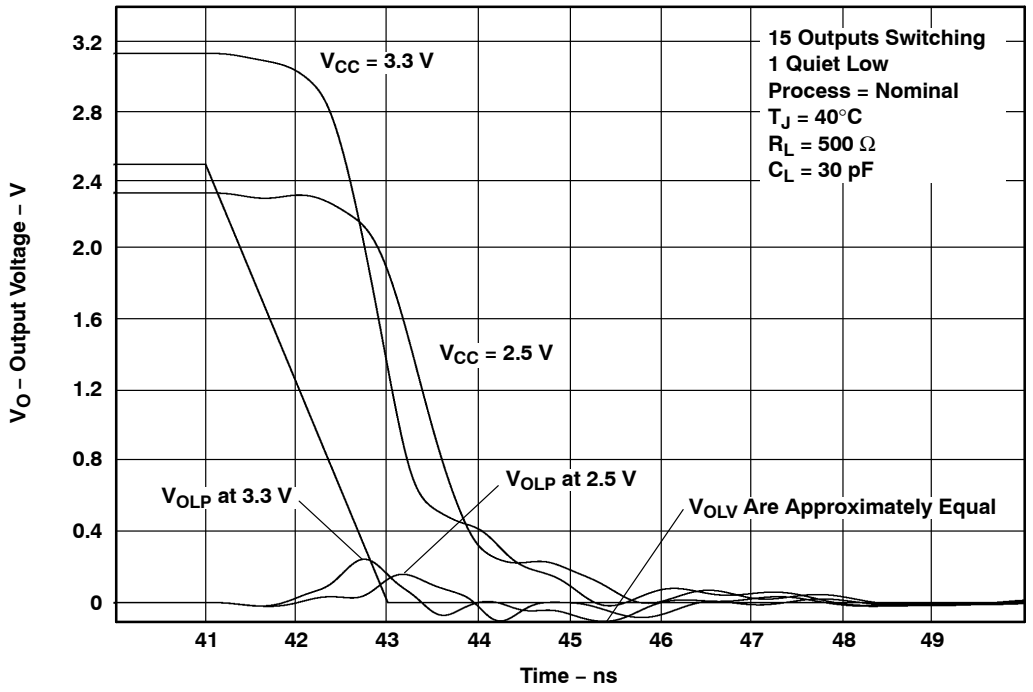


Figure 17. Simultaneous-Switching Voltage (V_{OLP}, V_{OLV}) vs Time

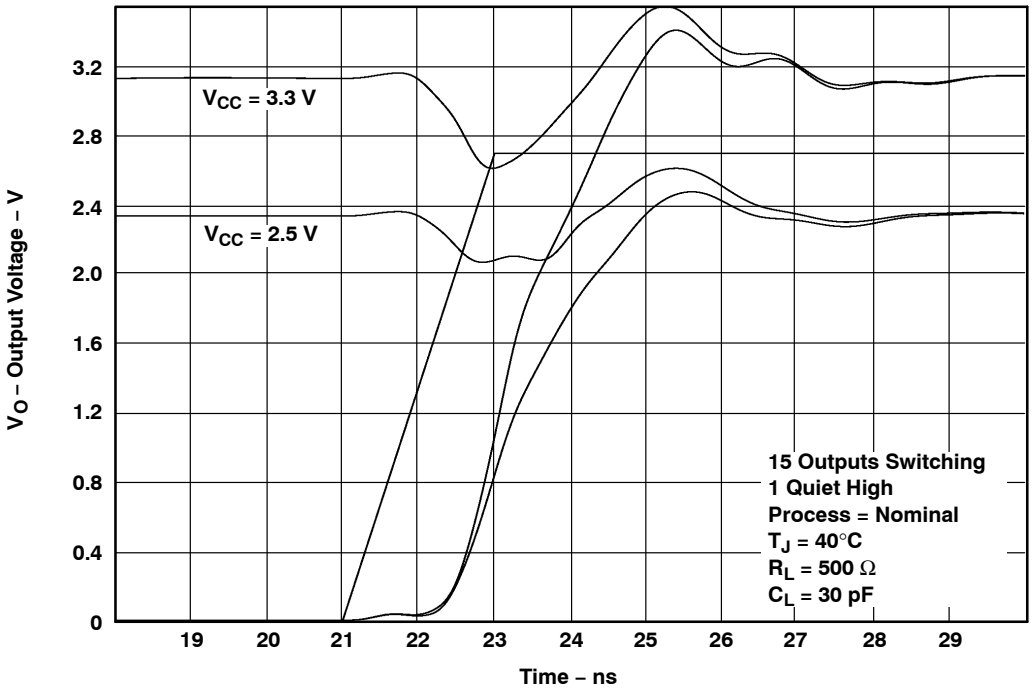


Figure 18. Simultaneous-Switching Voltage (V_{OHP}, V_{OHV}) vs Time

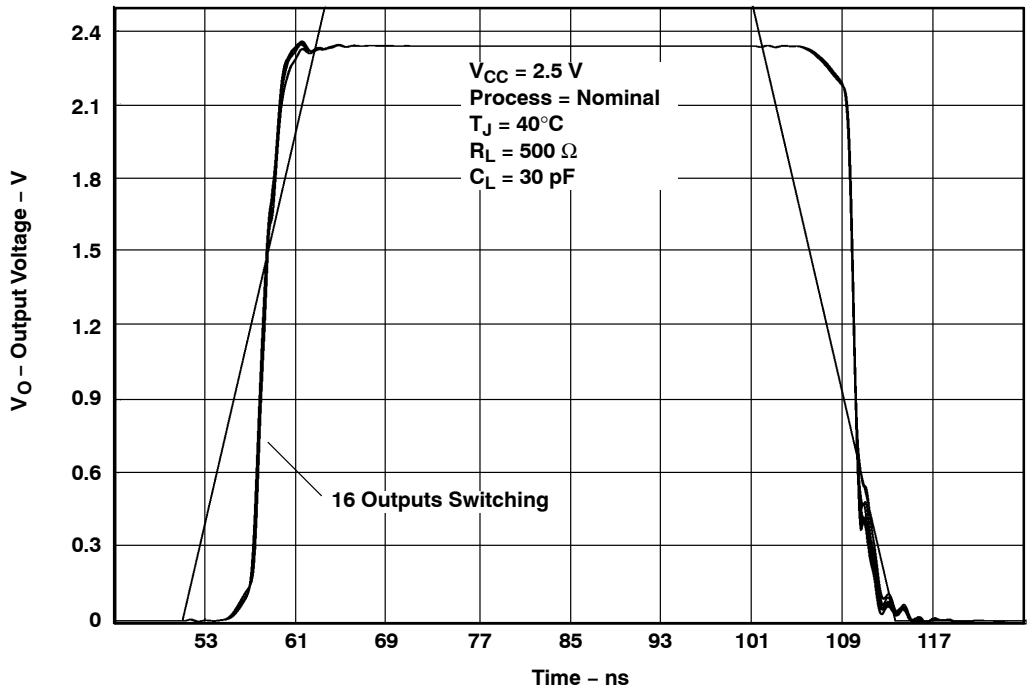


Figure 19. Slow Input-Transition Time

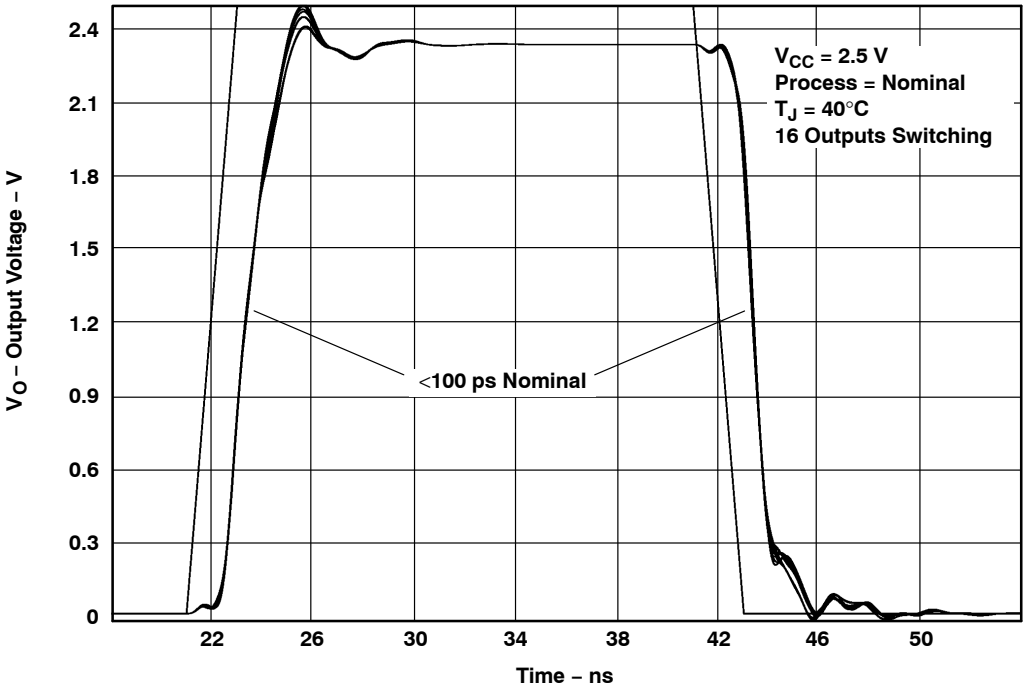


Figure 20. Pin-to-Pin Skew (t_{PHL}, t_{PLH}) (<100 ps nominal)

Output Characteristics With DOC

Selecting a component with improved output drive characteristics simplifies the design engineer's job of ensuring signal integrity and meeting timing requirements. For signal integrity, the output must have an output impedance that minimizes overshoots and undershoots. A component with 26-Ω series damping resistors on the output ports was sometimes necessary to improve the match of the impedance with the transmission-line load on the output of the buffer. The opposing characteristic that must be considered is having sufficient drive to meet the timing requirements. The AVC family features TI's DOC circuit that automatically lowers the output impedance of the circuit during a signal transition and subsequently raises the impedance to reduce overshoot and undershoot. Figures 21 and 22 contain typical voltage and current curves that illustrate the operation of the circuit as it transitions from one state to another.

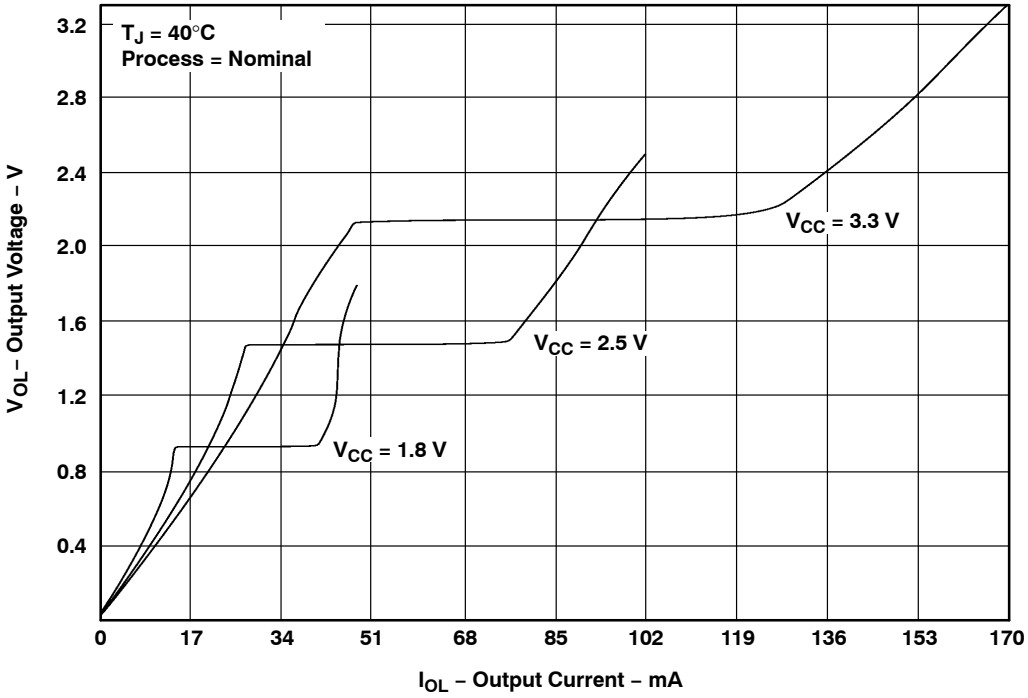


Figure 21. V_{OL} vs I_{OL}

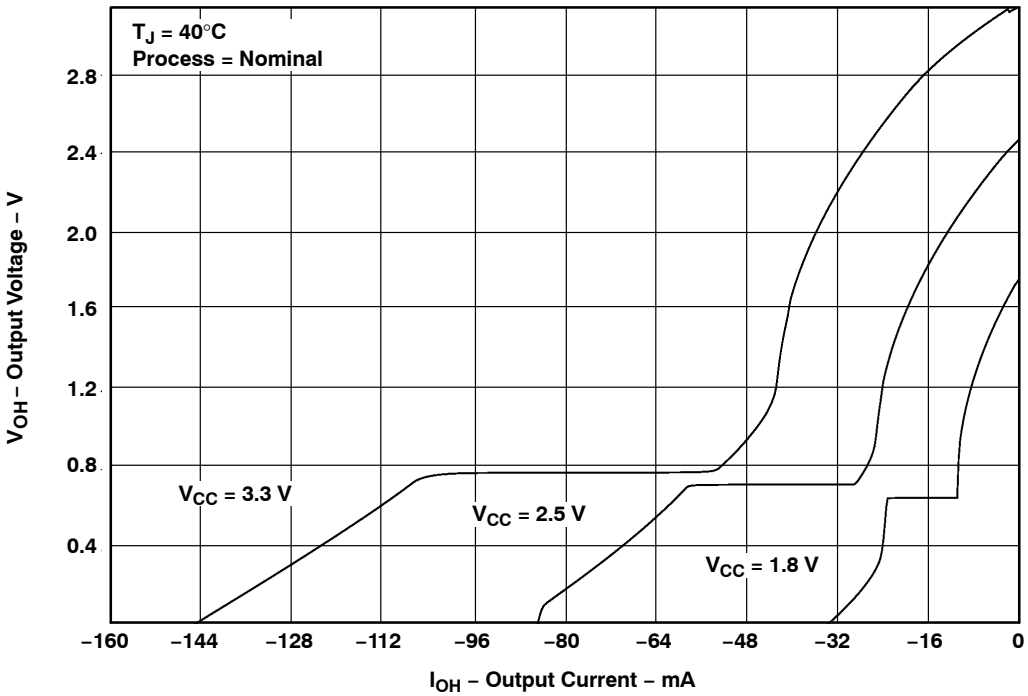


Figure 22. V_{OH} vs I_{OH}

The DOC circuitry provides enough drive current to achieve faster slew rates and meet timing requirements, but quickly switches the impedance level to reduce the overshoot and undershoot noise that is often found in high-speed logic. This feature of AVC logic eliminates the need for damping resistors in the output circuit, which are often used in series, and sometimes integrated with logic devices, to limit electrical noise. Damping resistors reduce the noise, but increase propagation delay due to the decreased drive current.

Because of the excellent signal integrity characteristics of the DOC output, transmission-line termination typically is unnecessary. Due to the high-impedance drive characteristics of the output in the static state, *the use of dc termination is specifically discouraged*. The output current that is required to bias a dc termination network could exceed the static-state output-drive capabilities of the device. AVC with DOC circuitry is ideally suited for any high-speed, point-to-point application or unterminated distributed load, such as high-speed memory interfacing.

Design Support

Examination of the characteristics of the device is a critical portion of a successful design. To aid the design engineer in analysis of device characteristics, the latest versions of IBIS models can be obtained from TI's website at http://www.ti.com. SPICE models are also available from TI. Please contact your local TI field sales representative for more information.

Features and Benefits

Table 2 provides selected AVC family features and benefits.

Table 2. Selected AVC Family Features and Benefits

FEATURES	BENEFITS
Optimized for 2.5-V V_{CC}	Enables low-power designs
Broad product offerings	Simplifies component choice
Advanced EPIC fabrication process; turbo-circuit design	Sub-2-ns (maximum) speeds at 2.5 V. Easier to meet timing windows in advanced high-speed designs
DOC outputs do not require series damping resistors internally or externally	Reduced ringing without series output resistors, increased performance and cost savings
Bus-hold option	Eliminates pullup or pulldown resistors on inputs
I_{OFF} – reverse-current paths to V_{CC} blocked on the inputs and outputs	Outputs disabled during power off for use in partial power down and mixed-voltage designs

Conclusion

For designs that require 1.8-V, 2.5-V, and 3.3-V logic functions with the highest performance, the AVC family provides the fastest, quietest logic devices optimized for 2.5-V and unterminated load conditions. AVC offers a broad line of Widebus and Widebus+ functions, logic gates, and octal bus-interface functions.

Acknowledgment

The authors of this application report are Stephen M. Nolan and Tim Ten Eyck.

Glossary

A

AVC	Advanced very-low-voltage CMOS

C

CMOS	Complementary metal-oxide semiconductor

D

DOC	Dynamic output control (patent pending)

E

EPIC	Enhanced-performance implanted CMOS

I

IBIS	I/O buffer information specification
I_I	Input current
$I_{I(hold)}$	Input current (bus hold)
I_{OH}	High-level output current
I_{OL}	Low-level output current

L

LVTTL	Low-voltage TTL (3.3-V power supply and interface levels)

P

PC	Personal computer

S

SPICE	Simulation program with integrated-circuit emphasis

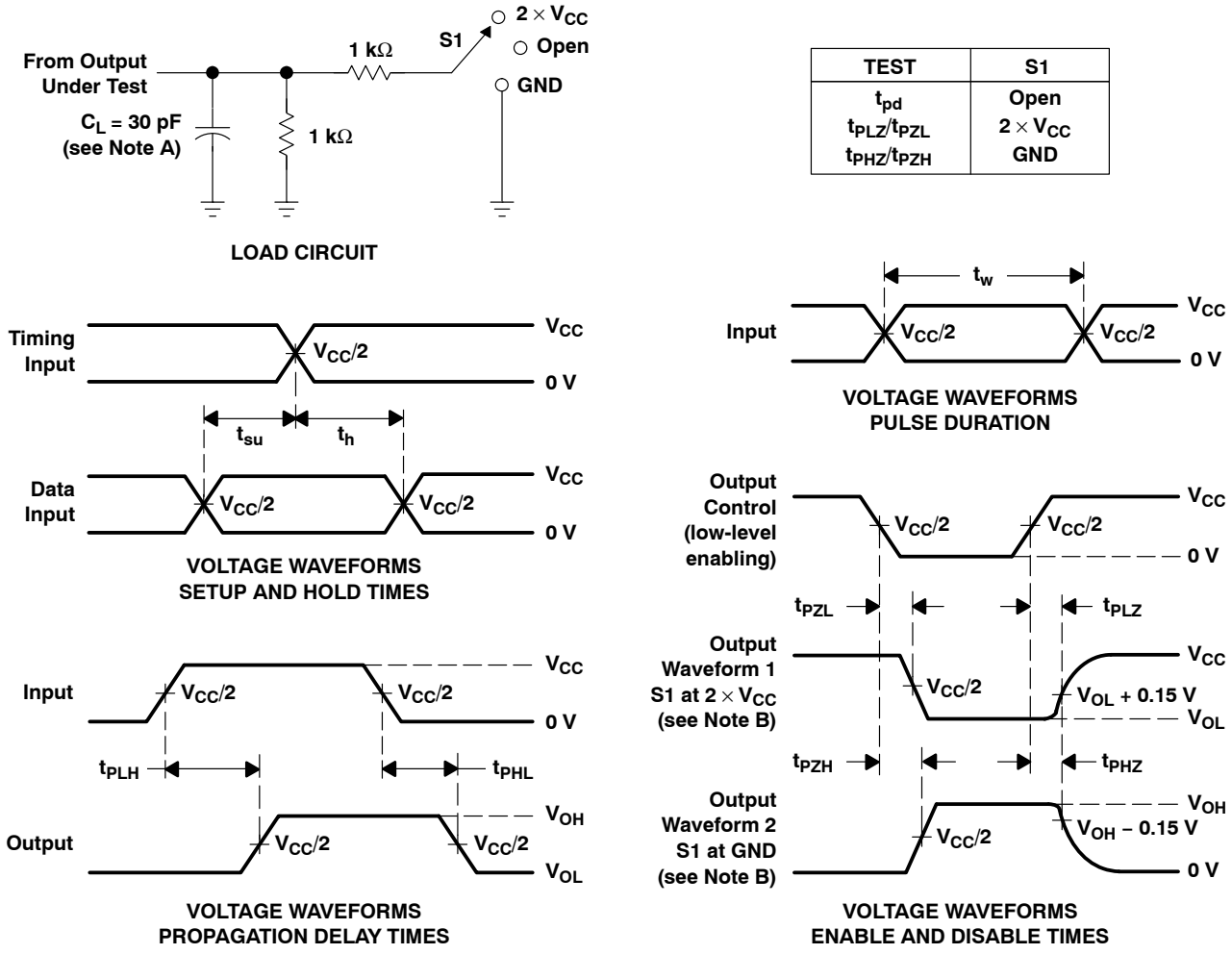
T

t_{pd}	Propagation delay time
t_{PHL}	Propagation delay time, high- to low-level output
t_{PLH}	Propagation delay time, low- to high-level output
TSSOP	Thin shrink small-outline package
TTL	Transistor-transistor logic

V

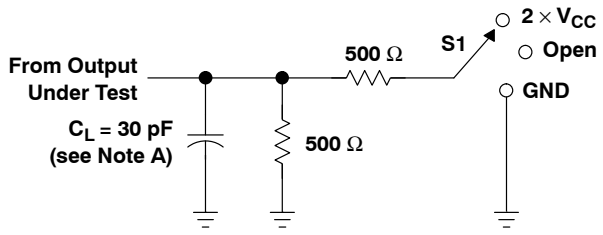
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_{OHP}	High-level output voltage peak
V_{OHV}	High-level output voltage valley
V_{OLP}	Low-level output voltage peak
V_{OLV}	Low-level output voltage valley

Appendix A – Parameter Measurement Information



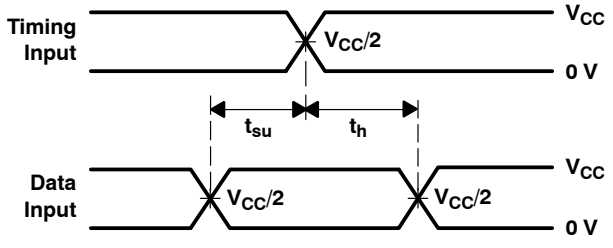
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure A–1. AVC Parameter Measurement Information (1.8 V ± 0.15 V)

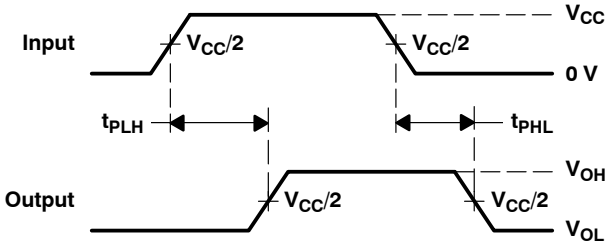


TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 × V_{CC}
t_{PHZ}/t_{PZH}	GND

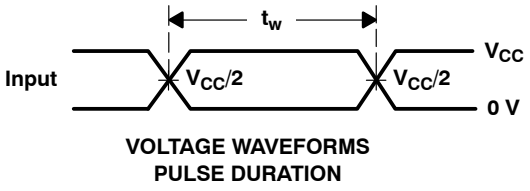
LOAD CIRCUIT



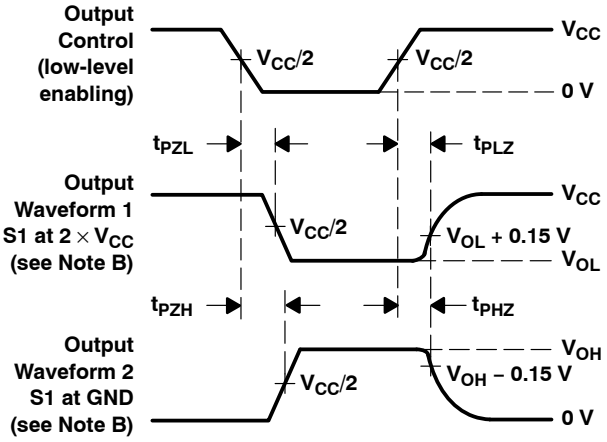
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



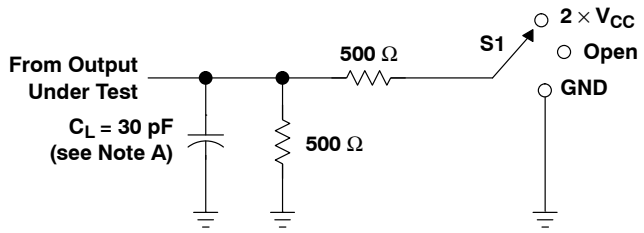
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

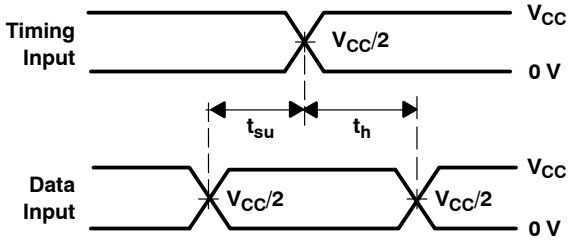
NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure A–2. AVC Parameter Measurement Information (V_{CC} = 2.5 V ± 0.2 V)

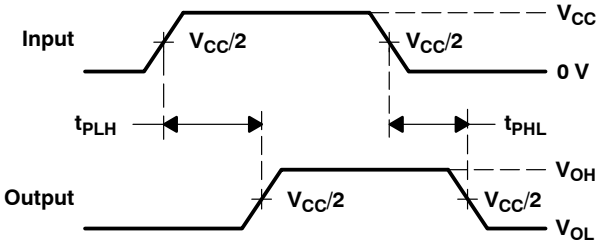


TEST	S1
t_{pd} t_{PLZ}/t_{PZL} t_{PHZ}/t_{PZH}	Open 2 × V_{CC} GND

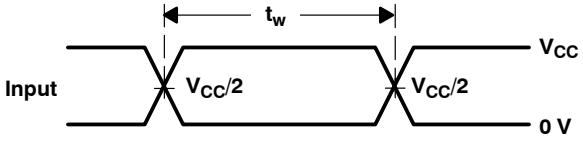
LOAD CIRCUIT



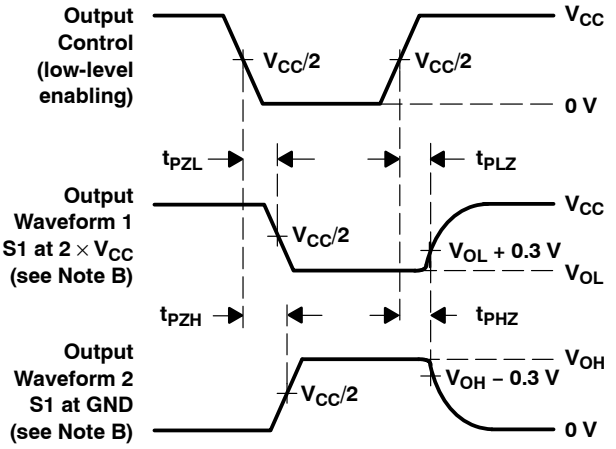
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure A–3. AVC Parameter Measurement Information (V_{CC} = 3.3 V ± 0.3 V)

Migration From 3.3-V to 2.5-V Power Supplies for Logic Devices

SCEA005
December 1997

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Contents

Introduction

Powering systems at the 5-V level has been a standard practice for approximately 30 years. Power consumption is always a concern in system design and, because reducing the supply voltage yields an exponential decrease in power consumption, lower supply voltages are commonly used. Thus, a transition from the common 5-V power-supply level to the 3.3-V level is occurring. Furthermore, the next voltage level for which specified switching levels have been defined is 2.5 V. During this transition, parts of a system may be designed for a lower supply voltage while other parts may not. This raises concerns of input-voltage tolerance, interfacing or translating, and level shifting. This application report explores the possibilities for migrating to 3.3-V and 2.5-V power supplies and discusses the implications.

Customers are successfully using a wide range of low-voltage, 3.3-V logic devices. These devices are within Texas Instruments (TI™) advanced low-voltage CMOS (ALVC), crossbar technology (CBT), crossbar technology with integrated diode (CBTD), low-voltage crossbar technology (CBTLV) and low-voltage CMOS “A” revision (LVC-A) logic families. Additionally, TI plans to release a level shifter that generates valid 3.3-V and 2.5-V signals.

The transition from 5-V to 3.3-V logic began with core logic converting first to the lower power-supply level. Although memory is still primarily at the 5-V level, it is being converted to 3.3 V, and this conversion will continue. The same method of migration is expected for 3.3 V to 2.5 V, with memory logic following core logic by several years.

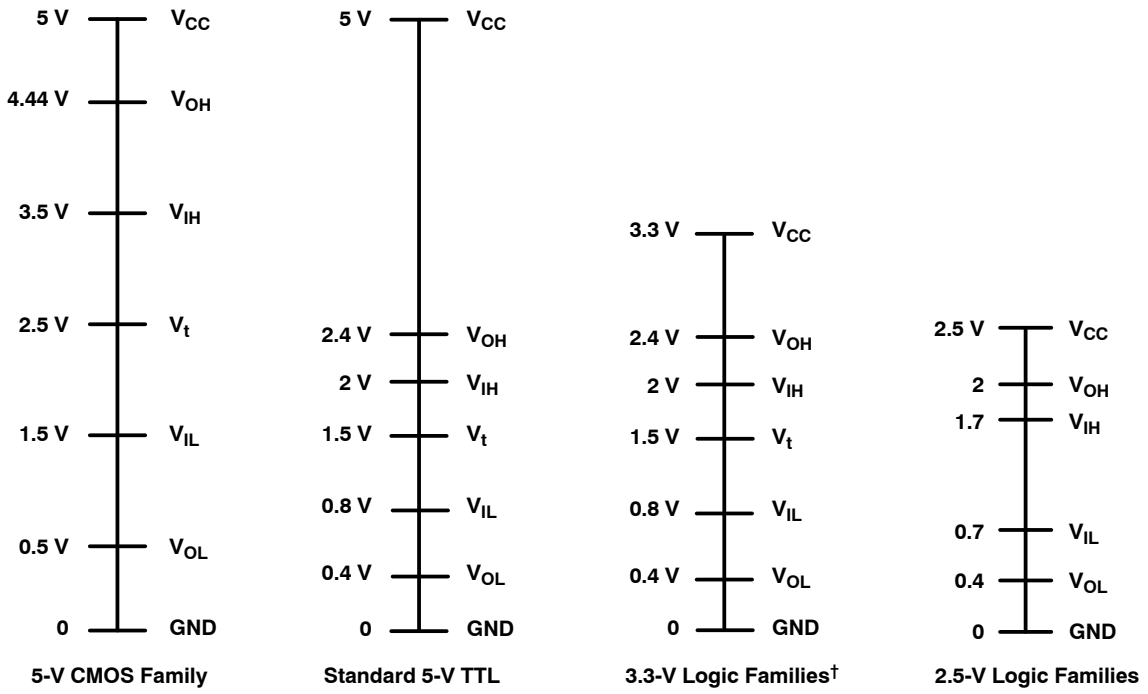
The main topics in this application report are:

- Background
- Technology
- Features and Uniqueness of Devices
- Typical Design Applications
- Laboratory Testing
- Results
- SPICE/IBIS Models
- Package Information
- Frequently Asked Questions
- Conclusion
- Glossary
- Bibliography

Background

The transition from one power-supply level to a lower one is driven primarily by a desire to reduce power consumption. For approximately the last 30 years, 5-V power supplies have been the standard for both core and memory logic. However, core logic has begun to migrate to 3.3-V power-supply levels, and memory has followed. The next commonly accepted power-supply level is 2.5 V and designers are beginning to incorporate it in their systems. This sets the stage for 1.8-V logic, for which a standard has not been established.

For each power-supply level, a standard exists for defining commonly agreed-upon levels of input and output voltages. Figure 1 shows the appropriate switching levels for 5-V, 3.3-V, and 2.5-V V_{CC} families.



† In accordance with JEDEC Standard 8-A for LV interface levels

Figure 1. Switching Levels for 5-V, 3.3-V, and 2.5-V V_{CC} Families

Technology

Table 1 lists the logic families TI produces that operate at 3.3-V V_{CC}. The process, the power-supply level for which the device was designed and optimized, and whether the device can operate at 3.3-V and 2.5-V V_{CC} levels are included.

Table 1. Logic Family Technology Summary

LOGIC FAMILY	PROCESS	OPTIMIZED POWER SUPPLY LEVEL	OPERATIONAL AT V_{CC} = 3.3 V	OPERATIONAL AT V_{CC} = 2.5 V
AHC	CMOS	5 V	Yes	Yes
ALVC	CMOS	3.3 V	Yes	Yes
CBT	CMOS†	5 V	Yes	Yes
CBTD	CMOS	5 V	Yes	Yes
CBTLV	CMOS	3.3 V	Yes	Yes
LVC-A	CMOS	3.3 V	Yes	Yes

† The CBT16232, CBT16233, and CBT16390 devices are BiCMOS.

In Table 1, CMOS process indicates that the devices contain solely CMOS circuitry. The BiCMOS process indicates that a combination of bipolar and CMOS transistors may be implemented in the circuitry.

Features and Uniqueness of Devices

When discussing interactions between different power-supply levels, the distinction between input-voltage tolerance, interfacing or translating, and level shifting is important. Input-voltage tolerance applies when a device with a lower power supply can withstand the presence of a higher voltage without being damaged. For example, a 3.3-V device drives a 2.5-V device without harming the receiver. Under this concept, there is no implication about the device being able to produce a signal compatible with the higher power-supply level. Interfacing or translating implies that a device can generate valid input and output voltage levels, even though a single power-supply level is being used. A device is a level shifter when it implements two power supplies and can produce signals that conform to the switching requirements of both the lower-voltage power supply and the higher-voltage power supply.

All devices in the families listed in Table 1 operate and function correctly when powered at 3.3-V and 2.5-V V_{CC}. The following paragraphs address how the devices interact when they are operated at one power-supply level and are exposed to signals from a device operated at a different power-supply level.

Figure 1 illustrates that a 3.3-V device can adequately drive a 2.5-V device. $V_{OL(3.3\text{-V logic})}$ (0.4 V) is less than $V_{IL(2.5\text{-V logic})}$ (0.7 V), which allows a 300-mV noise margin. Similarly, $V_{OH(3.3\text{-V logic})}$ (2.4 V) is greater than $V_{IH(2.5\text{-V logic})}$ (1.7 V), which allows for a 700-mV noise margin. Table 2 summarizes the compatibility between 3.3-V and 2.5-V devices when both are powered at 3.3-V V_{CC}.

Table 2. 3.3-V to 2.5-V Compatibility When V_{CC} = 3.3 V

LOGIC FAMILY	2.5-V TOLERANT	2.5-V SWITCHING LEVELS GENERATED
AHC	Yes	Yes
ALVC	Yes	Yes
CBT†	Yes	Yes
CBTD†	Yes	Yes
CBTLV†	Yes	Yes
LVC-A	Yes	Yes

† CBT, CBTD, and CBTLV families are limited by the input voltage.

A 2.5-V device cannot adequately drive a 3.3-V device. $V_{OL(2.5\text{-V logic})}$ (0.4 V) is less than $V_{IL(3.3\text{-V logic})}$ (0.8 V), which allows a 400-mV noise margin. However, $V_{OH(2.5\text{-V logic})}$ (2 V) is approximately equal to $V_{IH(3.3\text{-V logic})}$ (2 V), which theoretically allows no noise margin. Therefore, 2.5-V devices should not be used to drive 3.3-V devices. Table 3 summarizes the compatibility between 2.5-V and 3.3-V devices when both are powered at 2.5-V V_{CC}.

Table 3. 2.5-V to 3.3-V Compatibility When V_{CC} = 2.5 V

LOGIC FAMILY	3.3-V TOLERANT	3.3-V SWITCHING LEVELS GENERATED
AHC	Yes	No
ALVC	No	No
CBT	Yes	No
CBTD	Yes	No
CBTLV	Yes	No
LVC-A	Yes	No

Typical Design Applications

When migrating from 5-V power supplies to 3.3-V power supplies, migration from 3.3 V to 2.5 V is expected to occur in stages. Specifically, core logic will make the transition to 2.5 V, while memory and I/Os probably will lag. The configuration in Figure 2 likely will be commonplace.

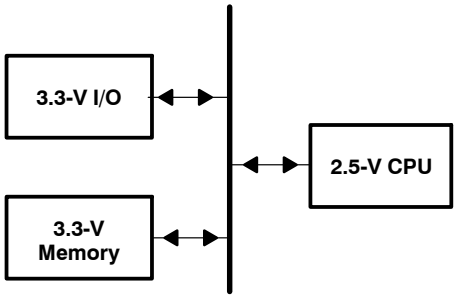


Figure 2. Typical Anticipated 3.3-V/2.5-V Architecture

The CPU operates at 2.5-V V_{CC} and must communicate with a 3.3-V V_{CC} memory and I/O. For all unidirectional data flow from the memory and I/O to the CPU, e.g., reading from memory and receiving input from the I/O, any device that is powered at 3.3-V V_{CC} is acceptable. However, for all communication and data transfer from the CPU to memory or the I/O, such as address buffering and printing, only a device with level-shifting capabilities that can generate true 3.3-V signals from a 2.5-V input should be used.

Laboratory Testing

To demonstrate the ability of TI devices to operate at both 3.3-V and 2.5-V V_{CC} levels, several devices were tested to determine typical propagation delay times. Because typical values were desired, V_{CC} was set to 3.3 V and 2.5 V, and the ambient temperature was 25°C. Tables 4 and 5 show the conditions under which the measurements were taken and the results obtained.

Results

Data in Tables 4 and 5 show that under the same conditions a device's propagation delay increases as V_{CC} is reduced and decreases as the capacitive load is decreased.

Table 4. Typical Propagation Delays When V_{CC} = 3.3 V

LOGIC FAMILY	DIRECTION	CAPACITIVE LOAD (pF)	t_{pd} OR t_{PLH}/t_{PHL} (TYPICAL)
AHC245	A <--> B	30	4.3/3.7 ns
		50	4.6/3.9 ns
AHC16245	A <--> B	30	4.3/3.7 ns
		50	6.8/5.6 ns
ALVC16245	A to B	30	1.4/1.7 ns
		50	1.8/2.2 ns
CBT	A <--> B	50	750 ps
CBTD	A <--> B	50	750 ps
CBTLV3245	A <--> B	50	600 ps
LVCH245A	A <--> B	50	2.7/3.1 ns
LVCH16245A	A to B	30	2.1/2.2 ns
		50	2.8/2.5 ns

Table 5. Typical Propagation Delays When V_{CC} = 2.5 V

LOGIC FAMILY	DIRECTION	CAPACITIVE LOAD (pF)	t_{pd} OR t_{PLH}/t_{PHL} (TYPICAL)
AHC245	A <--> B	30	5.6/4.6 ns
		50	6/5 ns
AHC16245	A <--> B	30	5.6/4.5 ns
		50	9.4/7.2 ns
ALVCH16245	A to B	30	2.4/2.5 ns
		50	3.6/2.8 ns
CBT	A <--> B	50	900 ps
CBTD	A <--> B	50	900 ps
CBTLV3245	A <--> B	30	500 ps
		50	700 ps
LVCH245A	A to B	50	3.1/3.6 ns
	B to A		3.1/3.5 ns
LVCH16245A	A to B	30	2.8/2.7 ns
		50	4.1/3.1 ns

SPICE/IBIS Models

SPICE and IBIS models are available for certain devices. Appendix A lists SPICE and IBIS models for given functions within a logic family.

The SPICE model is a level-13 model that consists of the input and output stages and can be obtained by contacting your local TI Sales Representative. The IBIS model consists of the input and output stages and can be obtained at the TI web site http://www.ti.com/sc/docs/asl/models/ibis.htm.

Package Information

The devices discussed in this application report are available in a variety of packages, including plastic dual-in-line package (PDIP), quarter-size outline package (QSOP), small-outline integrated circuit (SOIC), small-outline transistor (SOT), shrink small-outline package (SSOP), thin shrink small-outline package (TSSOP), and thin very small-outline package (TVSOP). TI's Logic Selection Guide, literature number SDYU001, lists devices and packages in which they are available.

Frequently Asked Questions

Question: How do I reconcile differences between the 3.3-V part of my system and the 2.5-V part?

Answer: When designing with multiple power-supply levels in a single system, ensure that the devices that are powered with the lower-voltage power supply are not damaged when interfacing with the part of the system that is powered by the higher-voltage power supply. This is accomplished by ensuring that all devices are voltage tolerant of the other devices. For the purposes of this application report, any 2.5-V device must be 3.3-V tolerant to ensure that no damage occurs to the 2.5-V device.

Question: With the CBT logic family, I could interface the 5-V part of my system with the 3.3-V part of my system by adding a diode between the external V_{CC} and the output-enable terminals. Can I use a similar method with the CBTLV family to interface between the 3.3-V part and 2.5-V part of my system?

Answer: To drive the CBTLV output levels fully to the rail, a PMOS transistor was added to the circuitry. This PMOS and its associated circuitry prevent the CBTLV family of devices from level translating between 3.3 V and 2.5 V. However, the CBT family is capable of performing this function. Please see item 1 in the bibliography.

Question: How do I get a copy of the SPICE and IBIS models?

Answer: The SPICE models can be obtained by contacting your local TI Sales Representative. The IBIS models can be obtained at http://www.ti.com/sc/docs/asl/models/ibis.htm.

Conclusion

As systems migrate from 3.3-V to 2.5-V power supplies, issues of input-voltage tolerance, interfacing or translating, and level shifting must be addressed. A 3.3-V device can drive a 2.5-V device, but a 2.5-V device cannot drive a 3.3-V device due to switching-level incompatabilities. TI offers a variety of logic families that are capable of operating at 3.3-V and 2.5-V V_{CC} levels.

Glossary

AHC	Advanced High-Speed CMOS
ALVC	Advanced Low-Voltage CMOS
CBT	Crossbar Technology
CBTLV	Low-Voltage Crossbar Technology
CPU	Central Processing Unit
IBIS	I/O Buffer Information Specification
I/O	Input/Output
LVC-A	Low-Voltage CMOS “A” Revision
LVTTL	Low-Voltage Transistor-Transistor Logic
PDIP	Plastic Dual-In-line Package
QSOP	Quarter-Size Outline Package
SOIC	Small-Outline Integrated Circuit
SOT	Small-Outline Transistor
SPICE	Simulation Program With Integrated-Circuit Emphasis
SSOP	Shrink Small-Outline Package
TI	Texas Instruments
TSSOP	Thin Shrink Small-Outline Package
TVSOP	Thin Very Small-Outline Package

Bibliography

1. 3.3-V to 2.5-V Translation with Texas Instruments Crossbar Technology, literature number SCDA004
2. Advanced Bus Interface SPICE I/O Models, 1995, literature number SCBD004A
3. AHC/AHCT, HC/HCT, and LV CMOS Logic Data Book, 1996, literature number SCLD004
4. CBT Bus Switches, Crossbar Technology Data Book, 1996, literature number SCDD001A
5. Logic Selection Guide, literature number SDYU001 (revised quarterly)
6. Low-Voltage CMOS Logic Data Book, 1997, literature number SCBD152
7. Low-Voltage Logic Data Book, 1996, literature number SCBD003B
8. Semiconductor Group Package Outlines Reference Guide, literature number SSYU001

Appendix A

Available SPICE and IBIS Models

LOGIC FUNCTION	LOGIC FAMILY†			
	AHC	ALVC	CBT	LVC-A
’00	S	NA	NA	S/I
’02	S	NA	NA	S/I
’04	S	NA	NA	S/I
’08	S	NA	NA	S/I
’10	NA	NA	NA	S/I
’14	S	NA	NA	S/I
’32	–––	NA	NA	S/I
’74	–––	NA	NA	S/I
’86	–––	NA	NA	S/I
’112	NA	NA	NA	S/I
’125	S	NA	NA	S/I
’126	S	NA	NA	S
’137	NA	NA	NA	S/I
’138	–––	NA	NA	S/I
’139	–––	NA	NA	S
’157	–––	NA	NA	S/I
’158	NA	NA	NA	S
’240	–––	NA	NA	S
’241	NA	NA	NA	S
’244	–––	NA	NA	S/I
’245	–––	NA	NA	S
’257	NA	NA	NA	S/I
’258	NA	NA	NA	S
’373	–––	NA	NA	S
’374	–––	NA	NA	S/I
’540	–––	NA	NA	S
’541	–––	NA	NA	S
’543	NA	NA	NA	S/I
’544	NA	NA	NA	S
’573	–––	NA	NA	S
’574	–––	NA	NA	S
’646	NA	NA	NA	S/I
’652	NA	NA	NA	S/I
’821	NA	NA	NA	S
’823	NA	NA	NA	S
’827	NA	NA	NA	S
’828	NA	NA	NA	S

LOGIC FUNCTION	LOGIC FAMILY†			
	AHC	ALVC	CBT	LVC-A
’841	NA	NA	NA	S
’843	NA	NA	NA	S
’861	NA	NA	NA	S
’863	NA	NA	NA	S
’2952	NA	NA	NA	S/I
’16233	NA	NA	S	NA
’16240	–––	S	NA	S/I
’162240	NA	S	NA	NA
’16241	NA	NA	NA	S
’16244	–––	S/I	NA	S/I
’162244	NA	S/I	NA	S/I
’16245	–––	S/I	NA	S/I
’162245	NA	S	NA	–––
’16260	NA	S	NA	NA
’162260	NA	S	NA	NA
’162268	NA	S	NA	NA
’16269	NA	S	NA	NA
’162269	NA	–––	NA	NA
’16270	NA	S	NA	NA
’16271	NA	S	NA	NA
’16272	NA	S	NA	NA
’16280	NA	S	NA	NA
’162280	NA	–––	NA	NA
’16282	NA	S	NA	NA
’162282	NA	–––	NA	NA
’16334	NA	S/I	NA	NA
’162334	NA	S/I	NA	NA
’16344	NA	S	NA	NA
’162344	NA	S	NA	NA
’16373	–––	S	NA	S/I
’162373	NA	S	NA	NA
’16374	–––	S/I	NA	S/I
’162374	NA	S	NA	NA
’16409	NA	S	NA	NA
’162409	NA	–––	NA	NA
’16500	NA	S	NA	NA
’16501	NA	S	NA	NA

† S = SPICE model exists; I = IBIS model exists; NA = Not applicable, indicating that the device does not exist for that particular family; ––– = neither SPICE nor IBIS model exists.

Available SPICE and IBIS Models (Continued)

LOGIC FUNCTION	LOGIC FAMILY†			
	AHC	ALVC	CBT	LVC-A
’16524	NA	–––	NA	NA
’16525	NA	–––	NA	NA
’16540	–––	S	NA	S/I
’162540	NA	S	NA	NA
’16541	–––	S	NA	S/I
’162541	NA	S	NA	NA
’16543	NA	S	NA	S/I
’16600	NA	S	NA	NA
’16601	NA	S	NA	NA
’162601	NA	S/I	NA	NA
’16646	NA	S	NA	S/I
’16652	NA	S	NA	S/I
’16721	NA	S/I	NA	NA
’162721	NA	S/I	NA	NA
’16820	NA	S	NA	NA
’162820	NA	S/I	NA	NA
’16821	NA	S/I	NA	NA
’16823	NA	S/I	NA	NA
’16825	NA	S	NA	NA

LOGIC FUNCTION	LOGIC FAMILY†			
	AHC	ALVC	CBT	LVC-A
’16827	NA	S/I	NA	NA
’162827	NA	S/I	NA	NA
’16828	NA	S	NA	NA
’16830	NA	S/I	NA	NA
’162830	NA	–––	NA	NA
’16831	NA	–––	NA	NA
’162831	NA	–––	NA	NA
’16832	NA	–––	NA	NA
’162832	NA	–––	NA	NA
’16835	NA	S/I	NA	NA
’162835	NA	S/I	NA	NA
’16836	NA	S/I	NA	NA
’162836	NA	S/I	NA	NA
’16841	NA	S	NA	NA
’162841	NA	–––	NA	NA
’16843	NA	S	NA	NA
’16863	NA	–––	NA	NA
’16901	NA	S	NA	NA
’16952	NA	S	NA	S/I

† S = SPICE model exists; I = IBIS model exists; NA = Not applicable, indicating that the device does not exist for that particular family; ––– = neither SPICE nor IBIS model exists.

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Bus-Interface Devices With Output-Damping Resistors or Reduced-Drive Outputs

SCBA012A
August 1997

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Introduction

The spectrum of bus-interface devices with damping resistors or balanced/light output drive currently offered by various logic vendors is confusing at best. Inconsistencies in naming conventions and methods used for implementation make it difficult to identify the best solution for a given application. This report attempts to clarify the issue by looking at several vendors' approaches and discussing the differences.

Output-Damping Resistors

The purpose of integrating output-damping resistors in line buffers and drivers is to suppress signal undershoots and overshoots on the transmission line through what is usually referred to as line-impedance matching (see Figure 1). The effective output impedance of the line driver (Z_O) is matched with the line impedance (Z_L). Thus, no signal reflection occurs at the line start ($Z_O = Z_L$; reflection coefficient at point A is 0). The input impedance of the receiving device (Z_I) is assumed to be several orders of magnitude higher than the line impedance. This is valid for CMOS and BiCMOS devices. In this case, the reflection coefficient at point B is approximately 1, such that almost all of the wave energy is reflected at the end of the line.

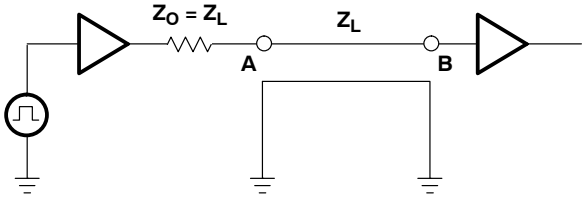


Figure 1. Line-Impedance Matching

Figure 2 illustrates the signal waveforms for a high-to-low transition for a line driver without and with output-damping resistors under these conditions. T is the line signal-transmission time, i.e., the time it takes for the signal wave to travel from point A to point B, or vice versa. The high-level signal prior to the output transition of the line driver has a level of about 3.3 V, typical for 5-V TTL-level devices, such as ABT or FCT-T, as well as for all 3.3-V logic devices. The line impedance is assumed to be 33 Ω.

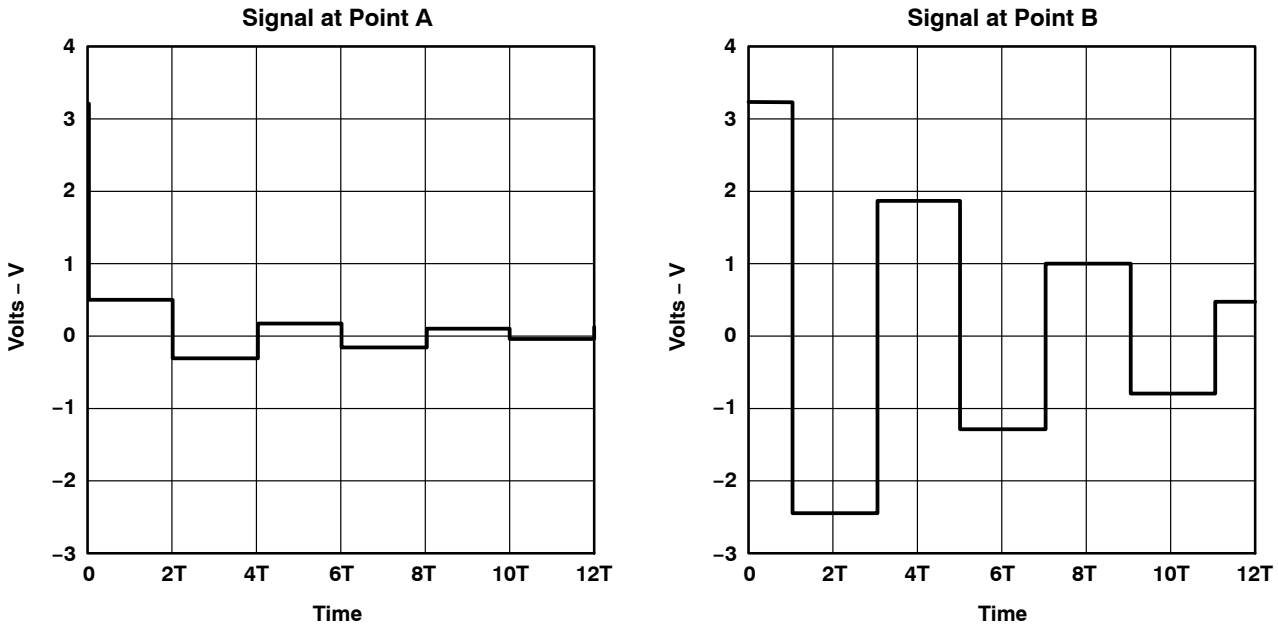
Without the damping resistor (see Figure 2a), a driver output impedance of 5 Ω is assumed. The incident wave at point A and t = 0 establishes a signal level of:

$$V_A = 3.3\ V \times \left(1 - \frac{33\ \Omega}{5\ \Omega + 33\ \Omega}\right) = 0.43\ V \quad (1)$$

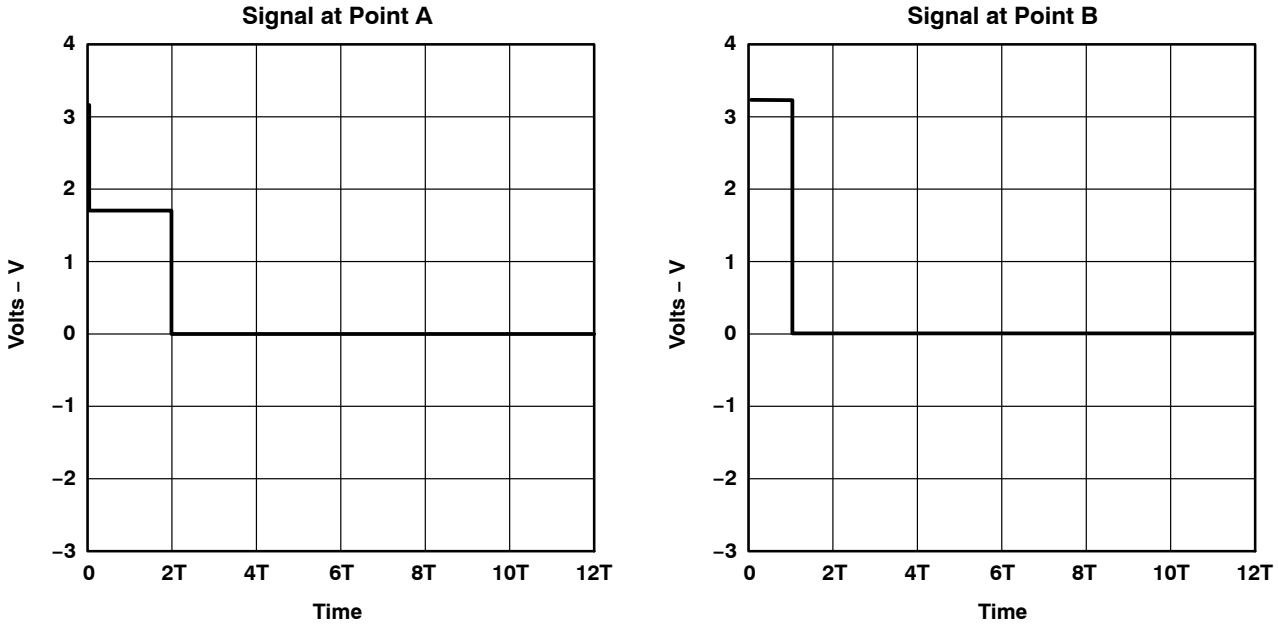
Due to the reflection at the line end, the receiver (point B) sees the initial line level dropping to

$$V_B = 3.3\ V - 2 \times (3.3\ V - 0.43\ V) = -2.44\ V \quad (2)$$

which represents a considerable undershoot. With a damping resistor, the effective output impedance is assumed to be 33 Ω, thus matching the line impedance. In this case, while there is a step in the signal at the driver output (point A), the receiver side (point B) sees a very clean signal transition without any significant undershoot or overshoot. Signal waveforms are analogous to this for a low-to-high transition, in which case the line without damping resistors shows significant signal overshoot.



a) SIGNAL WAVEFORMS WITHOUT DAMPING RESISTOR (Z_O = 5 Ω)

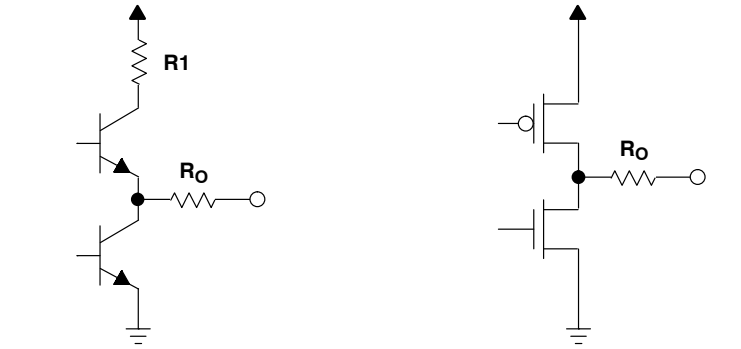


b) SIGNAL WAVEFORMS WITH DAMPING RESISTOR (Z_O = Z_L = 33 Ω)

Figure 2. Signal Waveforms Showing Effect of Damping Resistors

The damping-resistor solution is particularly important when designing memory arrays because excessive undershoots and overshoots can cause data loss in memory devices. Although line-impedance matching is optimized for point-to-point transmission where it helps establish near-perfect signal waveforms, it also works fine in most memory-array configurations where there is one driver and many receiving modules. Some of the modules may see a step in the signal waveform (see Figure 2b), but this is only for a short period of time (typically less than 1 ns) and does not affect data transmission. The goal to prevent excessive undershoots and overshoots is still fully accomplished.

Texas Instruments (TI), Philips, and a number of other manufacturers implement output-damping-resistor options in several logic families. The device nomenclature used by all these vendors is a “2” added in front of the device number, that is, the damping-resistor version of the popular ’244 octal buffer is referred to as a ’2244. Having been the first to introduce a ’2244 function with the SN74ALS2244 in the mid-1980s, TI quickly expanded its spectrum of devices with output-damping resistors. Today, it covers the ALS, F, BCT, ABT, LVT, LVC, and ALVC product lines as well as other specialized bus-interface devices.



a) BIPOLAR OR BiCMOS OUTPUT WITH DAMPING RESISTOR (e.g., ABT2xxx, LVT2xxx)

b) CMOS OUTPUT WITH DAMPING RESISTOR (e.g., LVC2xxx, ALVC162xxx)

Figure 3. Damping-Resistor Implementation

Figure 3 shows simplified output diagrams that illustrate how damping-resistor outputs are implemented in the ABT/LVT and LVC/ALVC families, respectively.[2,3] The value of the output-damping resistor (R_O) typically is about 25 Ω. The resistor value in the upper output stage of the bipolar/BiCMOS output, R1, is only a few ohms. Together with the impedance of the output stage itself, this leads to an effective total output impedance of about 33 Ω for all of these circuits. Because line impedance in memory systems is usually around 20 Ω to 50 Ω and some level of impedance mismatch is acceptable, this output impedance value covers almost all practical uses. A good rule of thumb is that a mismatch up to a factor of two has little effect on signal characteristics. Figures 4 and 5 show the signal condition for an output-damping-resistor device with a 33-Ω output impedance and line impedance of 20 Ω and 50 Ω, respectively. Signal distortion is still acceptable in both cases.

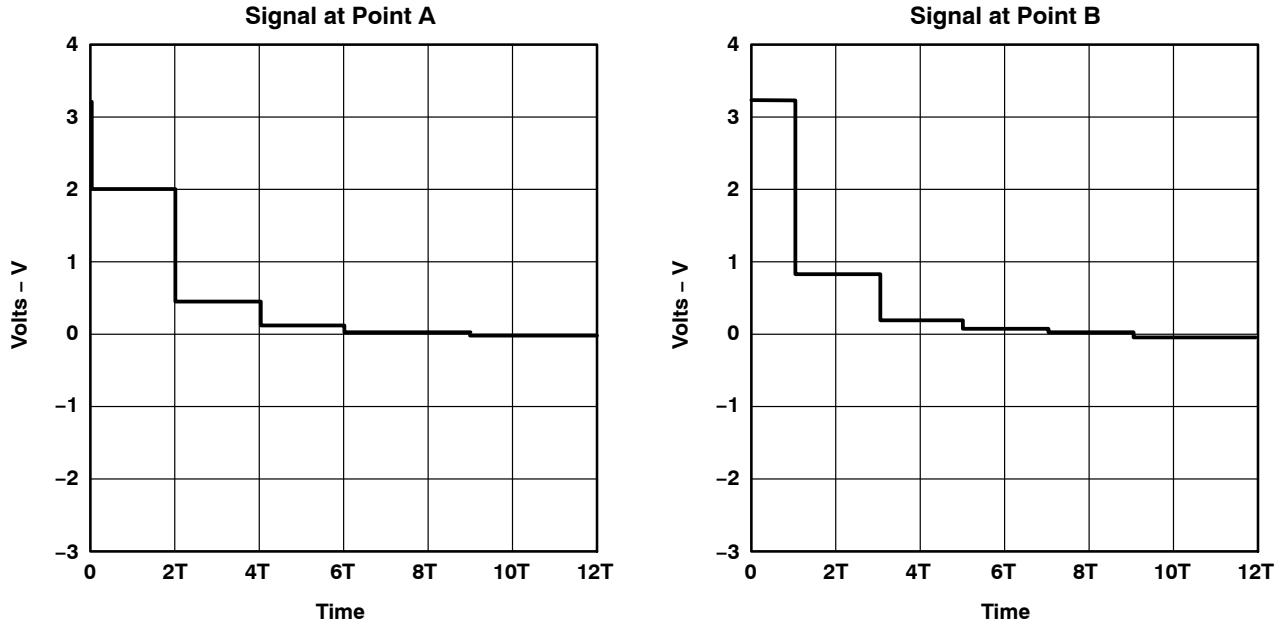


Figure 4. Signal Waveforms With Impedance Mismatch (Z_O = 33 Ω, Z_L = 20 Ω)

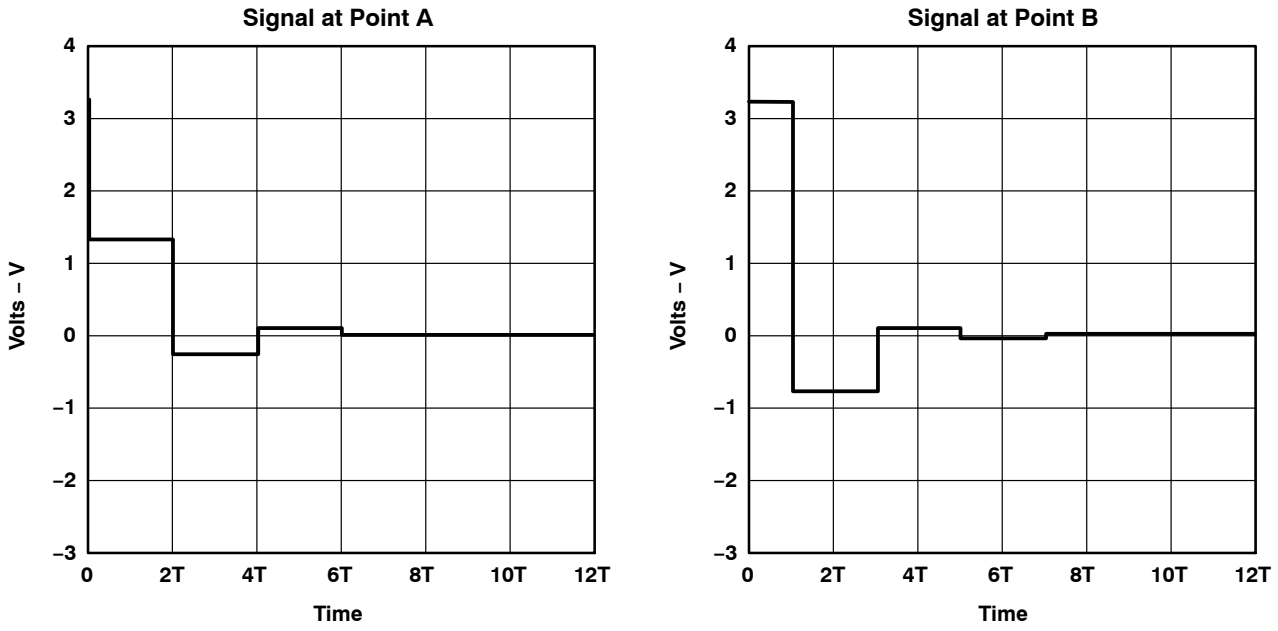


Figure 5. Signal Waveforms With Impedance Mismatch (Z_O = 33 Ω, Z_L = 50 Ω)

The output-stage dimensioning of devices with damping resistors usually remains unchanged. The introduction of the damping resistor reduces the nominal output drive currents, but still leaves a drive capability sufficient for most applications. Table 1 shows low- and high-level output drive specifications for the families previously mentioned. Note that I_{OH} and I_{OL} are balanced on all ’2xxx devices.

Table 1. Low- and High-Level Output Drive Specifications for Selected TI Logic Devices

TECHNOLOGY	OUTPUT CURRENT (mA)	
	I_{OH}	I_{OL}
ABTxxx/LVTxxx	–32	64
ABT2xxx/LVT2xxx	–12	12
LVCxxx/ALVC16xxx†	–24	24
LVC2xxx/ALVC162xxx†	–12	12

† ALVC devices are available in Widebus™ versions (16xxx/162xxx) only. All other technologies listed are available in octal and Widebus versions.

Reduced-Drive Outputs

Some vendors refer to balanced- and light-drive outputs. The idea behind these is based on a concept that is different from the damping resistor. While the basic device characteristics remain unchanged and no line termination is added, a balanced- or light-drive device shows significantly reduced output drive currents when compared with its standard high-drive equivalent. In essence, this supports the finding that lower drive currents result in a reduction in undershoot and overshoot.

Figure 6 shows implementations of this approach for FCT16xxx devices.[4] The impedance values given include the impedance of the FETs. Some manufacturers achieve reduced drive solely by reducing the dimensions of the output FETs, which, in turn, increases their impedance. In this case, no series resistors are added. This helps to reduce the amount of energy (that contributes to undershoots and overshoots), but does not necessarily establish true line-impedance matching because output impedance may remain too low (for example, see the lower output path in Figure 6b).

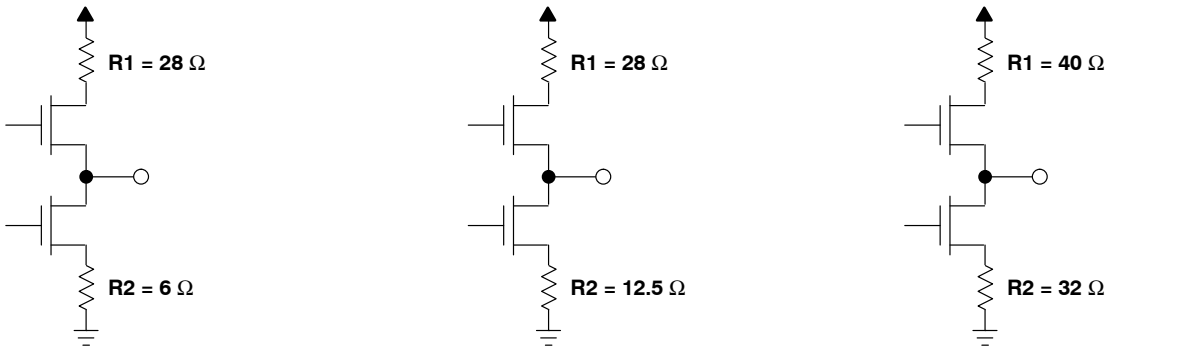


Figure 6. Implementation of Various Drive Concepts

Table 2 shows the resulting nominal output drive specifications.

Table 2. Low- and High-Level Output Drive Specifications for FCT16xxx Logic Devices

DRIVE TYPE		OUTPUT CURRENT (mA)	
		I_{OH}	I_{OL}
FCT16xxx	High drive	–32	64
FCT162xxx	Balanced drive	–24	24
FCT166xxx	Light drive	–8	8

Based on a line with Z_L = 33 Ω (see Figure 7) showing a high-to-low signal transition, Figures 8 through 10 illustrate the effect on signal undershoot and overshoot. As illustrated in Figure 6, the output impedance of the driver, Z_O, is 6 Ω, 12.5 Ω, or 32 Ω, for high-, balanced-, and light-drive outputs, respectively.

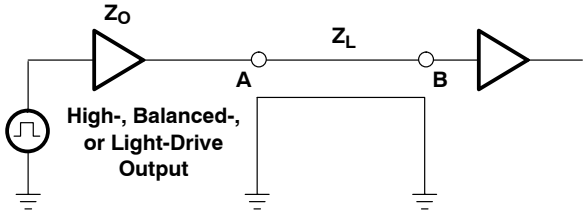


Figure 7. Line Driven By High-, Balanced-, or Light-Drive Device

As expected, the high-drive version (see Figure 8) exhibits signal characteristics very similar to those shown for a standard bus driver without an output-damping resistor (see Figure 2a).

Similarly, signal waveforms with the light-drive version (see Figure 10) resemble those of a bus driver with an output-damping resistor (see Figure 2b). The low nominal output drive of ±8 mA limits the applicability of these devices to systems where the output drives one or a few receivers only.

While not quite as severe as the high-drive version, the balanced-drive device (see Figure 9) still causes considerable undershoots because its low-level output impedance of 12.5 Ω is too low to match the line impedance. It becomes worse if line impedance is higher than 33 Ω. Figure 11 demonstrates this, assuming a line impedance of 50 Ω.

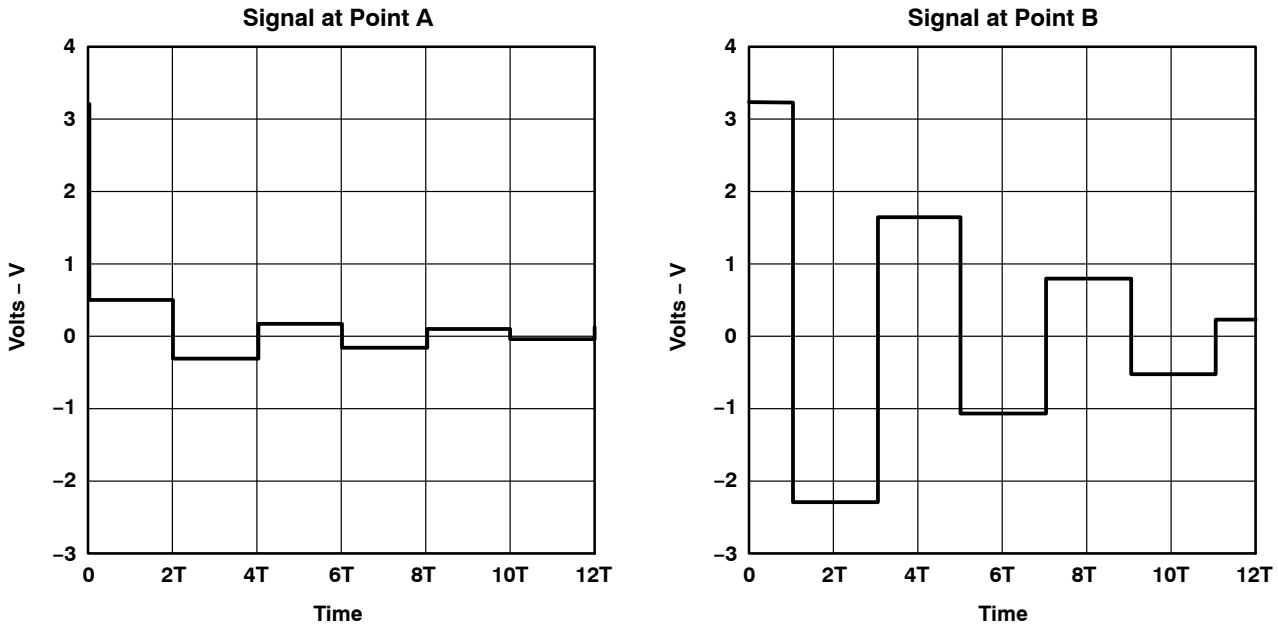


Figure 8. Signal Waveforms With High Drive (Z_O = 6 Ω, Z_L = 33 Ω)

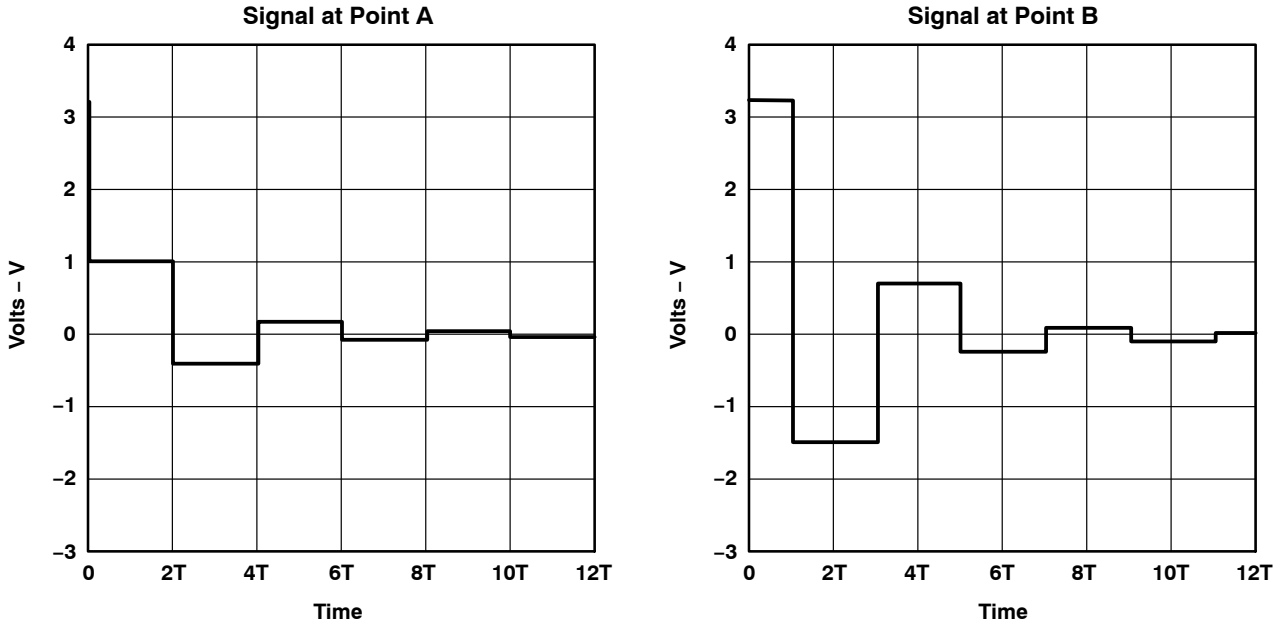


Figure 9. Signal Waveforms With Balanced Drive (Z_O = 12.5 Ω, Z_L = 33 Ω)

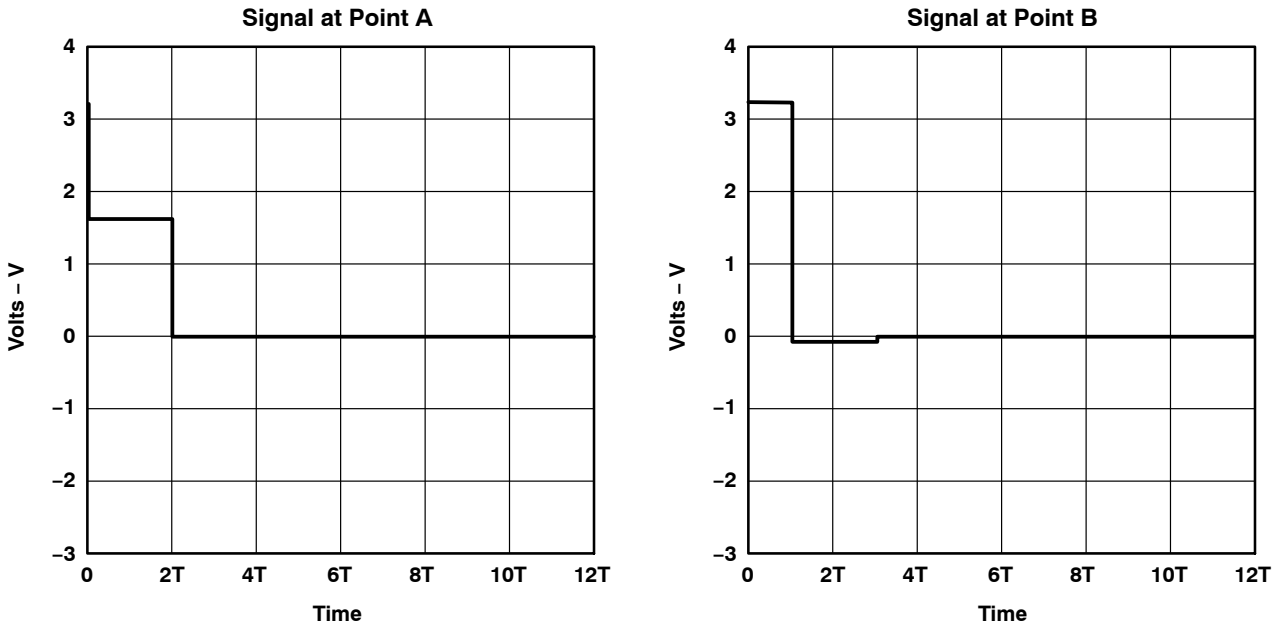


Figure 10. Signal Waveforms With Light Drive (Z_O = 32 Ω, Z_L = 33 Ω)

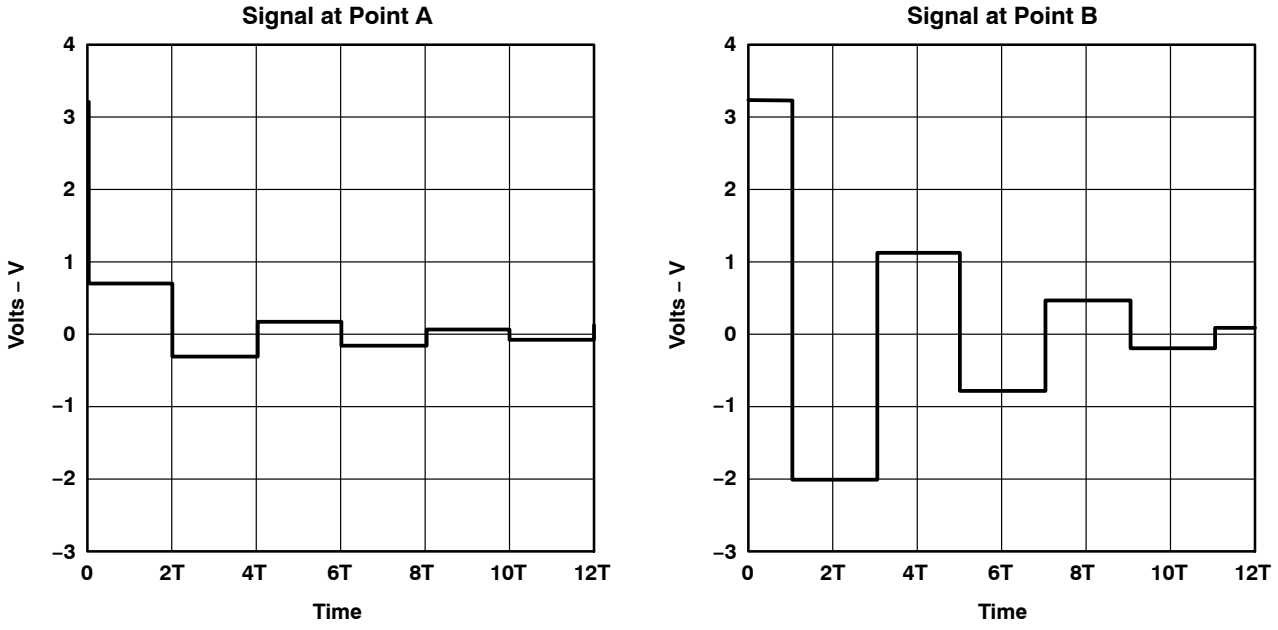


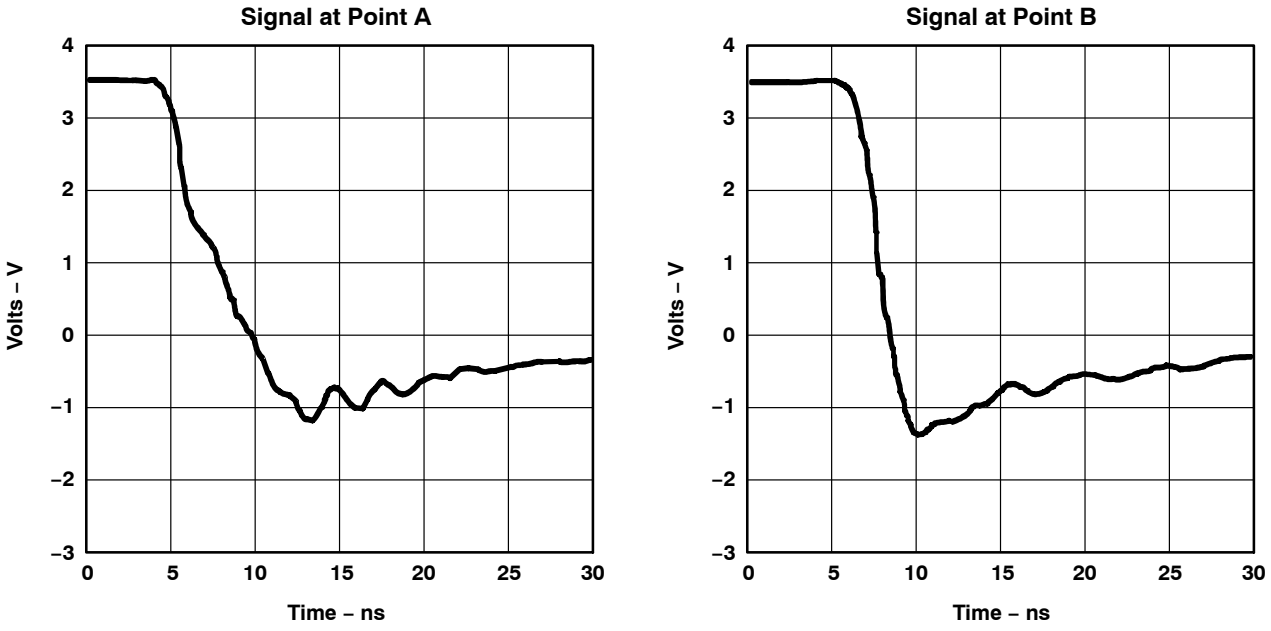
Figure 11. Signal Waveforms With Balanced Drive (Z_O = 12.5 Ω, Z_L = 50 Ω)

Practical Applicability of Wave Theory to Predict Signal Waveform Curves

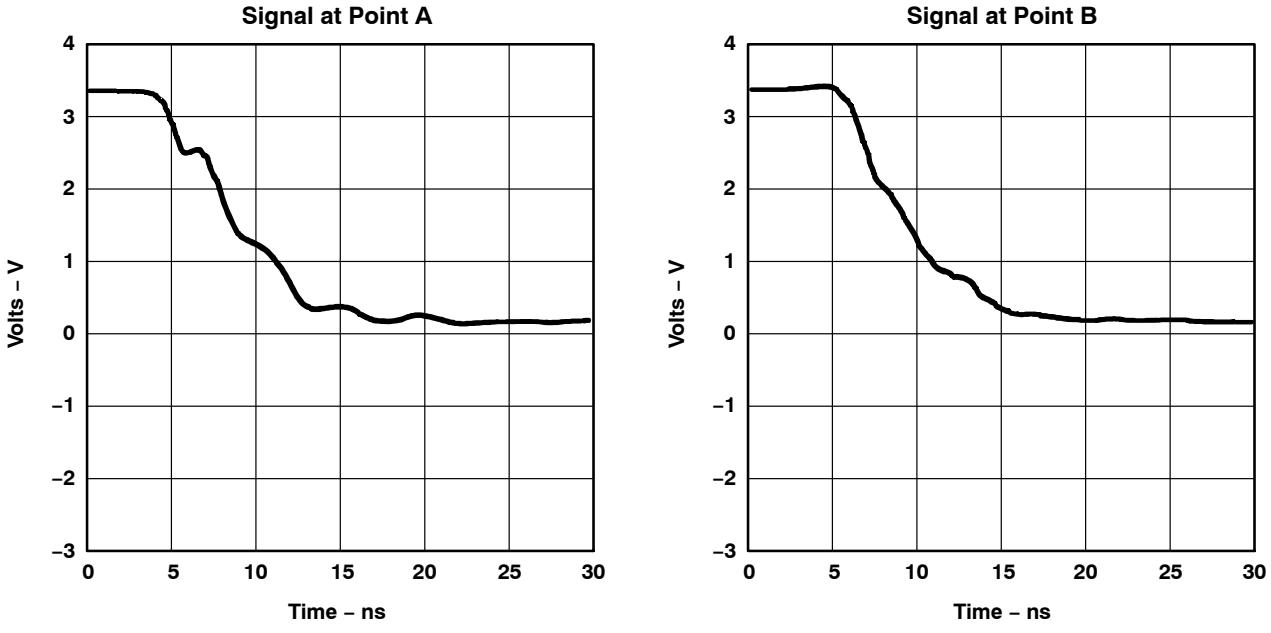
Obviously, all signal waveforms shown in Figures 2, 4, 5, and 8 through 11 are derived from wave theory. They assume a line without terminating impedance, which is an acceptable approximation when using today's CMOS receivers with their very high input impedances, but ignores the output loading effects by the capacitive loads that receiver inputs, connectors, traces, etc., represent. While these theoretical curves help in understanding the influence of output and line impedances, a necessary question is, therefore, whether the curves reflect real-world signal waveforms closely enough to be useful.

With heavily loaded outputs, typically with line impedances of 30 Ω or below, in practice, heavily distorted signal waveforms are found. Damping-resistor outputs do not improve this much. Other termination techniques may be more appropriate but lead to acceptable signal waveforms only of a line driver with very-high-output drive capability. The signal distortion often results in extended signal-propagation times because one or more reflections are needed before a well-defined signal level is established. Sometimes, slow signal slew rates prevent excessive signal bounces such that undershoots and overshoots do not reach critical levels. However, relying upon this to suppress undershoot and overshoots is not a good design practice. Figure 12 shows measured curves derived from SN74ABT244 and SN74ABT2244 devices, respectively, driving a SIMM memory module with 18 memory devices. As before, the driver output is referred to as point A and the receiver, in this case the memory device that is the farthest away from the driver, as point B. The curves illustrate quite well how the strong capacitive loading represented by the memories distorts the reflected waves. Signal undershoot on the receiver side is still overcritical in the standard device without a damping resistor, while the damping-resistor version ensures that no undershoot occurs.

Lightly loaded lines represent another problematic application for devices that do not have an output-damping resistor. Here, the aforementioned slew-rate reduction can be expected to improve things only marginally. Therefore, with line impedances of 50 Ω or more, that is, in applications where there are only a few receiving devices connected to the line, in practice, waveforms usually are very similar to theoretical ones. Large undershoots and overshoots occur if the line is left unterminated.



a) SN74ABT244 (WITHOUT DAMPING RESISTOR)



b) SN74ABT2244 (WITH DAMPING RESISTOR)

Figure 12. Signal Waveforms for SN74ABT244 and SN74ABT2244 Driving a SIMM Module

Overview of Technologies and Application Areas

As mentioned before, the spectrum of available bus-interface devices with damping resistors or reduced output drive currently offered by various logic vendors is very confusing. This is mainly because similar naming conventions are being used for different approaches. Tables 3 and 4 give an overview of advanced 5-V and 3.3-V logic families. Please note that the device series field ignores other vendor-specific parts of device names, such as device revisions or indicators for bus-hold device inputs.

Table 3. Advanced 5-V Buffers With Damping Resistor or Reduced-Drive Options

DEVICE SERIES	VENDOR	TYPE	I_{OH} (mA)	I_{OL} (mA)	COMMENTS
ABTxxx	TI, Philips, et al.	High drive	–32	64	
ABT16xxx	TI, Philips, et al.	High drive	–32	64	Same as octal version (ABTxxx)
ABT2xxx	TI, Philips, et al.	Damping resistor	–12	12	
ABT162xxx	TI, Philips, et al.	Damping resistor	–12	12	Same as octal version (ABT2xxx)
AC/ACTxxx	TI, Motorola, et al.	Balanced drive	–24	24	
AC/ACT16xxx	TI	Balanced drive	–24	24	Same as octal version (AC/ACTxxx)
AHC/AHCTxxx	TI, Philips, et al.	Light drive	–8	8	
FCTxxx	IDT, QSI, et al.	High drive	–15	64	
FCT16xxx	IDT, QSI, et al.	High drive	–32	64	I_{OH} differs from octal version (FCTxxx)
FCT2xxx	IDT, QSI, et al.	Balanced drive	–15	12	
FCT162xxx	IDT, QSI, et al.	Balanced drive	–24	24	I_{OH}, I_{OL} differ from octal version (FCT2xxx)
FCT162Qxxx	Pericom	Damping resistor	–12	12	No octal version
FCT166xxx	IDT	Light drive	–8	8	No octal version

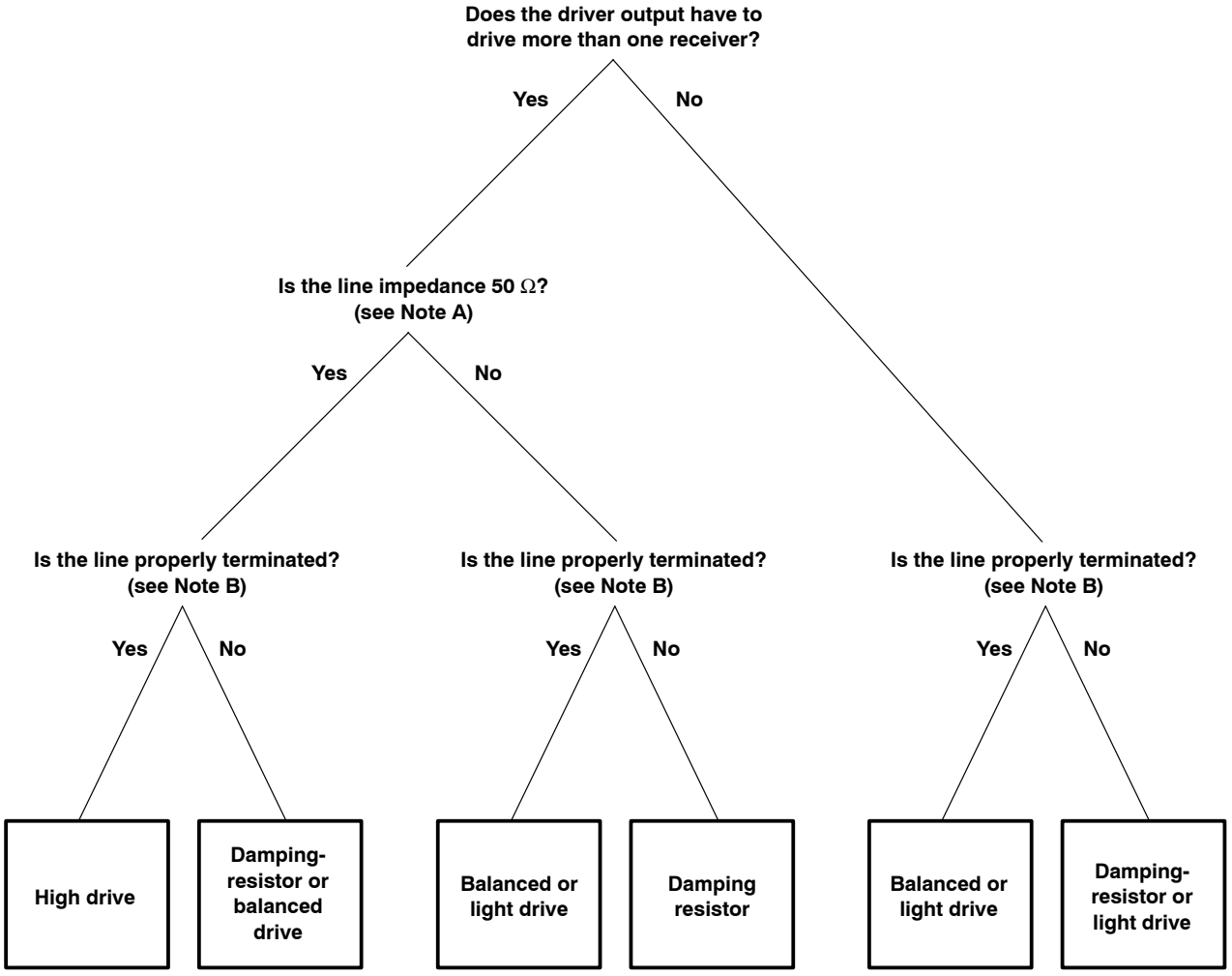
While FCT16xxx versions have the same output drive as ABT, FCT162xxx corresponds to technologies such as AC and ACT. FCT166xxx has the low output drive of families like HC/HCT or AHC/AHCT. Note that FCT characteristics are different for octals and 16-bit versions. This may lead to different signal waveforms in practical applications. All TI logic families have identical characteristics for octal and Widebus devices.

Table 4. Advanced 3.3-V Buffers With Damping Resistor or Reduced-Drive Options

DEVICE SERIES	VENDOR	TYPE	I_{OH} (mA)	I_{OL} (mA)	COMMENTS
LVTxxx	TI, Philips, et al.	High drive	–32	64	
LVT16xxx	TI, Philips, et al.	High drive	–32	64	Same as octal version (LVTxxx)
ALVT16xxx	TI, Philips, et al.	High drive	–32	64	No octal version
LVT2xxx	TI, Philips, et al.	Damping resistor	–12	12	
LVT162xxx	TI, Philips, et al.	Damping resistor	–12	12	Same as octal version (LVT2xxx)
ALVT162xxx	TI, Philips, et al.	Damping resistor	–12	12	No octal version
LVCxxx	TI, Philips, et al.	Balanced drive	–24	24	
LVC16xxx	TI, Philips, et al.	Balanced drive	–24	24	Same as octal version (LVCxxx)
LVC2xxx	TI	Damping resistor	–12	12	
LVC162xxx	TI	Damping resistor	–12	12	Same as octal version (LVC2xxx)
ALVC16xxx	TI, Philips, et al.	Balanced drive	–24	24	No octal version
ALVC162xxx	TI	Damping resistor	–12	12	No octal version
LVxxx	TI, Philips, et al.	Light drive	–8	8	
LCXxxx	Fairchild, et al.	Balanced drive	–24	24	No reduced-drive versions available
LCX16xxx	Fairchild, et al.	Balanced drive	–24	24	Same as octal version (LCXxxx)
FCT3xxx	IDT, QSI, et al.	Reduced, unbalanced drive	–8	24	No high-drive versions available
FCT163xxx	IDT, QSI, et al.	Reduced, unbalanced drive	–8	24	Same as octal version (FCT3xxx)

LVT and ALVT are the only high-drive 3.3-V logic families available in the market. For 3.3 V, only the LVT, ALVT, LVC, and ALVC product families offer true damping-resistor options. FCT3xxx and FCT163xxx devices have significantly lower drive capability than their 5-V equivalents. Also, their I_{OH}/I_{OL} drive currents are unbalanced, which limits their use in certain applications.

Application areas for damping-resistor and reduced-drive line buffers and transceivers cover many different types of end equipment. In addition to required device function, output loading (line impedance) and available termination are the decisive factors when choosing a device. The decision tree shown in Figure 13 provides a general guideline. However, specific requirements may represent further constraints.



NOTES: A. If exact line impedance is unknown, a good rule of thumb is that line impedance is lower than 50 Ω if more than four or five receiver inputs are connected to the line.

B. Examples of other line-termination methods are a split-resistor (Thevenin) network, an R-C combination, or clamping diodes. A more detailed discussion of advantages and disadvantages of these and other termination methods is found in reference 3.

Figure 13. Decision Tree for Selecting Driver Output Type

Transceivers With Output-Damping Resistors or Reduced-Drive Outputs

So far, this report has dealt with buffers and line drivers only, and has shown that several different output versions support a wide range of output load configurations.

The number of choices is even larger when looking at transceivers because any combination of output versions can be chosen independently for the A port and B port of the device. Not all possible combinations are being offered in the market, but the list of drive types is extensive.

1. High-drive outputs on both ports
2. High-drive outputs on one port and damping-resistor outputs on the other port
3. Balanced-drive outputs on one port and damping-resistor outputs on the other port
4. Balanced-drive outputs on both ports
5. Damping-resistor outputs on both ports
6. Light-drive outputs on both ports
7. Reduced-, unbalanced-drive outputs on both ports

The best combination for a particular application can be determined using the decision tree in Figure 13 independently for the A and B ports of the transceiver. In general, applications that require a transceiver between a backplane and a local board require types 1 or 2 (type 3 may work in some applications). Applications with more lightly loaded local buses on both sides require any one of types 2 through 5, while type 6 addresses point-to-point transmission requirements.

The spectrum of devices offered in the market is complex and difficult to comprehend. Tables 5 through 11 show the options available for each type.

Table 5. Advanced Transceivers With High-Drive Outputs on Both Ports (Type 1)

DEVICE	V_{CC}	VENDOR	COMMENTS
ABTxxx	5 V	TI, Philips, et al.	
ABT16xxx	5 V	TI, Philips, et al.	
FCTxxx	5 V	IDT, QSI, et al.	
FCT16xxx	5 V	IDT, QSI, et al.	I_{OH} differs from octal version (FCTxxx)
LVTxxx	3.3 V	TI, Philips, et al.	
LVT16xxx	3.3 V	TI, Philips, et al.	

Table 6. Advanced Transceivers With High-Drive Outputs on One Port and Damping-Resistor Outputs on the Other Port (Type 2)

DEVICE	V_{CC}	VENDOR
ABT2xxx	5 V	TI
ABT162xxx	5 V	TI
LVT2xxx	3.3 V	TI
LVT162xxx	3.3 V	TI
ALVT162xxx	3.3 V	TI

Table 7. Advanced Transceivers With Balanced-Drive Outputs on One Port and Damping-Resistor Outputs on the Other Port (Type 3)

DEVICE	V_{CC}	VENDOR
LVC2xxx	3.3 V	TI
LVC162xxx	3.3 V	TI
ALVC162xxx	3.3 V	TI

Table 8. Advanced Transceivers With Balanced-Drive Outputs on Both Ports (Type 4)

DEVICE	V_{CC}	VENDOR	COMMENTS
AC/ACTxxx	5 V	TI, Motorola, et al.	
AC/ACT16xxx	5 V	TI	
FCT2xxx	5 V	IDT, QSI, et al.	
FCT162xxx	5 V	IDT, QSI, et al.	I_{OH}, I_{OL} differ from octal version (FCT2xxx)
LVCxxx	3.3 V	TI, Philips, et al.	
LVC16xxx	3.3 V	TI, Philips, et al.	
ALVC16xxx	3.3 V	TI, Philips, et al.	
LCXxxx	3.3 V	Fairchild, et al.	
LCX16xxx	3.3 V	Fairchild, et al.	

Table 9. Advanced Transceivers With Damping-Resistor Outputs on Both Ports (Type 5)

DEVICE	V_{CC}	VENDOR	COMMENTS
ABTRxxx	5 V	TI	Same nomenclature, but different type from TI ABT162xxx
ABT162xxx	5 V	Philips	
FCT162Qxxx	5 V	Pericom	
LVCR2xxx	3.3 V	TI	
LVCR162xxx	3.3 V	TI	
ALVCR162xxx	3.3 V	TI	
ALVC162xxx	3.3 V	Philips	Same nomenclature, but different type from TI ALVC162xxx
LVT162xxx	3.3 V	Philips	Same nomenclature, but different type from TI LVT162xxx
ALVT162xxx	3.3 V	Philips	Same nomenclature, but different type from TI ALVT162xxx

Table 10. Advanced Transceivers With Light-Drive Outputs on Both Ports (Type 6)

DEVICE	V_{CC}	VENDOR
AHC/AHCTxxx	5 V	TI, Philips, et al.
FCT166xxx	5 V	IDT
LVxxx	3.3 V	TI, Philips, et al.

Table 11. Advanced Transceivers With Reduced-, Unbalanced-Drive Outputs on Both Ports (Type 7)

DEVICE	V_{CC}	VENDOR	COMMENTS
FCT3xxx	3.3 V	IDT, QSI, et al.	
FCT163xxx	3.3 V	IDT, QSI, et al.	I_{OH}, I_{OL} differ from octal version (FCT3xxx)

The majority of solutions offered are symmetrical, that is, they use the same output type on the A port and on the B port. While this may appear logical, it does not address the needs of most backplane-based applications where the backplane usually requires a high-drive output. TI was the first to introduce a transceiver with output-damping resistors, the SN74BCT2245, and since then has used the AAA2xxx or AAA162xxx concept (AAA = family indicator, xxx = device number) to indicate a device with standard (high or balanced) drive on one side and damping-resistor outputs on the other side. Others, including Philips, use the same nomenclature to indicate both output sides having damping resistors. TI uses AAAR2xxx or AAAR162xxx for this arrangement.

Conclusion

While buffers or transceivers with integrated output-damping resistors or reduced-drive outputs are required by many applications, the system designer needs to carefully choose a solution because vendors' denomination methods for these devices may be confusing. In particular, the difference between true damping resistors, i.e., integrated series resistors in the output path, and reduced-drive outputs, where the output drive is limited through changing the dimensioning and/or adding a resistor to the upper and lower transistor of the output stage, needs to be understood relative to different applications.

TI is the only vendor who offers 5-V and 3.3-V versions of all driver output types discussed in this report.

Acknowledgment

The author of this document is Lothar Katz.

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1 Curtis, Rick; Forstner, Peter; "Memory Driver Application Report", EB 205E, Texas Instruments (www.ti.com/sc/docs/asl/lit/eb205.htm).

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CMOS Power Consumption and C_{pd} Calculation

SCAA035B
June 1997

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Introduction

Reduction of power consumption makes a device more reliable. The need for devices that consume a minimum amount of power was a major driving force behind the development of CMOS technologies. As a result, CMOS devices are best known for low power consumption. However, for minimizing the power requirements of a board or a system, simply knowing that CMOS devices may use less power than equivalent devices from other technologies does not help much. It is important to know not only how to calculate power consumption, but also to understand how factors such as input voltage level, input rise time, power-dissipation capacitance, and output loading affect the power consumption of a device. This application report addresses the different types of power consumption in a CMOS logic circuit, focusing on calculation of power-dissipation capacitance (C_{pd}), and, finally, the determination of total power consumption in a CMOS device.

The main topics discussed are:

- Power-consumption components
- Static power consumption
- Dynamic power consumption
- Power-dissipation capacitance (C_{pd}) in CMOS circuits
- C_{pd} comparison among different families
- Power economy
- Conclusion

Power-Consumption Components

High frequencies impose a strict limit on power consumption in computer systems as a whole. Therefore, power consumption of each device on the board should be minimized. Power calculations determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculations also can determine the maximum reliable operating frequency.

Two components determine the power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

CMOS devices have very low static power consumption, which is the result of leakage current. This power consumption occurs when all inputs are held at some valid logic level and the circuit is not in charging states. But, when switching at a high frequency, dynamic power consumption can contribute significantly to overall power consumption. Charging and discharging a capacitive output load further increases this dynamic power consumption.

This application report addresses power consumption in CMOS logic families (5 V and 3.3 V) and describes the methods for evaluating both static and dynamic power consumption. Additional information is also presented to help explain the causes of power consumption, and present possible solutions to minimize power consumption in a CMOS system.

Static Power Consumption

Typically, all low-voltage devices have a CMOS inverter in the input and output stage. Therefore, for a clear understanding of static power consumption, refer to the CMOS inverter modes shown in Figure 1.

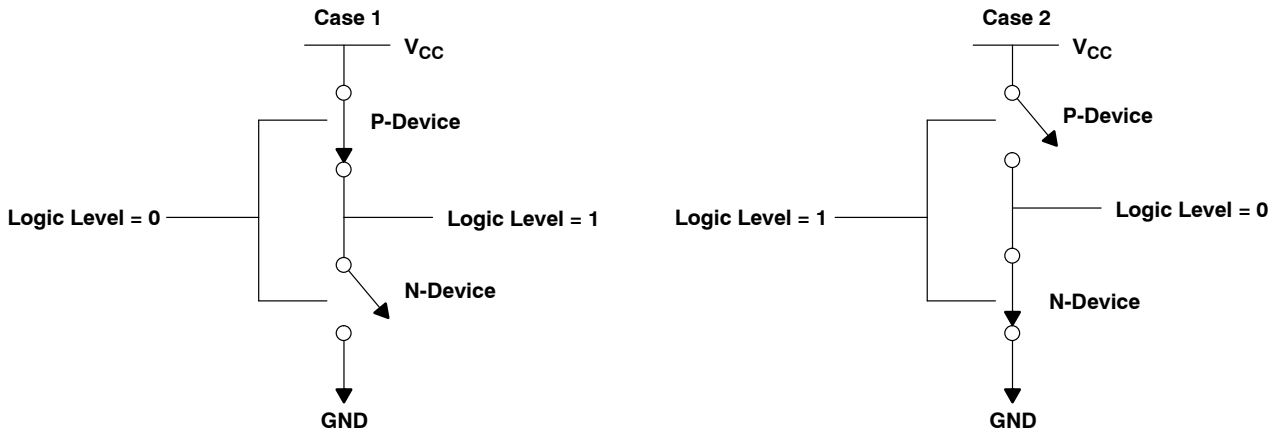


Figure 1. CMOS Inverter Mode for Static Power Consumption

As shown in Figure 1, if the input is at logic 0, the n-MOS device is OFF, and the p-MOS device is ON (Case 1). The output voltage is V_{CC}, or logic 1. Similarly, when the input is at logic 1, the associated n-MOS device is biased ON and the p-MOS device is OFF. The output voltage is GND, or logic 0. Note that one of the transistors is always OFF when the gate is in either of these logic states. Since no current flows into the gate terminal, and there is no dc current path from V_{CC} to GND, the resultant quiescent (steady-state) current is zero, hence, static power consumption (P_q) is zero.

However, there is a small amount of static power consumption due to reverse-bias leakage between diffused regions and the substrate. This leakage inside a device can be explained with a simple model that describes the parasitic diodes of a CMOS inverter, as shown in Figure 2.

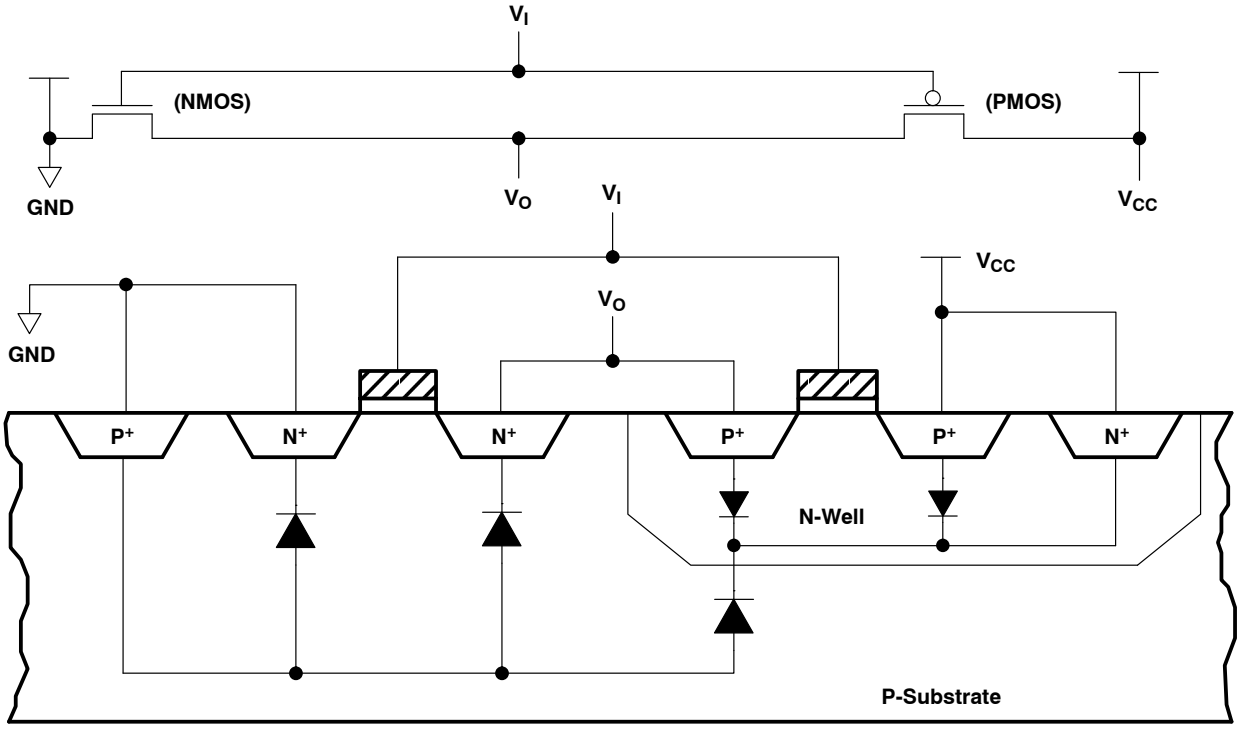


Figure 2. Model Describing Parasitic Diodes Present in CMOS Inverter

The source drain diffusion and N-well diffusion form parasitic diodes. In Figure 2, the parasitic diodes are shown between the N-well and substrate. Because parasitic diodes are reverse biased, only their leakage currents contribute to static power consumption. The leakage current (I_{lkg})of the diode is described by the following equation:

$$I_{lkg} = i_s\left(e^{qV/kT} - 1\right) \quad \textbf{(1)}$$

Where:

i_s = reverse saturation current
V = diode voltage
k = Boltzmann's constant (1.38×10^{-23} J/K)
q = electronic charge (1.602×10^{-19} C)
T = temperature

Static power consumption is the product of the device leakage current and the supply voltage. Total static power consumption, P_S, can be obtained as shown in equation 2.

$$P_S = \Sigma\,(\text{leakage current}) \times (\text{supply voltage}) \quad \textbf{(2)}$$

Most CMOS data sheets specify an I_{CC} maximum in the 10-μA to 40-μA range, encompassing total leakage current and other circuit features that may require some static current not considered in the simple inverter model.

The leakage current I_{CC} (current into a device), along with the supply voltage, causes static power consumption in the CMOS devices. This static power consumption is defined as quiescent, or P_S, and can be calculated by equation 3.

$$P_S = V_{CC} \times I_{CC} \quad \textbf{(3)}$$

Where:

V_{CC} = supply voltage
I_{CC} = current into a device (sum of leakage currents as in equation 2)

Another source of static current is ΔI_{CC}. This results when the input levels are not driven all the way to the rail, causing the input transistors to not switch off completely.

Dynamic Power Consumption

The dynamic power consumption of a CMOS IC is calculated by adding the transient power consumption (P_T), and capacitive-load power consumption (P_L).

Transient Power Consumption

Transient power consumption is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This is a result of the current required to charge the internal nodes (*switching current*) plus the *through current* (current that flows from V_{CC} to GND when the p-channel transistor and n-channel transistor turn on briefly at the same time during the logic transition). The frequency at which the device is switching, plus the rise and fall times of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible compared to the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the IC and the charge and discharge current of the load capacitance.

Transient power consumption can be calculated using equation 4.

$$P_T = C_{pd} \times V_{CC}^2 \times f_I \times N_{SW} \quad \textbf{(4)}$$

Where:

P_T = transient power consumption
V_{CC} = supply voltage
f_I = input signal frequency
N_{SW} = number of bits switching
C_{pd} = dynamic power-dissipation capacitance

In the case of single-bit switching, N_{SW} in equation 4 is 1.

Dynamic supply current is dominant in CMOS circuits because most of the power is consumed in moving charges in the parasitic capacitor in the CMOS gates. As a result, the simplified model of a CMOS circuit consisting of several gates can be viewed as one large capacitor that is charged and discharged between the power-supply rails. Therefore, the power−dissipation capacitance (C_{pd}) is often specified as a measure of this equivalent capacitance and is used to approximate the dynamic power consumption. C_{pd} is defined as the internal equivalent capacitance of a device calculated by measuring operating current without load capacitance. Depending on the output switching capability, C_{pd} can be measured with no output switching (output disabled) or with any of the outputs switching (output enabled). C_{pd} is discussed in greater detail in the next section.

Capacitive-Load Power Consumption

Additional power is consumed in charging external load capacitance and is dependent on switching frequency. The following equation can be used to calculate this power if all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times V_{CC}^2 \times f_O \times N_{SW} \text{ (C_L is the load per output)} \quad \textbf{(5)}$$

Where:

P_L = capacitive-load power consumption
V_{CC} = supply voltage
f_O = output signal frequency
C_L = external (load) capacitance
N_{SW} = total number of outputs switching

In the case of different loads and different output frequencies at all outputs, equation 6 is used to calculate capacitive-load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times V_{CC}^2 \quad \textbf{(6)}$$

Where:

Σ = sum of n different frequencies and loads at n different outputs
f_{On} = all different output frequencies at each output, numbered 1 through n (Hz)
V_{CC} = supply voltage (V)
C_{Ln} = all different load capacitances at each output, numbered 1 through n.

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions and can be expressed as shown in equation 7, equation 8 (single-bit switching), and equation 9 (multiple-bit switching with variable load and variable output frequencies).

$$P_D = P_T + P_L \quad \textbf{(7)}$$

$$P_D = \left(C_{pd} \times f_I \times V_{CC}^2\right) + \left(C_L \times f_O \times V_{CC}^2\right) \quad \textbf{(8)}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma(C_{Ln} \times f_{On})\right] \times V_{CC}^2 \quad \textbf{(9)}$$

Where:

C_{pd} = power-consumption capacitance (F)
f_I = input frequency (Hz)
f_{On} = all different output frequencies at each output, numbered 1 through n (Hz)
N_{SW} = total number of outputs switching
V_{CC} = supply voltage (V)
C_{Ln} = all different load capacitances at each output, numbered 1 through n.

Total power consumption is the sum of static and dynamic power consumption.

$$P_{tot} = P_{(static)} + P_{(dynamic)} \quad \textbf{(10)}$$

Power-Dissipation Capacitance (C_{pd}) in CMOS Circuits

C_{pd} is an important parameter in determining dynamic power consumption in CMOS circuits. It includes both internal parasitic capacitance (e.g., gate-to-source and gate-to-drain capacitance) and *through currents* present while a device is switching and both n-channel and p-channel transistors are momentarily conducting.

Testing Considerations

Proper setup is vital to achieving proper correlation. Some of the more important issues in performing the measurement are discussed in this section.

Input Edge Rates

When measuring C_{pd}, the input edge rate should be $t_r = t_f = 1$ ns from 10% to 90% of the input signal. Power-dissipation capacitance is heavily dependent on the dynamic supply current, which, in turn, is sensitive to input edge rates. As previously noted, while an input is switching, there is a brief period when both p-channel and n-channel transistors are conducting, which allows *through current* to flow from V_{CC} to GND through the input stage. The amount of dynamic *through current* measured is directly proportional to the amount of time the input signal is at some level other than V_{CC} or GND.

Bypassing

Any circuit must be properly bypassed to function correctly at high frequencies. The bypass capacitor between V_{CC} and GND serves to reduce power-supply ripple and provides a more accurate measure of the current being drawn by the device under test. Improper bypassing can result in erratic voltage at the V_{CC} pin and can disrupt the test. Texas Instruments (TI) uses a 0.1-µF bypass capacitor (from V_{CC} to GND) on the test board.

Pin Combination

Different pin combinations are valid and may be chosen to best suit the application at hand. For example, it is valid to test a device with the outputs either enabled or disabled. For multisection devices, set the device so that the minimum number of sections is active. Virtually any pin combination that causes at least one output to switch at a known frequency is acceptable.

Test Conditions

The test conditions for C_{pd} calculation for any device requires the following information (an LVC device is used as an example):

V_{CC}	5 V
Ambient temperature, T_A	25°C
AC bias levels	0 V, 3.3 V
DC bias level	0 V, 3.3 V
Input edge rates	$t_r = t_f$ = 1 ns (smallest possible)
Input frequencies	0.1, 1, 2, 3, ...20, 25, 30, ...75 MHz
C_{pd} frequency	10 MHz
Duty cycle	50%

Similarly, the test conditions for I_{CC} versus frequency are also applicable to determine the C_{pd} for CMOS devices. An AHC00 device is considered as an example for test conditions to calculate C_{pd} through I_{CC} versus frequency data and using the C_{pd} equation described in the next section (*Calculating C_{pd}*).

V_{CC}	5 V
Ambient temperature, T_A	25°C
AC bias levels	0 V, 5V
DC bias level	5 V
Input edge rates	$t_r = t_f$ = 2 ns (smallest possible)
Input frequencies	0.1, 1, 2, 3, ...20, 25, 30, ...75 MHz
Duty cycle	50%

For nontransceiver devices with 3-state outputs, testing is performed with the outputs enabled and disabled. When disabled, pullup resistors are not required. For a transceiver with 3-state outputs, testing also is performed with outputs enabled and disabled. However, in the disabled mode, 10-kΩ pullup resistors to the V_{CC} power supply or to GND must be added to all inputs and outputs.

Calculating C_{pd}

C_{pd} is calculated by putting the device in the proper state of operation and measuring the dynamic I_{CC} using a true RMS multimeter. Testing is done at an input frequency of 1 MHz to reduce the contribution of the dc supply current to the point that it can be ignored. Measurements for all devices are made at V_{CC} = 5 V or 3.3 V, T_A = 25°C. The test frequency must be low enough to allow the outputs to switch from rail to rail. For this reason, devices with 3-state outputs are measured at 10 MHz.

C_{pd} Measurement Procedures

For devices that have several gates in the same package (for example, AHC04 has six individual inverter circuits as shown in Figure 3), the average C_{pd} per output is specified in the data sheet as a typical (TYP) value.

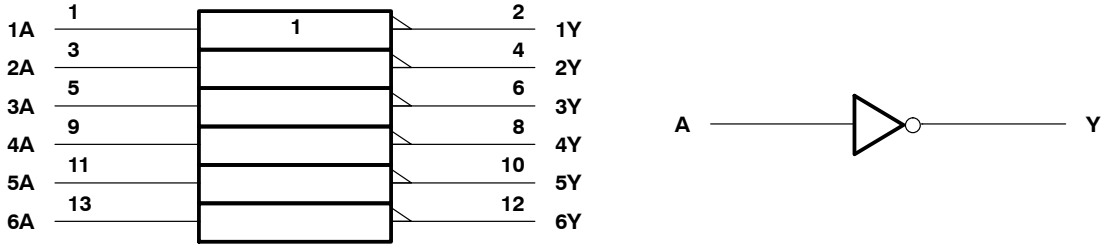


Figure 3. Hex Inverter AHC04

For devices that have several circuits switching simultaneously from a single clock or input (such as the AHC374 in Figure 4), switch all outputs and deduct P_L for each output. In the case of multiple-output switching at different frequencies (i.e., divide counters with parallel outputs) each P_L will have a different frequency factor.

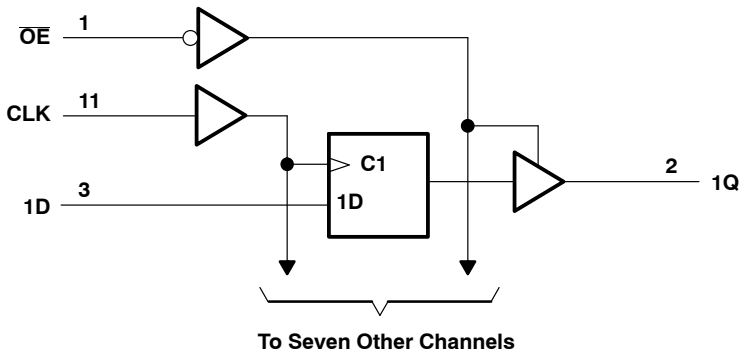


Figure 4. Several Circuits Switching, AHC374

In the case of devices such as ALVC, LVC, and LV, test and calculate C_{pd} for both the enable and disable mode. Typically, C_{pd} in the enable mode is greater than C_{pd} in the disable mode ($C_{pd\_EN} > C_{pd\_DIS}$).

Determination of C_{pd} (Laboratory Testing)

In the laboratory, determine C_{pd} for any device, such as AHC00, by measuring the I_{CC} being supplied to the device under the conditions in the *Test Conditions* section. Figure 5 provides the I_{CC} and frequency data for the AHC00 that can be used to calculate C_{pd} for the device, using equation 6 with a no-load condition.

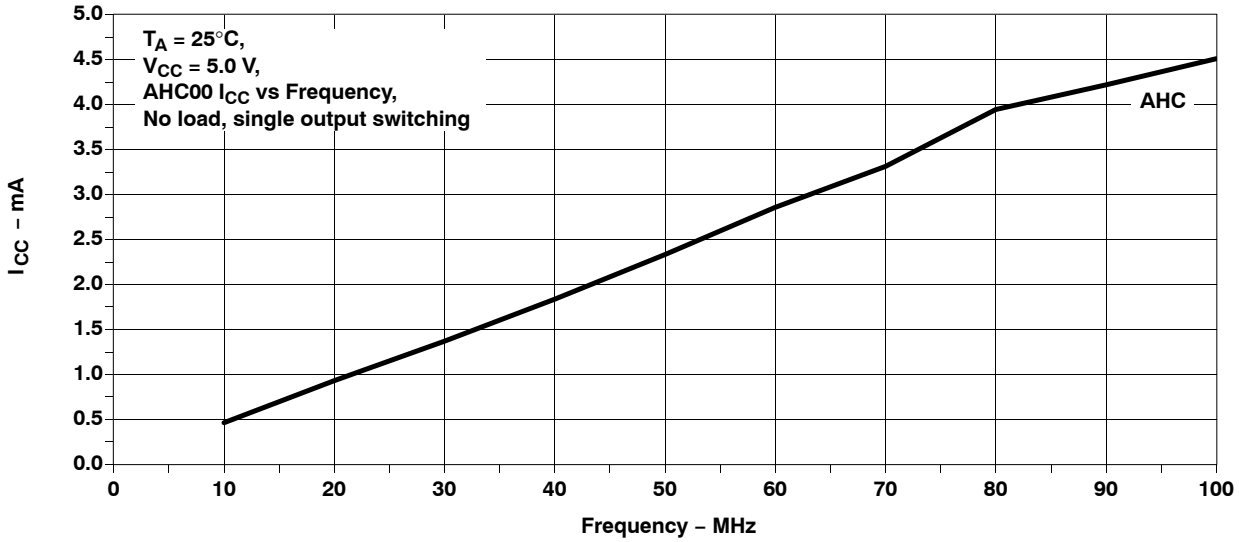


Figure 5. I_{CC} vs Frequency for AHC00

Note that the total capacitance for the switching output must be measured under open-socket conditions for accurate calculations. Considering these conditions, the data sheet C_{pd} is calculated using equation 11. Due to the automatic test-equipment constraints, C_{pd} is not assigned a maximum value in the data sheet.

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \quad \textbf{(11)}$$

Where:

f_I = input frequency (Hz)
V_{CC} = supply voltage (V)
$C_{L(eff)}$ = effective load capacitance on the board (F)
I_{CC} = measured value of current into the device (A)

The effective load capacitance is calculated according to equation 12 (assuming C_L is equal in all outputs).

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_O}{f_I} \quad \textbf{(12)}$$

Where:

f_O/f_I = ratio of output and input frequency (Hz)
N_{SW} = number of bits switching
C_L = load capacitance (F)

To explain the C_{pd} and the method of calculating dynamic power, see Table 1, which gives the C_{pd} test conditions for AHC devices. The symbols used in Table 1 for C_{pd} of AHC devices are:

V = V_{CC} (5 V)
G = ground (GND) (0 V)
1 = high logic level = V_{CC} (5 V)
0 = low logic level = ground (0 V)
X = irrelevant: 1 or 0, but not switching
C = 50% duty cycle input pulse (1 MHz), (see Figure 6)
D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 6)
S = standard ac output load (50 pF to GND)

The table shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations 8 and 9.

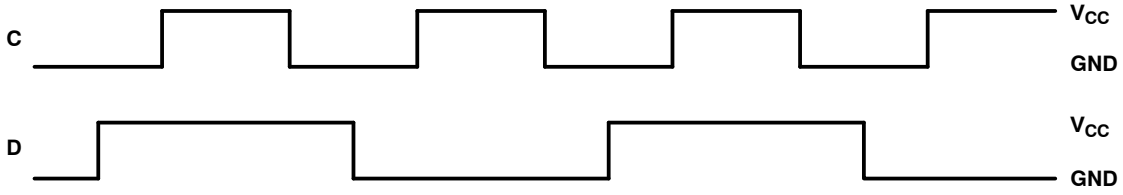


Figure 6. Input Waveform

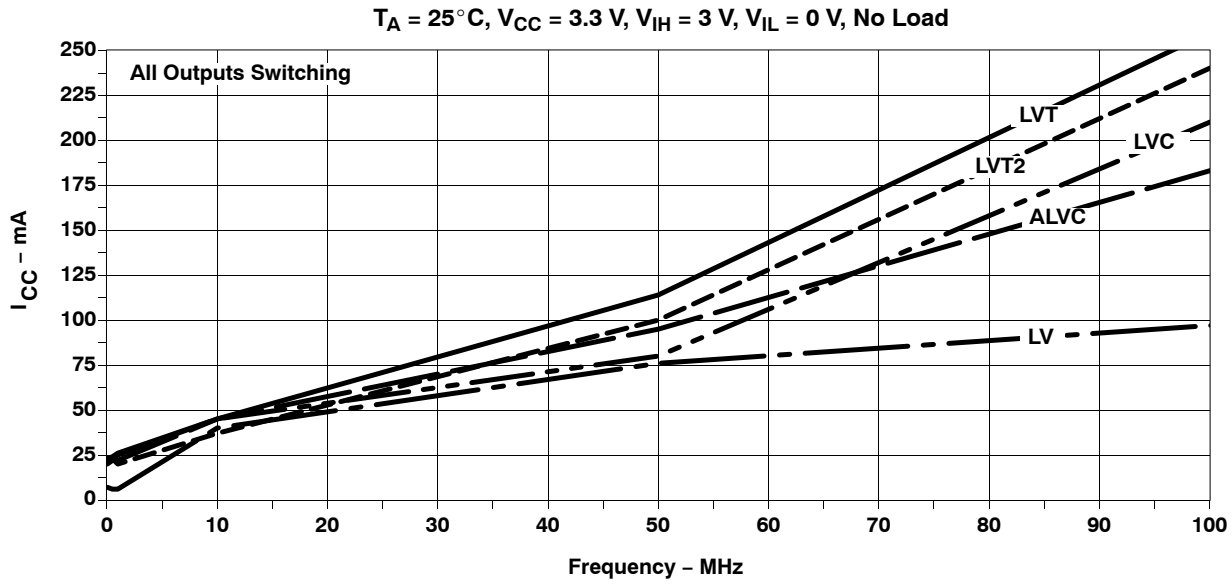
Table 1. C_{pd} Test Conditions With One- or Multiple-Bit Switching

TYPE	PIN																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V						
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V				
AHC139	0	C	0	S	S	S	S	G	S	S	S	S	X	X	X	V				
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC374‡	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switchings, but with no active clock signal
‡ All bits switching

Comparison of Supply Current Versus Frequency

C_{pd} and dynamic power consumption can be measured through supply-current-versus-frequency plots. Supply current is critical because it indicates the amount of power consumed by the device. A small value for I_{CC} is desirable because reducing the amount of power consumed yields many benefits. Less power consumed means less heat is generated and the problems of dissipating the heat are reduced. The reliability of a system is also improved, because lower stress gradients are present on the device and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. Figures 7 and 8 illustrate I_{CC} versus frequency data for TI's '245 device in different families for both 5 V and 3.3 V.



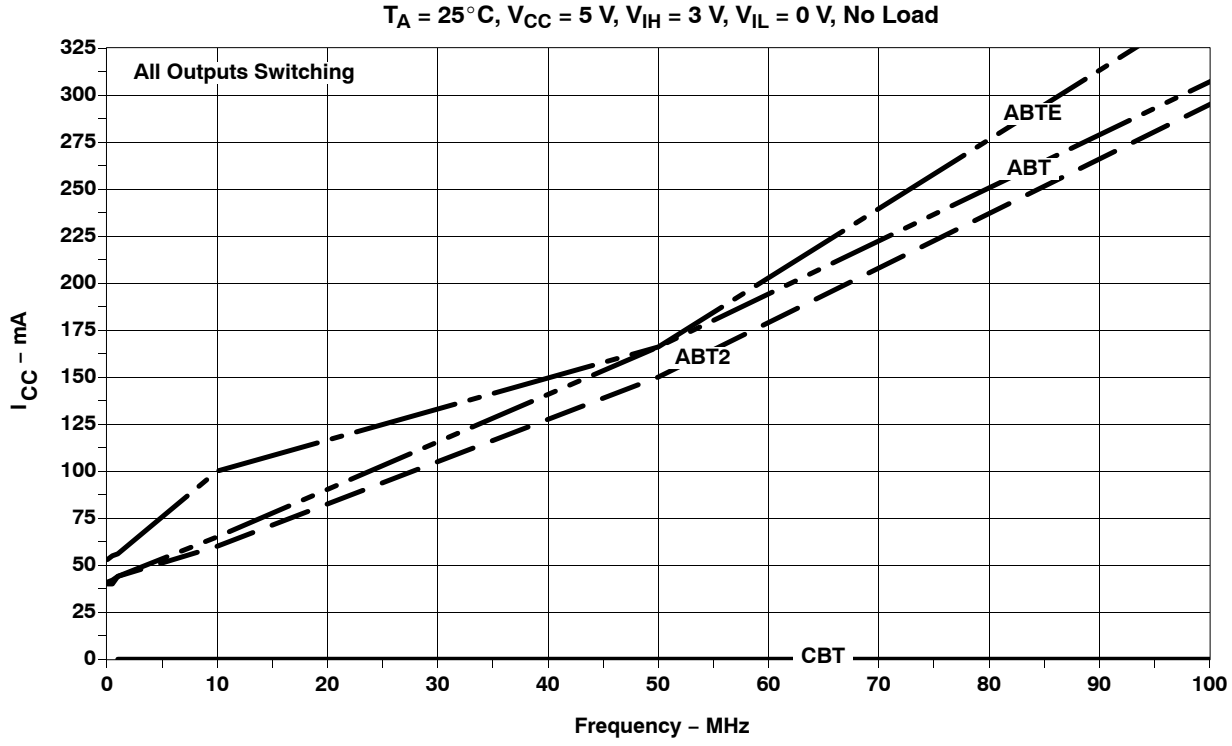


Figure 7. Power Consumption With All Outputs Switching

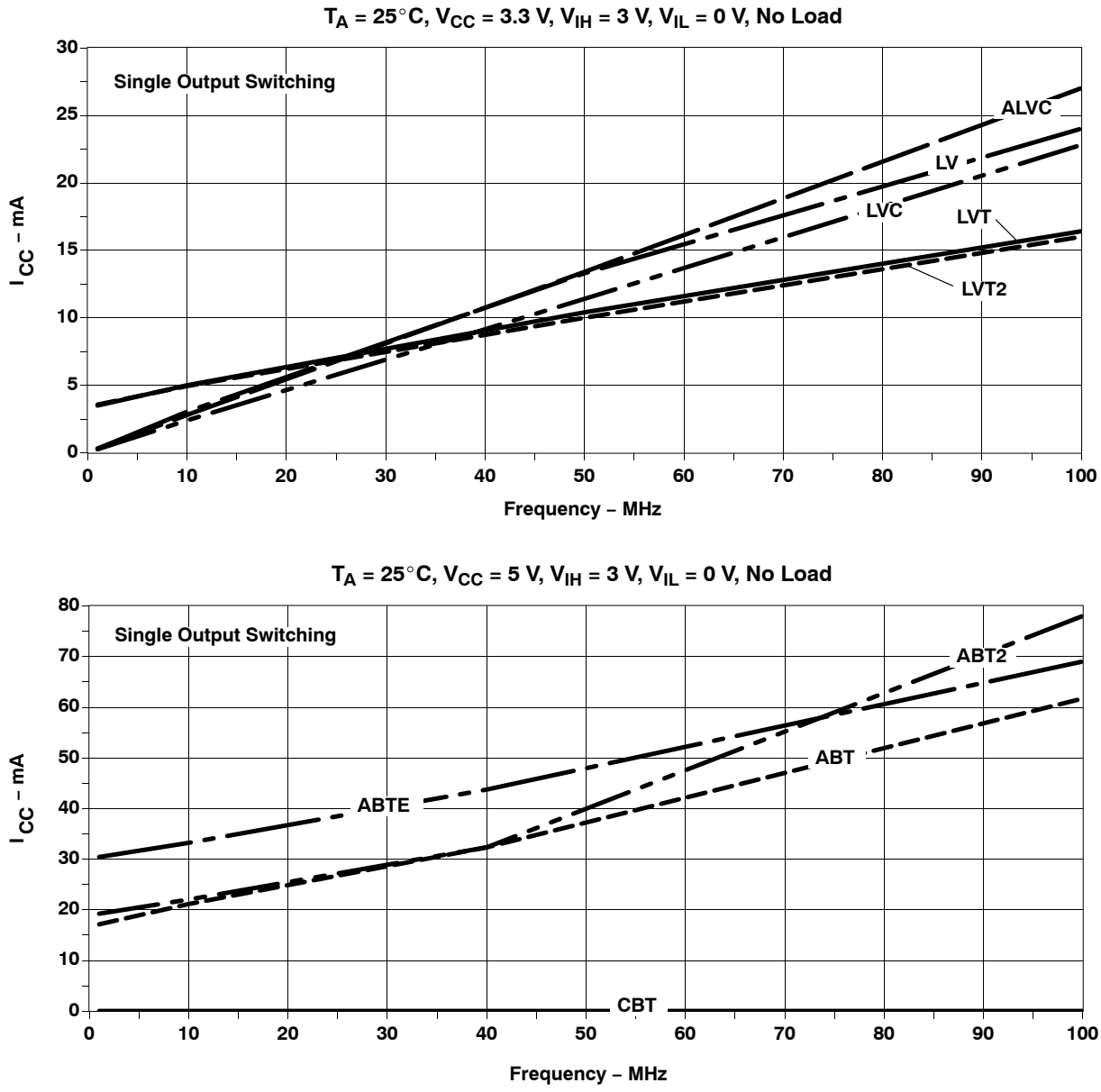


Figure 8. Power Consumption With a Single Output Switching

Power Economy

As noted previously, the industry trend has been to make devices more robust and faster while reducing their size and power consumption. This section describes the rationale and methods used to minimize power consumption in a CMOS circuit. For a CMOS system design, each module is allocated a fixed power budget. This is a power consumption that the module must not exceed. It is important to meet this power consumption allocation constraint, along with other constraints, to achieve a balanced design.

Power consumption minimization can be achieved in a number of ways. The dc power consumption can be reduced to leakage by using only CMOS logic gates, as opposed to bipolar and BiCMOS. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. One of the system design considerations is the choice of low-power devices, with systems today using devices in the 1.5-V to 3.3-V V_{CC} range. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and frequency at which the logic is clocked.

Consider TI's low-power CMOS devices, such as advanced low-voltage CMOS (ALVC) technology as an example. ALVC is the highest-performance 3.3-V bus-interface family. These specially designed 3-V products are processed in 0.6-µm CMOS technology, giving typical propagation delays of less than 3 ns, along with a current drive of 24 mA. This low supply voltage reduces both static and dynamic power consumption for the ALVC family. ALVC also has ultra-low standby power.

Conclusion

Power consumption is a function of load capacitance, frequency of operation, and supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

Acknowledgment

The author of this application report is Abul Sarwar.

Dynamic Output Control (DOC™) Circuitry Technology and Applications

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July 1999

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Abstract

Texas Instruments (TI™) next-generation logic is called the Advanced Very-low-voltage CMOS (AVC) family. The AVC family features TI's Dynamic Output Control (DOC™) circuit (patent pending). DOC circuitry automatically lowers the output impedance of the circuit at the beginning of a signal transition, providing enough current to achieve high signaling speeds, then subsequently raises the impedance to limit the overshoot and undershoot noise inherent in high-speed, high-current devices. This allows a single device to have characteristics similar to both series-damping-resistor outputs during static conditions and to high-current outputs during dynamic conditions, eliminating the need for series damping resistors. Due to the characteristics of the DOC output, the dc drive-current specifications for DOC devices are not useable as a relative indicator of the dynamic performance. A thorough understanding of static and dynamic drive-current conditions is required to design with the DOC feature of AVC logic.

Introduction

Performance

Trends in advanced digital electronics design continue to include lower power consumption, lower supply voltages, faster operating speeds, smaller timing budgets, and heavier loads. Many designs are making the transition from 3.3 V to 2.5 V, and bus speeds are increasing beyond 100 MHz. Trying to meet all of these goals makes the requirement of signal integrity harder to achieve. For designs that require very-low-voltage logic and bus-interface functions, TI announces the AVC family featuring TI's DOC circuit. The DOC circuit limits overshoot and undershoot noise inherent in high-speed, high-current devices, while still providing propagation delays of less than 2 ns, maximum, at 2.5 V.

Impedance Matching

The design engineer must carefully consider a logic component's output characteristics to ensure signal integrity and meet timing requirements. The output must have an impedance that minimizes overshoots and undershoots for signal integrity. The opposing characteristic that must be considered is having sufficient drive to meet the timing requirements. In the past, the selection of a component with integrated 26-Ω series damping resistors on the output ports or the use of external resistors was sometimes necessary. These resistors improve the impedance match of the driver output with the impedance of the transmission-line load and limit overshoot and undershoot noise. Damping resistors reduce the noise, but decrease slew rate and increase propagation delay due to the decreased drive current.

TI's DOC circuitry provides enough drive current to achieve fast slew rates and meet timing requirements, but quickly changes the output impedance level during the output transition to reduce the overshoot and undershoot noise that often is found in high-speed logic. This feature of AVC logic eliminates the need for series damping resistors in the output circuit, thereby improving the output slew rate and propagation-delay characteristics.

The dynamic drive current varies through the transition due to the dynamically changing output impedance. The static on-resistance (R_{ON}) of the output can be calculated from the V_{OH} vs I_{OH} and V_{OL} vs I_{OL} curves (see Figure 1 and Figure 2). At any specific point on the V_{OH} vs I_{OH} curves, $R_{ON} = (V_{OH} - V_{CC})/I_{OH}$. At any specific point on the V_{OL} vs I_{OL} curves, $R_{ON} = V_{OL}/I_{OL}$. The impedance during dynamic conditions is characterized by the slope of the V_O vs I_O line at any specific point on the graph.

The V_{OL} vs I_{OL} curves (see Figure 1) illustrate the impedance characteristics of the output in the low state. The curves represent the amount of sink current available (at a given V_{CC}) to drive the load, as the output voltage decreases from V_{CC} to 0 V when the output is sinking current (i.e., driving low). The V_{OL} vs I_{OL} curve for 2.5-V V_{CC} has two distinct regions of sink current availability. At the beginning of the transition from high to low, the portion of the output from 2.5-V to 1.5-V has a high amount of sink current available. In that region, the curve has characteristics that are similar to a circuit with an output resistance of approximately 20 Ω. Then, during the transition through 1.5 V, there is a steep drop in the drive current available. In the region from 1.5 V to ground, the curve has characteristics that are similar to a circuit with an output resistance of approximately 50 Ω. The V_{OL} vs I_{OL} curves for 1.8-V and 3.3-V V_{CC} have similar characteristics.

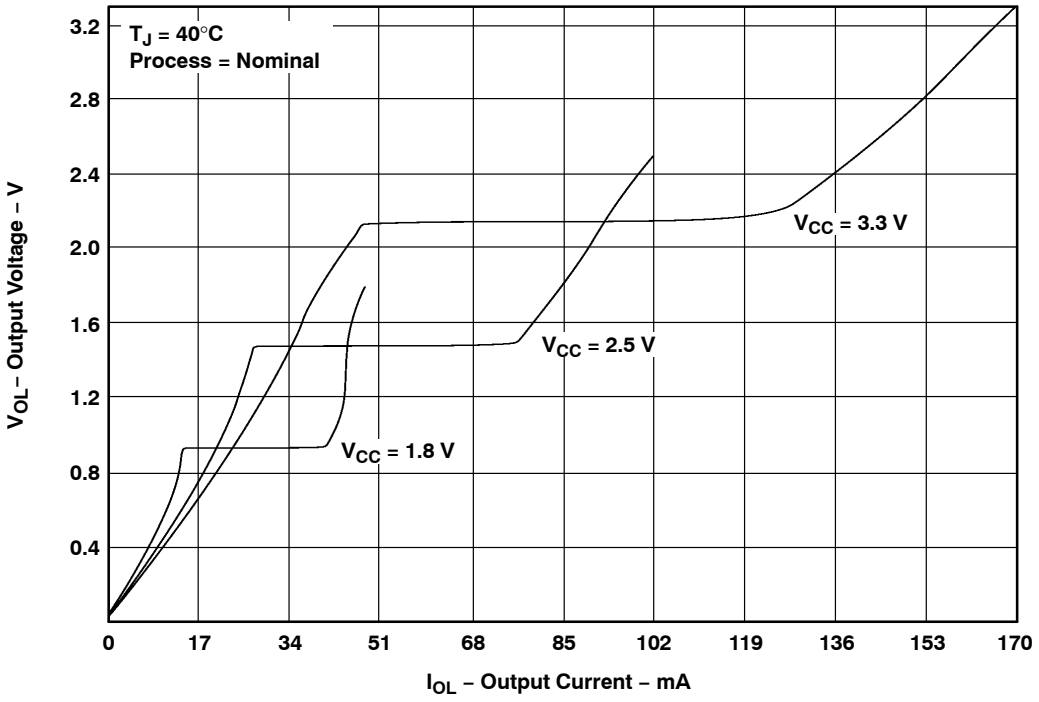


Figure 1. V_{OL} vs I_{OL}

The V_{OH} vs I_{OH} curves (see Figure 2) illustrate the impedance characteristics of the output in the high state. The curves represent the amount of source current available (at a given V_{CC}) to drive the load, as the output voltage increases from 0 V to V_{CC} when the output is sourcing current (i.e., driving high). The operation of the output in the high state is similar to the operation in the low state. There are two distinct regions of source current availability, each with an output resistance (at 2.5-V V_{CC}) of approximately 30 Ω and 50 Ω, respectively. The V_{OH} vs I_{OH} curves for 1.8-V and 3.3-V V_{CC} have similar characteristics.

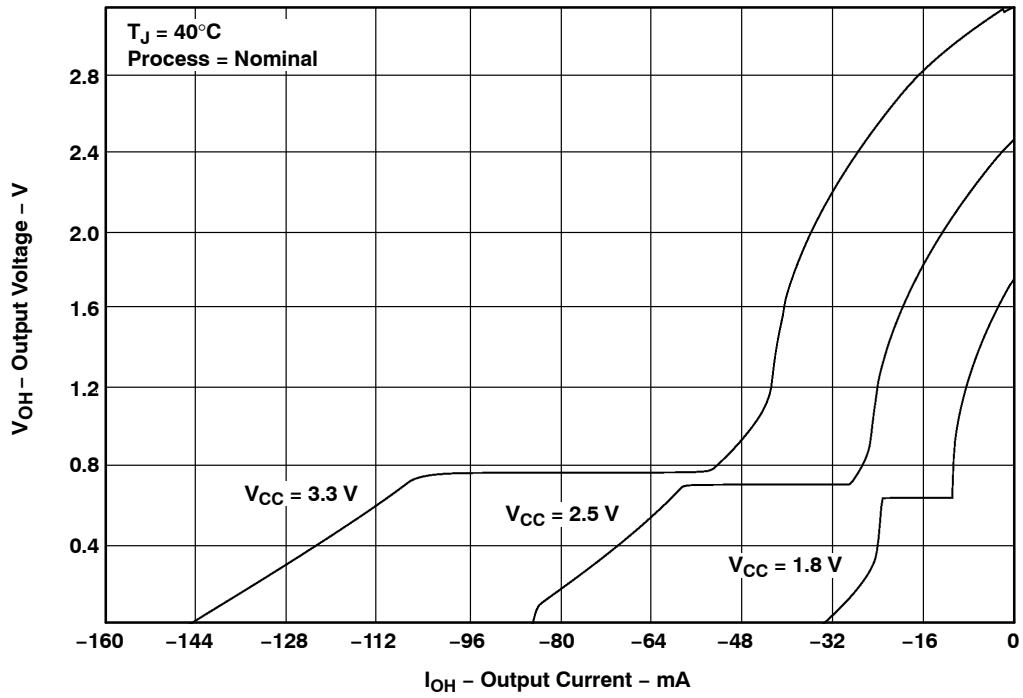


Figure 2. V_{OH} vs I_{OH}

The dual-impedance regions of the DOC output allow a single device to have characteristics similar to a ±24-mA high-drive device, providing fast edge rates and propagation-delay times. During the latter portion of the transition and during static conditions, the device has the characteristics of a series-damping-resistor part, with reduced ringing. Figure 3 illustrates the dual-impedance nature of the DOC output as compared to the fixed-impedance outputs of both a high-drive part and a series-damping-resistor part by showing the V_{OL} vs I_{OL} curves of all three.

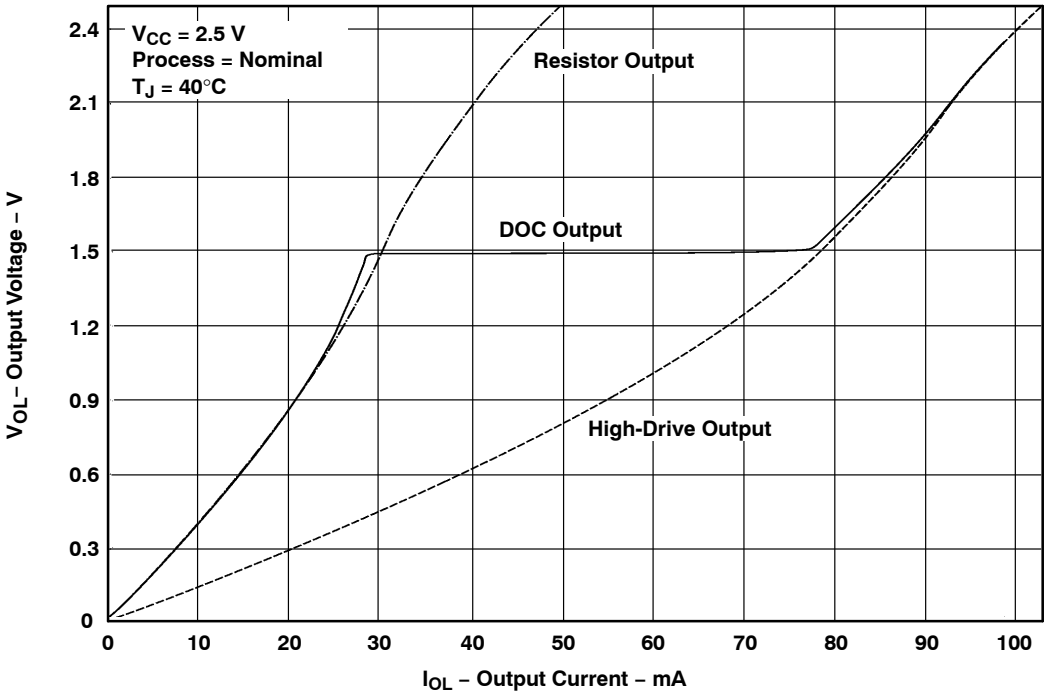


Figure 3. DOC Output Curve Superimposed on Resistor-Output and High-Drive-Output Curves

Output Circuitry

What Happens at the Output in the Transition

A standard device with a fixed low-impedance output delivers high current to the load during the entire transition. At the top of the transition from low to high, high-drive circuits can experience a tremendous overshoot and ringing due to the fast slew rate (see Figure 4). The DOC circuit counteracts this by switching to a higher output impedance, thereby slowing the slew rate as the output approaches the top of the transition.

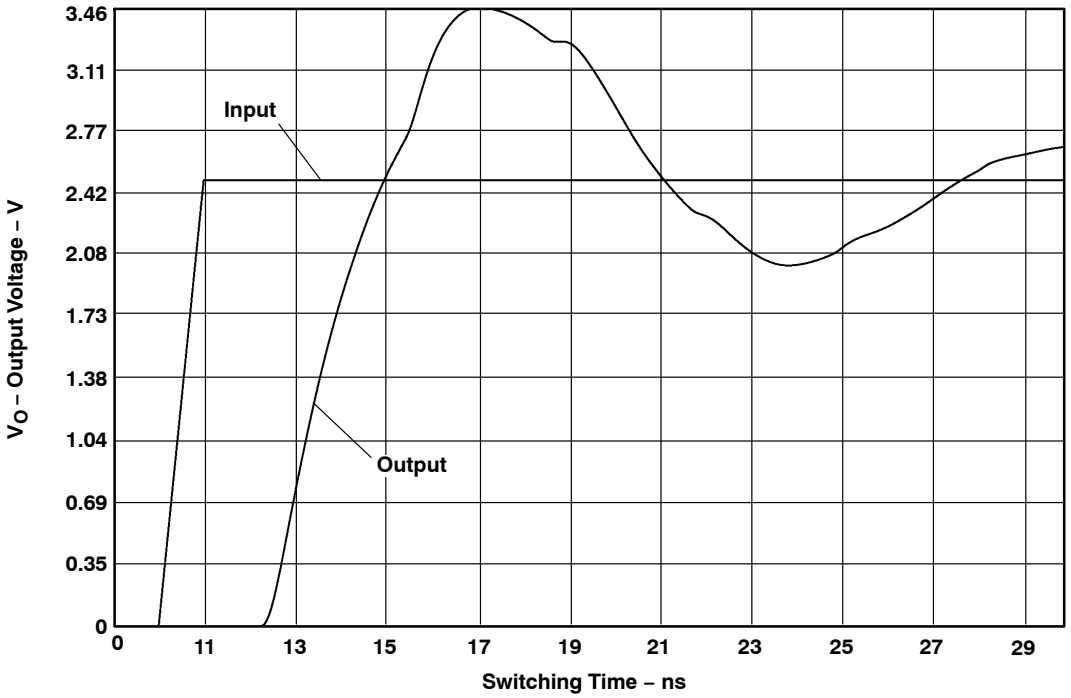


Figure 4. Switching Transition of a Fixed Low-Impedance Driver

Figure 5 illustrates the output of the DOC driver in the transition from low to high. Initially, the output is at a static low level. The 2.5-V V_{OL} vs I_{OL} impedance-characteristic curve (see Figure 1) shows that, with an output at 0 V, the output resistance in the low state is approximately 50 Ω. When the transition from low to high begins, the 2.5-V V_{OH} vs I_{OH} curve (see Figure 2) illustrates the impedance characteristics of the output. Initially, the output resistance is approximately 30 Ω. Under typical conditions, this low-impedance output can deliver nearly 84 mA to the load, providing a very fast slew rate. After the output voltage passes through the threshold (1.5 V) in the transition from low to high, the output resistance is switched from approximately 30 Ω to approximately 50 Ω. This increase in output resistance reduces the amount of drive current available. This decreases the slew rate and rolls off the transition, producing a smooth knee at the top and reducing overshoot or ringing. When the final output voltage is reached, due to the high output resistance, the amount of drive current available to hold the output voltage at a valid logic level is at a minimum, providing relatively low static-state power levels.

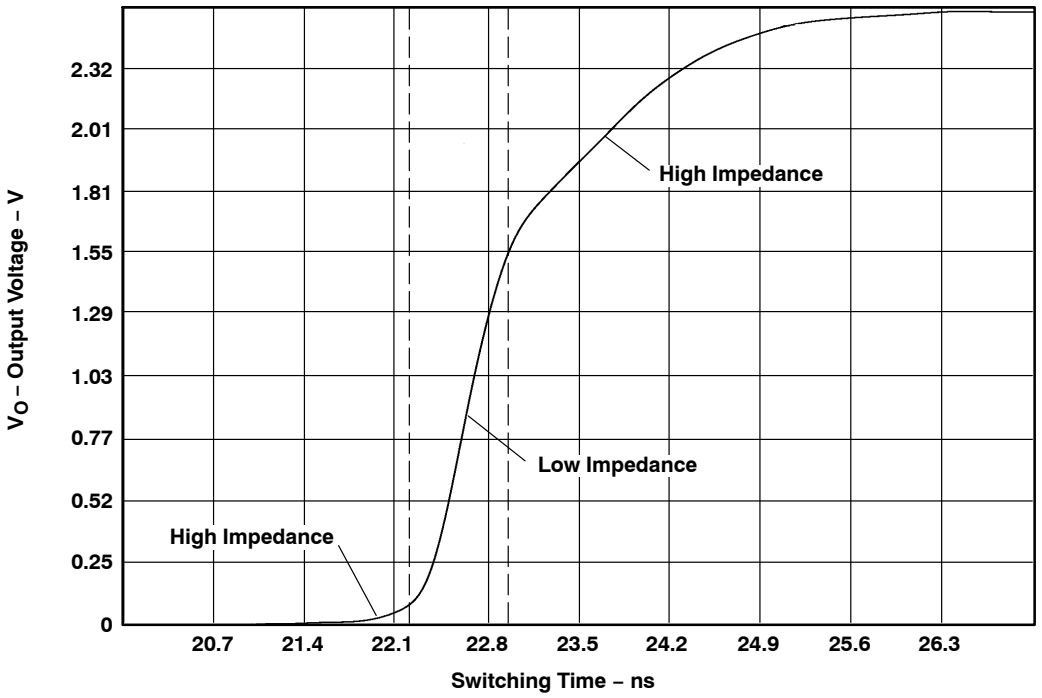


Figure 5. Impedance Through Switching Transitions

A transition from high to low behaves in a similar manner and can be understood by the same principles. When the transition from high to low begins, the 2.5-V V_{OL} vs I_{OL} curve (see Figure 1) illustrates the impedance characteristics of the output. Initially, the output resistance is approximately 20 Ω. Under typical conditions, this low output impedance can deliver nearly 105-mA to the load. Then, as the output voltage passes through the threshold (1.5 V), the output resistance is switched from approximately 20 Ω to approximately 50 Ω. This results in minimal, or no undershoot.

DOC Circuit Description

Figure 6 shows a simplified output stage of a typical logic circuit. When the input is low, the n-channel transistor (Q_n) turns off and the p-channel transistor (Q_p) turns on and begins to conduct, and the output voltage V_O is pulled high. Conversely, when the input is high, Q_p turns off, Q_n begins to conduct, and V_O is pulled low. This action is similar to an inverter, and several of these inverting stages typically are cascaded in series to form a buffer/driver.

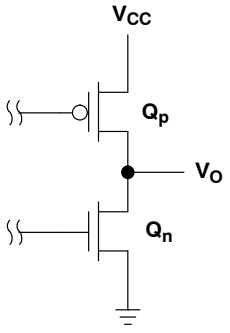


Figure 6. Simplified Totem-Pole Output Stage

The sizes of the output transistors Q_p and Q_n determine the output impedance. The transistors are designed with the sizes of the n-channel FET and p-channel FET selected to provide an output impedance of a specific design value. The sizes can be selected so that the on-resistance of the output is, for example, characteristically approximately 25 Ω, which is the typical output impedance of a conventional low-voltage CMOS logic device. Figure 7 illustrates a driver with the output transistors sized to provide a 25-Ω output. The driver is shown driving a transmission-line load consisting of a length of transmission line that is terminated into a capacitor. The waveform showing the signal incident at the capacitor depicts the fast slew rates and small propagation delays that are characteristic of low-impedance drivers. The fast edge rates create large overshoots and unacceptable ringing.

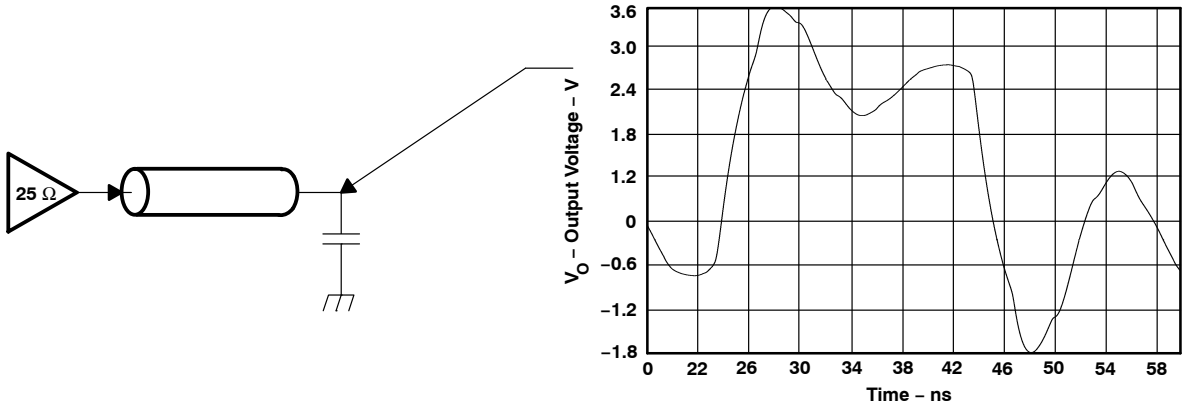


Figure 7. 25-Ω Driver Driving Transmission-Line Load and Waveform at the Load

One method of reducing the ringing and electrical noise is to slow down the edge rates. This can be accomplished by the addition of a damping resistor in series with the output. This creates a high-impedance low-drive output. Figure 8 illustrates a driver with a 25-Ω output and a series 26-Ω damping resistor driving the transmission-line load. The resultant signal is much cleaner, but the slower edge rate increases the propagation delay time. Depending on the total timing budget available, this could be an unacceptable solution. Series resistors also can raise the dc low-voltage level of a signal. This reduces noise immunity of the receiving logic. Finally, series damping resistors should be used only on point-to-point nets, and never with distributed loads, because of the half voltage that propagates down the transmission line due to incident wave switching.

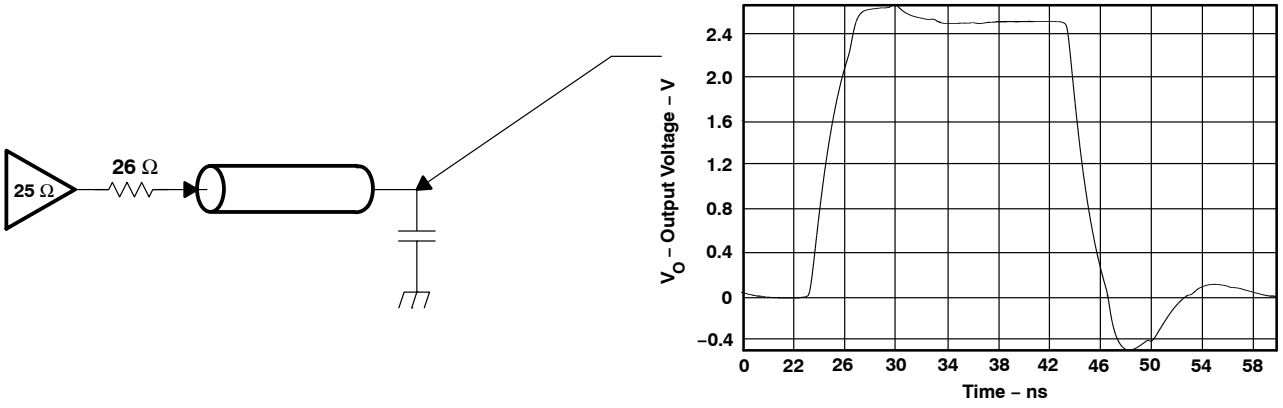


Figure 8. 25-Ω Driver and 26-Ω Series Resistor Driving Transmission-Line Load and Waveform at the Load

Another method that can be used to improve the impedance match of the output with the load is to reduce the size of the output transistors. If their sizes are decreased, the output impedance increases. This provides a low-drive output. Figure 9 illustrates a driver with the output transistor sizes selected to provide a 50-Ω output. The driver is shown driving the same transmission-line load and the resultant waveform at the load exhibits similar characteristics to the series-damping-resistor version.

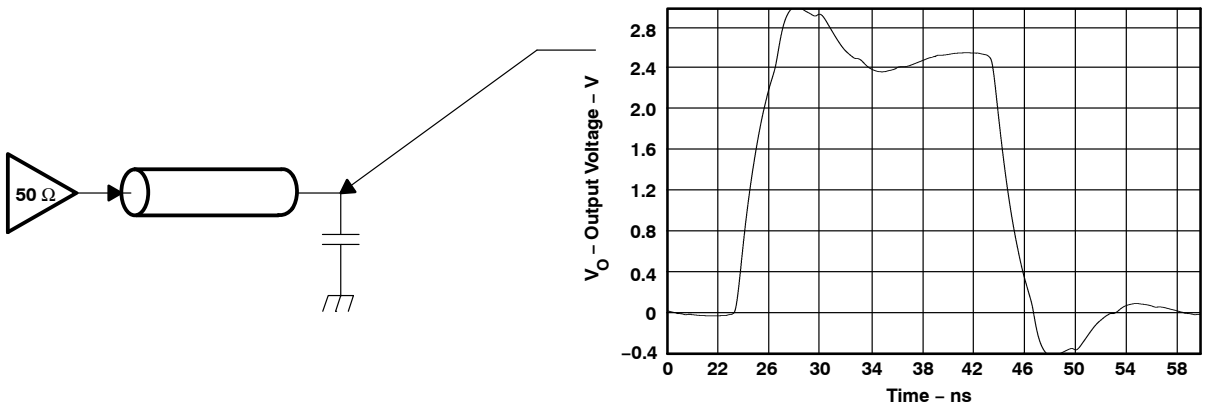


Figure 9. 50-Ω Driver Driving Transmission-Line Load and Waveform at the Load

It is also interesting to explore the attributes of two drivers in parallel. Figure 10 represents two 50-Ω drivers in parallel. The resultant waveform at the load exhibits characteristics similar to the single 25-Ω driver. In fact, the parallel combination of the two has the same output impedance as a single 25-Ω impedance driver. This effectively creates a low-impedance high-drive output.

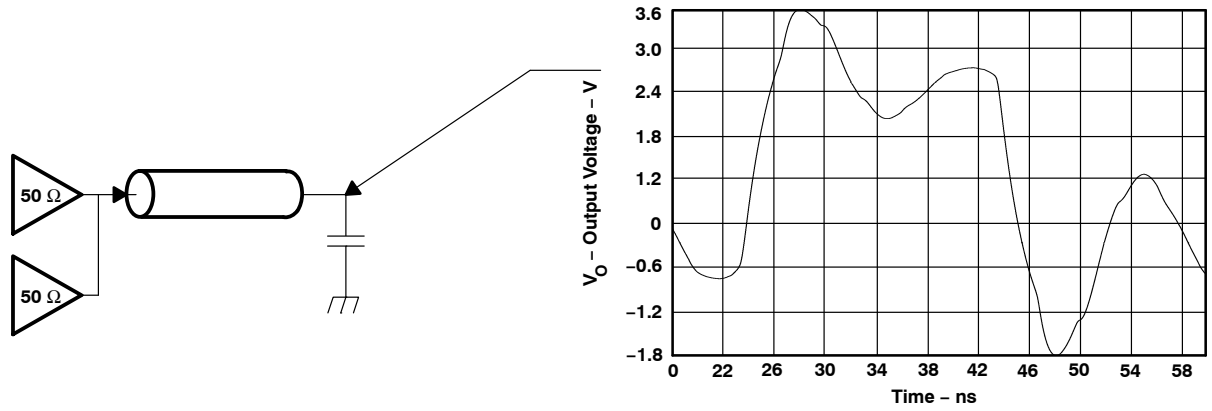


Figure 10. Two 50-Ω Drivers In Parallel, Driving Transmission-Line Load and Waveform at the Load

Increasing the output impedance reduces overshoots and undershoots, but at the cost of increased propagation delays. Decreasing the output impedance decreases propagation delays, but at the cost of increased overshoots and undershoots. A desirable circuit would have a low output impedance for the beginning portion of the output transition and a high output impedance for the latter portion of the output transition. This would provide fast propagation delays, with minimal, or no overshoot or undershoot.

Figure 11 is a block diagram of the DOC circuit, which consists of a fixed driver with a nominal 50-Ω on-resistance. The 50-Ω driver functions like a typical high-impedance low-drive output, with good electrical and noise characteristics. In parallel with the 50-Ω driver is a controllable 50-Ω nominal on-resistance driver, with an output that can be enabled or disabled similar to the output of a 3-state device. When a device is disabled, its output is in a very high-impedance state and contributes nothing to the drive or to the loading of the output. When it is enabled, the parallel combination of the 50-Ω drivers has the same output characteristics as a single 25-Ω impedance driver. This effectively creates a low-impedance high-drive output. The impedance control circuit (ZCC) enables and disables the controllable driver by controlling its ON signal. The ZCC monitors the output and controls the controllable driver at the appropriate times during the signal transition to achieve a high-drive, fast slew-rate transition.

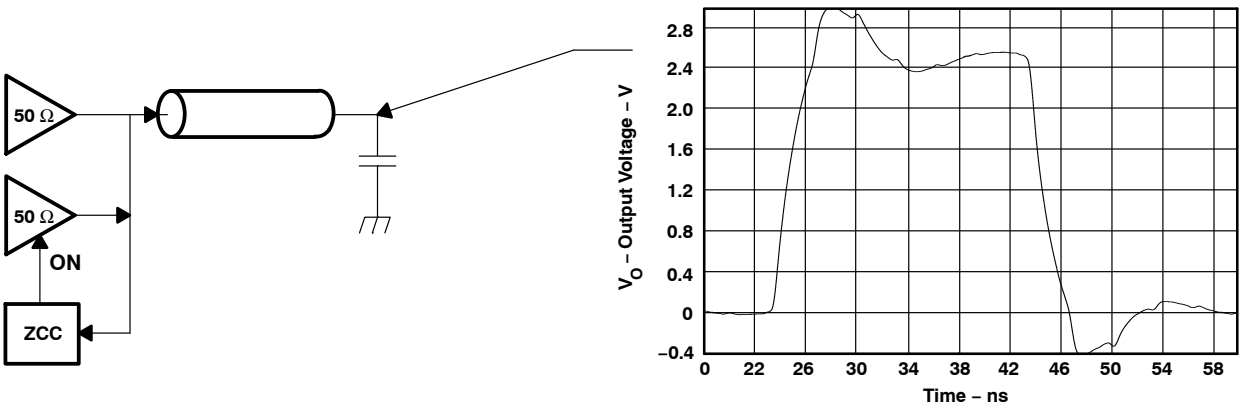


Figure 11. DOC Circuit Driving Transmission-Line Load and Waveform at the Load

The operation of the DOC begins with the output in a static state, for example, at a logic low state. In the static low state, the ZCC has the controllable 50-Ω driver disabled and the n channel of the fixed 50-Ω driver sinks current to ground from the output. When the input transitions from low to high, the n-channel transistor in the fixed 50-Ω driver turns off, and the p channel turns on, sourcing current to the output and beginning the output transition from low to high. Simultaneously, the ZCC enables the p channel in the controllable 50-Ω driver. The parallel p channels of the drivers have a combined on-resistance of approximately 25 Ω. This low impedance provides a high drive current to cause a fast slew-rate signal transition. The ZCC senses the output voltage, and as the voltage passes through threshold in the transition from low to high, the ZCC disables the output p channel of the controllable 50-Ω driver. The increase in output impedance decreases the slope and rolls off the output signal, reducing the overshoot.

The operation of the high-to-low transition is similar.

AC Dynamic Drive vs DC Static Drive

The dc drive-current ratings in the recommended operating-conditions table of a device data sheet typically are selected to show the static-drive capability of a device when the output voltage is at a worst-case valid logic level, such as $V_{OH(MIN)}$ or $V_{OL(MAX)}$. Historically, these dc drive-current ratings were used as a relative measure of a component's ac dynamic-drive performance. For a device with a fixed output on-resistance, this was an acceptable method, because the dc current at a given logic level could be extrapolated to determine the amount of ac drive current available through the transition.

With DOC circuitry, the output impedance characteristics change dynamically during a transition. *The dc drive-current specification is not a useable indicator of the devices' dynamic performance capability.* The dc output ratings of DOC devices (see Table 1) can be used loosely as a relative comparison to the dc output ratings of devices with integral series damping resistors (see Table 2), and this is a good indication of the DOC circuit's excellent low-noise and low-power characteristics. However, unlike a part with a fixed low-drive output, the DOC circuitry provides good ac performance. The DOC output provides a very strong ac drive during dynamic conditions, capable of driving very heavily capacitive CMOS loads.

Table 1. Recommended Static Output Current for DOC Circuits[1]

			MIN	MAX	UNIT
I_{OHS}	Static high-level output current	V_{CC} = 1.65 V to 1.95 V		–4	mA
		V_{CC} = 2.3 V to 2.7 V		–8	
		V_{CC} = 3 V to 3.6 V		–12	
I_{OLS}	Static low-level output current	V_{CC} = 1.65 V to 1.95 V		4	mA
		V_{CC} = 2.3 V to 2.7 V		8	
		V_{CC} = 3 V to 3.6 V		12	

Table 2. Recommended Output Current for ALVC Device With Damping Resistor[2]

			MIN	MAX	UNIT
I_{OH}	High-level output current	V_{CC} = 2.3 V		–6	mA
		V_{CC} = 2.7 V		–8	
		V_{CC} = 3 V		–12	
I_{OL}	Low-level output current	V_{CC} = 2.3 V		6	mA
		V_{CC} = 2.7 V		8	
		V_{CC} = 3 V		12	

The DOC device performs like a high-drive part during signal transition. *Under typical conditions at 2.5-V V_{CC}, the drive current that is available during the beginning of a transition from low to high is about 84 mA, and from high to low is about 105 mA*. Figure 12 illustrates the output current of the DOC circuit driving a standard load through the low-to-high and high-to-low transitions. Note the large peak currents during the transition.

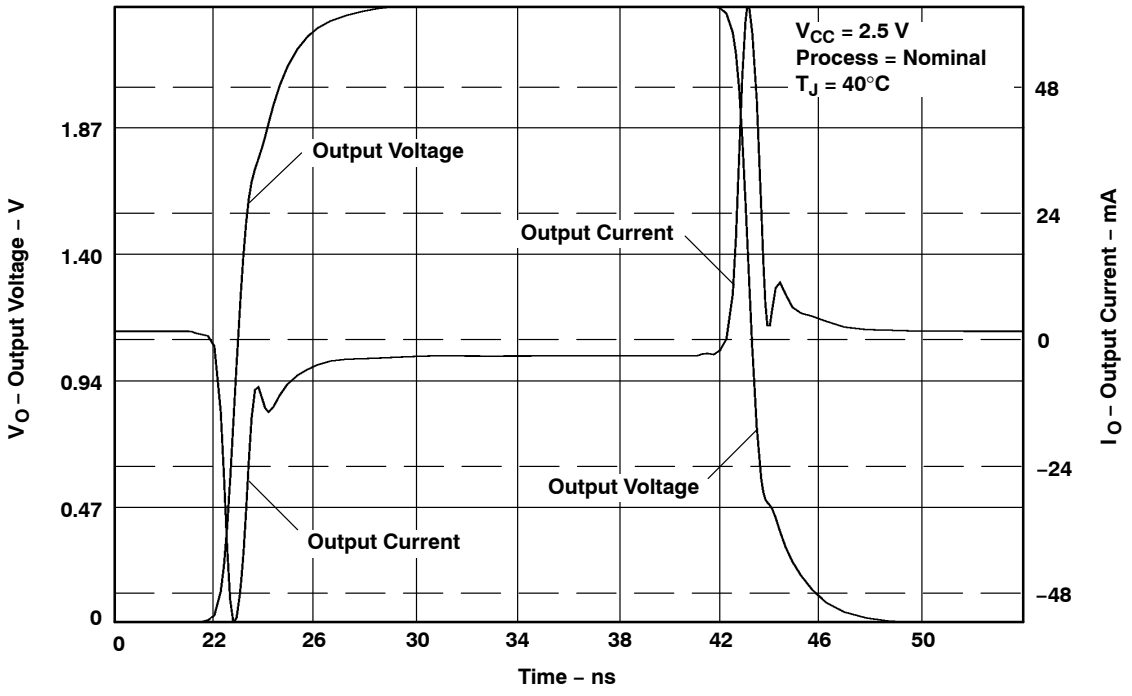


Figure 12. DOC Device Output Current Through the Transition

The dynamic drive current is not specified on the data sheet for devices with DOC outputs because of its transient nature, but it is similar to the dynamic drive current that is available from a ±24-mA (at 2.5-V V_{CC}) high-drive standard-output device (see Figure 13).

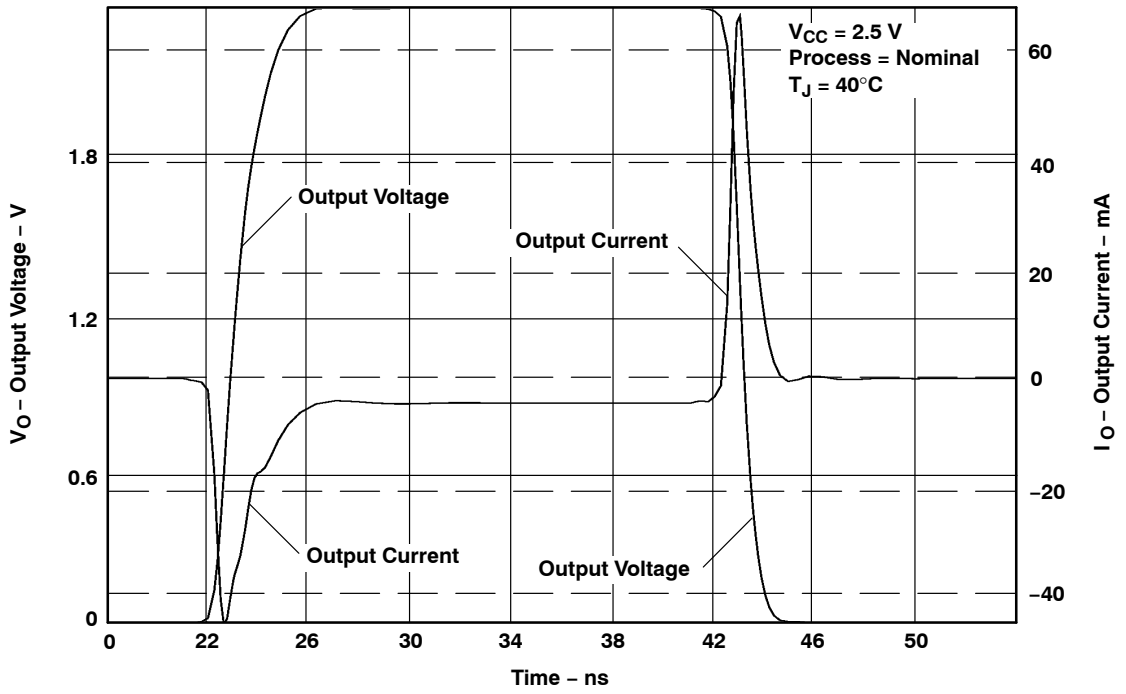


Figure 13. Output Current Through the Transition, ±24-mA High-Drive Standard-Output Device

Because a typical CMOS load is purely capacitive, with very little bias (leakage) current necessary to hold a valid static logic level, the amount of dc drive required of most drivers is small. The dc drive is specified on the data sheet of DOC output devices. The output parameters are static and testable values that are enumerated in terms of minimum and maximum output voltages at specific output currents (see Table 3).

Table 3. Output Voltage Characteristics Over Recommended Operating Free-Air Temperature Range[1]

PARAMETER	TEST CONDITIONS		V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	I_{OH} = –100 μA		1.65 V to 3.6 V	V_{CC}–0.2			V
	I_{OH} = –4 mA,	V_{IH} = 1.07 V	1.65 V	1.2			
	I_{OH} = –8 mA,	V_{IH} = 1.7 V	2.3 V	1.75			
	I_{OH} = –12 mA,	V_{IH} = 2 V	3 V	2.3			
V_{OL}	I_{OL} = 100 μA		1.65 V to 3.6 V			0.2	V
	I_{OL} = 4 mA,	V_{IL} = 0.57 V	1.65 V			0.45	
	I_{OL} = 8 mA,	V_{IL} = 0.7 V	2.3 V			0.55	
	I_{OL} = 12 mA,	V_{IL} = 0.8 V	3 V			0.7	

Termination (AC vs DC)

Because of the excellent signal-integrity characteristics of the DOC output, transmission-line termination typically is unnecessary. Due to the high-impedance characteristics of the output in the static state, *the use of dc termination is specifically discouraged*. The output current that is required to bias a dc termination network could exceed the static-state output-drive capabilities of the device. AVC family devices with DOC circuitry are suited ideally for any high-speed, point-to-point application or unterminated distributed load, such as high-speed memory interfaces.

Waveforms – Comparison of ALVCH Standard and Resistor Outputs

Figures 14 and 15 show the SPICE results comparing SN74AVC16827 with SN74ALVCH16827 and SN74ALVCH162827 into a standard lumped load (see Appendix A) for V_{CC} = 2.5 V and V_{CC} = 3.3 V, respectively. The results show the relative propagation delay and noise performance of the DOC circuit.

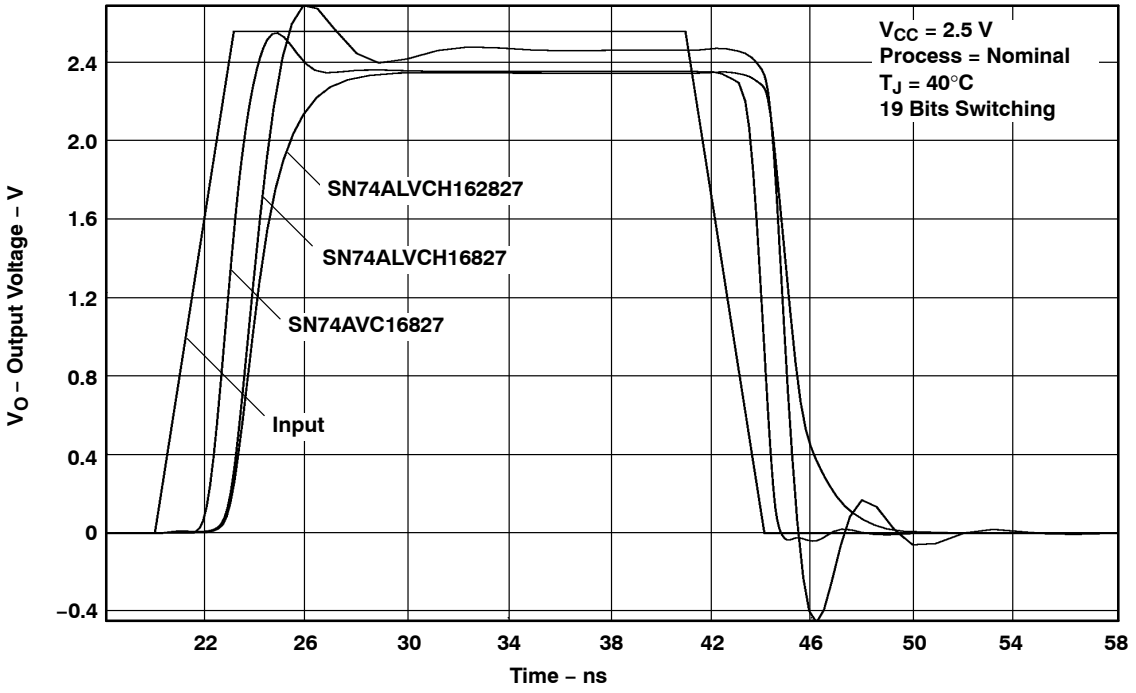


Figure 14. Outputs Driving a Standard Lumped Load, V_{CC} = 2.5 V

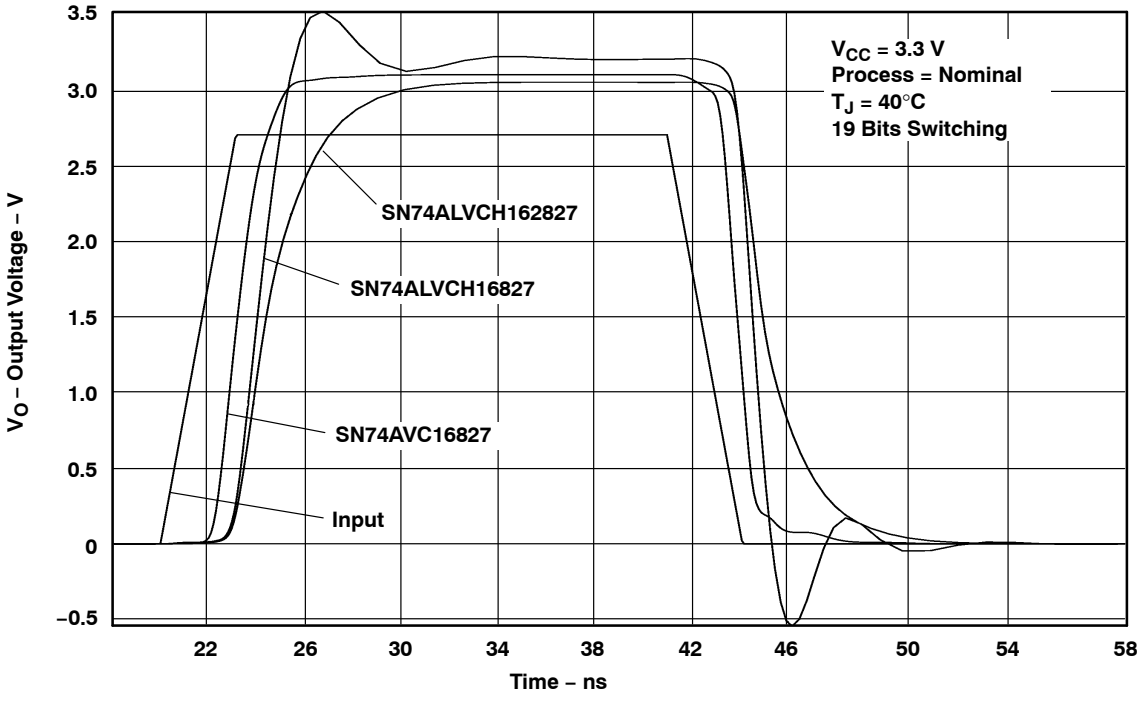


Figure 15. Outputs Driving a Standard Lumped Load, V_{CC} = 3.3 V

Figures 16 and 17 show the SPICE modeling of the SN74AVC16827 with the DOC circuit, an SN74ALVCH16827 with low-impedance output circuit, and an SN74ALVCH162827 with series damping resistors driving a PC100 DQM load for V_{CC} = 2.5 V and V_{CC} = 3.3 V, respectively. The DQM load is defined in the Intel™ *PC SDRAM Registered DIMM Specification*, Revision 1.0, February 1998[3]. For this example, the 256-Mbyte load was used. The transmission lines have a characteristic impedance of 70 Ω. The lengths of the transmission lines are specified in the PC100 specification; series resistor R1 was specified as zero. This resistor is not necessary when using the DOC circuit. The six SDRAM loads were modeled by the circuit shown in Figure 18.

The waveforms shown in Figures 16 and 17 were measured at the input to the memory devices. The low-impedance driver exhibits excessive overshoots and undershoots, while the DOC circuit and the driver with series damping resistors does not. The DOC circuit is faster than the series-damping-resistor circuit. This improvement in speed is more pronounced when the simulations are run under worst-case weak conditions.

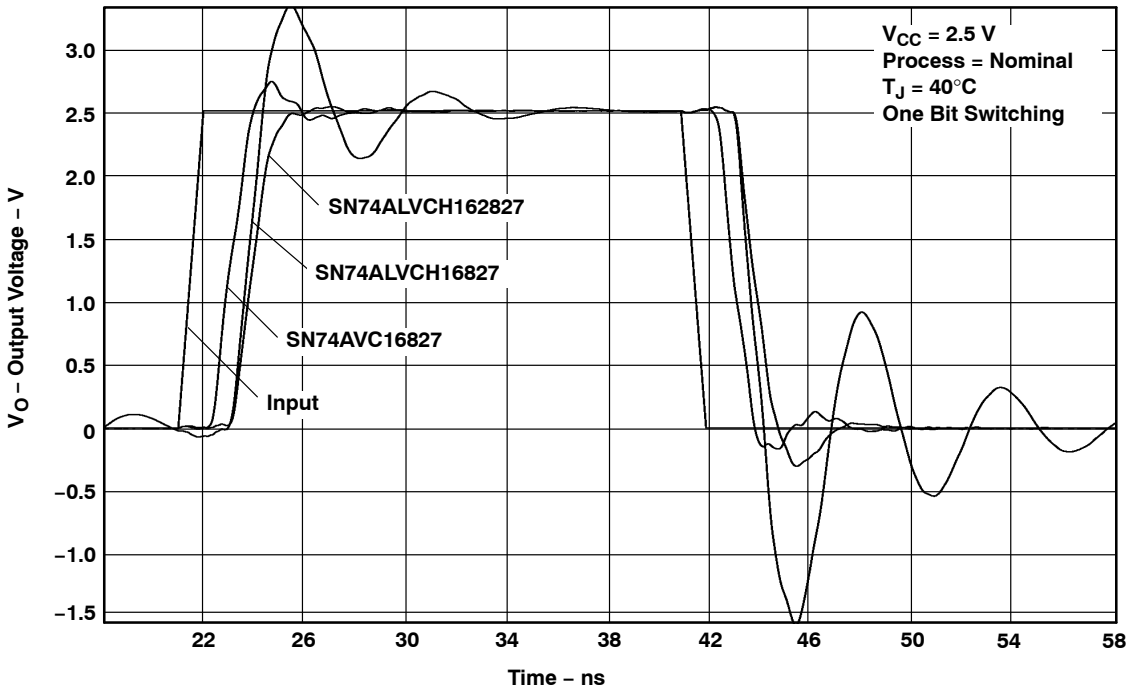


Figure 16. Outputs Driving a PC100 Load Network, V_{CC} = 2.5 V

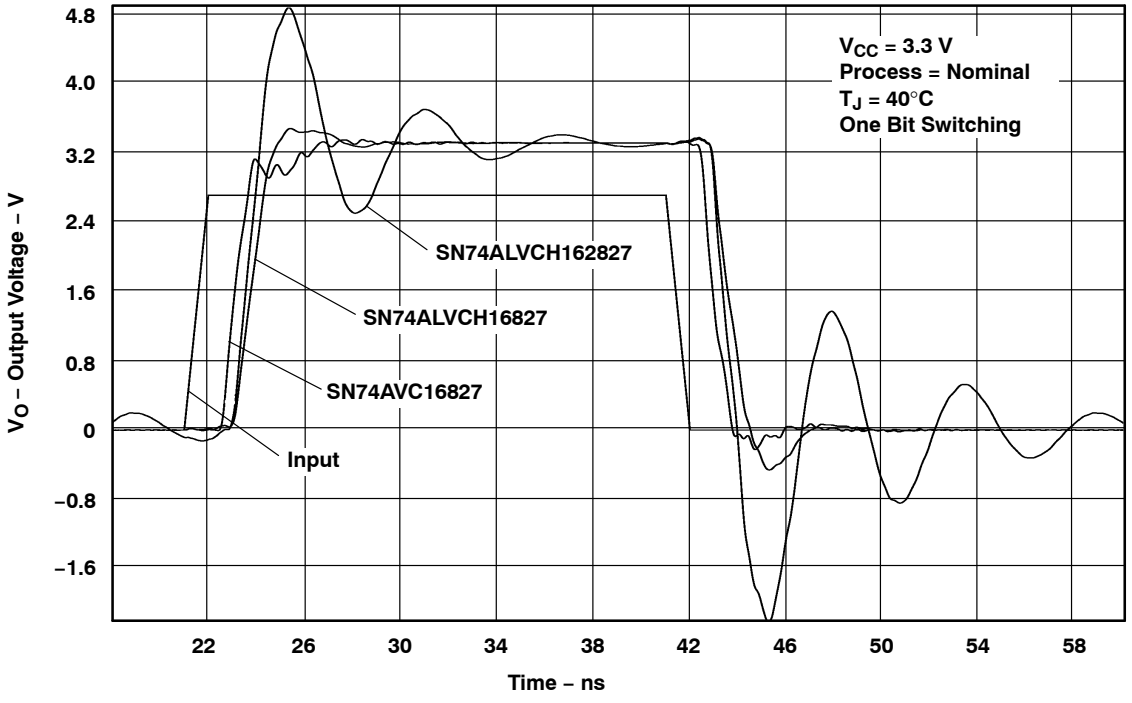


Figure 17. Outputs Driving a PC100 Load Network, V_{CC} = 3.3 V

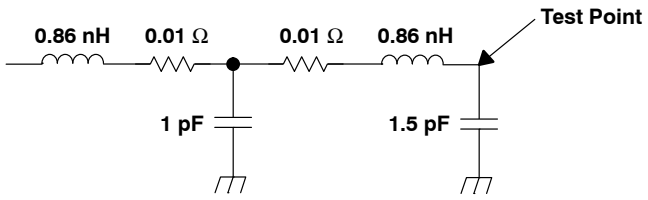


Figure 18. SDRAM Load Model

Features and Benefits

Table 4 summarizes DOC circuit features and some of the benefits of those features.

Table 4. Features and Benefits of DOC Circuitry

FEATURES	BENEFITS
Optimized for 2.5-V V_{CC}. No damping resistors	Enables low-power designs
Low-impedance, high-drive output during the beginning of a signal transition	Fast edge-rates and small propagation delays
High output impedance for the later portion of the ouput transition	Minimal, or no overshoot or undershoot
High-impedance, low-drive steady-state output after signal transition	Enables low-power designs
DOC outputs do not require series damping resistors internally or externally	Reduced ringing without series output resistors; increased performance; cost savings
I_{OFF} – reverse-current paths to V_{CC} blocked	Outputs disabled during power off for use in partial power-down designs

Conclusion

The DOC circuitry provides a low-impedance, high-drive output during the beginning of a signal transition, to provide fast edge rates and small propagation delays. Then, as the output passes through the threshold, the DOC switches to a high-impedance, low-drive output to roll off the signal and reduce ringing. The amount of static dc drive current specified in the data sheets of devices with DOC features does not reflect the large amount of dynamic current that is available to drive a typical large capacitive CMOS load.

Frequently Asked Questions

1. Q: What is DOC?

   A: DOC is the Dynamic Output Control circuit (patent pending). It is the output circuit of TI's AVC family of devices that changes the output impedance during the signal transition.

2. Q: Why use DOC output?

   A: During the beginning of the signal transition, DOC output provides the desirable characteristics of high drive to supply fast edge-rates and small propagation delays. As the signal passes through the threshold, the DOC output decreases the drive to roll off the signal and reduce ringing without the use of damping resistors.

3. Q: How does DOC work?

   A: The DOC output has an impedance-control circuit that monitors the output signal. When a transition begins, the impedance-control circuit enables the outputs of two parallel drivers to provide a low-impedance, high-drive output. As the output passes through the threshold, the impedance-control circuit disables the output of one of the drivers, providing a high-impedance, low-drive output.

4. Q: Should I use series damping resistors on the output of DOC devices?

   A: It is not necessary to use series damping resistors to reduce ringing because the DOC output provides a high-impedance, low-drive output at the end of the signal transition. Using series damping resistors would defeat the high-drive benefit of the DOC output.

5. Q: Can I use dc termination on the output of DOC devices?

   A: *Do not use dc termination*. The use of dc termination could exceed the static-drive capability of the DOC output. Due to the excellent signal-integrity characteristics of the DOC output, termination should be unnecessary.

6. Q: What is the maximum drive-current capability of the DOC output?

   A: The DOC output has ±8-mA dc static-drive current capability at 2.5-V V_{CC}. Under typical conditions at 2.5-V V_{CC}, the amount of ac dynamic-drive current that the DOC output can supply varies from a maximum of about 84 mA at the beginning of the transition from low to high. At the beginning of the transition from high to low, it varies from a maximum of about 105 mA.

7. Q: What is the output impedance of a DOC circuit?

   A: The impedance during dynamic conditions is characterized by the slope of the V_O vs I_O line, at any specific point on the graph. The output R_{ON} can be calculated from the V_{OH} vs I_{OH} and V_{OL} vs I_{OL} curves (see Figure 1 and Figure 2). At any specific point on the V_{OH} vs I_{OH} curves, $R_{ON} = (V_{OH} - V_{CC})/I_{OH}$. At any specific point on the V_{OL} vs I_{OL} curves, $R_{ON} = V_{OL}/I_{OL}$. In the high state, the output R_{ON} varies from approximately 50 Ω in the high-impedance mode to approximately 30 Ω in the low-impedance mode. In the low state, the output R_{ON} varies from approximately 50 Ω in the high-impedance mode to approximately 20 Ω in the low-impedance mode.

8. Q: Are devices with DOC output circuitry fast?

   A: Yes, the DOC output provides a very fast edge-rate to decrease the propagation delay times, while maintaining the excellent signal-integrity characteristics associated with the slower series-damping-resistor parts.

9. Q: Why aren't ac dynamic-drive specifications included in the data sheet?

   A: The dynamic-drive current is not specified on the data sheet for devices with DOC outputs because of its transient nature, but it is similar to the drive current available from a standard-output device with an I_{OH} and I_{OL} of ±24 mA at 2.5-V V_{CC}.

10. Q: In data sheets for devices with DOC outputs, is the dc static-drive specification an indicator of the devices' dynamic performance?

    A: No. The devices perform like high-drive devices during signal transition. This is not reflected in the dc static-drive specification on the data sheet.

11. Q: Since the DOC output provides high-drive, does it suffer from poor simultaneous switching performance? How does its simultaneous switching performance compare to standard and resistor devices?

    A: At 2.5-V V_{CC} with output into a standard load, SPICE analysis shows that the SN74AVC16245 DOC outputs have a maximum V_{OLV} = −165 mV, standard outputs have a maximum V_{OLV} = −574 mV, and resistor outputs have a maximum V_{OLV} = −36 mV (15 outputs switching, one steady-state low).

12. Q: Do DOC outputs contribute to a device's low-power performance?

    A: Compared to a damping-resistor output where a portion of the output drive is dissipated in the resistor and not delivered to the load, the DOC output offers better low-power performance. The devices in the AVC family that feature DOC outputs are designed for 2.5-V V_{CC} operation, enabling low-power designs.

Acknowledgment

The authors of this application report are Stephen M. Nolan and Tim Ten Eyck.

References

1. TI *SN74AVC16245 16-Bit Bus Transceiver With 3-State Outputs*, literature number SCES142.
2. TI *SN74ALVC162245 16-Bit Bus Transceiver With 3-State Outputs*, literature number SCES064.
3. *Intel PC SDRAM Registered DIMM Specification*, Revision 1.0, February 1998.

Glossary

A

A	Amperes
ac	Alternating current
ALVC	Advanced Low-Voltage CMOS
AVC	Advanced Very-low-voltage CMOS

B

B	Byte

C

C	Celsius
CMOS	Complementary metal-oxide semiconductor

D

dc	Direct current
DIMM	Dual-inline memory module
DOC	Dynamic output control (patent pending)
DQM	Data mask
DRAM	Dynamic random-access memory

F

F	Farad
FET	Field-effect transistor

H

H	Henry

I

IBIS	I/O buffer information specification
I_I	Input current
I_{OFF}	Current into a pin when V_{CC} = 0 V
I_{OH}	High-level output current
I_{OHS}	Static high-level output current
I_{OL}	Low-level output current
I_{OLS}	Static low-level output current
IV	Current vs voltage

M

Max	Maximum
Min	Minimum

P

PC	Personal computer

R

R_{ON}	On-state output resistance

S

s	Seconds
SDRAM	Synchronous DRAM
SPICE	Simulation program with integrated-circuit emphasis

T

TI	Texas Instruments

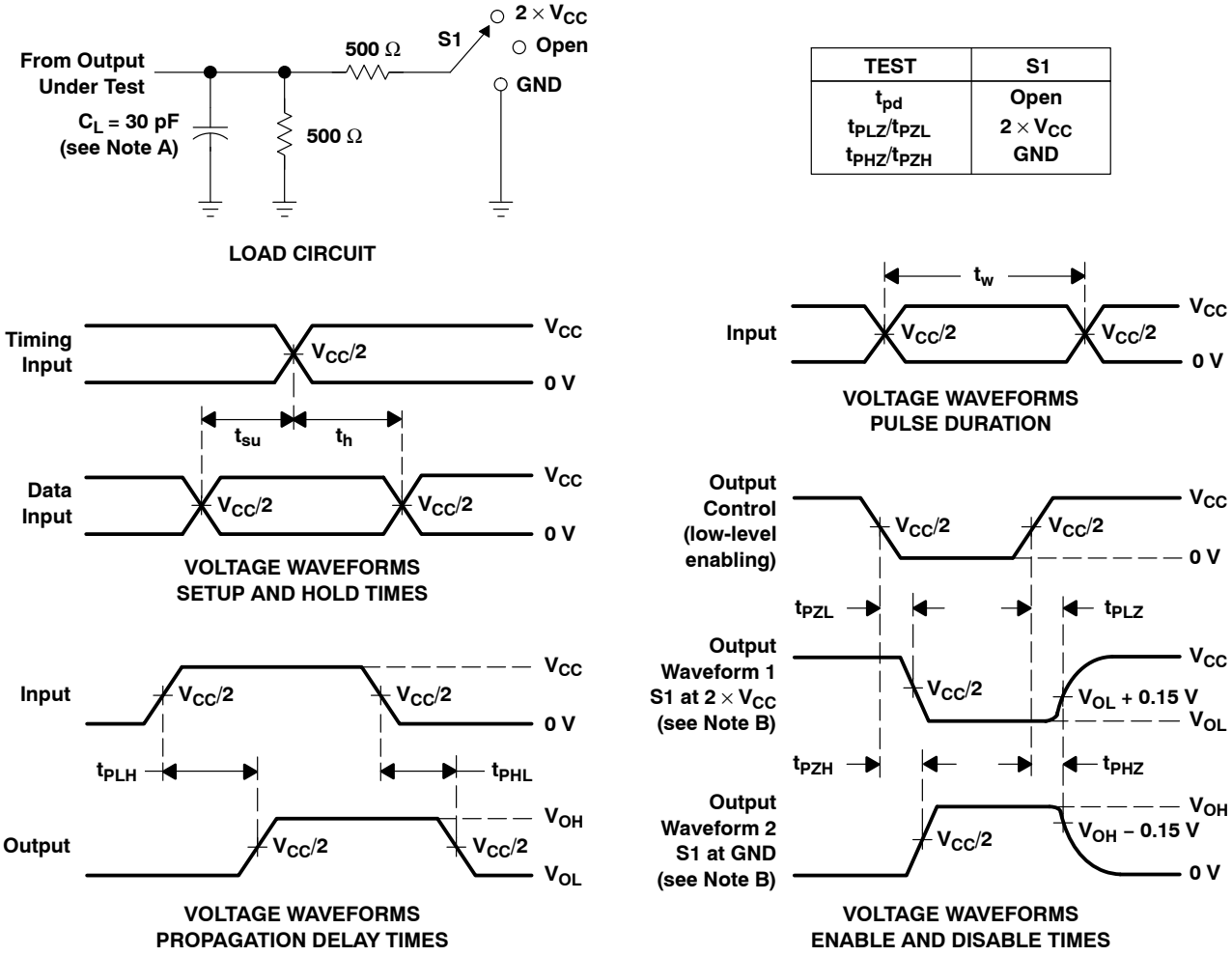
V

V	Volts
V_{CC}	Supply voltage
V_O	Output voltage
V_{OH}	High-level output voltage
V_{OL}	Low-level output voltage
V_{OHP}	High-level output voltage peak
V_{OHV}	High-level output voltage valley
V_{OLP}	Low-level output voltage peak
V_{OLV}	Low-level output voltage valley

Z

ZCC	Impedance control circuit

Appendix A – Parameter Measurement Information



NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2 ns, t_f ≤ 2 ns.
D. The outputs are measured one at a time with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.

Figure A–1. AVC Load Circuit and Voltage Waveforms (V_{CC} = 2.5 V ± 0.2 V)

Implications of Slow or Floating CMOS Inputs

SCBA004C
February 1998

TEXAS INSTRUMENTS

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Contents

List of Illustrations

Introduction

In recent years, CMOS (AC/ACT, AHC/AHCT, ALVC, CBT, CBTLV, HC/HCT, LVC, LV/LV-A) and BiCMOS (ABT, ALVT, BCT, FB, GTL, and LVT) logic families have further strengthened their position in the semiconductor market. New designs have adopted both technologies in almost every system that exists, whether it is a PC, a workstation, or a digital switch. The reason is obvious: power consumption is becoming a major issue in today's market. However, when designing systems using CMOS and BiCMOS devices, one must understand the characteristics of these families and the way inputs and outputs behave in systems. It is very important for the designer to follow all rules and restrictions that the manufacturer requires, as well as to design within the data-sheet specifications. Because data sheets do not cover the input behavior of a device in detail, this application report explains the input characteristics of CMOS and BiCMOS families in general. It also explains ways to deal with issues when designing with families in which floating inputs are a concern. Understanding the behavior of these inputs results in more robust designs and better reliability.

Characteristics of Slow or Floating CMOS Inputs

Both CMOS and BiCMOS families have a CMOS input structure. This structure is an inverter consisting of a p-channel to V_{CC} and an n-channel to GND as shown in Figure 1. With low-level input, the p-channel transistor is on and the n-channel is off, causing current to flow from V_{CC} and pulling the node to a high state. With high-level input, the n-channel transistor is on, the p-channel is off, and the current flows to GND, pulling the node low. In both cases, no current flows from V_{CC} to GND. However, when switching from one state to another, the input crosses the threshold region, causing the n-channel and the p-channel to turn on simultaneously, generating a current path between V_{CC} and GND. This current surge can be damaging, depending on the length of time that the input is in the threshold region (0.8 to 2 V). The supply current (I_{CC}) can rise to several milliamperes per input, peaking at approximately 1.5-V V_I (see Figure 2). This is not a problem when switching states within the data-sheet-specified input transition time limit specified in the recommended operating conditions table for the specific devices. Examples are shown in Figure 3.

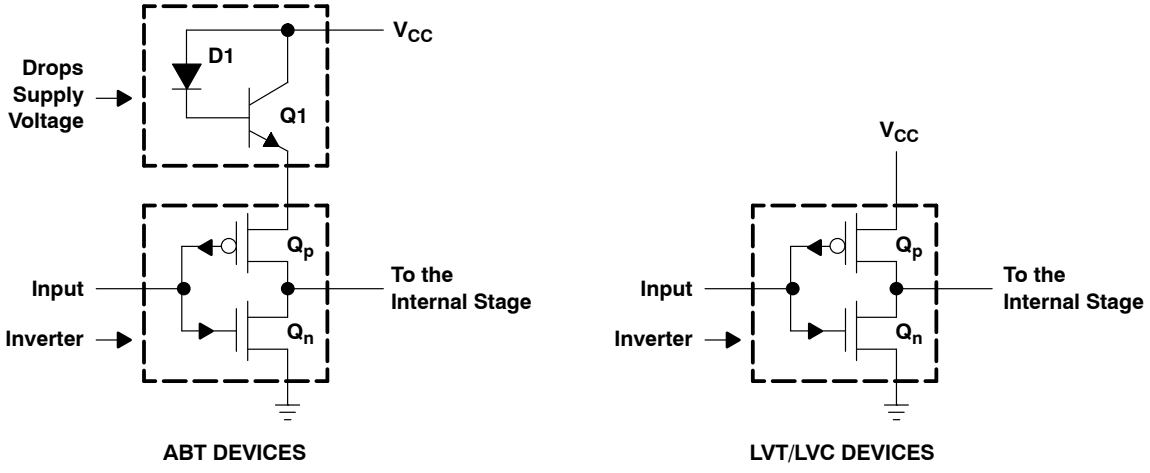

Figure 1. Input Structures of ABT and LVT/LVC Devices

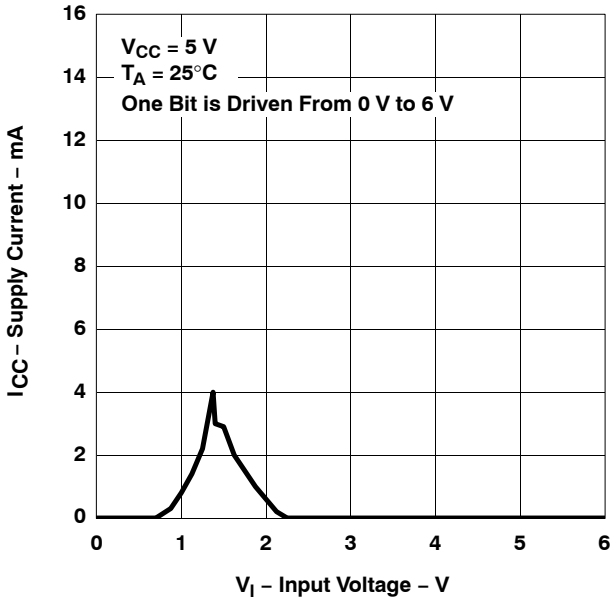

Figure 2. Supply Current Versus Input Voltage (One Input)

recommended operating conditions†

				MIN	MAX	UNIT
$\Delta t/\Delta v$	Input transition rise or fall rate	ABT octals			5	ns/V
		ABT Widebus™ and Widebus+™			10	
		AHC, AHCT			20	
		FB			10	
		LVT, LVC, ALVC, ALVT			10	
		LV			100	
		LV-A	V_{CC} = 2.3 V to 2.7 V		200	
			V_{CC} = 3 V to 3.6 V		100	
			V_{CC} = 4.5 V to 5.5 V		20	
t_t	Input transition (rise and fall) time	HC, HCT	V_{CC} = 2 V		1000	ns
			V_{CC} = 4.5 V		500	
			V_{CC} = 6 V		400	

† Refer to the latest TI data sheets for device specifications.

Figure 3. Input Transition Rise or Fall Rate as Specified in Data Sheets

Slow Input Edge Rate

With increased speed, logic devices have become more sensitive to slow input edge rates. A slow input edge rate, coupled with the noise generated on the power rails when the output switches, can cause excessive output errors or oscillations. Similar situations can occur if an unused input is left floating or is not actively held at a valid logic level.

These functional problems are due to voltage transients induced on the device's power system as the output load current (I_O) flows through the parasitic lead inductances during switching (see Figure 4). Because the device's internal power-supply nodes are used as voltage references throughout the integrated circuit, inductive voltage spikes, V_{GND}, affect the way signals appear to the internal gate structures. For example, as the voltage at the device's ground node rises, the input signal, V_I', appears to decrease in magnitude. This undesirable phenomenon can then erroneously change the output if a threshold violation occurs.

In the case of a slowly rising input edge, if the change in voltage at GND is large enough, the apparent signal, V_I', at the device appears to be driven back through the threshold and the output starts to switch in the opposite direction. If worst-case conditions prevail (simultaneously switching all of the outputs with large transient load currents), the slow input edge is repeatedly driven back through the threshold, causing the output to oscillate. Therefore, the maximum input transition time of the device should not be violated, so no damage to the circuit or the package occurs.

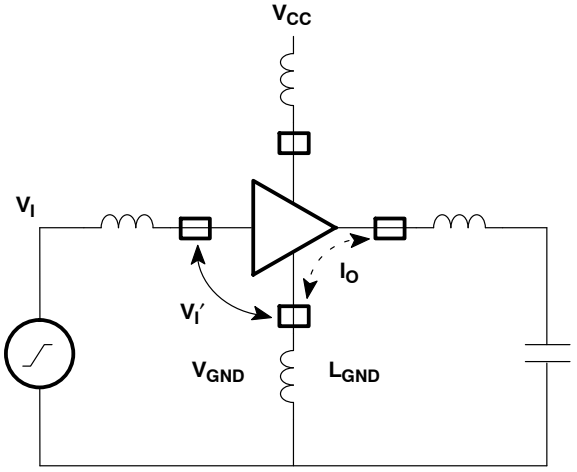

Figure 4. Input/Output Model

Floating Inputs

If a voltage between 0.8 V and 2 V is applied to the input for a prolonged period of time, this situation becomes critical and should not be ignored, especially with higher bit count and more dense packages (SSOP, TSSOP). For example, if an 18-bit transceiver has 36 I/O pins floating at the threshold, the current from V_{CC} can be as high as 150 mA to 200 mA. This is approximately 1 W of power consumed by the device, which leads to a serious overheating problem. This continuous overheating of the device affects its reliability. Also, because the inputs are in the threshold region, the outputs tend to oscillate, resulting in damage to the internal circuit over a long period of time. The data sheet shows the increase in supply current (ΔI_{CC}) when the input is at a TTL level [for ABT V_I = 3.4 V, ΔI_{CC} = 1.5 mA (see Figure 5)]. This becomes more critical when the input is in the threshold region as shown in Figure 6.

These characteristics are typical for all CMOS input circuits, including microprocessors and memories.

For CBT or CBTLV devices, this applies to the control inputs. For FB and GTL devices, this applies to the control inputs and the TTL ports only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)†

PARAMETER		TEST CONDITIONS			MIN	MAX	UNIT
ΔI_{CC}‡	ABT, AHCT	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		1.5	mA
	CBT Control inputs	V_{CC} = 5.5 V,	One input at 3.4 V,	Other inputs at V_{CC} or GND		2.5	
ΔI_{CC}‡	CBTLV Control inputs	V_{CC} = 3.6 V,	One input at 3 V,	Other inputs at V_{CC} or GND		750	μA
ΔI_{CC}‡	LVT	V_{CC} = 3 V to 3.6 V,	One input at V_{CC} – 0.6 V,	Other inputs at V_{CC} or GND		0.2	mA
	LVC, ALVC, LV					0.5	

† Refer to the latest TI data sheets for device specifications.

‡ This is the increase in supply current for each input that is at the specified TTL voltage level rather than V_{CC} or GND.

Figure 5. Examples of Supply-Current Change of the Input at TTL Level as Specified in Data Sheets

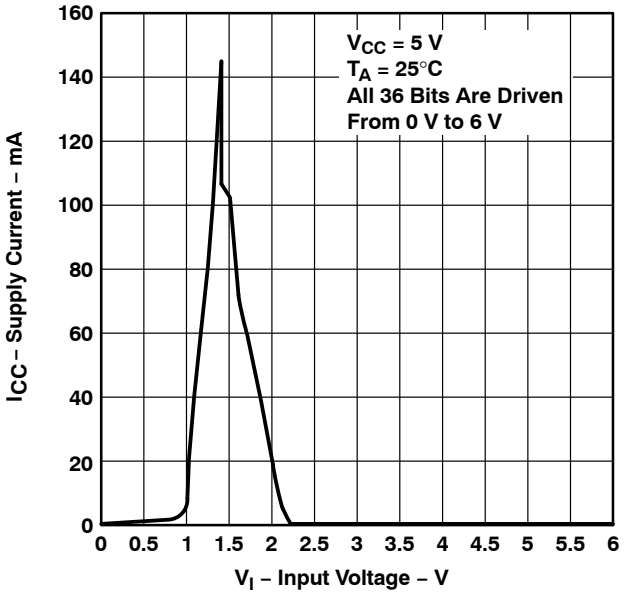

Figure 6. Supply Current Versus Input Voltage (36 Inputs)

As long as the driver is active in a transmission path or bus, the receiver's input is always in a valid state. No input specification is violated as long as the rise and fall times are within the data-sheet limits. However, when the driver is in a high-impedance state, the receiver input is no longer at a defined level and tends to float. This situation can worsen when several transceivers share the same bus. Figure 7 is an example of a typical bus system. When all transceivers are inactive, the bus-line levels are undefined. When a voltage that is determined by the leakage currents of each component on the bus is reached, the condition is known as a *floating state*. The result is a considerable increase in power consumption and a risk of damaging all components on the bus. Holding the inputs or I/O pins at a valid logic level when they are not being used or when the part driving them is in the high-impedance state is recommended.

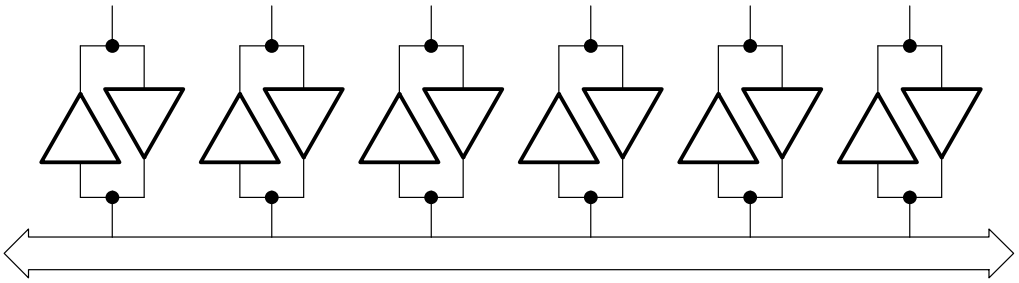

Figure 7. Typical Bidirectional Bus

Recommendations for Designing More-Reliable Systems

Bus Control

The simplest way to avoid floating inputs in a bus system is to ensure that the bus always is either active or inactive for a limited time when the voltage buildup does not exceed the maximum V_{IL} specification (0.8 V for TTL-compatible input). At this voltage, the corresponding I_{CC} value is too low and the device operates without any problem or concern (see Figures 2 and 4).

To avoid damaging components, the designer must know the maximum time the bus can float. First, assuming that the maximum leakage current is $I_{OZ} = 50\ \mu A$ and the total capacitance (I/O and line capacitance) is C = 20 pF, the change in voltage with respect to time on an inactive line that exceeds the 0.8-V level can be calculated as shown in equation 1.

$$\Delta V/\Delta t = \frac{I_{OZ}}{C} = \frac{50\ \mu A}{20\ pF} = 2.5\ V/\mu s \quad (1)$$

The permissible floating time for the bus in this example should be reduced to 320 ns maximum, which ensures that the bus does not exceed the 0.8-V level specified. The time constant does not change when multiple components are involved because their leakage currents and capacitances are summed.

The advantage of this method is that it requires no additional cost for adding special components. Unfortunately, this method does not always apply because buses are not always active.

Pullup or Pulldown Resistors

When buses are disabled for more than the maximum allowable time, other ways should be used to prevent components from being damaged or overheated. A pullup or a pulldown resistor to V_{CC} or GND, respectively, should be used to keep the bus in a defined state. The size of the resistor plays an important role and, if its resistance is not chosen properly, a problem may occur. Usually, a 1-kΩ to 10-kΩ resistor is recommended. The maximum input transition time must not be violated when selecting pullup or pulldown resistors (see Figure 3). Otherwise, components may oscillate, or device reliability may be affected.

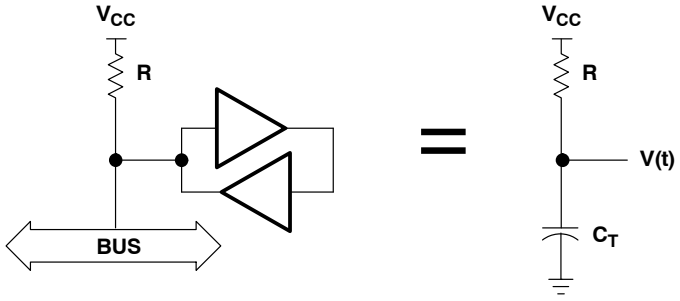

Figure 8. Inactive-Bus Model With a Defined Level

Assume that an active-low bus goes to the high-impedance state as modeled in Figure 8. C_T represents the device plus the bus-line capacitance and R is a pullup resistor to V_{CC}. The value of the required resistor can be calculated as shown in equation 2.

$$V(t) = V_{CC} - [e^{-t/RC_T}(V_{CC} - V_i)] \quad (2)$$

Where:

- $V(t)$ = 2 V, minimum voltage at time t
- V_i = 0.5 V, initial voltage
- V_{CC} = 5 V
- C_T = total capacitance
- R = pullup resistor
- t = maximum input rise time as specified in the data sheets (see Figure 3).

Solving for R, the equation becomes:

$$R = \frac{t}{0.4 \times C_T} \quad (3)$$

For multiple transceivers on a bus:

$$R = \frac{t}{0.4 \times C \times N} \quad (4)$$

Where:

C = individual component and trace capacitance
N = number of components connected to the bus

Assuming that there are two components connected to the bus, each with a capacitance C = 15 pF, requiring a maximum rise time of 10 ns/V and t = 15-ns total rise time for the input (2 V), the maximum resistor size can be calculated:

$$R = \frac{15 \text{ ns}}{0.4 \times 15 \text{ pF} \times 2} = 1.25 \text{ k}\Omega \quad (5)$$

This pullup resistor method is recommended for ac-powered systems; however, it is not recommended for battery-operated equipment because power consumption is critical. Instead, use the bus-hold feature that is discussed in the next section. The overall advantage of using pullup resistors is that they ensure defined levels when the bus is floating and help eliminate some of the line reflections, because resistors also can act as bus terminations.

Bus-Hold Circuits

The most effective method to provide defined levels for a floating bus is to use Texas Instruments (TI™) built-in bus-hold feature on selected families or as an external component like the SN74ACT1071 and SN74ACT1073 (refer to Table 1).

Table 1. Devices With Bus Hold

DEVICE TYPE	BUS HOLD INCORPORATED
SN74ACT1071	10-bit bus hold with clamping diodes
SN74ACT1073	16-bit bus hold with clamping diodes
ABT Widebus+ (32 and 36 bit)	All devices
ABT Octals and Widebus	Selected devices only
AHC/AHCT Widebus	TBA (Selected devices only)
Low Voltage (LVT and ALVC)	All devices
LVC Widebus	All devices

Bus-hold circuits are used in selected TI families to help solve the floating-input problem and eliminate the need for pullup and pulldown resistors. Bus-hold circuits consist of two back-to-back inverters with the output fed back to the input through a resistor (see Figure 9). To understand how the bus-hold circuit operates, assume that an active driver has switched the line to a high level. This results in no current flowing through the feedback circuit. Now, the driver goes to the high-impedance state and the bus-hold circuit holds the high level through the feedback resistor. The current requirement of the bus-hold circuit is determined only by the leakage current of the circuit. The same condition applies when the bus is in the low state and then goes inactive.

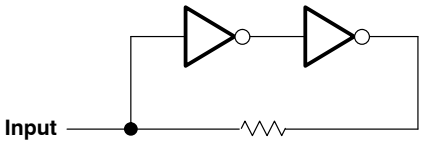

Figure 9. Typical Bus-Hold Circuit

As mentioned previously in this section, TI offers the bus-hold capability as stand-alone 10-bit and 16-bit devices (SN74ACT1071 and SN74ACT1073) with clamping diodes to V_{CC} and GND for added protection against line reflections caused by impedance mismatch on the bus. Because purely ohmic resistors cannot be implemented easily in CMOS circuits, a configuration known as a transmission gate is used as the feedback element (see Figure 10). An n-channel and a p-channel are arranged in parallel between the input and the output of the buffer stage. The gate of the n-channel transistor is connected to V_{CC} and the gate of the p-channel is connected to GND. When the output of the buffer is high, the p-channel is on, and when the output is low, the n-channel is on. Both channels have a relatively small surface area — the on-state resistance from drain to source, R_{dson}, is about 5 kΩ.

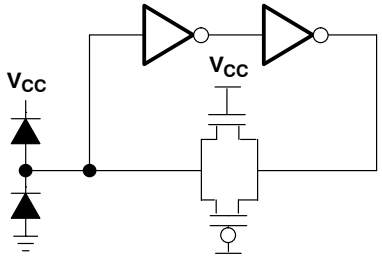

Figure 10. Stand-Alone Bus-Hold Circuit (SN74ACT107x)

Assume that in a practical application the leakage current of a driver on a bus is I_{OZ} = 10 μA and the voltage drop across the 5-kΩ resistance is V_D = 0.8 V (this value is assumed to ensure a defined logic level). Then, the maximum number of components that a bus-hold circuit can handle is calculated as follows:

$$N = \frac{V_D}{I_{OZ} \times R} = \frac{0.8\ V}{10\ \mu A \times 5\ k\Omega} = 16\ \text{components} \quad (6)$$

The 74ACT1071 and 74ACT1073 also provide clamping diodes as an added feature to the bus-hold circuit. These diodes are useful for clamping any overshoot or undershoot generated by line reflections. Figure 11 shows the characteristics of the diodes when the input voltage is above V_{CC} or below GND. At V_I = −1V, the diode can source about 50 mA, which can help eliminate undershoots. This can be very useful when noisy buses are a concern.

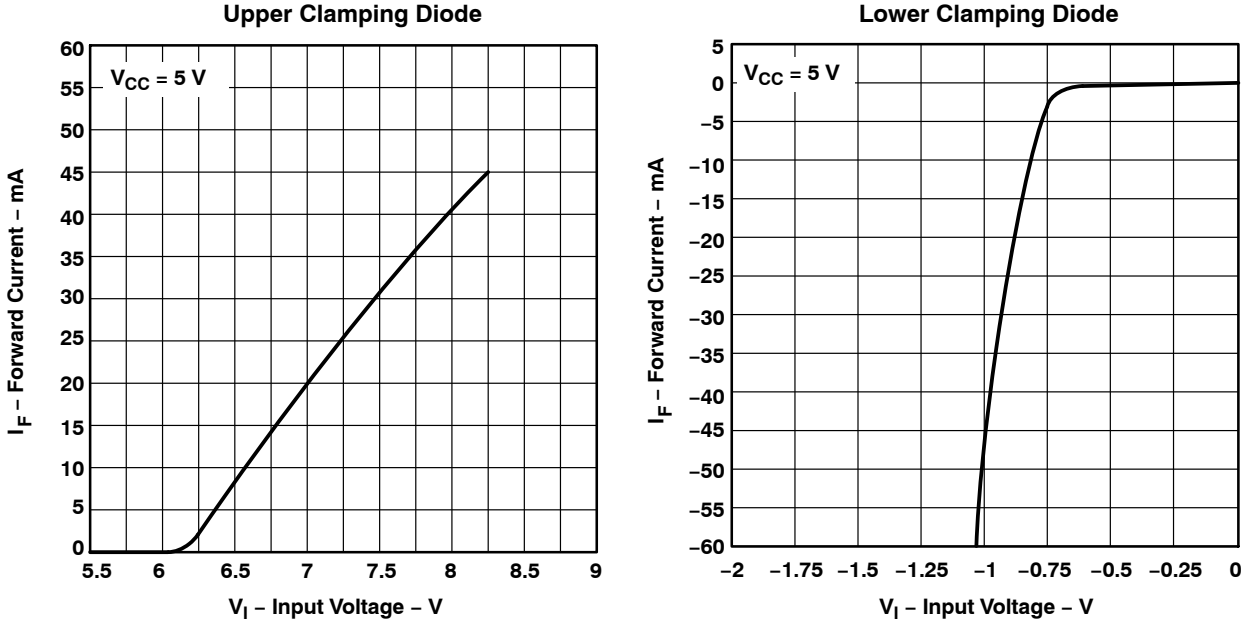

Figure 11. Diode Characteristics (SN74ACT107x)

TI also offers the bus-hold circuit as a feature added to some of the advanced-family drivers and receivers. This circuit is similar to the stand-alone circuit, with a diode added to the drain of the second inverter (ABT and LVT only, see Figure 12). The diode blocks the overshoot current when the input voltage is higher than V_{CC} ($V_I > V_{CC}$), so only the leakage current is present. This circuit uses the device's input stage as its first inverter; a second inverter creates the feedback feature. The calculation of the maximum number of components that the bus-hold circuit can handle is similar to the previous example. However, the advantage of this circuit over the stand-alone bus-hold circuit is that it eliminates the need for external components or resistors that occupy more area on the board. This becomes critical for some designs, especially when wide buses are used. Also, because cost and board-dimension restrictions are a major concern, designers prefer the easy fix: drop-in replaceable parts. TI offers this feature in most of the commonly used functions in several families (refer to Table 1 for more details).

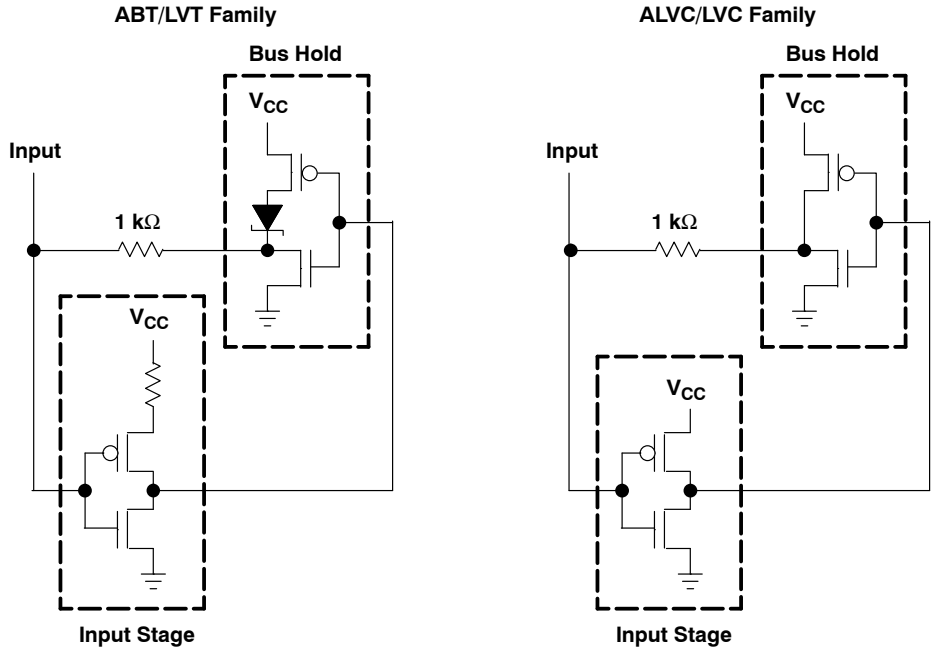

Figure 12. Input Structure of ABT/LVT and ALVC/LVC Families With Bus-Hold Circuit

Figure 13 shows the input characteristics of the bus-hold circuit at 3.3-V and 5-V operations, as the input voltage is swept from 0 to 5 V. These characteristics are similar in behavior to a weak driver. This driver sinks current into the part when the input is low and sources current out of the part when the input is high. When the voltage is near the threshold, the circuit tries to switch to the other state, always keeping the input at a valid level. This is the result of the internal feedback circuit. The plot also shows that the current is at its maximum when the input is near the threshold. $I_{I(hold)}$ maximum is approximately 25 μA for 3.3-V input and 400 μA for 5-V input.

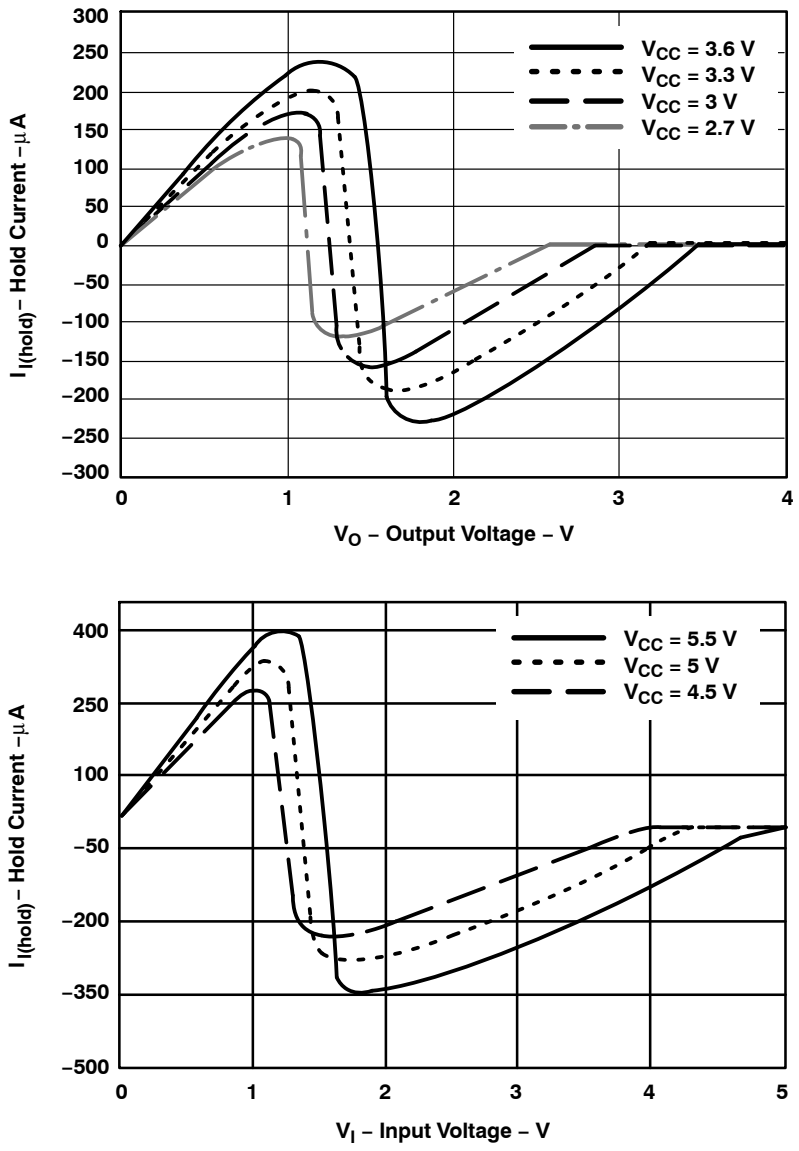

Figure 13. Bus-Hold Input Characteristics

When multiple devices with bus-hold circuits are driven by a single driver, there may be some concern about the ac switching capability of the driver becoming weaker. As small drivers, bus-hold circuits require an ac current to switch them. This current is not significant when using TI CMOS and BiCMOS families. Figure 14 shows a 4-mA buffer driving six LVTH16244 devices. The trace is a 75-Ω transmission line. The receivers are separated by 1cm, with the driver located in the center of the trace. Figure 15 shows the bus-hold loading effect on the driver when connected to six receivers switching low or high. It also shows the same system with the bus-hold circuit disconnected from the receivers. Both plots show the effect of bus hold on the driver's rise and fall times. Initially, the bus-hold circuit tries to counteract the driver, causing the rise or fall time to increase. Then, the bus-hold circuit changes states (note the crossover point), which helps the driver switch faster, decreasing the rise or fall time.

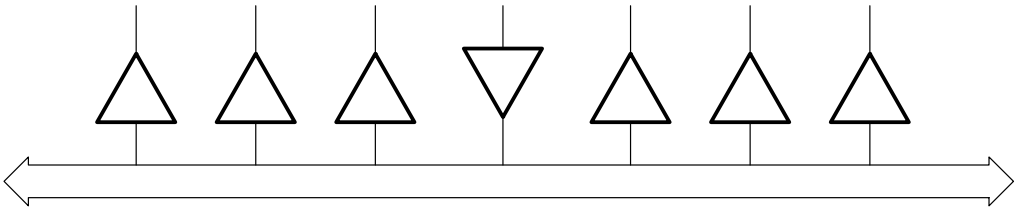

Figure 14. Driver and Receiver System

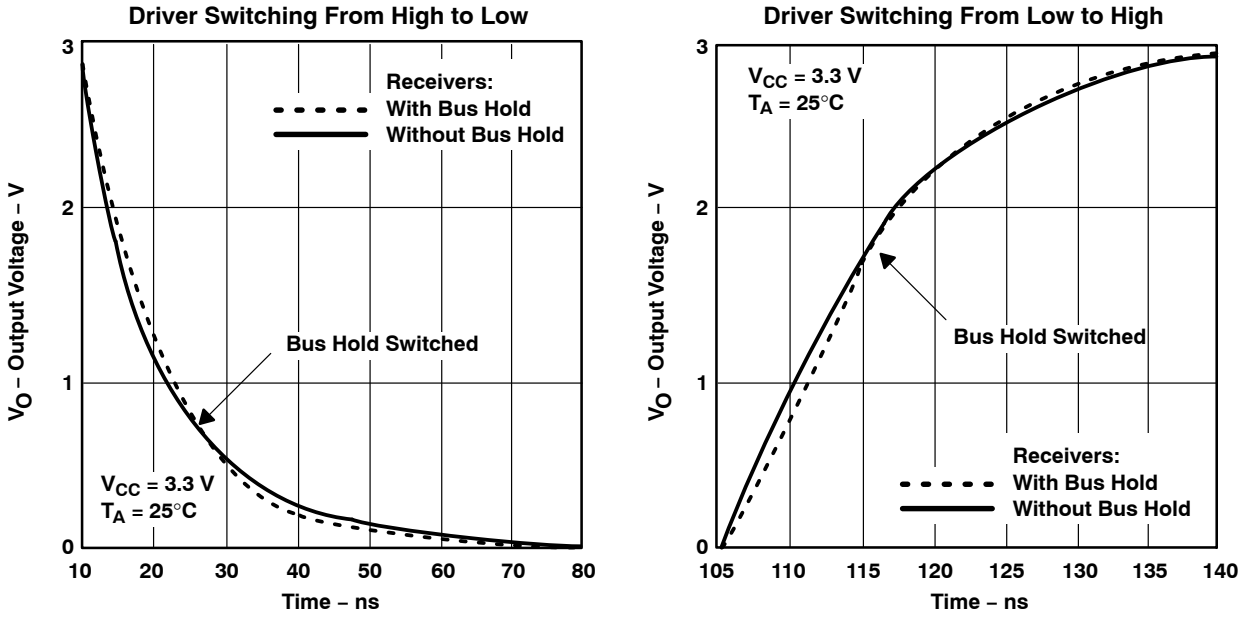

Figure 15. Output Waveforms of Driver With and Without Receiver Bus-Hold Circuit

Figure 16 shows the supply current (I_{CC}) of the bus-hold circuit as the input is swept from 0 to 5 V. The spike at about 1.5-V V_I is due to both the n-channel and the p-channel conducting simultaneously. This is one of the CMOS transistor characteristics.

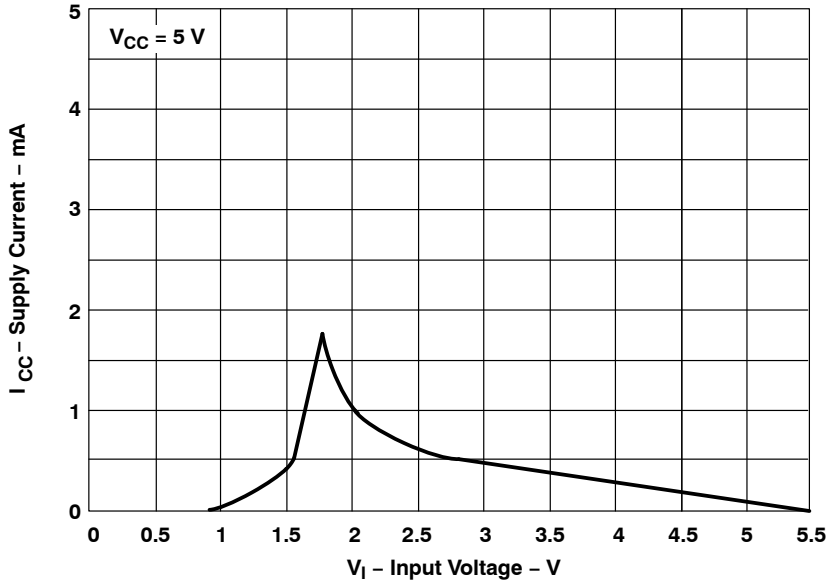

Figure 16. Bus-Hold Circuit Supply Current Versus Input Voltage

The power consumption of the bus-hold circuit is minimal when switching the input at higher frequencies. Figure 17 shows the power consumed by the input at different frequencies, with or without bus hold. The increase in power consumption of the bus-hold circuit at higher frequencies is not significant enough to be considered in power calculations.

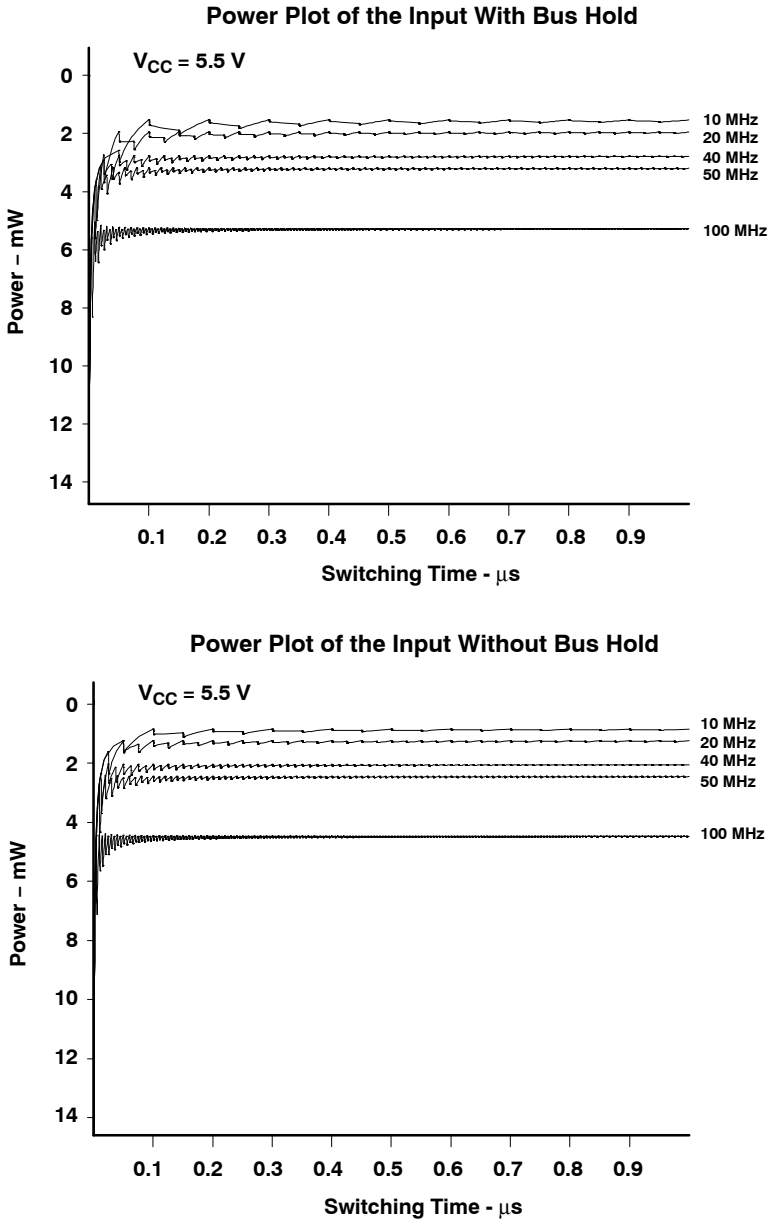

Figure 17. Input Power With and Without Bus Hold at Different Frequencies

Figure 18 shows the data-sheet dc specifications for bus hold. The first test condition is the minimum current required to hold the bus at 0.8 V or 2 V. These voltages meet the specified low and high levels for TTL inputs. The second test condition is the maximum current that the bus-hold circuit sources or sinks at any input voltage between 0 V and 3.6 V (for low-voltage families) or between 0 V and 5.5 V (for ABT). The bus-hold current becomes minimal as the input voltage approaches the rail voltage. The output leakage currents, I_{OZH} and I_{OZL}, are insignificant for transceivers with bus hold because a true leakage test cannot be performed due to the existence of the bus-hold circuit. Because the bus-hold circuit behaves as a small driver, it tends to source or sink a current that is opposite in direction to the leakage current. This situation is true for transceivers with the bus-hold feature only and does not apply to buffers. All LVT, ABT Widebus+, and selected ABT octal and Widebus devices have the bus-hold feature (refer to Table 1 or contact the local TI sales office for more information).

electrical characteristics over recommended operating free-air temperature range (for families with bus-hold feature)†

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
$I_{I(hold)}$	Data inputs or I/Os	LVT, LVC, ALVC	V_{CC} = 3 V	V_I = 0.8 V	75		μA
				V_I = 2 V	−75		
		LVC, ALVC	V_{CC} = 3.6 V,	V_I = 0 to 3.6 V		±500	
		ABT Widebus+ and selected ABT	V_{CC} = 4.5 V	V_I = 0.8 V	100		
				V_I = 2 V	−100		
I_{OZH}/I_{OZL}	Transceivers with bus hold	ABT	This test is not a true I_{OZ} test because bus hold always is active on an I/O pin. Bus hold tends to supply a current that is opposite in direction to the output leakage current.			±1	μA
		LVT, LVC, ALVC					
	Buffers with bus hold	ABT	This test is a true I_{OZ} test since bus hold does not exist on an output pin.			±10	
		LVT, LVC, ALVC				±5	

† Refer to the latest TI data sheets for device specifications.

Figure 18. Example of Data-Sheet Minimum Specification for Bus Hold

Summary

Floating inputs and slow rise and fall times are important issues to consider when designing with CMOS and advanced BiCMOS families. It is important to understand the complications associated with floating inputs. Terminating the bus properly plays a major role in achieving reliable systems. The three methods recommended in this application report should be considered. If it is not possible to control the bus directly, and adding pullup or pulldown resistors is impractical due to power-consumption and board-space limitations, bus hold is the best choice. TI designed bus hold to reduce the need for resistors used in bus designs, thus reducing the number of components on the board and improving the overall reliability of the system.

LVC07A: Applications of an Open-Drain Hex Buffer

SCEA012
April 1999

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Abstract

The Texas Instruments (TI™) LVC07A hex buffer, with open-drain outputs, and its inverting counterpart, LVC06A, operate in the 1.65-V to 3.6-V V_{CC} range, but can accept input voltages up to 5.5 V. Laboratory results show superior propagation times versus competitors, natural I_{off} protection, and output-breakdown capability versus a competitor. Applications of the LVC07A and LVC06A include bus-contention protection, voltage translation, and implementation of active-high wired-AND/active-low wired-OR functions.

Introduction

Low-voltage technology is a growing trend. The need for faster, less expensive, low-power devices is causing a shift to devices that operate at lower voltages. The TI LVC06A and LVC07A address these needs for low-voltage applications. The LVC07A is a noninverting hex buffer with an open-drain output, and the LVC06A is the inverting hex buffer (the LVC07A, plus an extra stage of inversion). These buffers/inverters are designed to operate in the 1.65-V to 3.6-V V_{CC} range; however, inputs and outputs can function with a 5.5-V V_{CC}. Figure 1 is a generalized circuit model of the LVC07A.

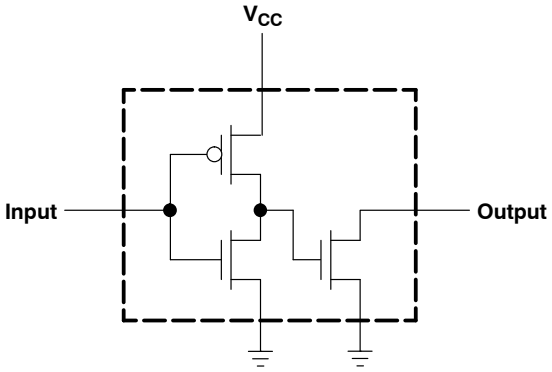


Figure 1. Generalized Circuit Model of LVC07A Showing Open-Drain Structure at Output

The LVC07A can be used in many applications. This application report concentrates on the following points:

- Laboratory results illustrating:
  - Fast propagation times
  - Natural output-leakage-protection capability. The open-drain structure provides natural I_{off} protection.
  - Breakdown features (output-voltage vs output-current plots) of the LVC07A versus a competitor's XXX07A

- Applications of the LVC07A include:
  - Bus-contention control
  - Voltage translation. Because the LVC07A is an open-drain device, it can be used for high-voltage to low-voltage translation, or low-voltage to high-voltage translation (for voltages not exceeding 5.5 V).
  - Implementation of active-high wired-AND or active-low wired-OR functions

Laboratory Results

In the following discussion, the TI LVC07A and two competitors' XXX07A and YYY07 devices are compared. Comparisons include propagation delays obtained from the data sheets and I_{off} capability. The differences between TI, Competitor 1, and Competitor 2 devices are shown in Table 1.

Table 1. Differences Between TI LVC07A and Competitors' Devices

PARAMETER	TI	COMPETITOR 1 XXX07A	COMPETITOR 2 YYY07
Process	CMOS	Bipolar	Bipolar
Operating range V_{CC}	1.65 V to 5.5 V	4.5 V to 5.5 V	4.75 V to 5.25 V
Operating temperature	–40°C to 85°C	0°C to 70°C	0°C to 70°C
I_{CC} maximum specification	10 μA	45 mA	41 mA
I_I maximum specification	5 μA	100 μA	1 mA

Propagation Time

Fast propagation time is very important in designs using integrated circuits. The LVC07A provides very fast propagation times when compared with similar devices from Competitor 1 and Competitor 2. The propagation times were measured (and guardbanded) from 5.5 V to 1.65 V. Table 2 provides the propagation times (t_{pd}) of devices from TI, Competitor 1, and Competitor 2.

Table 2. t_{pd} for TI's LVC07A vs Competitors' Devices

PARAMETER	V_{CC}	TI LVC07A†	COMPETITOR 1 XXX07A‡	COMPETITOR 2 YYY07§	UNIT
		1.65 V TO 5.5 V, –40°C TO 85°C	4.5 V TO 5.5 V, 0°C TO 70°C	4.75 V TO 5.5 V, 0°C TO 70°C	
t_{pd}	5.0 ± 0.5 V	2.6	17.0	30.0	ns
	3.3 ± 0.3 V	2.9	N/A	N/A	
	2.5 ± 0.2 V	2.8	N/A	N/A	
	1.8 ± 0.15 V	3.5	N/A	N/A	

† V_{CC} = 5.0 ± 0.5 V, C_L = 50 pF, and R_L = 250 Ω
V_{CC} = 3.3 ± 0.3 V, C_L = 50 pF, and R_L = 250 Ω
For lower V_{CC}s, C_L = 30 pF and R_L = 250 Ω
‡ C_L =15 pF and R_L = 110 Ω
§ C_L =15 pF and R_L = 100 Ω

Natural Output-Leakage-Protection (I_{off}) Capability

The LVC07A device has no current paths to the V_{CC} pin at V_{CC} = 0 V because it has an open-drain output structure. The open-drain structure provides a high impedance at the output pin when powered off. This is especially important in partial-power-off applications where the device's low I_{off} leakage-current specification is significant. Partial-power-off operation mode is a key issue today in systems design, playing a major role in the personal computer (PC) market and the telecommunications industry.

In Figure 2, the I_{off} characteristic of the LVC07A comes into play when port A goes into the partial-power-off mode. The open-drain output of the LVC07A provides a path of very high resistance to V_{CC} so that the data flow is not disrupted on the bus, i.e., there is a very minimal amount of leakage from the bus to V_{CC}.

The LVC07A isolates port A from port B when it is necessary to power down port A, while leaving port B powered up (partial power down). The I_{off} capability allows port B to operate safely without being degraded by leakage when port A is powered down. This is essential if circuitry must be replaced without turning off the entire system, or if part of the system must be turned off to conserve power.

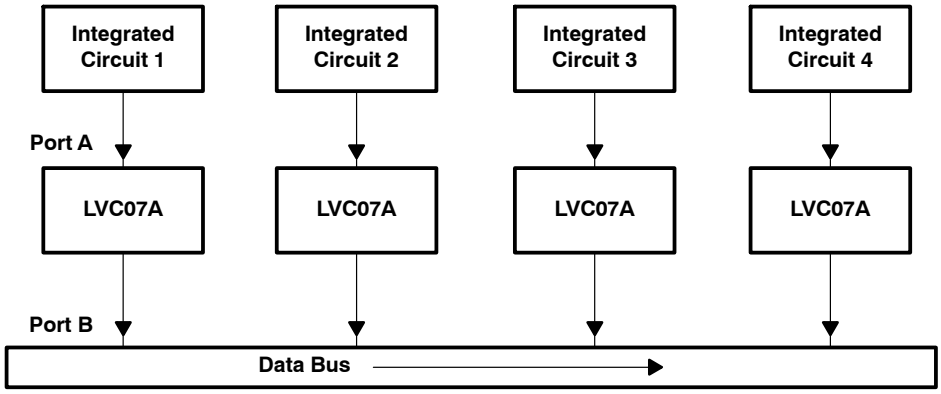


Figure 2. I_{off} Protection Concept Using LVC07A

The I_{off} specification in the data sheet is 10 μA for the LVC family. Figure 3 and Table 3 illustrate the I_{off} performance of the LVC06A and LVC07A. To obtain the data shown in Figure 3, V_{CC} was tied to 0 V and an increasing voltage was swept on the output. Measured values of I_{off} for the LVC06A and LVC07A for different V_{off} voltages are listed in Table 3.

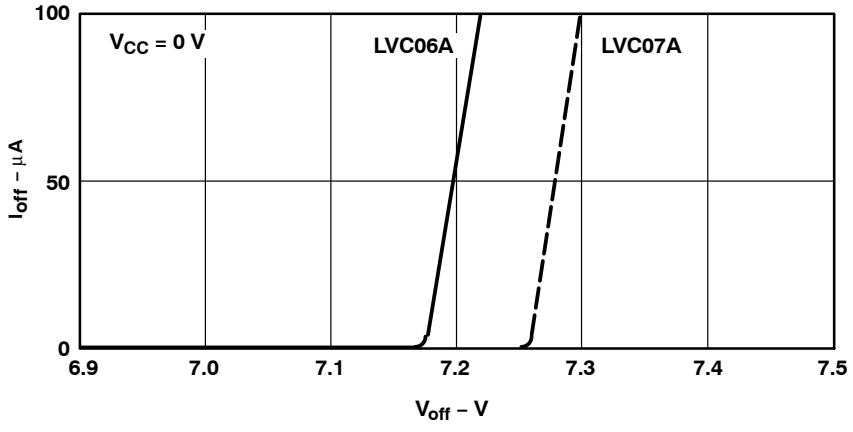


Figure 3. Output Leakage Current vs Output Voltage on Output Pins of LVC06A and LVC07A

Table 3. LVC06A and LVC07A Output Leakage Currents in Off State

V_{off} (V)	I_{off} (nA)	
	LVC06A	LVC07A
0	0.005	0.0021
2.222	1.957	0.4058
2.323	2.463	0.4997
2.424	2.991	0.6215
2.525	3.560	0.7816
2.626	4.201	1.02
3.535	10.85	5.545
3.636	11.96	6.415
5.05	44.64	35.36
5.454	66.75	54.61
5.555	74.11	60.96
5.656	82.55	68.36
6.06	127.1	110.1
6.161	143.6	124.6
6.262	162.5	141.3

Breakdown-Feature Comparison Between LVC07A and Competitor 1 XXX07A

Experiments were conducted on both the LVC07A and the Competitor 1 XXX07A to determine the output-current versus output-voltage characteristics at various V_{CC}s. Plots were made for the worst-case V_{CC} of 5.5 V. These plots illustrate the devices' ability to handle output voltages at the worst-case V_{CC}s. In the case of the LVC07A, the breakdown output voltage (V_{OH}) was 7.39 V for a V_{CC} of 5.5 V (see Figure 4).

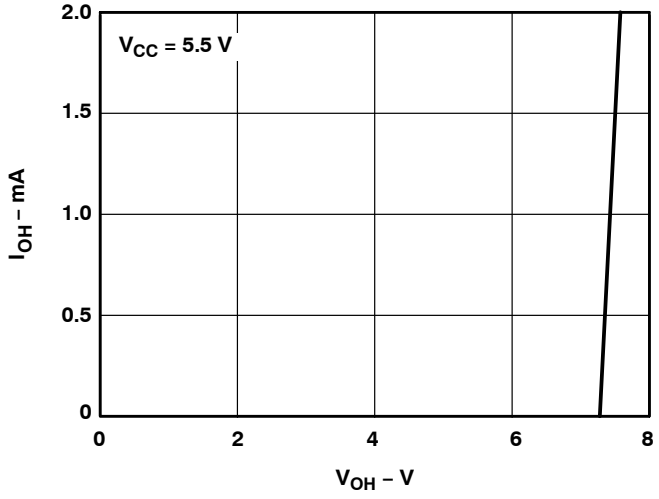


Figure 4. I_{OH} vs V_{OH} for the LVC07A at V_{CC} = 5.5 V

The Competitor 1 XXX07A has better output-breakdown capabilities than the TI device. The output breakdown voltage (V_{OH}) was 16.50 V for a V_{CC} of 5.5 V (see Figure 5).

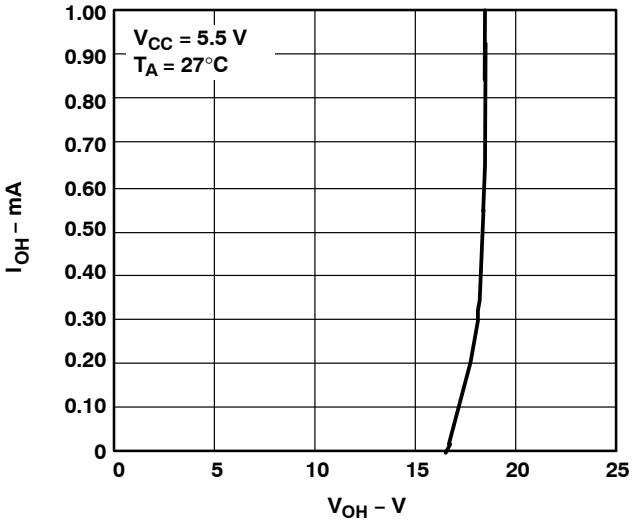


Figure 5. I_{OH} vs V_{OH} for Competitor 1 XXX07A for V_{CC} = 5.5 V

The Competitor 1 XXX07A is better suited for designs where high output voltages are desired and propagation delays are not as important. The TI LVC07A is desirable for designs where the voltage across the LVC07A output structure does not exceed the recommended specification of 5.5 V and *propagation times are important*.

LVC07A Applications

In this section, important applications of the LVC07A are discussed: bus-contention protection, voltage translation, and implementation of active-high wired-AND or active-low wired-OR functions.

Bus-Contention Protection

The open-drain feature of the LVC07A is useful in preventing bus contention. Figure 6 illustrates the concept of bus contention.

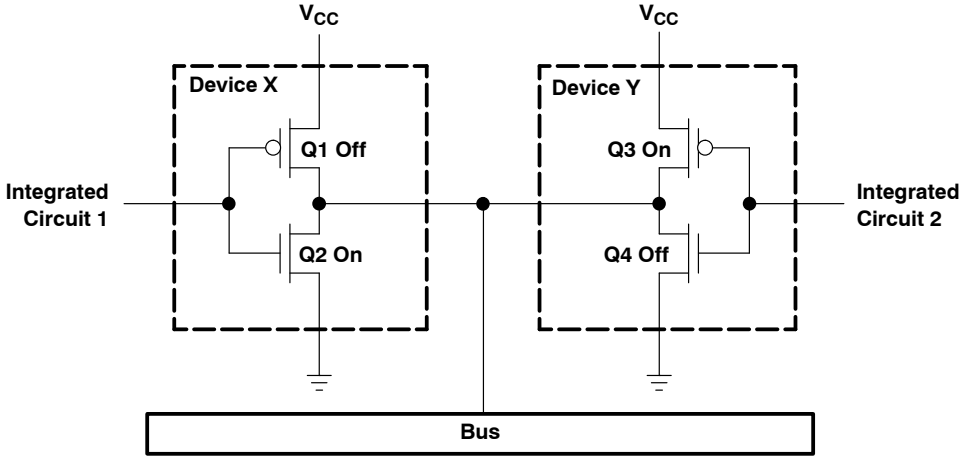


Figure 6. Bus-Contention Example Not Using LVC07A

If Q3 and Q2 were in the on state, a short circuit would be created that would destroy both Q2 and Q3. For example, if V_{CC} = 5 V and the on-state resistance of each transistor is 5 Ω, a current of 0.5 A would flow and easily destroy Q2 and Q3.

However, if the output structures in Figure 6 (devices X and Y) are replaced by the LVC07A (see Figure 7), the problem of bus contention is solved because the current flowing through the pulldown transistor (Q2) is controlled by the size of the resistor at the open-drain output.

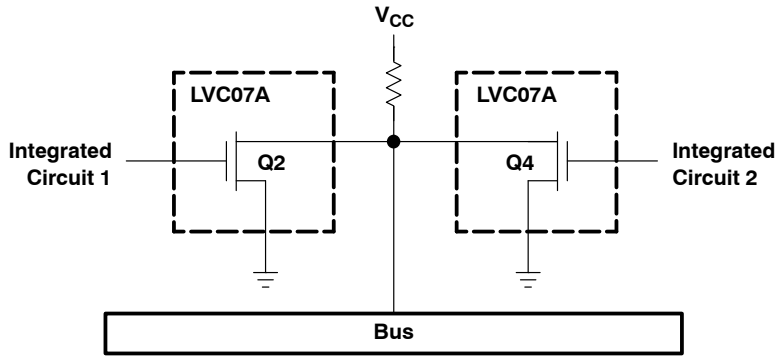


Figure 7. Bus-Contention Protection Using LVC07A

Voltage Translation

Voltage translation is essential for the operation of integrated circuits that have different voltage tolerances. The open-drain structure of the LVC07A presents the designer with the option of a voltage translator. Because the input structure of the LVC07A accepts voltages from 1.65 V to 5.5 V, voltage translation from a lower voltage to a higher voltage, or vice versa, is possible. Without the p-channel pullup on the output structure of the LVC07A, the entire output voltage drops across the n-channel transistor (see Figure 8). With the help of a pullup resistor that is connected to the designer's choice of voltage (not exceeding 5.5 V), voltage translation is achieved because the V_{IH} and V_{IL} levels supplied to the 5-V tolerant device in the circuit shown in Figure 9 are high enough to drive the 5-V tolerant device. If the output structure of the LVC07A were not open drain, the output voltage would drop across the p- and n-channel transistors, and would not provide enough drive to the 5-V-tolerant device.

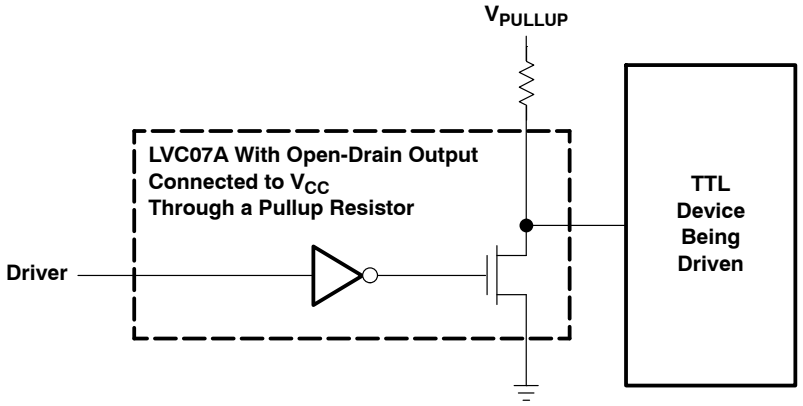


Figure 8. Circuit for Voltage Translation From Lower to Higher Voltages (CMOS to TTL)

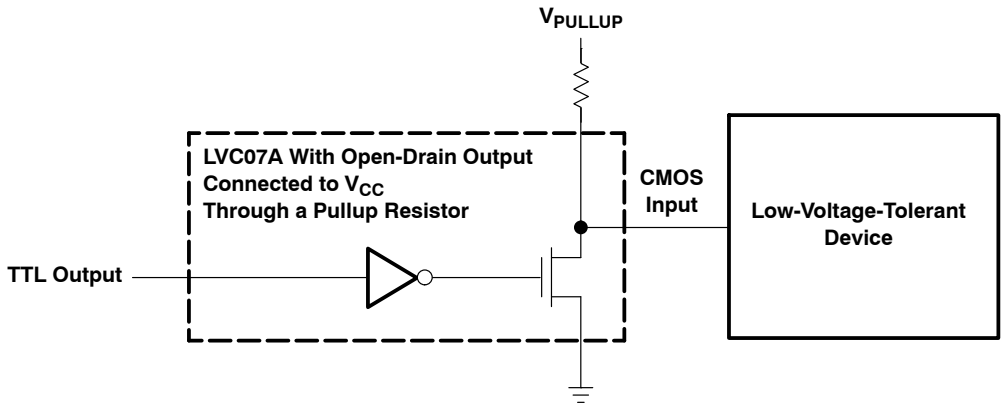


Figure 9. Circuit for Voltage Translation From Higher to Lower Voltages (TTL to CMOS)

The switching standard of 5-V CMOS devices is different than the switching standard for 5-V TTL and 3.3-V TTL devices (see Figure 10).

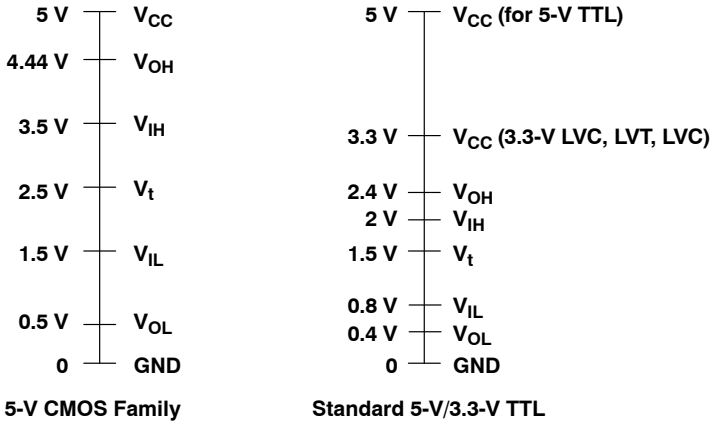


Figure 10. Comparison of 5-V CMOS and 5-/3.3-V TTL Switching Standards

The switching standards shown in Figure 10 clearly indicate that a TTL device cannot drive a CMOS device directly because the V_{IH}, V_{IL}, and V_t levels of the TTL devices are lower than the respective levels of the CMOS device. This problem can be solved by placing the LVC07A between the TTL and the CMOS devices. The pullup resistor from a V_{CC} not exceeding 5.5 V that is connected to the open-drain output of the LVC07A increases the V_{IH} levels sufficiently to drive the CMOS device, as illustrated in Figure 9. The capability of the LVC07A to provide voltage translation (high-to-low or low-to-high voltage) provides an essential function for future-technology integrated circuits using V_{CC} ranges of 1.8 V and below.

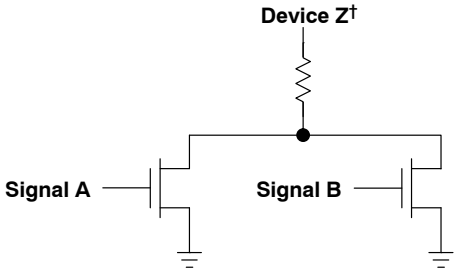
The voltage translation provided by the LVC07A also can be used between CMOS ports. Table 4 illustrates parameters necessary for voltage translation between two devices, A and B. Appropriate V_{CC}s (device A) and pullup voltages (applied on the output structure of the LVC07A) are included Table 4.

Table 4. Requirements for Voltage Translation Between Devices A and B

DEVICE A	DEVICE B	V_{CC}	V_{PULLUP}
5-V TTL	3.3-V TTL = 3.3-V CMOS	3.3 V	3.3 V
3.3-V TTL = 3.3-V CMOS	5-V TTL	3.3 V	5.5 V
2.5-V CMOS	5-V TTL	2.5 V	5.5 V
1.8-V CMOS	3.3-V/5-V TTL	1.8 V	3.3 V/5.5 V
1.5-V CMOS	3.3-V/5-V TTL	1.5 V	3.3 V/5.5 V

Implementation of Active-High Wired-AND or Active-Low Wired-OR Functions

Another useful function of the LVC07A open-drain feature is to provide active-high wired-AND or active-low wired-OR functions (see Figure 11).



† Open-drain structures of the LVC07A are connected together to provide either an active-high wired-AND or an active-low wired-OR function, depending on signal-A and signal-B levels.

Figure 11. Implementation of Active-High Wired-AND or Active-Low Wired-OR Function

Summary

The LVC07A hex buffer addresses requirements of today's low-voltage technology. The advantages of the LVC07A discussed in this application report are:

- Functionality in the 1.65-V to 5.5-V region
- Capability to provide voltage translation between CMOS and TTL or between TTL and CMOS devices
- Bus-contention protection
- Natural output-leakage (I_{off}) protection
- Provision for implementation of active-high wired-AND or active-low wired-OR functions

All of these characteristics make the LVC07A an ideal hex buffer/driver for designs involving PC motherboards and other designs in which signals must be translated between TTL and CMOS devices.

Acknowledgments

The authors of this application report are Hari Garimella, James W. Johnson, and Michael R. Brown. James (Jim) W. Johnson passed away prior to the publication of this application report. Jim was a key contributor in the success of the TI Logic New Products Engineering group for several years. On behalf of Jim's family, friends, and colleagues, the authors would like to acknowledge his extensive contributions in the technical field at TI.

In addition, the authors would like to thank the following people for assistance during the writing of this application report: Mac McCaughey, Ramzi Ammar, and Nalin Yogasundram.

Glossary

A

Active-high wired-AND function	AND function in which one of the inputs is a constant logic 1
Active-low wired-AND function	OR function in which one of the inputs is a constant logic 0. It provides the same logic function as the active-high wired-AND function.

I

I_{off}	Specification used for partial-power-off applications. I_{off} is the leakage current through the output pin when V_{CC} is tied to ground and a voltage is applied at the output pin.

O

Open-drain output	Output that does not have a pullup transistor (p-channel)

P

Partial power off	System function in which it is desired to power off part of the system to conserve power

V

Voltage translation	Capability of transmitting a signal from a device with a low voltage tolerance to a device with a high voltage tolerance, or vice versa

Logic Solutions for IEEE Std 1284

SCEA013
June 1999

TEXAS INSTRUMENTS

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Abstract

Since the creation of IEEE Std 1284, designers have been using this signaling method to interface between the personal computer and peripheral devices. Bulky discrete components, such as termination and pullup resistors and capacitors, were used extensively. To integrate into single-chip solutions that comply with IEEE Std 1284, Texas Instruments (TI™) offers three bus-interface devices that provide board-area savings and flexible level-type selection.

Introduction

This application report presents a brief overview of IEEE Std 1284-1994, provides information on each device available from TI that is a bus-interface solution for this standard, and discusses how to use the devices in applications. TI offers the SN74ACT1284, which is a 7-bit bus-interface transceiver, and the SN74LVC161284 and SN74LV161284, which are 19-bit bus-interface transceivers, as discrete IEEE Std 1284 bus-interface solutions.

Brief Overview of IEEE Std 1284

IEEE Std 1284, “Standard Signaling Method for a Bidirectional Parallel Peripheral Interface for Personal Computers,” is a high-speed, high-integrity parallel-port method for a bidirectional peripheral interface for personal computers. This standard was developed to provide an open path for communications between computers and peripherals. Furthermore, it recommends new electrical interfaces, cabling, and interface hardware that provides improved performance, while retaining backward compatibility.

Purpose and Benefits of IEEE Std 1284

With increased technology development in the personal computer (PC), a need for improved parallel-port performance has emerged. Pre-existing methods used a wide variety of hardware and software products, each with unique and incompatible signaling schemes. Using existing parallel-port architecture, the maximum data transfer rate is about 150 kbyte/s, and external cables are limited to 6 feet.

IEEE Std 1284 was created because of the need for an existing defined standard for bidirectional parallel communication between the PC and printing peripherals. Being backward compatible with the old Centronics specifications, this standard offers more functionality and performance for new PC and peripheral products. Data rates are increased to greater than 1Mbyte/s and maximum cable length is increased to 32 feet for the defined cable type.

IEEE Std 1284 Data Transfer Modes

IEEE Std 1284 defines five modes of data transfer. Not all modes are required in all peripherals; forward is defined as data transfer from host to peripheral, and reverse is defined as data transfer from peripheral to host. The bidirectional mode provides both forward and reverse transfer mode within the same operational mode. The modes are:

- Compatibility Mode: This is the basic mode of operation for all parallel communications. It is asynchronous, byte wide, forward direction, and offers 50-kbyte/s to 150-kbyte/s data-transfer rate.
- Nibble Mode: This asynchronous, reverse-channel mode provides two sequential, 4-bit nibbles to the host. It is used with the compatibility mode to implement a bidirectional channel. The data transfer rate is the same as in the compatibility mode.
- Byte Mode: This mode allows the transfer of data in the reverse direction if the data lines are bidirectional. The data transfer rate is the same as in the compatibility and nibble modes.
- Enhanced Parallel Port (EPP): This mode allows high-speed transfers of bytes in either direction. EPP is ideal for real-time-controlled peripherals, such as network adapters, data acquisition, portable hard drives, and other devices.
- Extended Capabilities Port (ECP): The ECP protocol was proposed as an advanced mode for communication with printer and scanner peripherals. Like the EPP protocol, ECP provides a high-performance, bidirectional communication path between the host and peripheral. ECP and EPP modes are ten times faster than the compatibility, nibble, and byte modes.

IEEE Std 1284 Driver Specification

IEEE Std 1284 specifies characteristics of parallel-port drivers and receivers, and describes two types of interfaces:

- Level I (open drain): Level I devices are designed to be consistent with the pre-existing installed devices. Applications using Level I should not be operated in the high-speed advanced modes, but should take advantage of reverse-channel capabilities of the standard.
- Level II (totem pole): Level II devices have stronger drivers and inputs with hysteresis. They are designed to operate in the advanced mode where a longer cable and higher data rates prevail. Level II offers better performance, while remaining compatible with the original interface.

IEEE Std 1284 Connectors

Three interface connectors defined in IEEE Std 1284 are:

- IEEE Std 1284-A: This is the existing DB25 connector, used primarily on the host side.
- IEEE Std 1284-B: This is the existing 36-pin, 0.085-inch centerline connector, used only on the peripheral side.
- IEEE Std 1284-C: This connector is a new 36-pin, 0.050-inch centerline connector recommended by IEEE Std 1284 that is used on both host and peripheral sides.

Since A- and B-type connectors do not have the same number of pins, Figures 1 and 2 detail pin connections for communication between the PC and peripheral. These connections (A host and B peripheral; A host and C peripheral) are the most commonly accepted in the industry.

As recommended in IEEE Std 1284, using the C-type connector on both host and peripheral sides provides a high-speed, high-integrity parallel port for reliable bidirectional communication. Figure 3 shows the straightforward connection between the two ports.

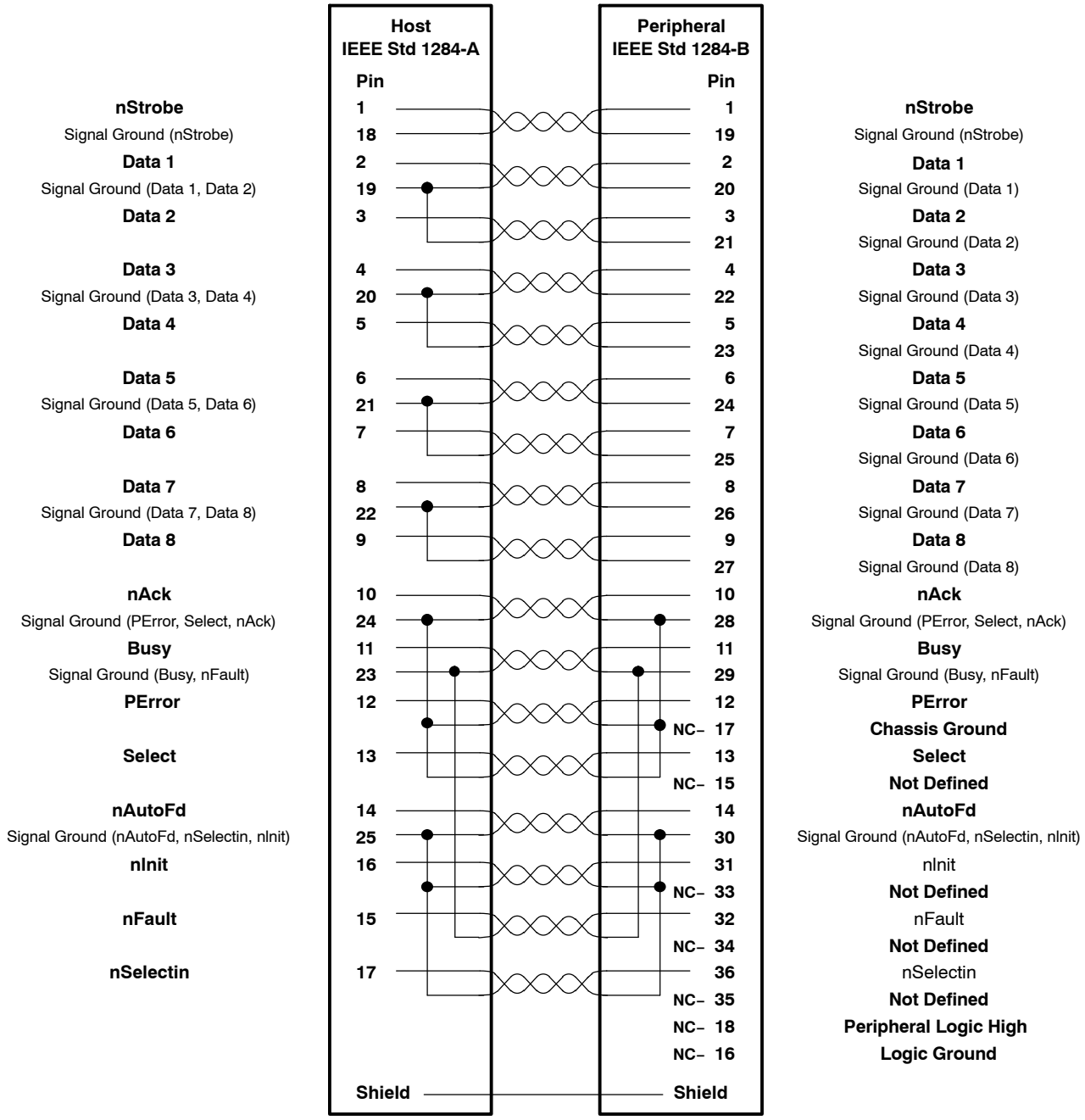


Figure 1. IEEE Std 1284-A (Host) to IEEE Std 1284-B (Peripheral) Wiring Diagram

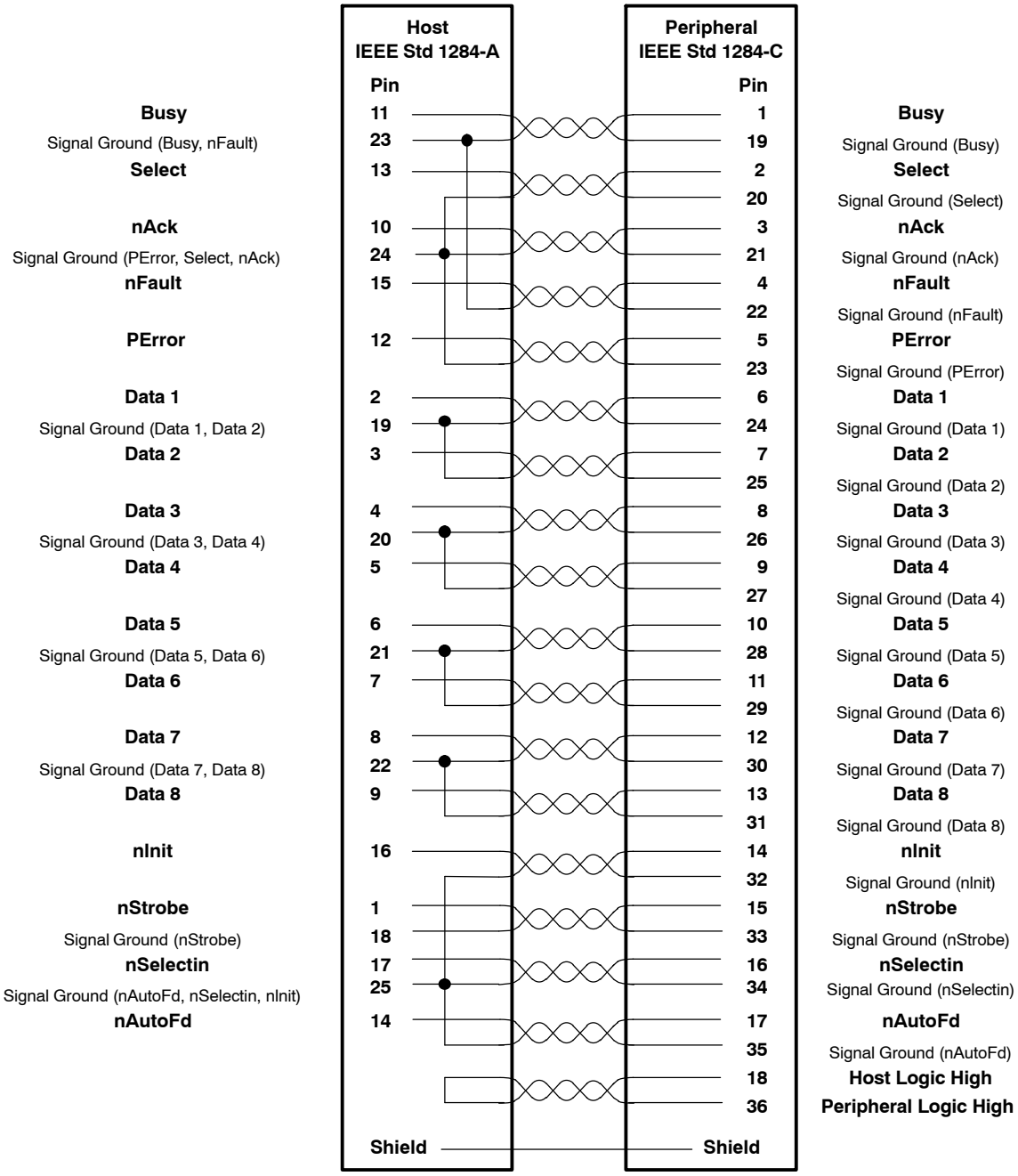


Figure 2. IEEE Std 1284-A (Host) to IEEE Std 1284-C (Peripheral) Wiring Diagram

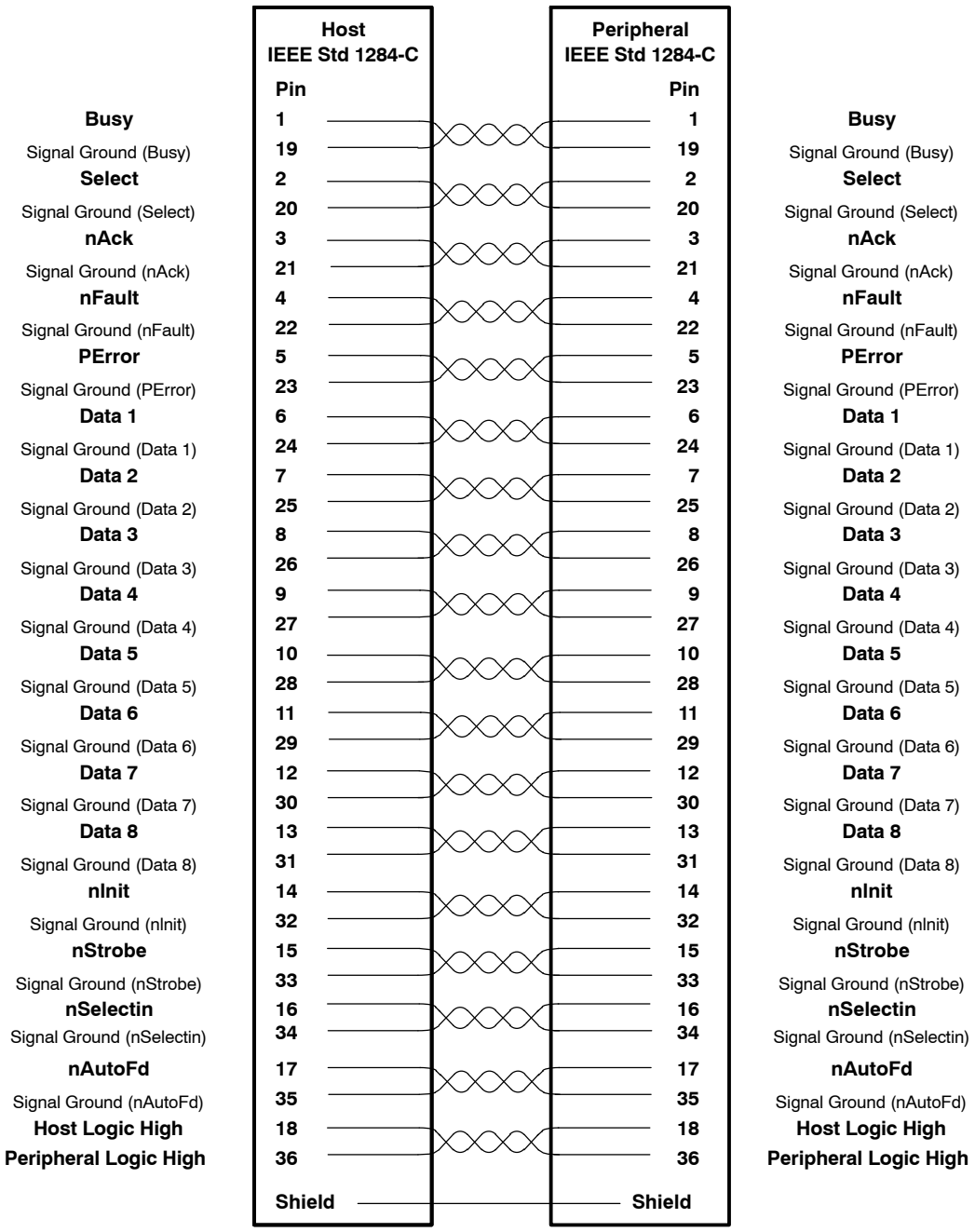


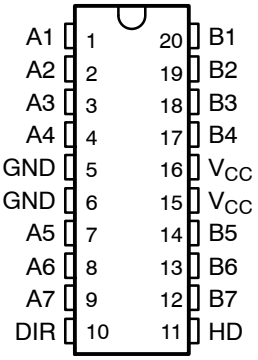
Figure 3. IEEE Std 1284-C (Host) to IEEE Std 1284-C (Peripheral) Wiring Diagram

Device Information

TI offers three bus-driver solutions that comply with the IEEE Std 1284 specification: SN74ACT1284, SN74LVC161284, and SN74LV161284. These devices can be used in the ECP mode to provide an asynchronous, bidirectional, parallel peripheral interface for personal computers. These devices allow data transmission in the A-to-B direction or B-to-A direction, depending on the logic level of the direction-control (DIR) pin. The output drive mode is determined by the high-drive (HD) control pin. HD enables the outputs (B and Y side only) to switch from open collector to totem pole. The A side outputs have totem-pole outputs only. This meets the drive requirements as specified in the IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) parallel peripheral-interface specifications. All these devices have two supply voltages, one for the cable side, and the other for the logic side. To reduce the chance of faulty signals being transferred over the system's parallel port, all these devices feature a finely tuned Output Edge-Rate Control (OEC™) circuit and an enhanced input hysteresis circuit.

The pinouts and function tables of these devices are given in Figures 4 and 5 and in Tables 1 and 2, respectively.

SN54ACT1284 . . . J OR W PACKAGE
SN74ACT1284 . . . DB, DW, N, OR PW PACKAGE
(TOP VIEW)



SN54ACT1284 . . . FK PACKAGE
(TOP VIEW)

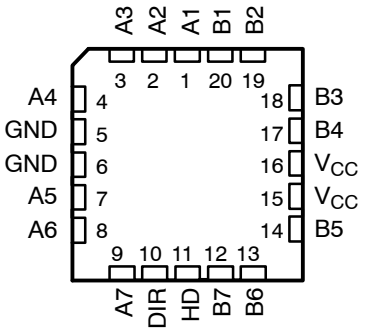


Figure 4. Pinout of SN54/SN74ACT1284

OEC is a trademark of Texas Instruments Incorporated.

DGG OR DL PACKAGE
(TOP VIEW)

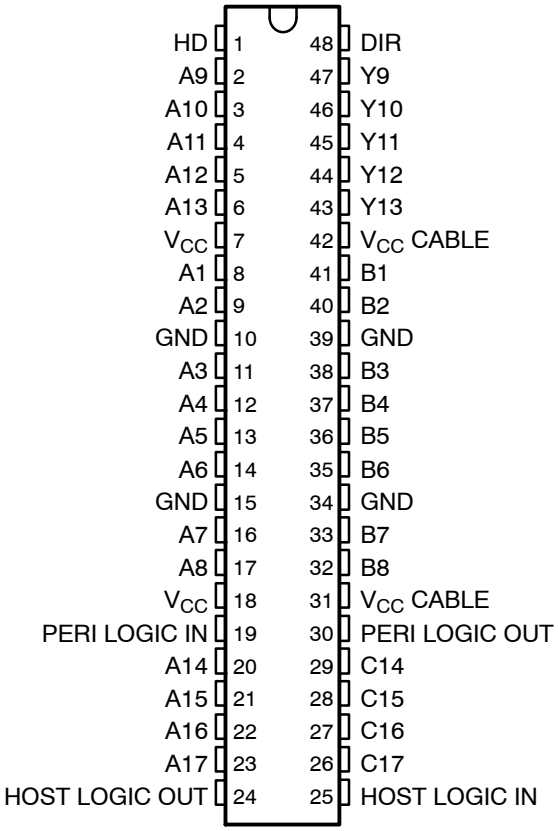


Figure 5. Pinout of SN74LV161284 and SN74LVC161284

Table 1. Function Table for SN74ACT1284

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A to B: Bits 5, 6, 7
		Totem pole	B to A: Bits 1, 2, 3, 4
L	H	Totem pole	B to A: Bits 1, 2, 3, 4 and A to B: Bits 5, 6, 7
H	L	Open drain	A to B: Bits 1, 2, 3, 4, 5, 6, 7
H	H	Totem pole	A to B: Bits 1, 2, 3, 4, 5, 6, 7

Table 2. Function Table for SN74LV161284 and SN74LVC161284

INPUTS		OUTPUT	MODE
DIR	HD		
L	L	Open drain	A9–A13 to Y9–Y13 and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	B1–B8 to A1–A8 and C14–C17 to A14–A17
L	H	Totem pole	B1–B8 to A1–A8, A9–A13 to Y9–Y13, PERI LOGIC IN to PERI LOGIC OUT, and C14–C17 to A14–A17
H	L	Open drain	A1–A8 to B1–B8, A9–A13 to Y9–Y13, and PERI LOGIC IN to PERI LOGIC OUT
		Totem pole	C14–C17 to A14–A17
H	H	Totem pole	A1–A8 to B1–B8, A9–A13 to Y9–Y13, C14–C17 to A14–A17, and PERI LOGIC IN to PERI LOGIC OUT

Features and Benefits

Tables 3 and 4 summarize the features and corresponding benefits for three TI devices that are IEEE Std 1284 compliant.

Table 3. Features and Benefits of the SN74ACT1284

FEATURES	BENEFITS
Flow-through architecture	Optimizes printed circuit board layout
Center-pin V_{CC} and GND configuration	Minimizes high-speed switching noise
Software configurable to IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) electrical specifications	Easy level-type selection
A-to-B and B-to-A transmission for bits 1, 2, 3, and 4	Configurable data flow

Table 4. Features and Benefits of the SN74LV161284 AND SN74LVC161284

FEATURES	BENEFITS
Integrated 1.4-kΩ pullup resistors on all open-drain cable-side outputs†	Eliminates the need for discrete resistors
Software-configurable to IEEE Std 1284-I (level-1 type) and IEEE Std 1284-II (level-2 type) electrical specifications	Easy level-type selection
Flow-through architecture	Optimizes printed circuit board layout
V_{CC}CABLE from 3 V to 5.5 V, V_{CC} from 3 V to 3.6 V (SN74LVC161284 only)	Wide voltage range
4.5-V to 5.5-V V_{CC} and V_{CC}CABLE (SN74LV161284 only)	Single supply
Eight bidirectional data bits, five cable drivers and four receivers	Complete peripheral solution
Integrated PMOS transistors between V_{CC} and cable-side data and receiver outputs‡	Avoids back-drive current
Integrated 33-Ω termination resistors to all cable-side outputs	Eliminates the need for discrete resistors
Dedicated buffers for Peripheral Logic High and Host Logic High signals§	Complete peripheral solution

† Pullup resistors ensure operation with a Level I compatible device and provide sufficient voltage and timing margins as specified by IEEE Std 1284. In addition, the pullup resistors add margin for noisy cable environments.

‡ Avoiding back-drive current keeps the peripheral from being powered up by the host when the peripheral is off and allows for a 5-V system to be connected to the cable side. Laboratory experiments using TI's SN74LVC161284 and a competitor's 1284 transceiver show how the two devices compare, while simulating a typical PC-to-peripheral application. In this situation, a '161284 is used on the peripheral.

§ Hosts and peripherals indicate their readiness to communicate by asserting Host Logic High and Peripheral Logic High, respectively. All hosts and peripherals with IEEE Std 1284-C connectors shall provide Host Logic High and Peripheral Logic High. Because devices with IEEE Std 1284-A or IEEE Std 1284-B connectors may or may not support Host Logic High or Peripheral Logic High, there are no reliable means of initiating a transfer.

Performance Comparison

As the Super I/O transmits a high level to the peripheral via the cable, the ’161284 on the printer side receives the signal because it is configured as a receiver. In TI’s laboratory, the host PC side is simulated by driving +5 V to the ’161284 receiver. Any back-drive current is measured and plotted as the peripheral device is being powered down and is receiving a high-level input (H level). The experiment is repeated for the competitor’s part. Figure 6 shows the test setup. Results, plotted on Figures 7, 8, 9, and 10, show the superior performance of the TI SN74LVC161284 vs a competitor’s equivalent device.

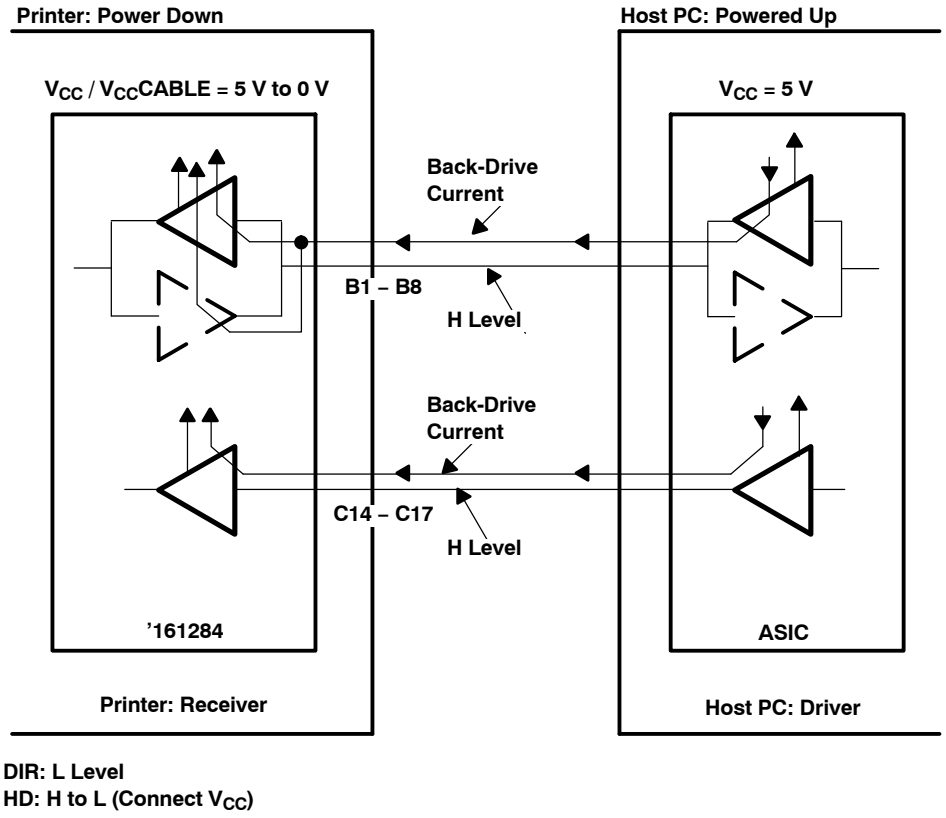


Figure 6. Test Setup for Back-Driving Current

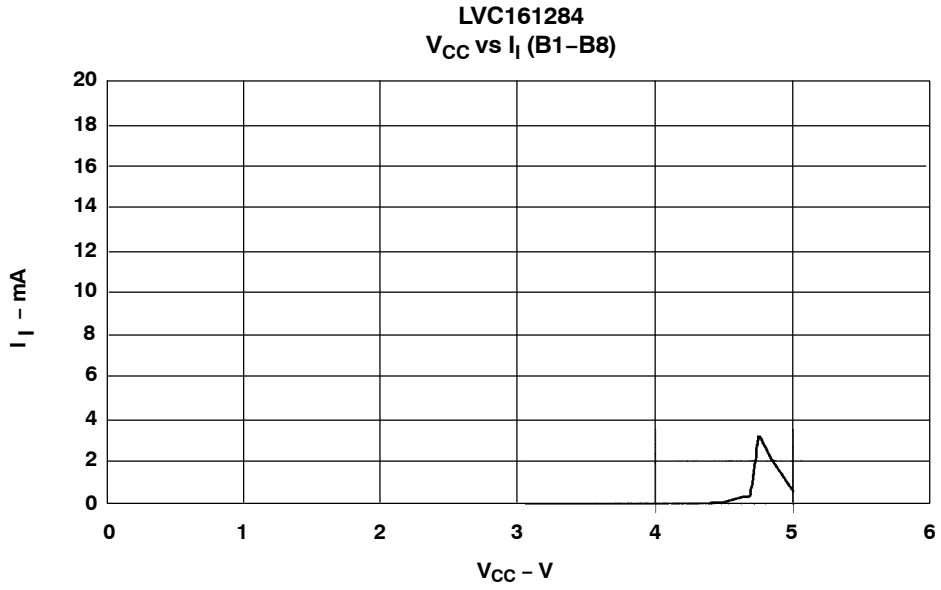


Figure 7. Back-Driving Current for LVC161284 for B1 to B8. (V_{CC} = V_{CC}CABLE = 5 V to 0 V)

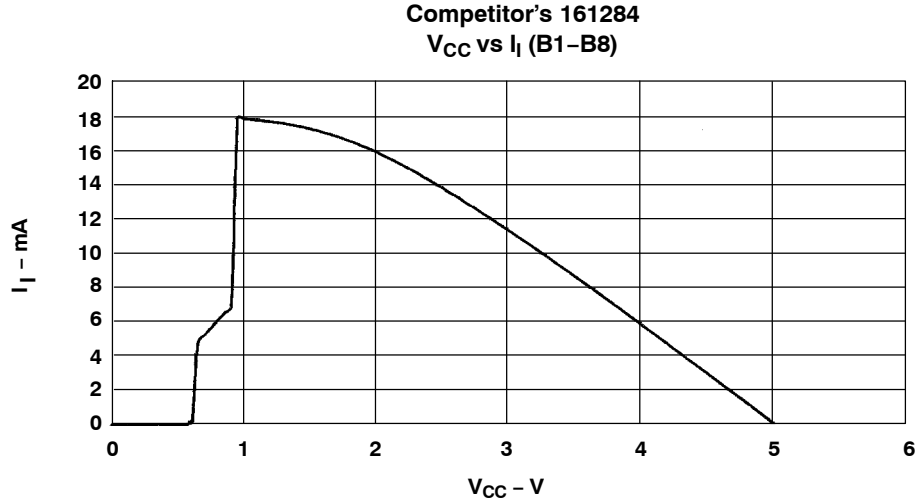


Figure 8. Back-Driving Current for Competitor's 161284 for B1 to B8. (V_{CC} = V_{CC}CABLE = 5 V to 0 V)

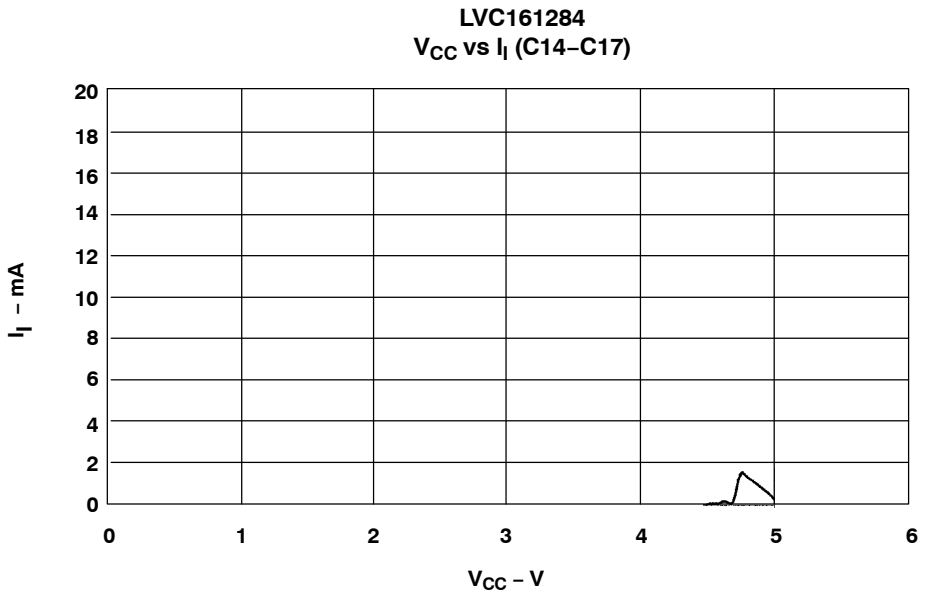


Figure 9. Back-Driving Current for LVC161284 for C14 to C17. (V_{CC} = V_{CC}CABLE = 5 V to 0 V)

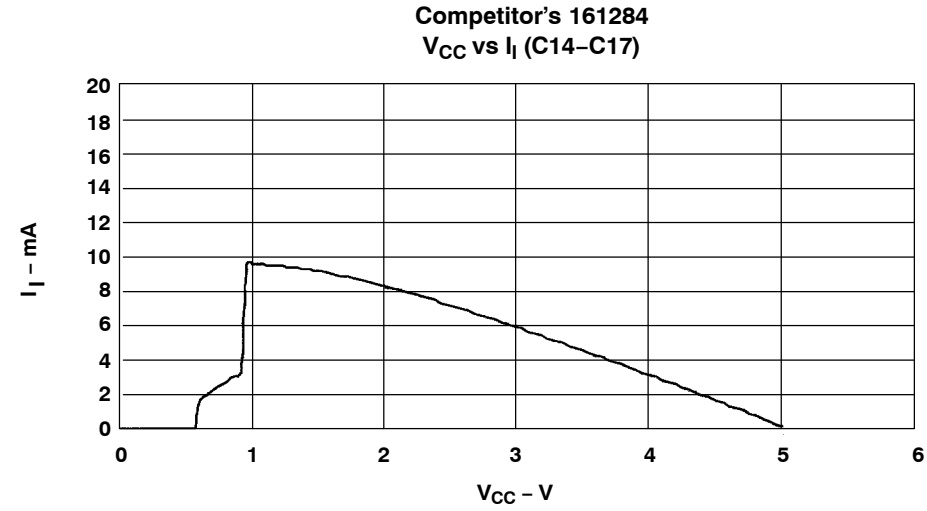


Figure 10. Back-Driving Current for Competitor's 161284 for C14 to C17. (V_{CC} = V_{CC}CABLE = 5 V to 0 V)

Table 5 provides a comparison of characteristics of the SN74ACT184, SN74LVC161284, and SN74LV161284 devices.

Table 5. Comparisons of Device Characteristics

DEVICE CHARACTERISTICS	SN74ACT1284	SN74LVC161284	SN74LV161284
Number of pins	20	48	48
Number of data bits	Four bidirectional bits	Eight bidirectional bits	Eight bidirectional bits
Number of control and status bits	Three unidirectional bits for control or status	Five driver and four receiver for status and control bits, one receiver for host logic, and one driver for peripheral logic	Five driver and four receiver for status and control bits, one receiver for host logic, and one driver for peripheral logic
Supply voltage	4.7 V ≤ V_{CC} ≤ 5.5 V	3 V ≤ V_{CC} ≤ 3.6 V 3 V ≤ V_{CC}CABLE ≤ 5.5 V V_{CC}CABLE ≥ V_{CC}	4.5 V ≤ V_{CC} ≤ 5.5 V 4.5 V ≤ V_{CC}CABLE ≤ 5.5 V V_{CC}CABLE ≥ V_{CC}
Temperature range	0°C to 70°C		−40°C to 85°C
Available package types	SOIC (DW) SSOP (DB) TSSOP (DW) DIP (N)	Plastic 300-mil Shrink Small-Outline (DL) Thin Shrink Small-Outline (DGG)	Plastic 300-mil Shrink Small-Outline (DL) Thin Shrink Small-Outline (DGG)
Input hysteresis	All inputs have hysteresis to provide noise margin		
Pullup resistors	No pullup resistor is included	1.4-kΩ pullup resistor is included in all cable-side pins, except for Host Logic and Peripheral Logic	1.4 k-Ω pullup resistor is included in all cable-side pins, except for Host Logic and Peripheral Logic
Termination resistors	No internal series termination resistor included	33-Ω series resistor integrated into cable-side data output	33-Ω series resistor integrated into cable-side data output

Application Information

Why the IEEE Std 1284 Driver is Needed

Before IEEE Std 1284, there was no defined electrical specification for driver, receiver, termination, and capacitance requirements that required compatibility between devices. Host adapters and peripherals were built with different pullup values on the control lines, open-collectors or open-drains, and totem-pole drivers for the data and control lines. Often, up to 10,000-pF capacitors on the data and strobe lines were used. Figure 11 shows a typical pre-IEEE Std 1284 application host solution. All capacitors and pullup and termination resistors are replaced by TI's discrete integrated bus-interface solution (dashed box around components in Figure 11) that provides efficient designs of parallel-port communication between the PC and peripheral.

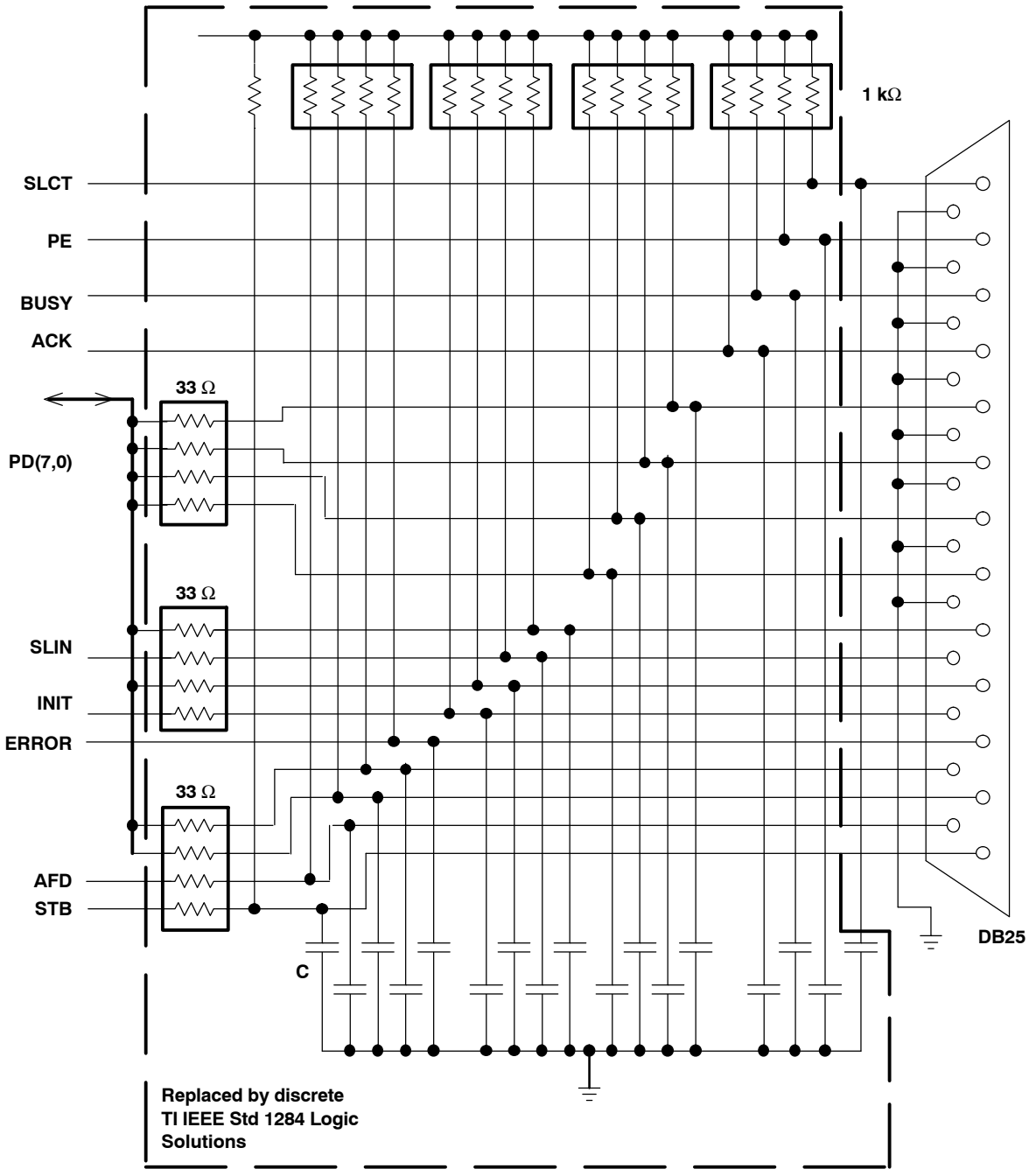


Figure 11. Pre-IEEE Std 1284 Parallel-Port Host Solution

IEEE Std 1284 Parallel-Port Solutions Using TI Bus-Interface Devices

Figure 12 is a basic block diagram of an IEEE Std 1284 parallel port. Only one SN74LV161284 or SN74LVC161284 is used per side, but two SN74ACT1284 devices are required per port.

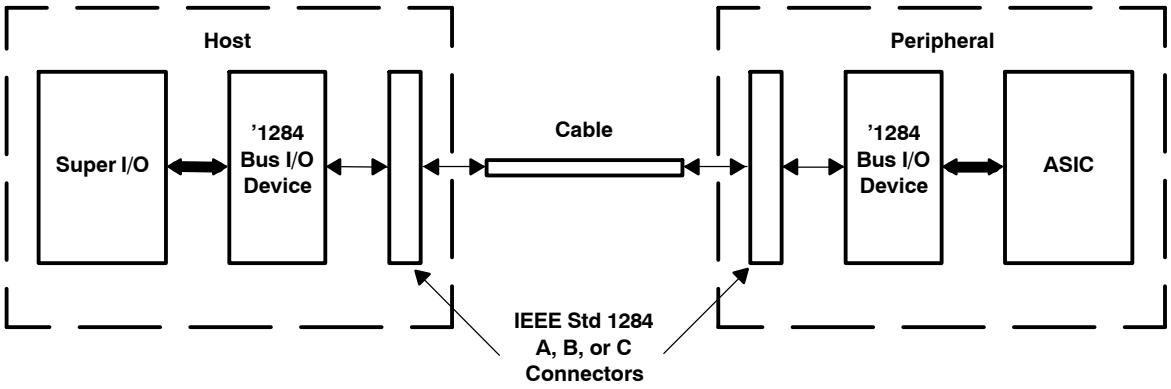


Figure 12. Block Diagram of Parallel Interface Port Between the PC and Peripheral

To illustrate how to apply the SN74ACT1284 as shown in Figure 12, Figures 13 and 14 explicitly show all data, control, and status lines from the Super I/O on the host side to the ASIC on the peripheral. The designer must decide which connector is suitable for a particular application and to what level type to set the devices using the HD pin.

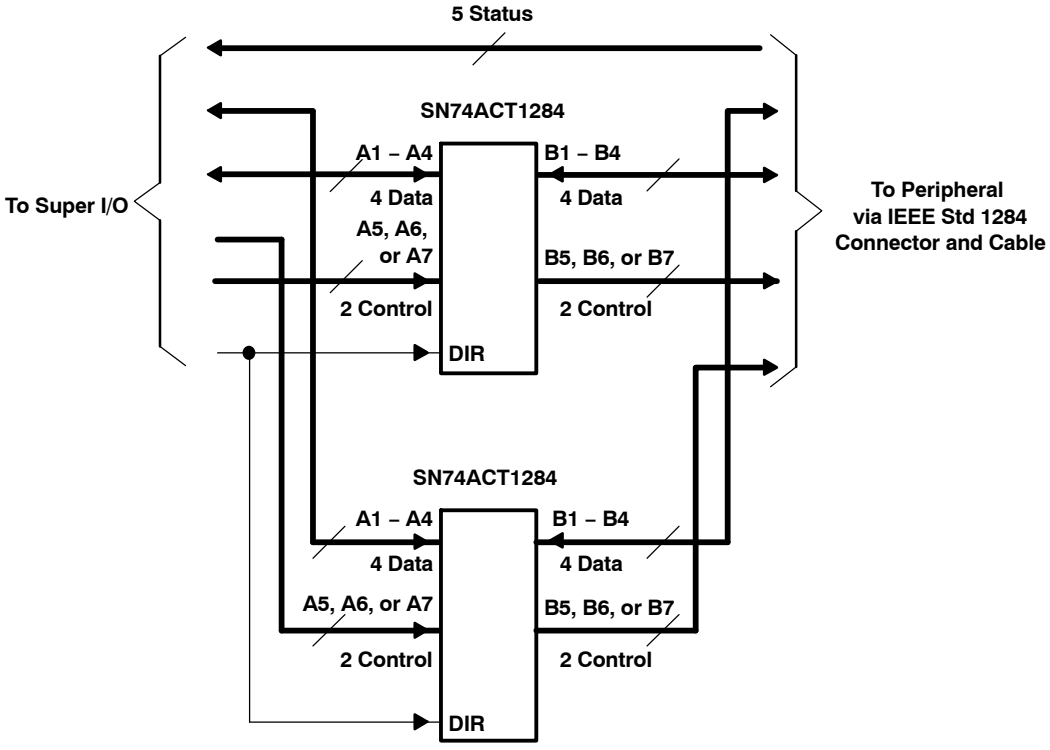


Figure 13. IEEE Std 1284 Host Solution Using Two SN74ACT1284 Devices

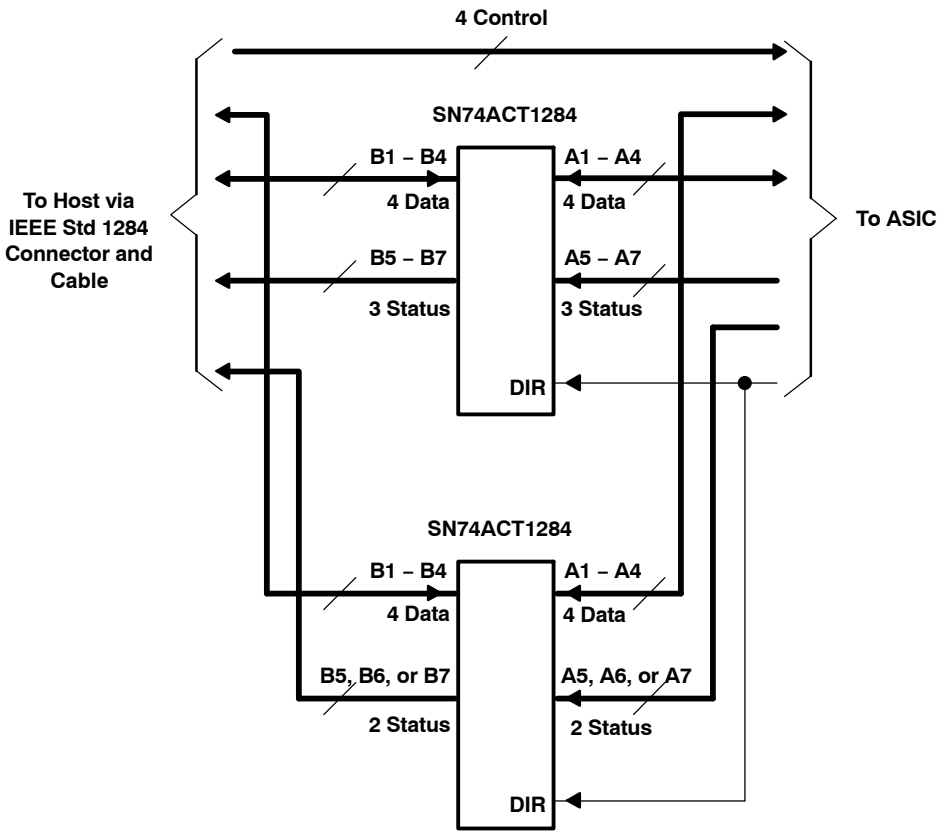


Figure 14. IEEE Std 1284 Peripheral Solution Using Two SN74ACT1284 Devices

While the SN74ACT1284 provides an acceptable two-chip solution, the SN74LV161284 and SN74LVC161284 devices provide optimum applicability−−specifically, on the peripheral side. Figures 15 and 16 show all data, control, and status lines from the Super I/O on the host to the ASIC on the peripheral using these 19-bit bus interface devices.

Note that Host Logic In (pin 25) on the host side is connected via the IEEE Std 1284 connector and cable to Peri Logic Out (pin 30) on the peripheral. Likewise, Peri Logic Out (pin 30) on the host is connected the IEEE Std 1284 connector and cable to Host Logic In (pin 25) on the peripheral.

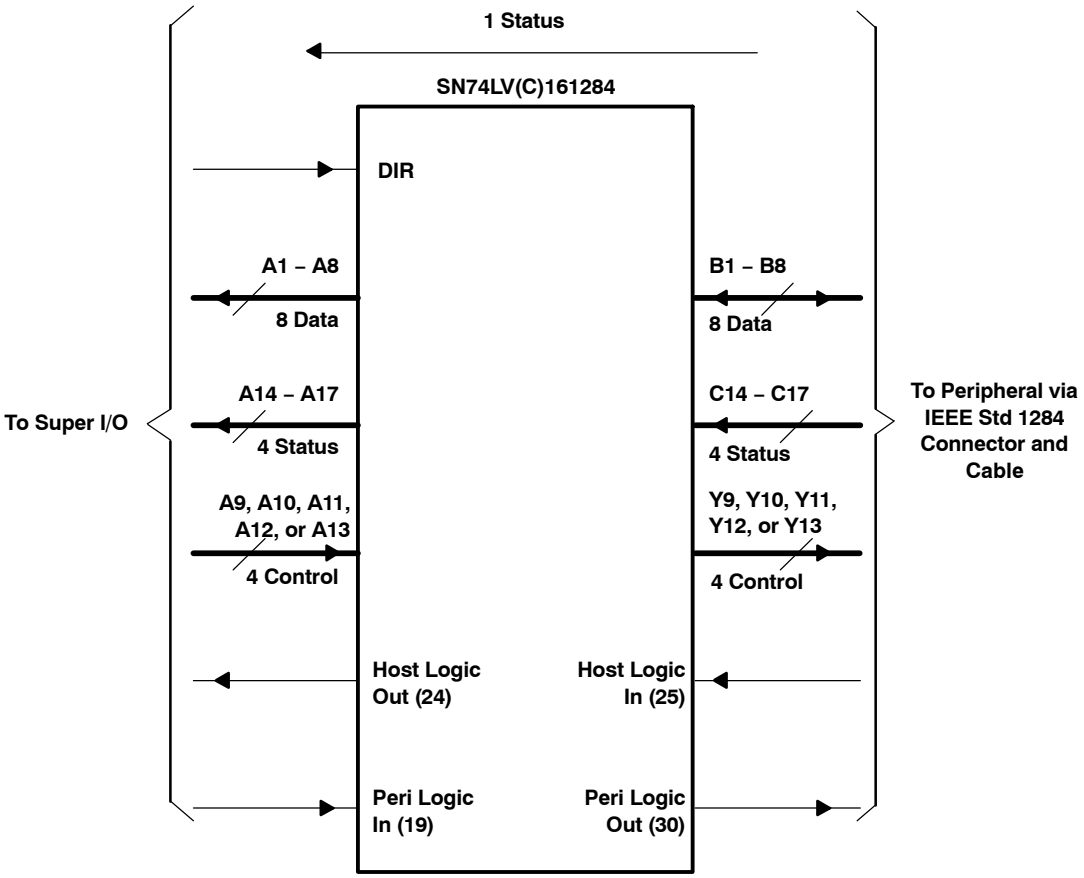


Figure 15. IEEE Std 1284 Host Solution Using the SN74LV161284 or SN74LVC161284

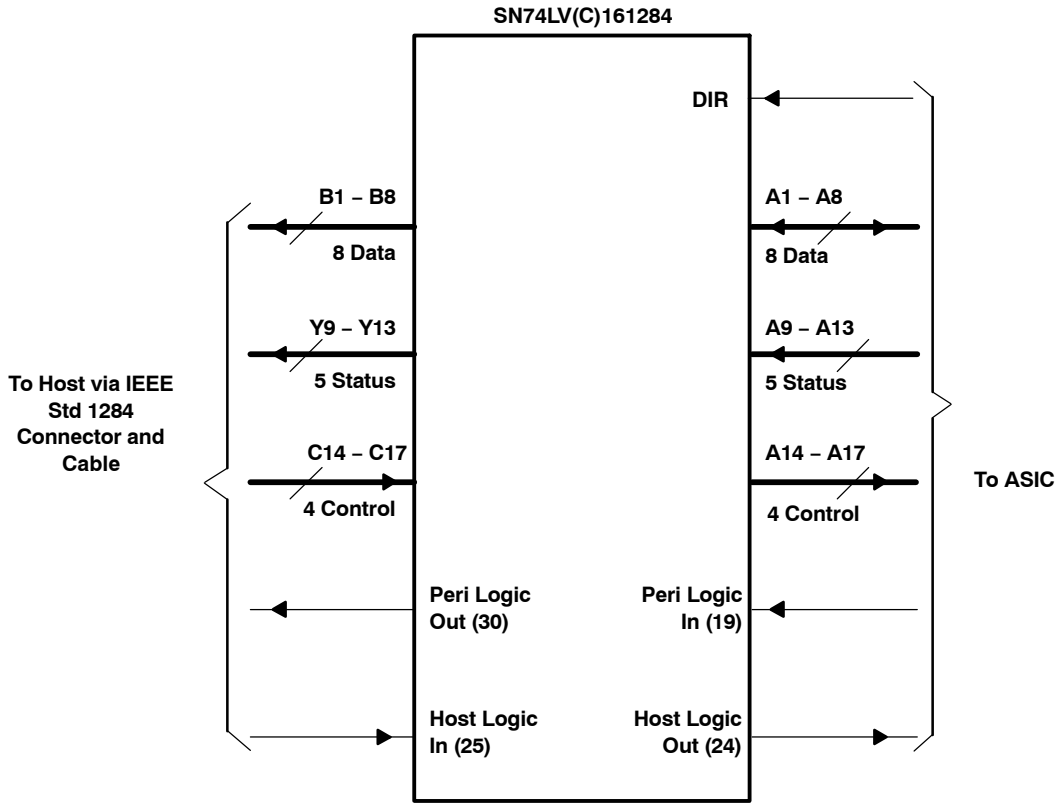


Figure 16. IEEE Std 1284 Peripheral Solution Using the SN74LV161284 or SN74LV161284

Conclusion

This report gives a brief description of IEEE Std 1284-1994 and TI's logic solutions that conform to this standard. TI offers the bus interface SN74ACT1284, SN74LVC161284, and SN74LV161284 devices as complete solutions for a high-performance parallel port, and, as shown by laboratory data, the '161284 devices offer superior performance in back-drive current generation when compared to the competition. Furthermore, this report guides designers in choosing the correct bus interface device in their IEEE Std 1284 applications.

Acknowledgment

The authors of this report are Nadira Sultana and Manny Soltero.

Commonly Asked Questions

1. How is the SN74LVC161284 used with a parallel port?

   The *Application Information* section of this application report, in conjunction with Figures 15 and 16, explains how to use the 'LVC161284 with the parallel port, whether it is on the host side or on the peripheral side.

2. If somebody wants an IEEE Std 1284 compliant design, is an IEEE Std 1284 transceiver required? What is so special about the SN74ACT1284, SN74LV161284, and SN74LVC161284?

   To comply fully with IEEE Std 1284, one of TI's IEEE Std 1284 transceiver solutions should be used. Separate device descriptions are discussed in full, and one can see that these devices are the optimum choice.

3. How does the back-drive current of these devices compare to our competition?

   The *Features and Benefits* section of this application report shows the excellent performance of the back-driving current of the SN74LVC161284. The SN74LV61284 has similar performance.

4. IEEE Std 1284 calls for series termination resistors on the driver lines before the pullup resistors. What is TI's recommendation for those termination resistors? Are they already included in the device (SN74ACT1284, SN74LVC161284, SN74LV161284)?

   The SN74ACT1284 does not have any series termination resistors, but the other two parts have 33-Ω series termination resistors included in the part to conform to IEEE Std 1284. An external 33-Ω series resistor must be connected if the SN74ACT1284 is used.

5. What is the driver configuration for an IEEE Std 1284 level-1 driver?

   The driver configuration for an IEEE Std 1284 level-1 driver is open drain.

6. Can the SN74LVC161284 be used on the host as well as on the peripheral side?

   Yes, the SN74LVC161284 can be used on the host side, but it is optimized for use on the peripheral side. However, on the host side, one status line cannot be buffered through the device. Figures 15 and 16 show this in detail.

7. If someone does not want to use Host Logic and Peri Logic, what should be done with those terminals––tie them high, or low, or leave them open?

   If the signal from the transmitting side is not to be used on their end, leave it open on the receiving side. However, the other signal should be driven true so that the other end of the cable sees it and can use it for better signal reliability.

Glossary

A

ASIC Application-Specific Integrated Circuit

E

ECP Extended-Capabilities Port

EPP Enhanced Parallel Port

H

HD High Drive

O

OEC™ Output Edge-Rate Control

P

PC Personal Computer

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Low-Voltage Bus-Switch Technology and Applications

SCDA005
December 1997

TEXAS INSTRUMENTS

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Introduction

Texas Instruments (TI™) introduced the crossbar technology (CBT) family of devices for a variety of purposes. The CBT devices are a 5-V family; they are basically a field-effect transistor (FET) that system design engineers use for isolation, or to interface a 5-V part to a 3.3-V part. With the reduction of power-supply voltages from 5 V to 3.3 V, TI has created a family of low-voltage crossbar technology (CBTLV) devices that operate from a 3.3-V power supply. This application report addresses the CBTLV logic family and compares it to the CBT family.

The main topics discussed are:

- Background
- Description of device
- Typical design applications
- SPICE model
- Package information
- Frequently asked questions
- Conclusion
- Glossary
- References

Background

The CBT family of devices has been largely successful for its ability to isolate one part of a system from another. Since the devices are essentially FET switches, when the transistor is on, they operate as a short circuit and the voltage on the input is passed through to the output. When the transistor is off, it functions as an open circuit and the input is completely isolated from the output. A second useful application for CBT devices is for interfacing a 5-V part of a system to a 3.3-V part. If a diode is added between the external power supply and the V_{CC} pin, the 5-V level is reduced by 0.7-V drop caused by the diode, and a voltage level of 4.3 V results. The FET has a characteristic 1-V drop across the gate to source terminals, and a 3.3-V level is achieved.

The CBTLV is a 3.3-V logic family with a variety of uses, some of which are similar to those of the CBT family and some of which are different. As with the CBT family, the CBTLV devices can be used for isolation purposes, and although they cannot serve as 3.3-V to 2.5-V level translators, they can be used for hot-plug or docking applications. This is discussed in further detail in this application report.

Description of Device

TI is in production of the first CBTLV device, the CBTLV3245, and will release approximately ten additional devices by 1H98. The CBTLV3245 is a low-voltage, octal FET bus switch that uses the standard ’245 device pinout. A function table of its operation is provided in Table 1.

Table 1. CBTLV3245 Function Table

INPUT $\overline{OE}$	FUNCTION
L	A port = B port
H	Disconnect

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A logic diagram is provided in Figure 1. The input is connected directly to the output when the transistor is conducting, and the input is totally disconnected from the output when the transistor is not conducting.

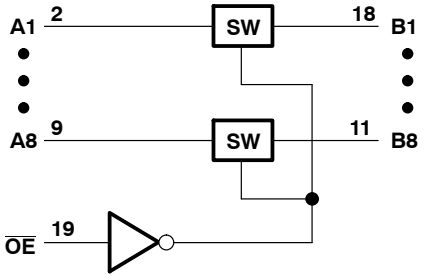

Figure 1. CBTLV3245 Logic Diagram

Although not yet released, the CBTLV16210, CBTLV16211, CBTLV16212, and CBTLV16215 are being designed to have a maximum off current of 20 mA when V_{CC} is 0 and V_I or V_O is 0 to 3.6 V, allowing them to be used in applications in which live-insertion is required. The I_{off} specification indicates the maximum amount of leakage current that enters a device when it is powered down.

Typical Design Applications

The 5-V CBT logic family is composed of an n-channel transistor that operates as a switch. When the transistor is conducting, the voltage on the A port is passed through to the B port and vice versa. Also, if a diode is added to reduce the 5-V power supply level to 4.3 V, then the additional 1-V drop across the gate to source (V_{GS} = 1 V), yields a 3.3-V signal. A transistor-level diagram of a typical CBT device is shown in Figure 2.

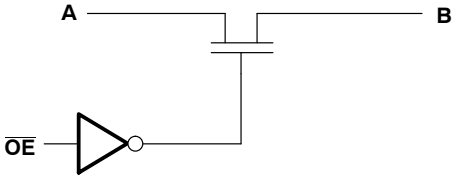

Figure 2. Typical 5-V CBT Device Transistor

The CBTLV3245 (as well as the other CBTLV devices when they are released to production) will provide the same isolation features that the CBT family of devices provides. However, the CBTLV devices have an additional p-channel (PMOS) transistor in parallel with the n-channel (NMOS) that allows them to operate at a 3.3-V power supply level. Additional circuitry needed to complement the functioning of the PMOS allows them to be used for hot-plug installation or docking purposes. A simplified transistor-level diagram of the CBTLV3245 is shown in Figure 3.

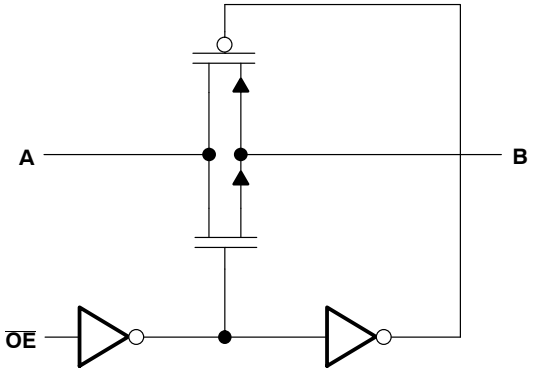

Figure 3. CBTLV3245 Simplified Transistor

SPICE Model

The SPICE model is available for the CBTLV3245 is a level-13 model consisting of the input and output stages, and can be obtained by contacting your local TI sales representative.

Package Information

The CBTLV3245 is a 20-pin device and is available in a small-outline integrated circuit (SOIC) package, a thin shrink small-outline package (TSSOP) and a thin very small-outline package (TVSOP). The pinout for the CBTLV3245 is shown in Figure 4.

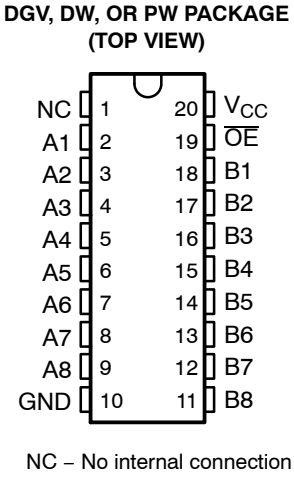

Figure 4. CBTLV3245 Pinout

Where applicable, other CBTLV devices will be available in 48-pin TSSOP and TVSOP packages. CBTLV devices will be drop-in replacements for their CBT counterparts.

Frequently Asked Questions

Question: With the CBT logic family, I could interface the 5-V part of my system with the 3.3-V part of my system by adding a diode and reducing the V_{CC} voltage. Can I use a similar method with the CBTLV family to interface between the 3.3-V part and 2.5-V part of my system?

Answer: This is not possible with the CBTLV family due to the existence of a p-channel transistor in parallel with the n-channel transistor. This additional p-channel and its associated circuitry allows hot-plug insertion, but disallows level shifting. Also, the CBTLV family is not 5-V tolerant, but is 3.3-V tolerant when powered by a 2.5-V power supply.

Question: How do I get a copy of the CBTLV3245 SPICE model?

Answer: The SPICE model for the CBTLV3245 can be obtained by contacting your local TI sales representative.

Question: Does the CBTLV consume less power than the CBT family?

Answer: Yes, due to the power supply being at a lower level, the CBTLV family consumes less power than the CBT family.

Question: What future releases are planned for the CBTLV family?

Answer: TI is designing the CBTLV3125, CBTLV3126, CBTLV3253, CBTLV3257, CBTLV3861, CBTLV16210, CBTLV16211, CBTLV16212, CBTLV16215, and the CBTLV16292. All of these devices are scheduled to be released to production by the end of June 1998.

Conclusion

TI has recently released the CBTLV3245 to production. It is a 20-pin, 3.3-V device that comprises an n-channel transistor in parallel with a p-channel transistor. It is available in SOIC, TSSOP, and TVSOP packages. TI plans to release an additional ten CBTLV devices during 1H98.

Glossary

CBT	Crossbar technology
CBTLV	Low-voltage crossbar technology
FET	Field-effect transistor
IBIS	I/O buffer information specification
SOIC	Small-outline integrated circuit
SPICE	Simulation program with integrated circuit emphasis
TSSOP	Thin shrink small-outline package
TVSOP	Thin very small-outline package
TI	Texas Instruments

References

CBT Bus Switches Crossbar Technology, 1996, literature number SCDD001

Semiconductor Group Package Outlines, 1997, literature number SSYU001

PCA8550 Nonvolatile 5-Bit Register With I²C Interface Technology and Applications

SZZA014
March 1999

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Abstract

As personal computer (PC) motherboard designs are advancing in sophistication and power, software-controllable system-configuration settings become an important factor in system administration and maintenance. The Texas Instruments (TI™) PCA8550 nonvolatile 5-bit register is designed for the specific application of multiplexing hardware signals with software-controllable configuration data. This application report discusses the logic functionality of the PCA8550, the specifics of the I^2C interface, the electrical characteristics of the device, and its use in the intended application. The information in this report, along with the data sheet, should enable the PC-motherboard designer to successfully implement an electrically erasable programmable read-only-memory multiplexer (EEMUX) solution.

Introduction

The current trend in PC design is to reduce the amount of discrete logic on the motherboard and to eliminate hardware programming jumpers. The reduction in discrete logic components cuts costs, saves board area, and increases system reliability. Eliminating hardware programming jumpers that configure hardware options and replacing the jumpers with software-controllable configuration data stored in electrically erasable programmable read-only memory (EEPROM) simplifies system configuration, administration, and maintenance. The TI PCA8550 accomplishes both of these goals. The PCA8550 replaces several logic gates and provides the equivalent functionality. It also takes the place of hardware programming jumpers by storing the data in EEPROM, which is software reprogrammable.

Background

Motherboards that are designed to support the Intel™ P6-family microprocessor interface must provide clock-multiplier information during reset. The phase-lock loop (PLL) inside the microprocessor is programmed by this clock-multiplier data from the motherboard. During reset, the microprocessor internal PLL locks at a multiple of the bus clock (BCLK) input to generate the core clock. Typically, hardware jumpers on the motherboard are used to hard-code the clock-multiplier data. These jumpers are configured for the specific clock-speed of the microprocessor, and they must be reconfigured manually if the microprocessor is replaced by one with a different clock rating.

To conserve pins, the microprocessor interface multiplexes several signals. Four inputs of the microprocessor, $\overline{\text{A20M}}$, $\overline{\text{IGNNE}}$, LINT[0]/INTR, and LINT[1]/NMI, have static data during a reset. The levels on these input pins are the jumper configuration data used to program the clock multiplier (see Table 1). These inputs are captured on the low-to-high transition of the $\overline{\text{RESET}}$ input of the microprocessor. After the reset, during normal operation, these four inputs receive regular run-time signals, which, in an Intel-chipset-based system, come from the 82371AB PCI-to-ISA/IDE XCELERATOR (PIIX4) southbridge chip.

On the Slot 1™ microprocessor connector, these pins are A5, A8, A17, and B16, as indicated in Table 1. They are CMOS inputs and are specified for 2.5-V operation. The recommended pullup resistor value is 150 Ω to 330 Ω. On the PIIX4, the $\overline{\text{A20M}}$, $\overline{\text{IGNNE}}$, INTR, and NMI signals are open-drain (OD) outputs that nominally are pulled up through 2.7-kΩ resistors to 3.3 V. To interface these signals, level translation or current limiting is necessary.

To support pin sharing, it is necessary to provide the multiplexing, level translation/current limiting, and configuration programming. The support hardware required for the previous discrete-logic method includes several buffer integrated circuits, pullup resistors, and DIP switches or header-connector pins and jumpers (see Figure 1).

Table 1. Clock-Multiplier Programming Data†

CLOCK MULTIPLIER	LINT[1] (PIN B16)	$\overline{\text{A20M}}$ (PIN A5)	$\overline{\text{IGNNE}}$ (PIN A8)	LINT[0] (PIN A17)
2	L	L	L	L
2.5	L	L	L	H
3	L	L	H	L
3.5	L	L	H	H
4	L	H	L	L
4.5	L	H	L	H
5	L	H	H	L
5.5	L	H	H	H
6	H	L	L	L
6.5	H	L	L	H
7	H	L	H	L
7.5	H	L	H	H
8	H	H	L	L
1.5	H	H	L	H
Reserved	H	H	H	L
2	H	H	H	H

† See the processor data sheet for supported settings.

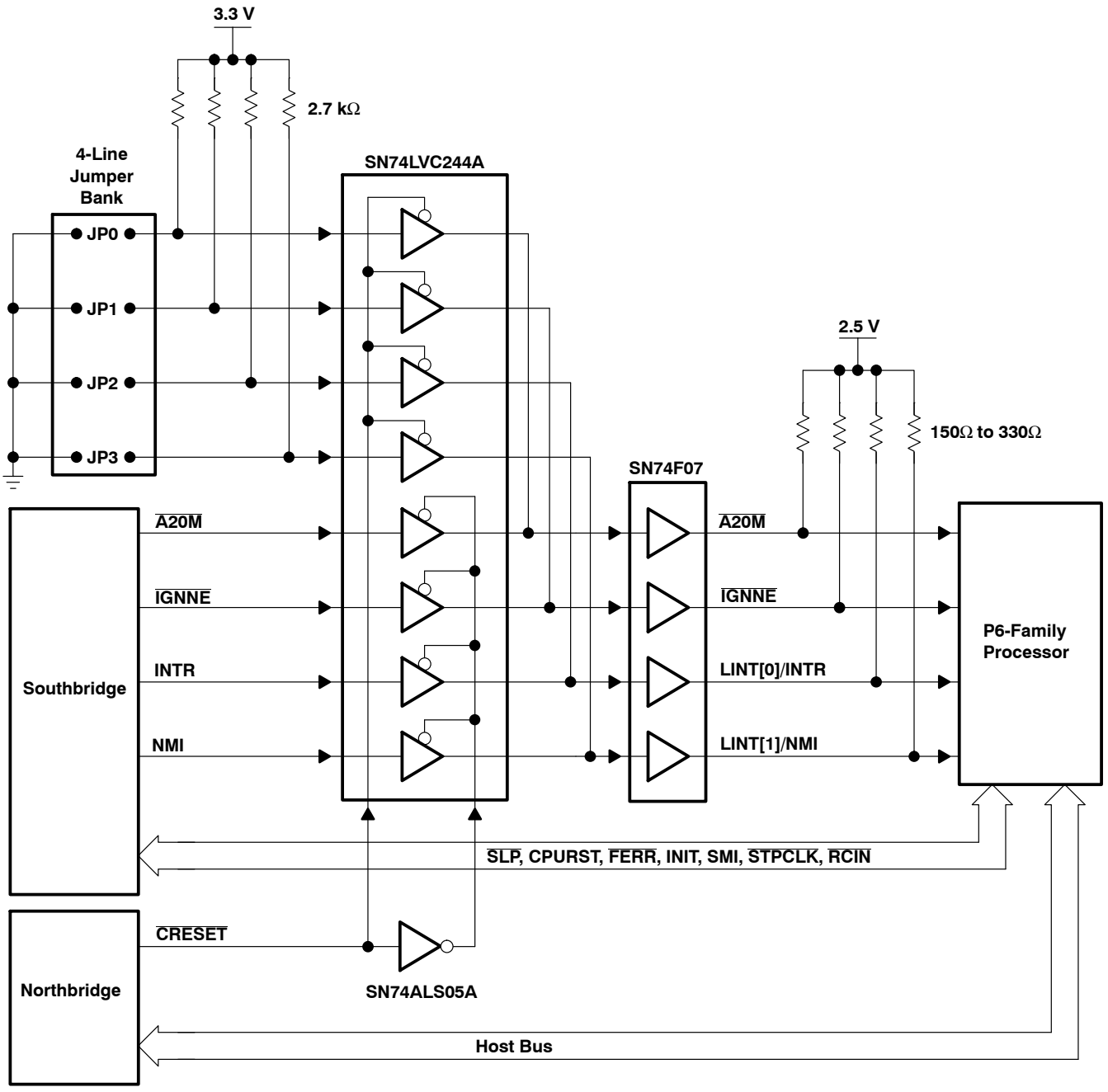

Figure 1. Discrete-Logic Implementation of Clock-Ratio Pin Sharing

All of this functionality is fully integrated into the TI PCA8550, an EEMUX. By replacing this complex circuitry with the PCA8550, circuit design is greatly simplified, less printed circuit board area is occupied, and reliability can be improved (see Figure 2). One of the most important benefits of migrating to the PCA8550 is the replacement of the hardware-configuration jumpers with a software-controllable EEPROM. By moving the configuration of the clock multiplier from hardware to software, the setup of the motherboard becomes a simpler, more user-friendly task for the hardware integrator. Original configuration could even become fully automated. Also, future processor upgrades become a less daunting task for the final consumer.

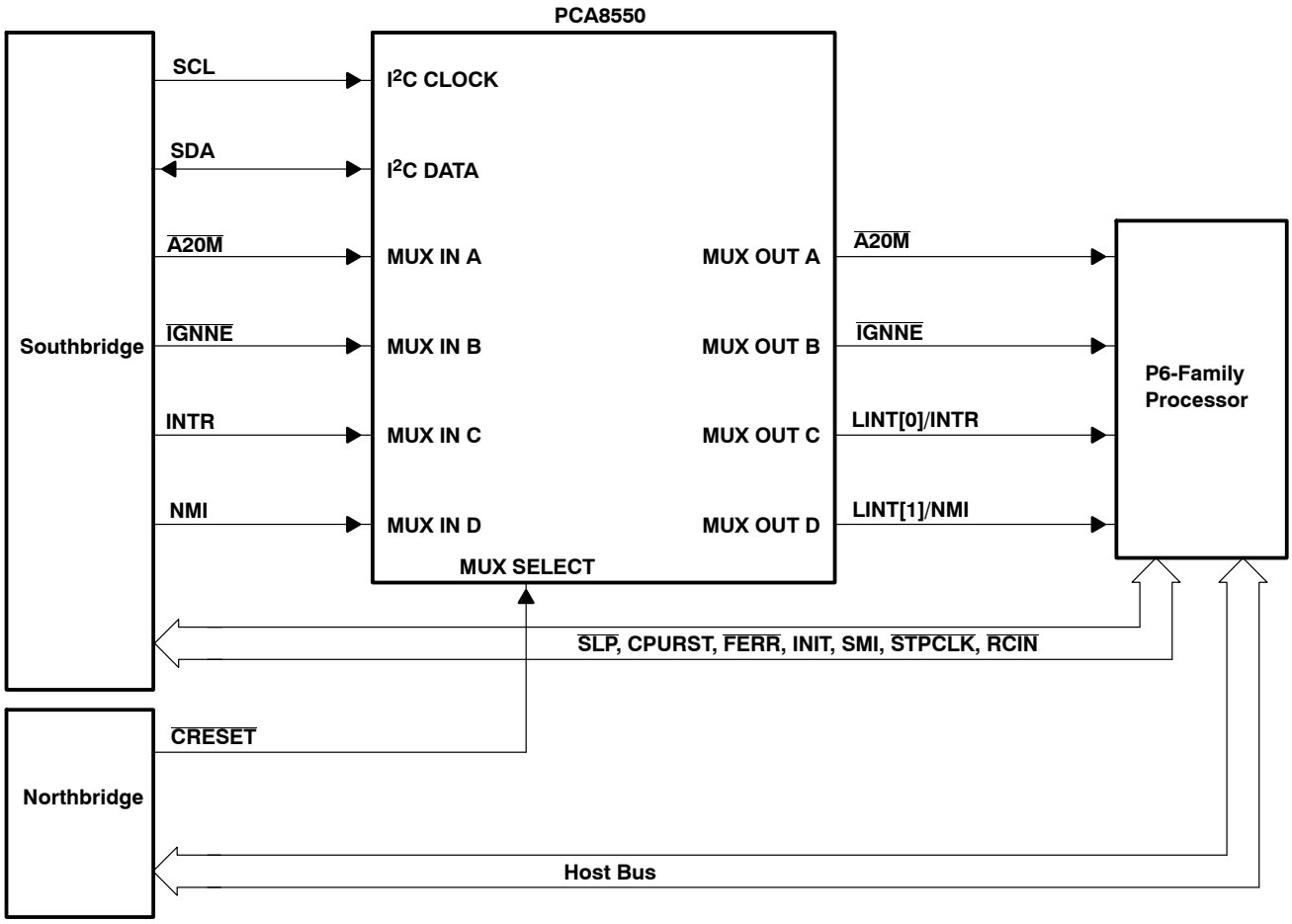

Figure 2. PCA8550 Implementation of Clock-Ratio Pin Sharing

Logic Functionality

The PCA8550 is designed to multiplex four bits of data, from parallel inputs or from data stored in a nonvolatile register (see Figure 3). An additional bit of register output also is provided, which is latched to prevent changes in the output value during the write cycle. The factory default for the contents of the register is all low. These stored values can be read from, or written to, using the I^2C bus. The ability to control writing to the register is provided by the write protect (WP) input. The override ($\overline{\text{OVERRIDE}}$) input, when asserted low, forces all the register outputs to a low. The MUX OUT outputs are 2.5-V CMOS outputs that are designed to drive directly the P6-family microprocessor inputs. The data on the outputs are determined according to the MUX SELECT input and the $\overline{\text{OVERRIDE}}$ input (see Table 2). The NON-MUXED OUT output is latched at the value present on its output at the time the MUX SELECT input transitions from a low to a high state.

The PCA8550 provides a fast-mode (400 kbit/s) or standard-mode (100 kbit/s) I^2C serial interface for data input and output. The implementation is as a slave. Both of the I^2C Schmitt-trigger inputs (SCL and SDA) provide integrated pullup resistors (typically 170 kΩ) and are 5-V tolerant.

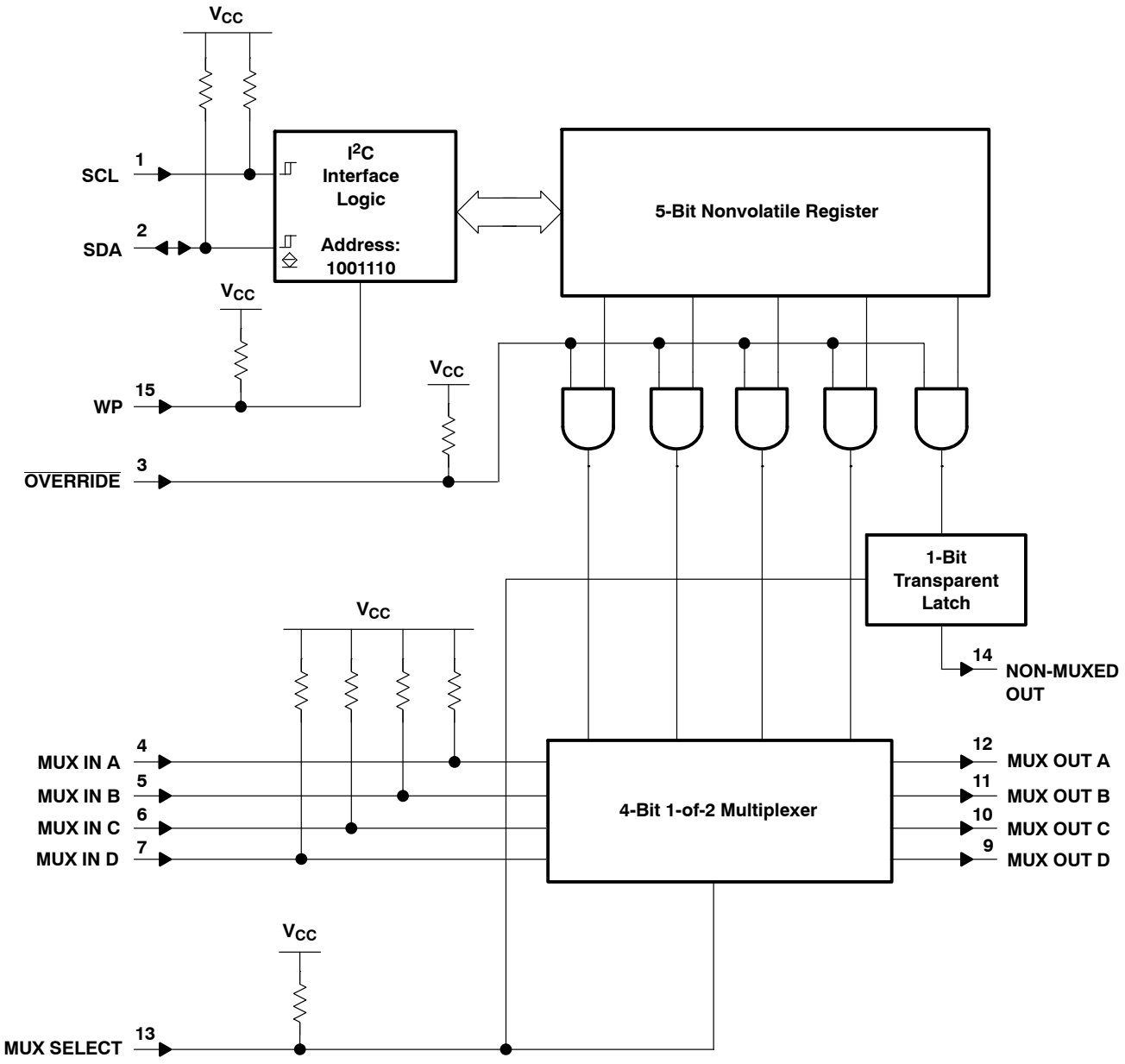

Figure 3. Logic Diagram (positive logic)

Table 2. PCA8550 Logic Function Table

INPUTS		OUTPUTS	
MUX SELECT	$\overline{\text{OVERRIDE}}$	MUX OUT	NON-MUXED OUT
L	L	L	L
L	H	Nonvolatile register	Nonvolatile register
H	X	MUX IN	Latched NON-MUXED OUT

I²C Protocol Overview

Typically, a complete I²C communication consists of a start (or repeated start) condition; a slave-address transfer, followed by a data-direction bit; a receiver-acknowledge bit; one or more data-byte transfers, each followed by a receiver-acknowledge bit; and a stop condition (see Figure 4).

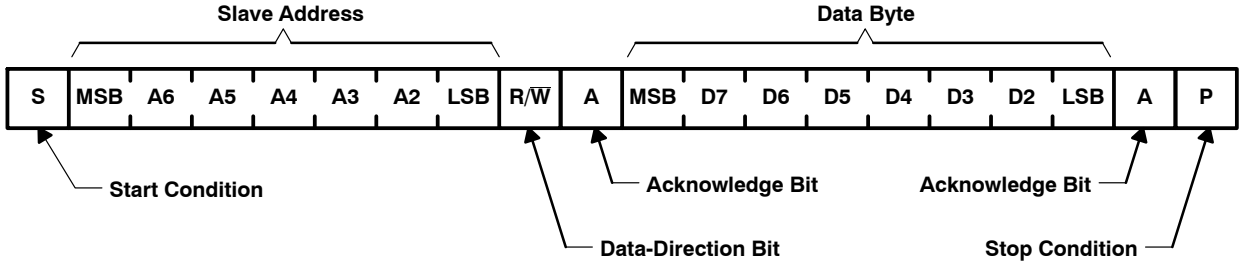

Figure 4. Complete I²C Communications

A start (or repeated start) condition is a high-to-low transition on the serial-data (SDA) input/output while the serial-clock (SCL) input is high (see Figure 5). A stop condition is a low-to-high transition on the SDA input/output while the SCL input is high. All other SDA transitions must occur only while SCL is low.

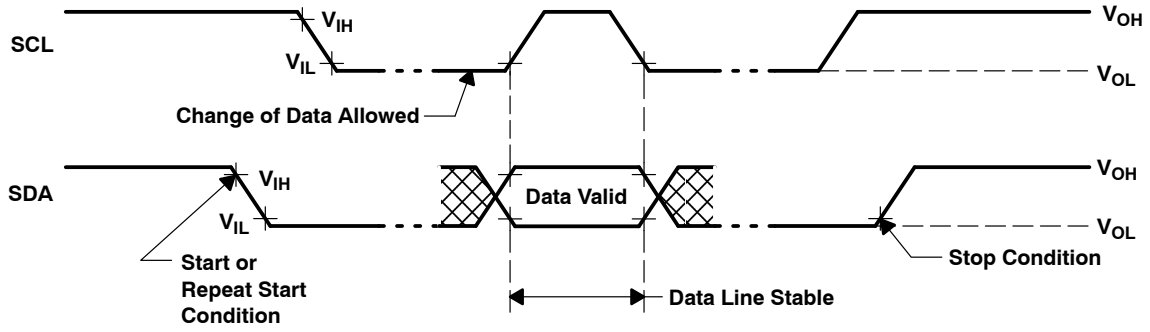

Figure 5. I²C Signals

Address and data transfers are composed of 8-bit bytes. Each byte transfer is followed by an acknowledge (ACK) clock cycle. The device that receives the data transfer should acknowledge the receipt (in some cases this may take the form of no acknowledge, or NACK). The address transfer usually is a 7-bit word (the I²C bus protocol also supports 10-bit addressing) followed by the data direction bit, read/$\overline{\text{write}}$ (R/$\overline{\text{W}}$).

If a device controls the clock line (SCL), it is considered to be a master. It initiates a data transfer by sending a start condition followed by an address word and R/$\overline{\text{W}}$ bit. The device that acknowledges the address sent by the master is considered the slave. The direction of data transfer on the bus determines whether the master is a receiver or transmitter. The same is true for the slave. If the R/$\overline{\text{W}}$ bit is low (0), a master has indicated a write transfer and is considered a master transmitter. The slave, whose address was sent by the master, acknowledges and becomes a slave receiver. Similarly, if the R/$\overline{\text{W}}$ bit is high (1), the master has requested a read transfer and it is considered a master receiver. The slave, whose address was sent by the master, acknowledges and becomes a slave transmitter.

For additional information on the I²C protocol, refer to *The I²C bus and how to use it (including specifications)*, Philips, April 1995.

PCA8550 I²C Interface

The PCA8550 cannot control the clock line (SCL is an input only) and is, therefore, always considered a slave device. Because the PCA8550 is capable of both receiving and transmitting data, it can be a slave transmitter or a slave receiver, depending on the state of the R/$\overline{W}$ bit in the address transfer.

I²C communication with the PCA8550 is initiated by a master sending a start condition (see Figure 6). After the start condition, the device address byte is sent, most significant bit (MSB) first, including the R/$\overline{W}$ bit. The 7-bit address of the PCA8550 is 1001110. The PCA8550 does not respond to the general call address. After receiving the valid address byte, the PCA8550 responds with an acknowledge, a low on the SDA input/output during the high of the acknowledge-related clock pulse.

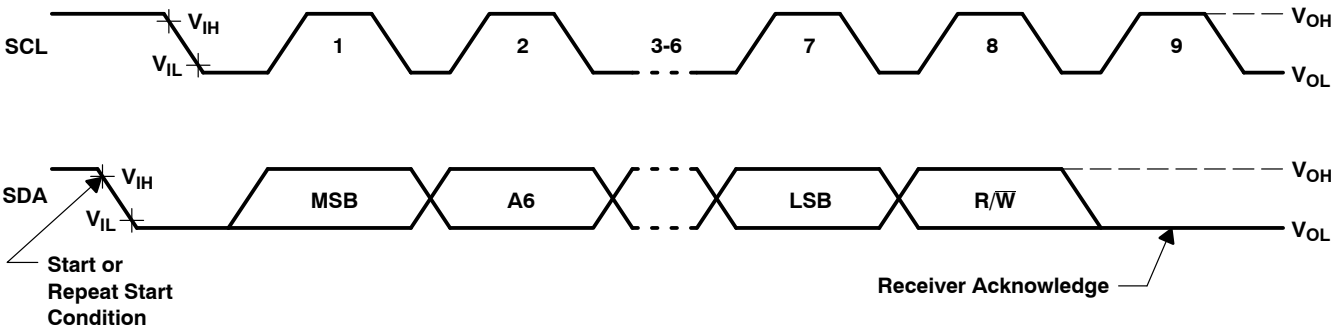

Figure 6. I²C Address Transfer

The data byte follows the address acknowledge (see Figure 7). If the R/$\overline{W}$ bit is high, the data from the PCA8550 are the values read from the nonvolatile register. If the R/$\overline{W}$ bit is low, the data are from the master, to be written into the register. A valid data byte is one in which the three high-order bits are low. The first valid data byte that is received is written into the register following the stop condition. If an invalid data byte is received, it is acknowledged, but it is not written into the register. The data byte is followed by an acknowledge sent from the PCA8550. Following the acknowledge of a valid data byte, if other data bytes are sent from the master, they are acknowledged by the PCA8550, but they are not written into the nonvolatile register.

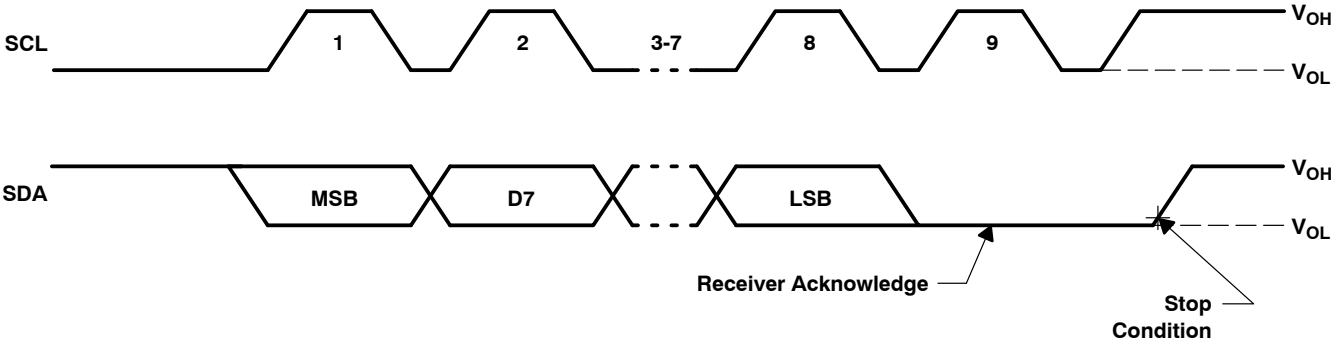

Figure 7. I²C Data Transfer

A stop condition is sent by the master (see Figure 7). If the WP input is low during the falling edge of the SCL input for the first valid data-byte-acknowledge clock pulse, and the R/$\overline{W}$ bit is low, the stop condition causes the I²C interface logic to write the data byte value into the nonvolatile register. Data are written only if complete bytes are received and acknowledged. Writing to the register takes time (t_{wr}), during which the device does not respond to its slave address. During the write to the nonvolatile register, the data out on the MUX OUT pins remains at the previous value until the write is complete. If the WP input is high, the I²C interface logic does not write to the register.

Electrical Characteristics

AC Performance

The TI PCA8550 is designed to meet or exceed the I²C-bus fast-mode ac performance requirements. System management bus (SMBus) is a similar two-wire bus protocol based on the I²C bus. In most cases, fast-mode I²C ac specifications exceed the requirements of the SMBus specification, which can be met with most of the I²C-bus standard-mode requirements. Table 3 provides a comparison of the ac specifications of the I²C-bus fast-mode limits versus the SMBus limits, along with the PCA8550 capability.

Table 3. Comparison of AC Specifications Between I²C Protocol and SMBus – Revision 1.1

SYMBOL	PARAMETER	I²C-BUS (FAST MODE)		SMBus		UNIT	PCA8550†
		MIN	MAX	MIN	MAX		
F_{BUS}	Operating frequency	0	400	10	100	kHz	Yes
T_{BUF}	Bus free time between stop and start conditions	1.3		4.7		µs	Yes
$T_{HD;STA}$	Hold time after (repeated) start condition	0.6		4		µs	Yes
$T_{SU;STA}$	Repeated-start condition setup time	0.6		4.7		µs	Yes
$T_{SU;STO}$	Stop condition setup time	0.6		4		µs	Yes
$T_{HD;DAT}$	Data hold time	0‡		300		µs	Yes
$T_{SU;DAT}$	Data setup time	100		250		µs	Yes
$T_{TIMEOUT}$	Clock low timeout value	N/A		25	35	ms	No§
T_{LOW}	Clock low period	1.3		4.7		µs	Yes
T_{HIGH}	Clock high period	0.6		4	50	µs	Yes
$T_{LOW;SEXT}$	Cumulative clock-low extend time (slave device)	N/A			25	ms	Yes¶
$T_{HIGH;MEXT}$	Cumulative clock-low extend time (master device)	N/A			10	ms	N/A
T_F	Clock/Data fall time		300		300	ns	Yes
T_R	Clock/Data rise time		300		1000	ns	Yes

† Does the TI PCA8550 meet or exceed the requirements of the SMBus specification Revision 1.1?
‡ The I²C-bus protocol requires that a device must internally provide a hold time of at least 300 ns.
§ The PCA8550 does not support timeout.
¶ The PCA8550 does not require the extension of the bus clock for operation. It can send and receive with a clock rate up to 400 kHz with T_{LOW} = 1.3 µs minimum and T_{HIGH} = 0.6 µs minimum. However, if a proper write-mode sequence is issued from a master device, the PCA8550 begins programming the nonvolatile memory upon receiving the stop condition. The specified typical write time (t_{WT}) is 10 ms. If the device is addressed during this required programming time, the device does not acknowledge. Operating in this fashion, the device does not tie up the bus during a program.

DC Performance

The TI PCA8550 is designed to meet or exceed the I²C-bus dc specifications. The PCA8550 SCL input and SDA I/O implement CMOS circuitry. In addition, each input has a 170-kΩ pullup resistor to V_{CC}. While these resistors represent a load to the bus, they assist the typically slow low-to-high transition of the I²C bus due to its passive pullups. Also, should the bus power down, the I²C inputs remain at a logic high. Table 4 provides a comparison of the dc specifications of the I²C-bus (fast-mode) limits for V_{CC}-related inputs versus the SMBus (Revision 1.1) limits, along with the PCA8550 capability.

Table 4. Comparison of DC Specifications Between I²C Protocol and SMBus-Revision 1.1, V_{CC}-Related Inputs

SYMBOL	PARAMETER	I²C-BUS (FAST MODE)		SMBUS		UNIT	PCA8550†
		MIN	MAX	MIN	MAX		
V_{IL}	Data, clock input-low voltage	−0.5	$0.3 \times V_{CC}$	−0.5	0.8	V	Yes
V_{IH}	Data, clock input-high voltage	$0.7 \times V_{CC}$	V_{CC}+0.5	2.1	5.5	V	Yes
V_{OL}	Data, clock output-low voltage	0	0.4‡		0.4§	V	Yes¶
I_{LEAK}	Input leakage current	N/A	N/A		±5	μA	No#
I_{PULLUP}	Current through pullup resistor or current source	N/A	N/A	100	300	μA	N/A‖

† Does the TI PCA8550 meet or exceed the requirements of the SMBus specification Revision 1.1?
‡ Maximum V_{OL} specified for 3-mA sink current
§ Maximum V_{OL} specified for I_{PULLUP} MAX
¶ The PCA8550 is a slave device and, therefore, does not control the SCL port. V_{OL} is applicable only to the SDA port.
# With the 170-kΩ internal pullup resistors to V_{CC} on SDA and SCL, this device should be configured in the system such that it is powered down only with the bus or is disconnected from an active bus when powered down.
‖ This specification is applicable to removable SMBus devices, such as a smart battery.

Application Circuitry

The PCA8550 takes the place of several discrete logic integrated circuits and passive components on the PC motherboard in the interface between the southbridge and the microprocessor. From the southbridge, the $\overline{\text{A20M}}$, $\overline{\text{IGNNE}}$, INTR, and NMI open-drain output signals are fed directly into the MUX IN inputs of the PCA8550. Discrete external pullup resistors are not necessary on these southbridge outputs because 2.2-kΩ (nominal) resistors to V_{CC} are integrated into the MUX IN inputs of the PCA8550. The MUX OUT outputs of the PCA8550 are regulated internally to a maximum V_{OH} of 2.625 V, meeting the requirements of the P6-family microprocessor input specification. The MUX OUT outputs can directly drive the P6-family microprocessor inputs without any additional level translation or current limiting.

The I²C SCL and I²C SDA pins of the PCA8550 are connected to the open-drain SMBus on the motherboard, which is controlled by the southbridge. External pullup termination resistors are required on the SMBus. The value of the termination is dependent upon the capacitive loading of the bus. The PCA8550 provides weak-pullup resistors (170-kΩ nominal) to V_{CC}, required to compensate the termination of the SMBus due to the input capacitance of this device. Therefore, the values of the external bus-termination resistors are not changed by adding this device to the bus.

The MUX SELECT input is driven by the $\overline{\text{CRESET}}$ output from the northbridge. During reset, when the MUX SELECT input is low, the MUX OUT outputs will be the nonvolatile register data used to configure the microprocessor PLL clock multiplier. The factory default for the contents of the nonvolatile register is all low. Therefore, if this is the first time to boot up with a new (not previously programmed) part, or if the $\overline{\text{OVERRIDE}}$ input is asserted low, the outputs are all low. If the outputs are all low, the microprocessor PLL is configured to operate at a 2× multiple of the bus speed. On the Pentium II, this is the slowest speed selection supported. This selection is for safe power-on only. This speed is used for initial configuration of a new system, or reconfiguration after replacing processors.

The maximum time required for the output data to be valid after the application of the MUX SELECT input, t_{SOV}, is 20 ns. To meet the long setup time of the processor inputs (t_{SU} = 1 ms for Pentium II processors), the northbridge must drive the MUX SELECT input low at least $t_{SOV} + t_{SU}$ prior to the rising edge of the system reset ($\overline{\text{RESET}}$).

Following the system reset, the northbridge drives the MUX SELECT input of the PCA8550 high and the MUX IN input signals from the southbridge are selected at the MUX OUT outputs.

Application Programming

In the PC motherboard application, where the BIOS complies with the *System Management Bus BIOS Interface Specification*, SMBus communication with the PCA8550 occurs using standard BIOS calls.

The SMBUS ACCESS call (53B0H) and the BIOS 15H Interrupt can be used for a real-mode not-connected, a real-mode connected, a 16-bit protected-mode connected, or a 32-bit protected-mode connected interface. Because the PCA8550 likely will only need to be programmed by the system BIOS when the user is changing the CMOS Setup and because of the simplicity of the PCA8550 communication, the real-mode not-connected call is all that is necessary in a typical system.

The PCA8550 supports the SEND BYTE (Protocol Code 01H), and the Receive Byte (02H) protocols. Because the PCA8550 requires a transfer of one single byte of data, without additional commands or data, the QUICK COMMAND (00H), WRITE BYTE (03H), READ BYTE (04H), WRITE WORD (05H), READ WORD (06H), BLOCK WRITE (07H), BLOCK READ (08H) and PROCESS CALL (09H) protocols do not apply and are not supported. The PCA8550 also does not support Packet Error Checking, which is an optional feature of SMBus. Also, the use of the SMBUS CRITICAL MESSAGES call (07H) is unnecessary with the PCA8550, as it does not push a data message onto the I^2C bus. It replies only with its nonvolatile register data when queried with a RECEIVE BYTE command. A typical programming cycle of the PCA8550 begins with the SMBUS REQUEST command.

Call With:

AX = 53B0H (SMBUS ACCESS call)

BH = 10H (SMBUS REQUEST command)

BL = 01H (SMBUS SEND BYTE protocol code)

CH = 4EH (PCA8550 address)

CL = N/A

DH = N/A

DL = data dependent upon the wiring (e.g., 05H might represent the 4.5X PLL multiplier code that is necessary for a 450-MHz processor running on a 100-MHz bus)

The SMBUS REQUEST command is then followed by polling the SMBUS REQUEST DATA AND STATUS (13H) command and waiting for a return of 00H (no data pending, transaction complete) in the CH register. After the command has been completed, typically, the software should wait 10 ms to allow the nonvolatile register to be programmed with the new data.

Following the wait time, the success of the nonvolatile register programming should be tested by issuing an SMBUS REQUEST (10H) command using the RECEIVE BYTE (02H) protocol. The SMBUS REQUEST command is then followed by polling the SMBUS REQUEST DATA AND STATUS (13H) command and waiting for a return of 00H (no data pending, transaction complete) in the CH register. If successful, the PCA8550 data is returned in the DX register and the data should match the byte of data that was originally written. An SMBUS DISCONNECT (05H) call is not necessary if the real-mode not-connected calling interface has been used.

Competitive Analysis

The TI PCA8550 is designed and characterized to have operational and electrical characteristics that are similar to the Philips PCA8550 device. The TI component can serve as a drop-in replacement for the Philips part, providing the customer with a true alternate source. There is one functional difference that TI intentionally has designed into the operation of the component. To obtain maximum flexibility of the device for use in a potentially broad range of applications, TI has implemented a nonvolatile register output that retains its original output condition during a write. The outputs of the Philips PCA8550 component are all driven to a high condition during a write. In the motherboard application, this functional difference is irrelevant. However, if the component is used in an alternative application that requires valid data on the outputs during a write, the TI part supports this functionality. The PCA8550 is offered in the standard TI 16-pin packages: SOIC, SSOP, and TSSOP (see Appendix A).

Conclusion

The TI PCA8550 provides a simple, cost-effective method of programming the PLL multiplier on PC motherboards. The I^2C interface is used to program a nonvolatile register with data that previously was set up using discrete jumpers. Programming allows the configuration to be changed with software, rather than hardware, which simplifies the motherboard setup process and allows the setup to be more automated. The I^2C interface can be programmed with the existing SMBus on the motherboard, and does not require additional, special control, or interface signals. The PCA8550 integrates the functions of several discrete devices into one component, saving board space, power, and overall cost for an optimum solution.

Refer to Table 5 for a summary of features and benefits of the PCA8550.

Table 5. Features and Benefits of the TI PCA8550

FEATURES	BENEFITS
Integrated pullup resistors on SCL, SDA	No need to change I^2C termination resistor values
Integrated pullup resistors on MUX IN inputs	No need to use discrete pullup resistors
2.5-V CMOS MUX OUT outputs	Directly drives P6-family microprocessor inputs without external translation logic
3.3-V CMOS NON-MUX OUT output	Directly drives an LVTTL input without external translation logic
One bit of latched nonmultiplexed output	Prevents changes in the output value during write
I^2C interface	Can be programmed with the SMBus on the motherboard
Nonvolatile register	No need to use discrete programming jumpers
Software programmable	End user does not need to open the case to reconfigure

Frequently Asked Questions (FAQ)

1. Q: What is the PCA8550?

   A: The PCA8550 is a 4-bit 1-of-2 multiplexer with I^2C input interface that integrates the functions of, and is designed to replace, several discrete components on PC motherboards.

2. Q: What is I^2C?

   A: I^2C is a two-wire, open-drain, serial bus that uses a simple master/slave communication protocol. It was developed for inter-integrated-circuit communication.

3. Q: What is SMBus?

   A: SMBus, the System Management Bus is another two-wire, open-drain, serial bus that is based on the principles of the I^2C bus and is optimized for use on PC motherboards.

4. Q: Do I need level translation or current limiting on the output of the PCA8550?

   A: No. The MUX OUT outputs are designed to be 2.5-V outputs that can directly drive the inputs of the P6-family microprocessor interface.

5. Q: What is the factory default for the contents of the nonvolatile register?

   A: All low

Acknowledgment

The authors of this application report are Stephen M. Nolan and Benjamin C. Diem.

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TI, PCA8550 data sheet, literature number SCPS050, March 1999

Glossary

A

APIC — Advanced programmable interrupt controller

$\overline{\text{A20M}}$ — Address 20 mask signal

C

CMOS — Complementary metal-oxide semiconductor

D

DIP — Dual-in-line package

E

EEMUX — EEPROM multiplexer

EEPROM — Electrically erasable programmable read-only memory

I

$\overline{\text{IGNNE}}$ — Ignore numeric error signal

INTR — Maskable interrupt request signal

I^2C — Inter-integrated circuit, an industry-standard, two-wire, open-drain, communications protocol

L

LINT[0] — Local APIC interrupt request signal

LINT[1] — Local APIC interrupt signal

M

MUX — Multiplexer

N

NMI — Nonmaskable interrupt request signal

P

PC	Personal computer
PLL	Phase-lock loop

S

SCL	I^2C serial clock
SDA	I^2C serial data
SMBus	System management bus
SOIC	Plastic small-outline integrated circuit package
SSOP	Shrink small-outline package

T

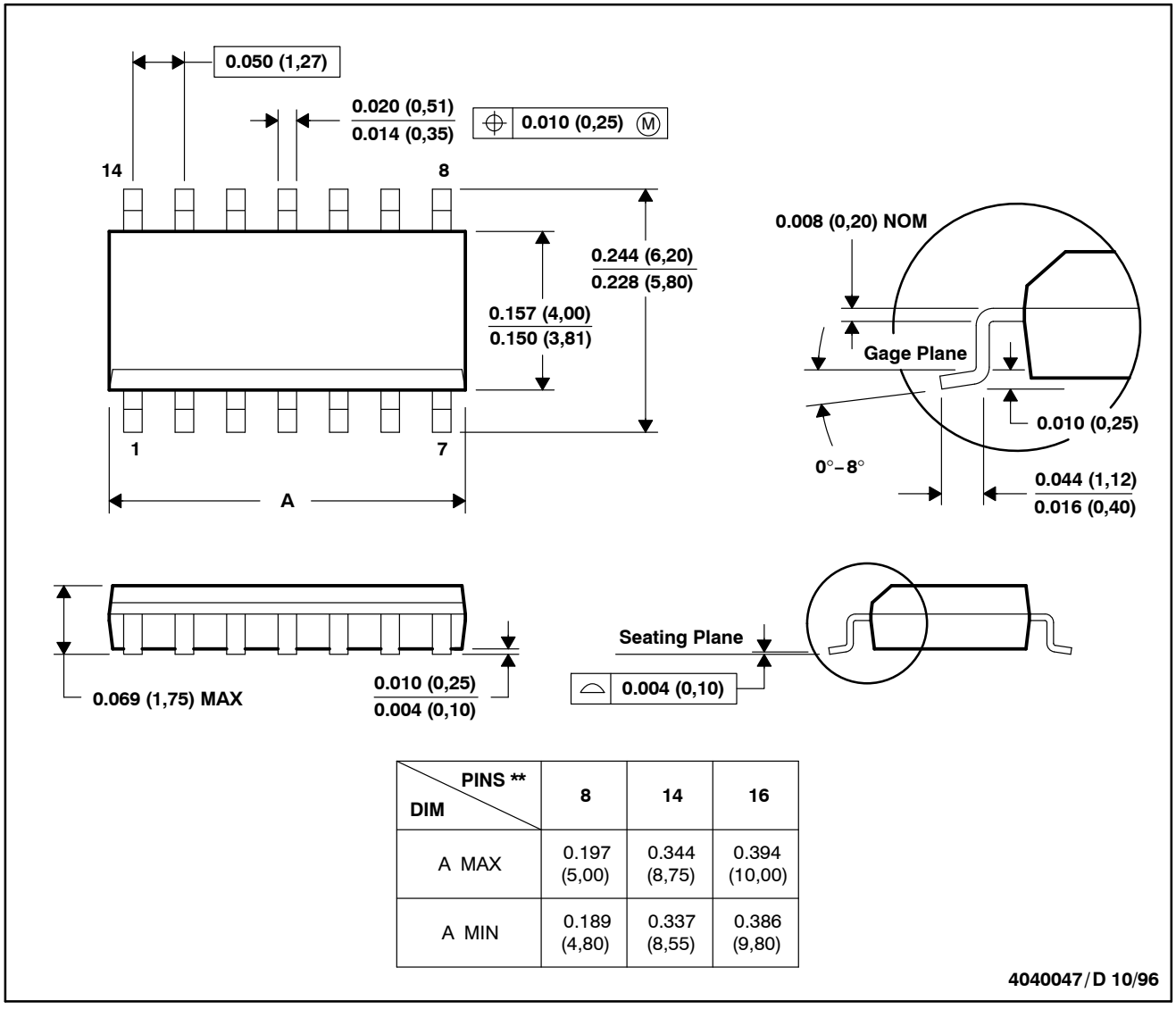
TI	Texas Instruments
TSSOP	Thin shrink small-outline package

Appendix A

Package Outline Drawings

D (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PIN SHOWN



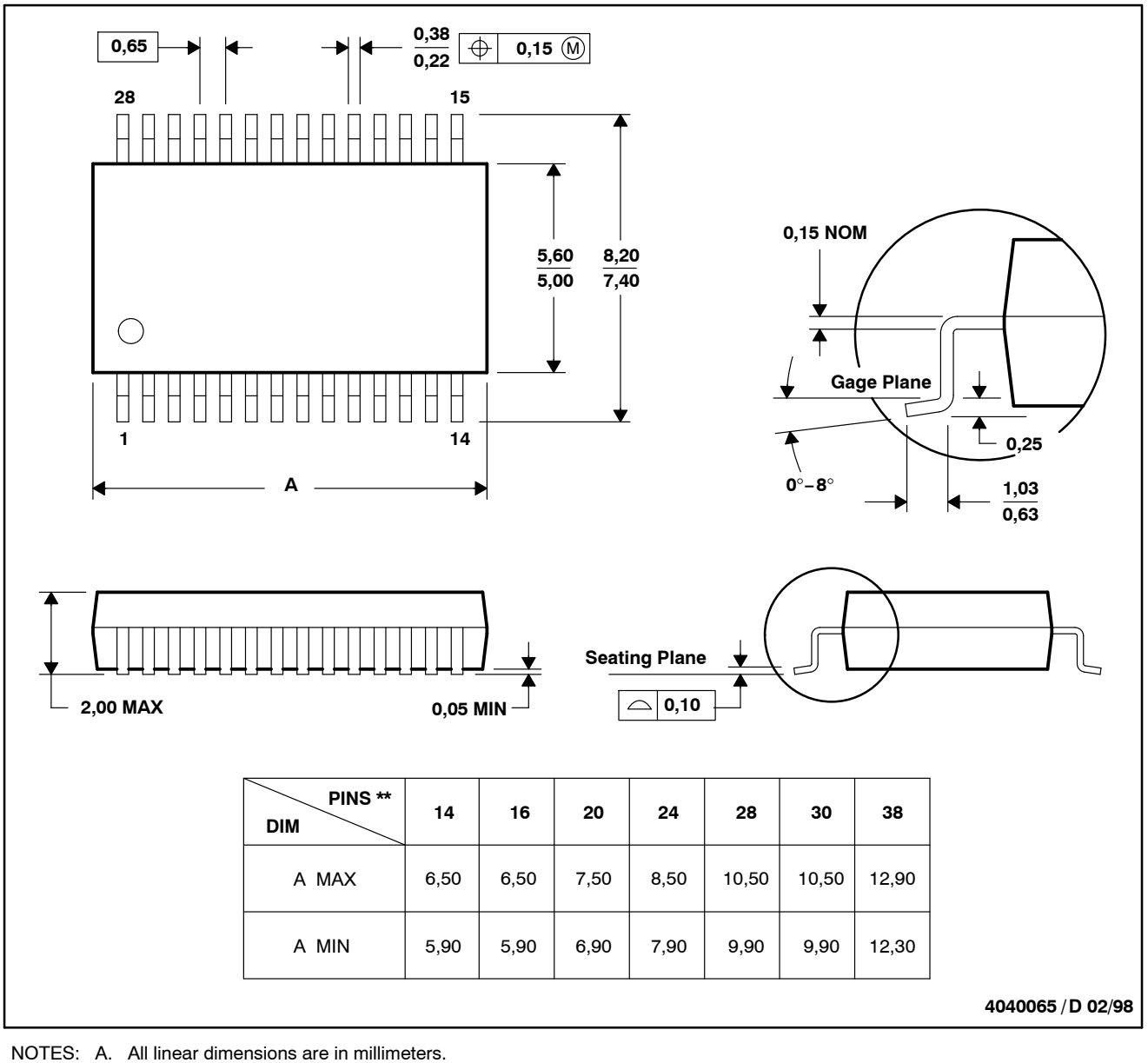
DIM \ PINS **	8	14	16
A MAX	0.197 (5,00)	0.344 (8,75)	0.394 (10,00)
A MIN	0.189 (4,80)	0.337 (8,55)	0.386 (9,80)

4040047/D 10/96

NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0.006 (0,15).
D. Falls within JEDEC MS-012

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

28 PIN SHOWN



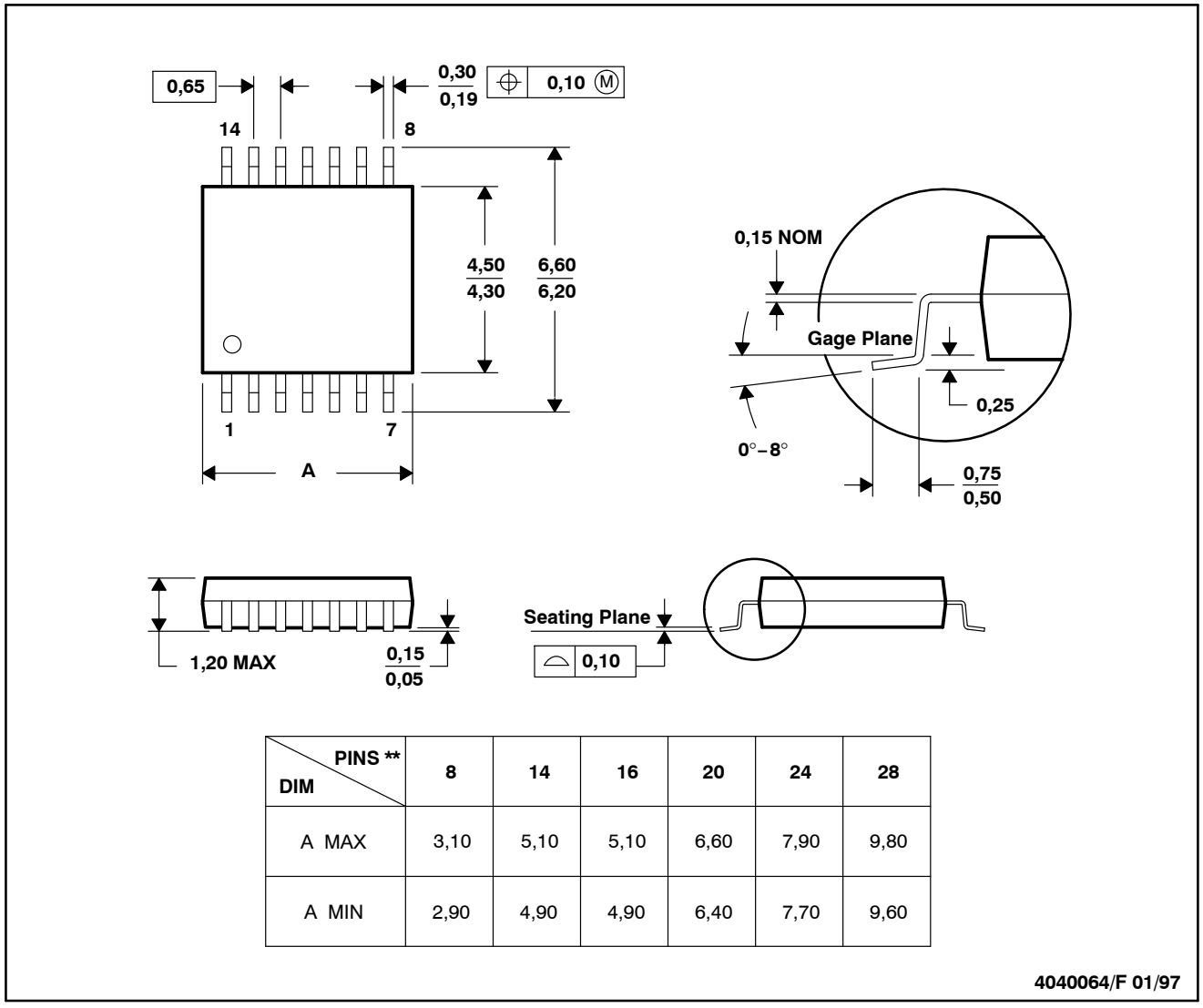
DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 / D 02/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

Insert Tab Here

Logic Solutions for PC100 SDRAM Registered DIMMs

SMOA001A
May 1998

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Introduction

Design of high-performance personal computer (PC) systems that are capable of meeting the needs imposed by modern operating systems and software includes the use of large banks of SDRAMs on DIMMs (see Figure 1). To meet the demands of stable functionality over the broad spectrum of operating environments, meet system timing needs, and to support data integrity, the loads presented by the large banks of SDRAMs on the DIMM modules require the use of buffers/drivers in the address and control signal paths. The PC SDRAM DIMM that is designed to operate at 100 MHz is known to the industry as PC100.[1] This report discusses some of the logic solutions that Texas Instruments (TI™) has available for the registered PC100 DIMM that provide improved performance, cost savings, and design optimization.

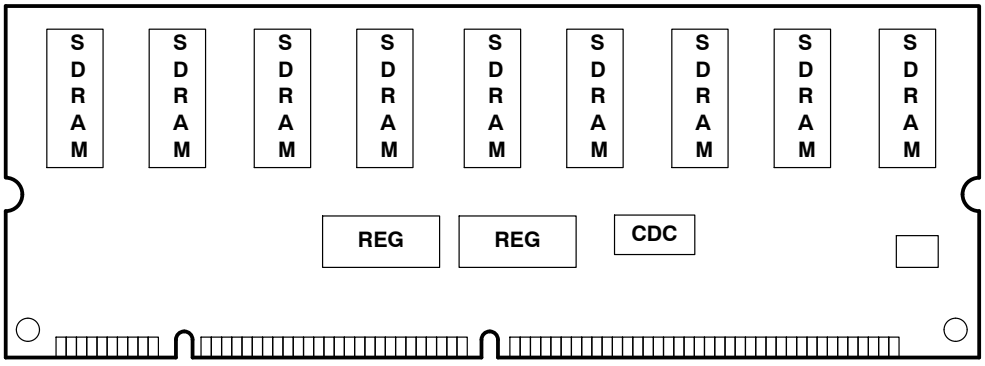


Figure 1. Registered SDRAM DIMM

Background

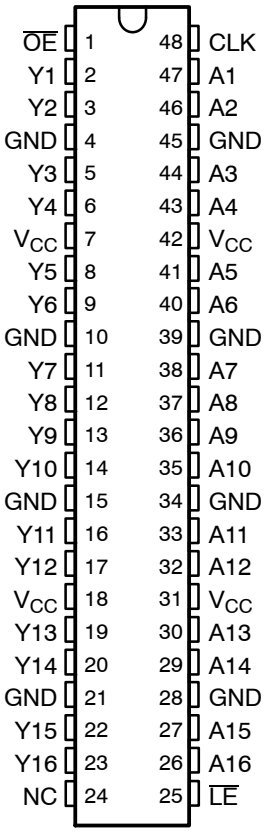
The 168-pin, 8-byte, registered SDRAM DIMM is a JEDEC-defined device.[2] Some of the defined signal paths include data signals, address signals, and control signals (see Table 1). There are up to 36 SDRAM integrated circuits (ICs) on the DIMM, with an SDRAM IC density of up to 128 megabits. This presents a large, highly capacitive load on the address and control signal paths to the memory controller. This load must be buffered with a logic buffer/driver IC. The buffer/driver IC choice that the designer makes is a way of differentiating the DIMM design to provide a competitive edge. The factors that *must* be considered in IC selection include propagation delay time (t_{pd}), input current (I_I), and output current versus voltage (IV) characteristics. But, there are the additional factors of bit-density and glue-logic requirements that, when properly considered, can result in a DIMM design that is simpler, more reliable, and more cost effective. To solve these needs, TI offers the ALVC family of devices. This application report addresses the following devices with respect to this application (see Figure 2):

- SN74ALVC16334[3]
- SN74ALVC162334[4]
- SN74ALVC16835[5]
- SN74ALVC162835[6]
- SN74ALVC162836[7]

Table 1. 168-Pin DIMM Pin Assignments

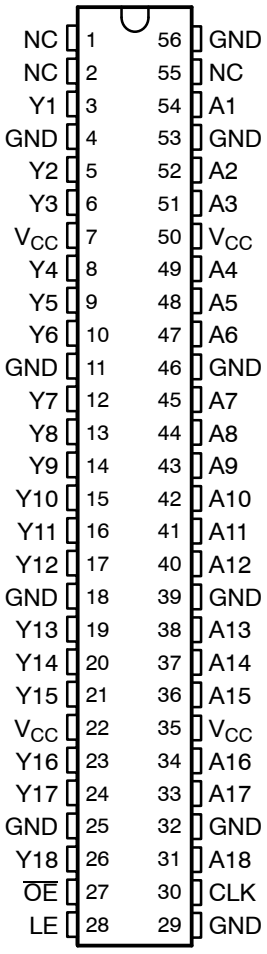
PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME	PIN NO.	SIGNAL NAME
1	V_{SS}	29	DQMB1	57	DQ18	85	V_{SS}	113	DQMB5	141	DQ50
2	DQ0	30	$\overline{S0}$	58	DQ19	86	DQ32	114	$\overline{S1}$	142	DQ51
3	DQ1	31	DU	59	V_{CC}	87	DQ33	115	$\overline{RAS}$	143	V_{CC}
4	DQ2	32	V_{SS}	60	DQ20	88	DQ34	116	V_{SS}	144	DQ52
5	DQ3	33	A0	61	NC	89	DQ35	117	A1	145	NC
6	V_{CC}	34	A2	62	Vref NC	90	V_{CC}	118	A3	146	Vref NC
7	DQ4	35	A4	63	CKE1	91	DQ36	119	A5	147	REGE
8	DQ5	36	A6	64	V_{SS}	92	DQ37	120	A7	148	V_{SS}
9	DQ6	37	A8	65	DQ21	93	DQ38	121	A9	149	DQ53
10	DQ7	38	A10/AP	66	DQ22	94	DQ39	122	BA0	150	DQ54
11	DQ8	39	BA1	67	DQ23	95	DQ40	123	A11	151	DQ55
12	V_{SS}	40	V_{CC}	68	V_{SS}	96	V_{SS}	124	V_{CC}	152	V_{SS}
13	DQ9	41	V_{CC}	69	DQ24	97	DQ41	125	CK1	153	DQ56
14	DQ10	42	CK0	70	DQ25	98	DQ42	126	A12	154	DQ57
15	DQ11	43	V_{SS}	71	DQ26	99	DQ43	127	V_{SS}	155	DQ58
16	DQ12	44	DU	72	DQ27	100	DQ44	128	CKE0	156	DQ59
17	DQ13	45	$\overline{S2}$	73	V_{CC}	101	DQ45	129	$\overline{S3}$	157	V_{CC}
18	V_{CC}	46	DQMB2	74	DQ28	102	V_{CC}	130	DQMB6	158	DQ60
19	DQ14	47	DQMB3	75	DQ29	103	DQ46	131	DQMB7	159	DQ61
20	DQ15	48	DU	76	DQ30	104	DQ47	132	A13	160	DQ62
21	CB0	49	V_{CC}	77	DQ31	105	CB4	133	V_{CC}	161	DQ63
22	CB1	50	NC	78	V_{SS}	106	CB5	134	NC	162	V_{SS}
23	V_{SS}	51	NC	79	CK2	107	V_{SS}	135	NC	163	CK3
24	NC	52	CB2	80	NC	108	NC	136	CB6	164	NC
25	NC	53	CB3	81	WP	109	NC	137	CB7	165	SA0
26	V_{CC}	54	V_{SS}	82	SDA	110	V_{CC}	138	V_{SS}	166	SA1
27	$\overline{WE}$	55	DQ16	83	SCL	111	$\overline{CAS}$	139	DQ48	167	SA2
28	DQMB0	56	DQ17	84	V_{CC}	112	DQMB4	140	DQ49	168	V_{CC}

SN74ALVC16334
OR
SN74ALVC162334



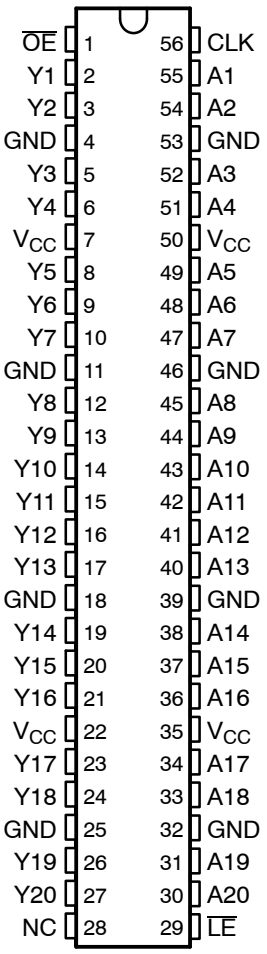
NC – No internal connection

SN74ALVC16835
OR
SN74ALVC162835



NC – No internal connection

SN74ALVC162836



NC – No internal connection

Figure 2. Pinouts (Top View)

Device Information

The devices being examined are members of the Texas Instruments Widebus™ family. They are manufactured using TI's EPIC™ (Enhanced-Performance Implanted CMOS) submicron process. These devices provide ESD protection exceeding 2000 V per MIL-STD-883, Method 3015, and exceeding 200 V using machine model (C = 200 pF, R = 0).

The SN74ALVC16334 and SN74ALVC162334 devices are 16-bit universal bus drivers with 3-state outputs, designed for 2.3-V to 3.6-V V_{CC} operation (see Table 2 and Figure 3). When the active-low latch-enable ($\overline{LE}$) input is low, the device operates in the transparent mode and the Y outputs follow the A inputs. If the clock (CLK) input is held in a high or low state, the device operates like a D-type latch, and the Y output data is latched when $\overline{LE}$ is taken high. If the CLK input is clocked when $\overline{LE}$ is high, the Y output data is stored in the flip-flop on the low-to-high transition of CLK. The 3-state outputs are controlled by the active-low output-enable ($\overline{OE}$) input. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are enabled. The SN74ALVC162334 also provides equivalent 26-Ω series resistors on the output port. Both the SN74ALVC16334 and SN74ALVC162334 devices are offered in 48-pin packages, which reduces the amount of required board space, as compared with the other devices being examined.

Table 2. Function Table for SN74ALVC16334 and SN74ALVC162334 Devices

INPUTS				OUTPUT
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L	X	Y_0†

† Output level before the indicated steady-state input conditions were established

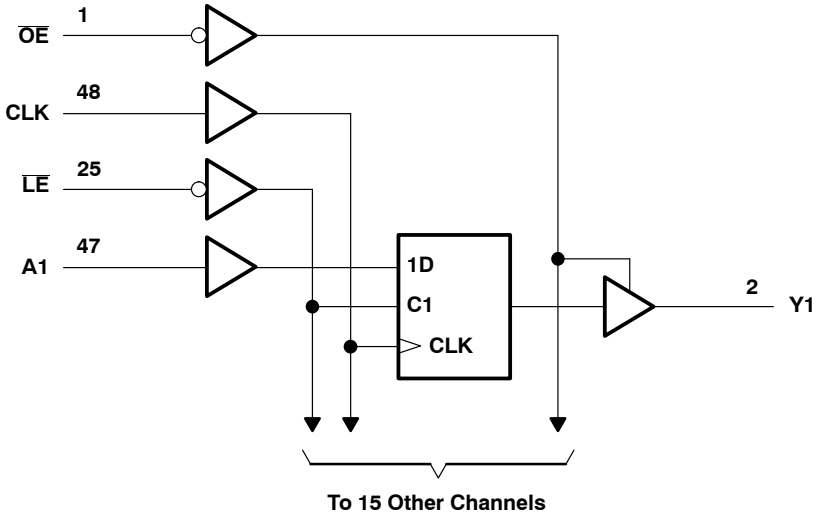


Figure 3. Logic Diagram for SN74ALVC16334 and SN74ALVC162334 Devices

EPIC and Widebus are trademarks of Texas Instruments Incorporated.

The SN74ALVC16835 and SN74ALVC162835 devices are 18-bit universal bus drivers with 3-state outputs, designed for 2.3-V to 3.6-V V_{CC} operation (see Table 3 and Figure 4). When LE is high, the device operates in the transparent mode and the Y outputs follow the A inputs. If CLK is held in a high or low state, the device operates like a D-type latch, and the Y output data is latched when LE is taken low. If CLK is clocked when LE is low, the Y output data is stored in the flip-flop on the low-to-high transition of CLK. The 3-state outputs are controlled by the $\overline{OE}$. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are enabled. The SN74ALVC162835 also provides 26-Ω equivalent series resistors on the output port.

Table 3. Function Table for SN74ALVC16835 and SN74ALVC162835 Devices

INPUTS				OUTPUT
$\overline{OE}$	LE	CLK	A	Y
H	X	X	X	Z
L	H	X	L	L
L	H	X	H	H
L	L	↑	L	L
L	L	↑	H	H
L	L	L	X	Y_0†

† Output level before the indicated steady-state input conditions were established.

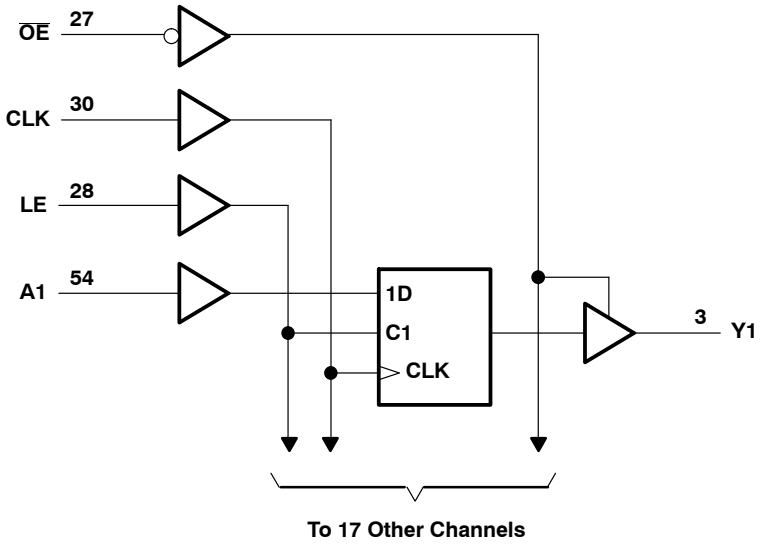


Figure 4. Logic Diagram for SN74ALVC16835 and SN74ALVC162835 Devices

The SN74ALVC162836 device is a 20-bit universal bus driver with 3-state outputs, designed for 2.3-V to 3.6-V V_{CC} operation (see Table 4 and Figure 5). When $\overline{LE}$ is low, the device operates in the transparent mode and the Y outputs follow the A inputs. If CLK is held in a high or low state, the device operates like a D-type latch, and the Y output data is latched when $\overline{LE}$ is taken high. If CLK is clocked when $\overline{LE}$ is high, the Y output data is stored in the flip-flop on the low-to-high transition of CLK. The 3-state outputs are controlled by $\overline{OE}$. When $\overline{OE}$ is high, the outputs are in the high-impedance state. When $\overline{OE}$ is low, the outputs are enabled. The SN74ALVC162836 also provides 26-Ω equivalent series resistors on the output port.

Table 4. Function Table for SN74ALVC162836 Device

INPUTS				OUTPUT
$\overline{OE}$	$\overline{LE}$	CLK	A	Y
H	X	X	X	Z
L	L	X	L	L
L	L	X	H	H
L	H	↑	L	L
L	H	↑	H	H
L	H	L	X	Y_0†

† Output level before the indicated steady-state input conditions were established

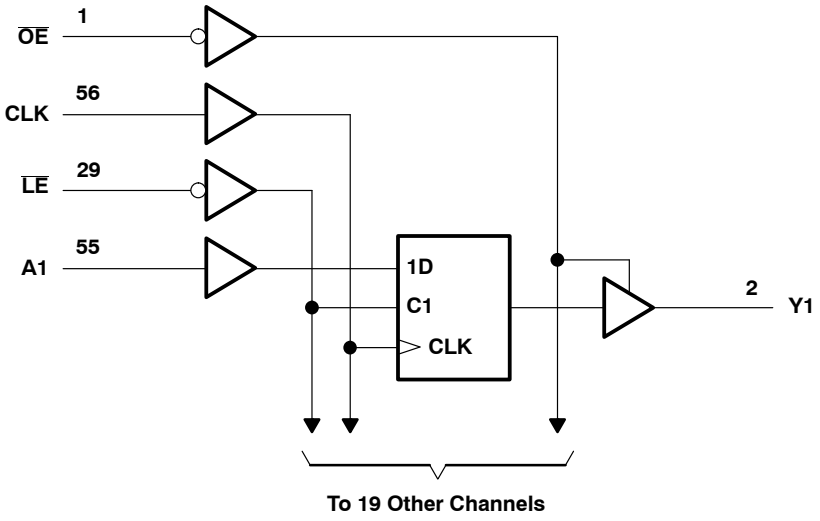


Figure 5. Logic Diagram for SN74ALVC162836 Device

The logic functionality of these devices is similar with one exception: the polarity of the latch-enable input. The ’835 function uses an active-high latch-enable control input, while the ’334 and ’836 functions use an active-low latch-enable control input. The latch-enable input is controlled, in the DIMM application, by the register enable (REGE) signal from the motherboard. REGE, when low, permits the DIMM to operate in the buffered mode. When REGE is high, the DIMM operates in the registered mode. REGE performs the logical-inverse function of the LE signal. To utilize an ’835-type device, an inverter is necessary between the DIMM’s REGE pin and the ’835 IC’s LE pin (see Figure 6). The SN74AHC microgate, packaged in the plastic small-outline transistor (SOT) package, is an ideal single-gate device for the inverter application. When utilizing the ’334- and ’836-type devices, the $\overline{\text{LE}}$ control input performs the *same* logical function as the REGE signal, and therefore, no inverter is necessary (see Figure 7). The elimination of an inverter from the DIMM by the choice of a ’334- or ’836-type device saves board space, simplifies board layout and trace routing, decreases costs, and increases the reliability of the DIMM. The use of the ’334 furthers these benefits by utilizing a 48-pin package, as opposed to the 56-pin package.

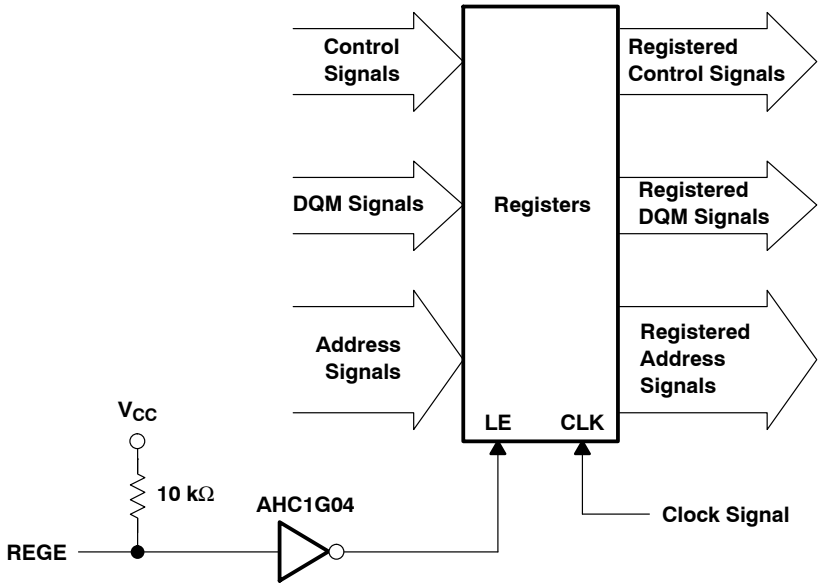


Figure 6. Inverted REGE Wiring for SN74ALVC16835 and SN74ALVC162835 Devices

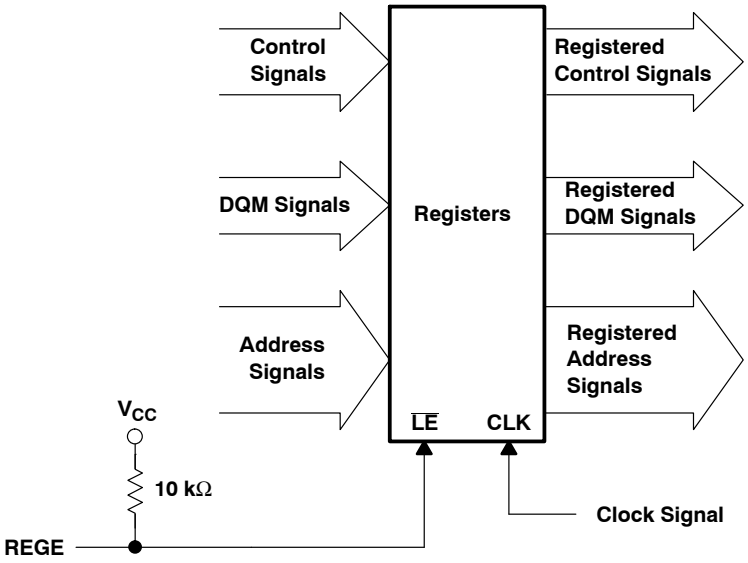


Figure 7. Straight-In REGE Wiring for SN74ALVC16334, SN74ALVC162334, and SN74ALVC162836 Devices

The bit density of the buffer/register IC should be considered when selecting a device for a DIMM design. The use of ICs with bit densities that result in the least number of unused inputs results in the most economical and optimal design.

The 64-MB DIMM has 28 signals that must pass through the buffer/register. The use of two 18-bit devices, like the ’835, results in eight unused bits; this is not an optimal solution. The use of two 16-bit devices, like the ’334, on the 64-MB DIMM would result in only four unused bits. While not an ideal bit density for the application, it represents a significant improvement (see Figure 8).

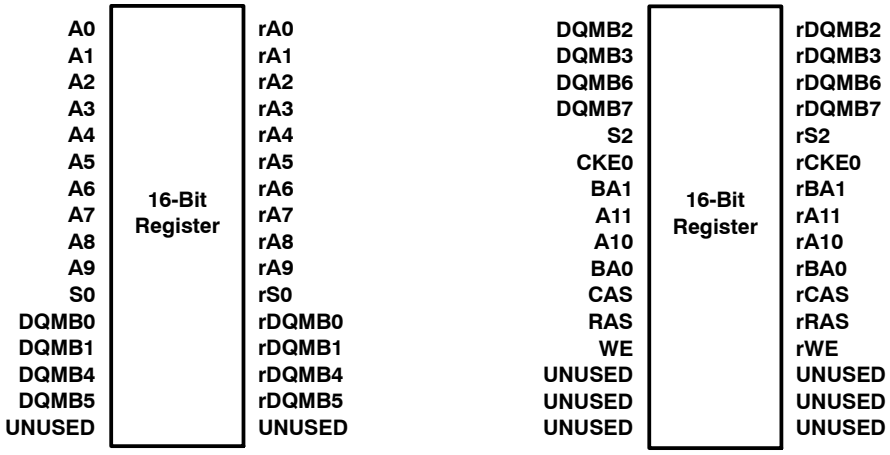


Figure 8. 64-MB DIMM Register Wiring

The 128-MB DIMM has 29 signals that must pass through the buffer/register. The use of two 18-bit devices, like the ’835, results in seven unused bits. The use of two 16-bit devices, like the ’334, on the 128-MB DIMM, would result in only three unused bits (see Figure 9).

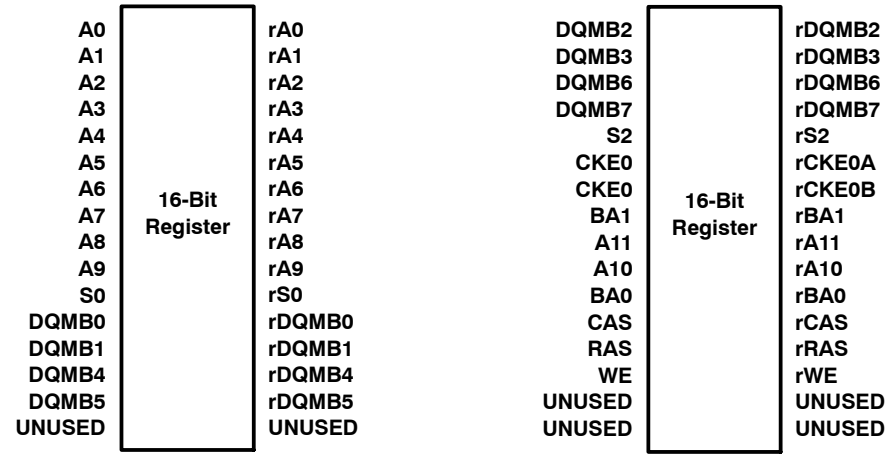


Figure 9. 128-MB DIMM Register Wiring

The 256-MB and 512-MB DIMMs have 50 signals that must pass through the buffer/register. The use of three 18-bit devices, like the ’835, results in four unused bits. The use of two 16-bit devices, like the ’334, and one 20-bit device, like the ’836, results in only two unused bits (see Figure 10).

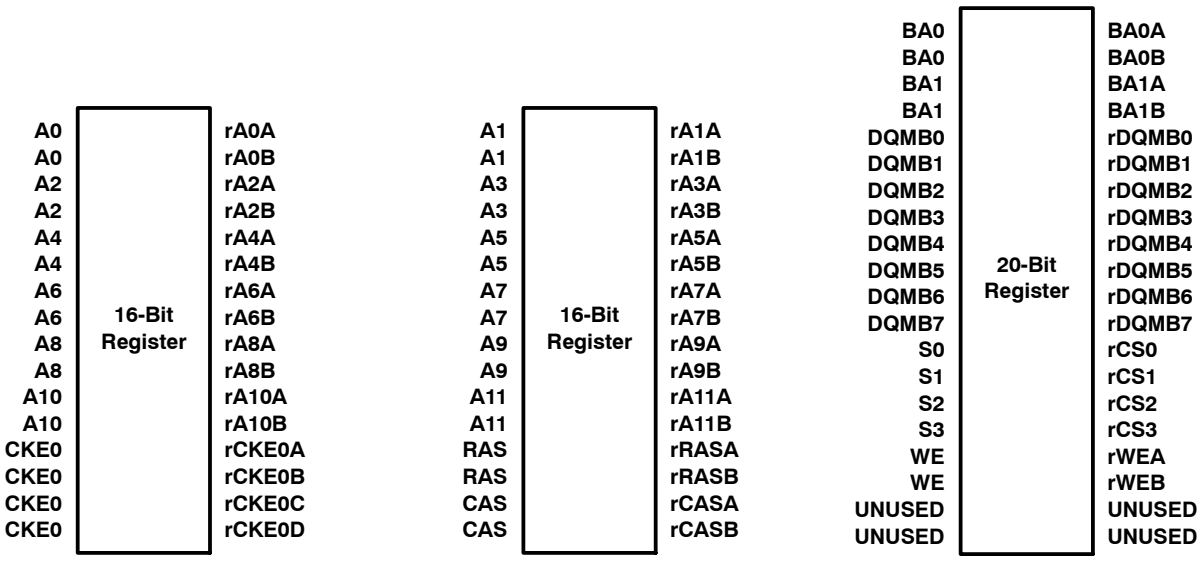


Figure 10. 256-MB and 512-MB DIMM Register Wiring

Minimizing the number of unused inputs becomes particularly important when considering the specifics of the DIMM application. Due to contention with the weak pullups in the output circuit of the memory controller, the buffer/register device *cannot* utilize bus hold on the inputs. Since unused CMOS inputs *must* be held at a valid logic high or low voltage, pullup or pulldown resistors are required on any unused buffer/register inputs.

Examination of the electrical characteristics of the outputs is a critical portion of a successful DIMM design. The output must have an output impedance that minimizes overshoots and undershoots for signal integrity. The selection of a component with equivalent 26-Ω series damping resistors on the output port is sometimes necessary to improve the impedance match with the distributed load of the DIMM. The opposing characteristic that must be considered is having sufficient drive to meet the timing requirements. Typically, in a CMOS totem-pole output structure, the p-channel pullup transistor is weaker than the n-channel pulldown transistor. Therefore, the factor to analyze with regard to output drive capability is I_{OH}, as the t_{PLH} time is the limiting factor to the device t_{pd}. The ’334 and ’836 devices have a p-channel output transistor that is almost twice as strong as the pullup output of the ’835 device. This results in much better overall electrical characteristics for this application. To aid the design engineer in analysis of electrical characteristics, TI makes IBIS models available on the Internet. The latest versions of IBIS models can be obtained from TI’s website, at http://www.ti.com.

Tables 5 through 9 show component specifications for products included in this report. Figures 11 through 15 show output characteristic comparisons to the Intel™ PC100 requirement

Intel is a trademark of Intel Corporation.

Table 5. SN74ALVC16334 Component Specifications

PARAMETER	CONDITIONS		SN74ALVC16334 V_{CC} = 3.3 V ± 0.3 V, T_A = −40°C to 85°C		UNIT
			MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1	4.1	ns
I_I	$V_I = V_{CC}$ or GND			±5	μA

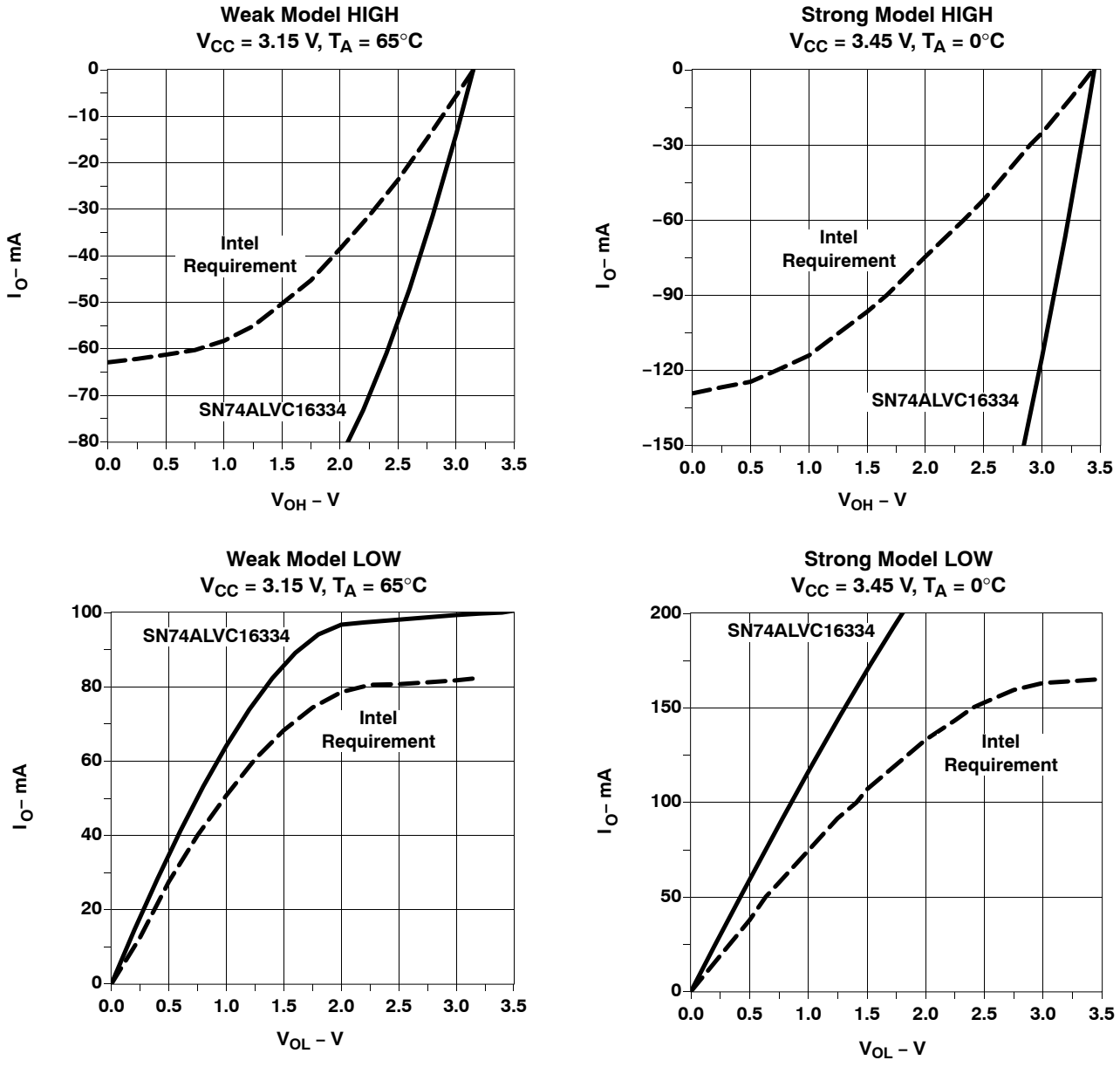


Figure 11. IV Characteristics for SN74ALVC16334 Register Output

Table 6. SN74ALVC162334 Component Specifications

PARAMETER	CONDITIONS		SN74ALVC162334 V_{CC} = 3.3 V ± 0.3 V, T_A = −40°C to 85°C		UNIT
			MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1	4.9	ns
I_I	$V_I = V_{CC}$ or GND			±5	µA

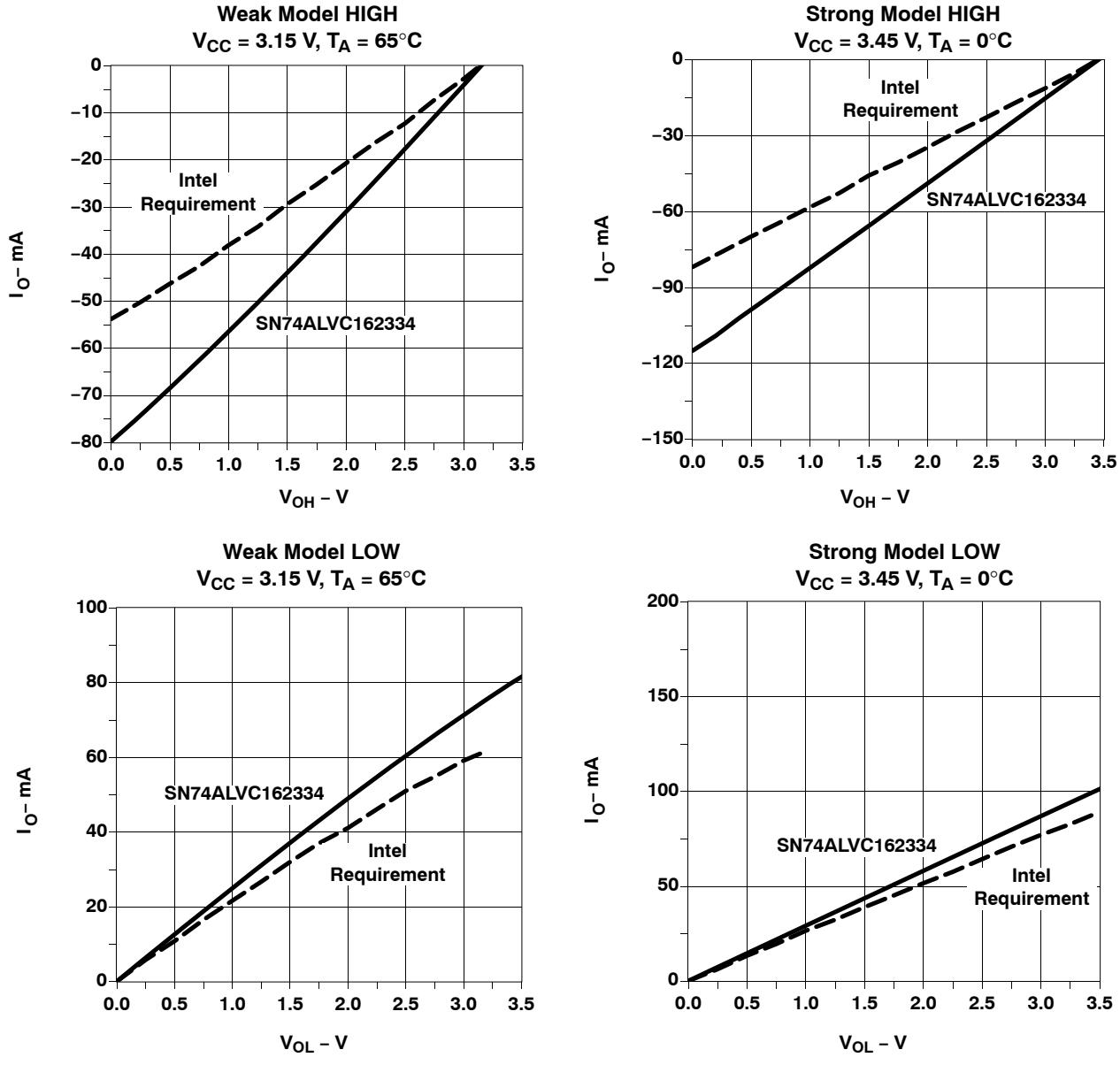


Figure 12. IV Characteristics for SN74ALVC162334 Register Output

Table 7. SN74ALVC16835 Component Specifications

PARAMETER	CONDITIONS		INTEL REQUIREMENTS V_{CC} = 3.3 V ± 0.15 V, T_A = 0°C to 65°C		SN74ALVC16835 V_{CC} = 3.3 V ± 0.15 V, T_A = 0°C to 65°C		UNIT
			MIN	MAX	MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1.7	4.5	1.7	4.5	ns
I_I	$V_I = V_{CC}$ or GND			±10		±5	µA

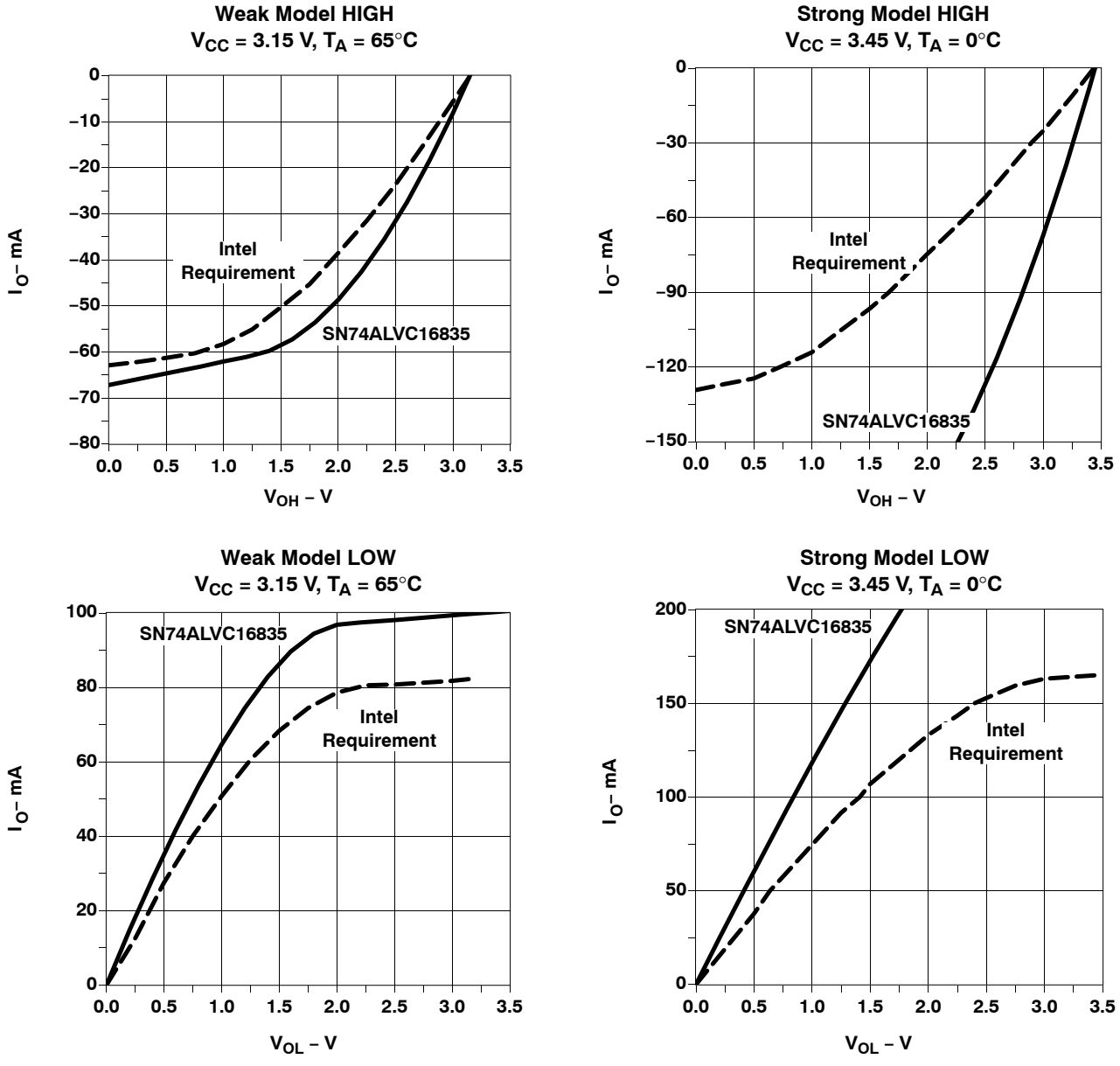


Figure 13. IV Characteristics for SN74ALVC16835 Register Output

Table 8. SN74ALVC162835 Component Specifications

PARAMETER	CONDITIONS		SN74ALVC162835 V_{CC} = 3.3 V ± 0.15 V T_A = −40°C to 85°C		UNIT
			MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1.4	5.4	ns
I_I	$V_I = V_{CC}$ or GND			±5	µA

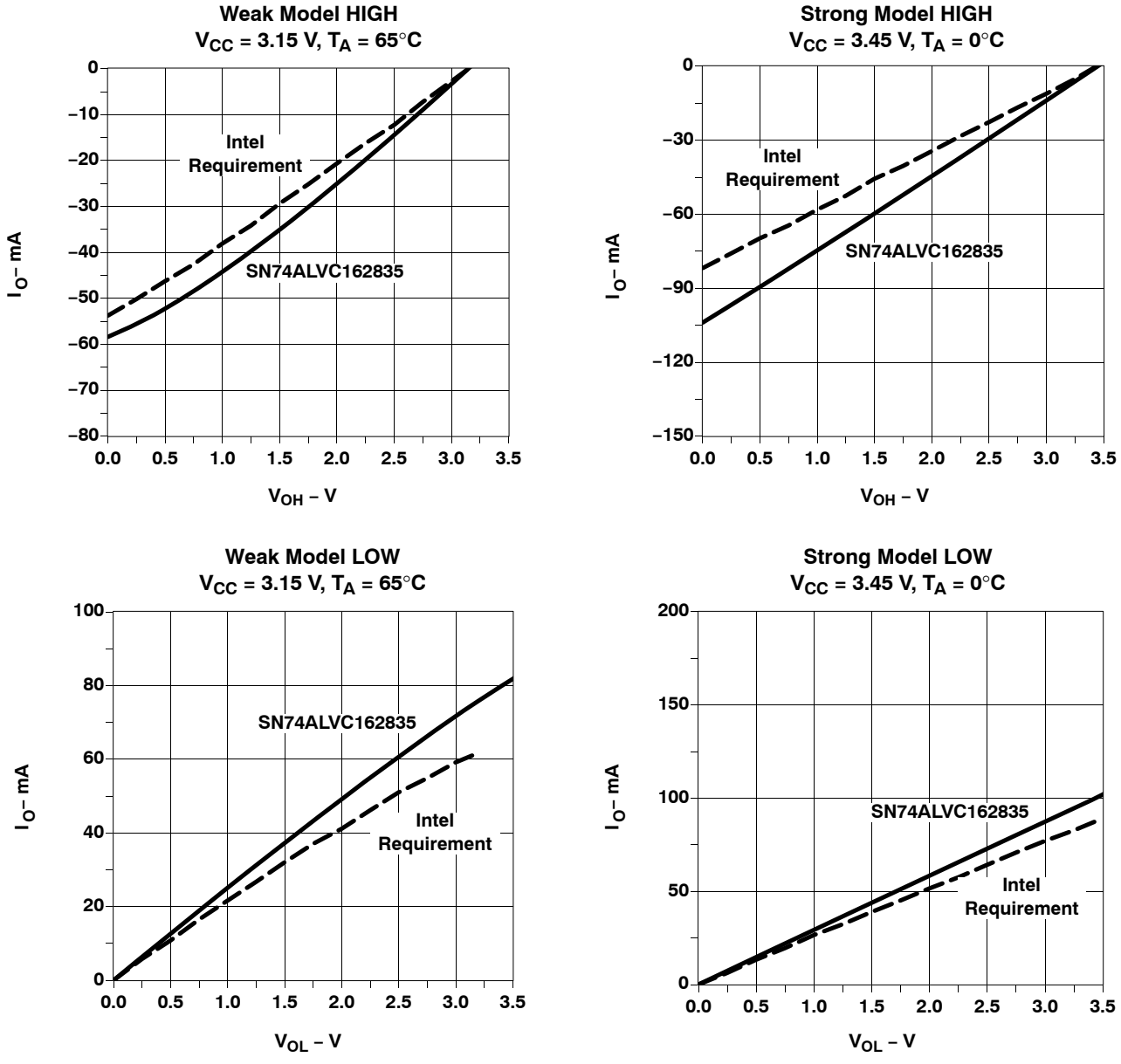


Figure 14. IV Characteristics for SN74ALVC162835 Register Output

Table 9. SN74ALVC162836 Component Specifications

PARAMETER	CONDITIONS		SN74ALVC162836 V_{CC} = 3.3 V ± 0.15 V, T_A = −40°C to 65°C		UNIT
			MIN	MAX	
t_{pd}	From (input) clock	To (output) Y	1.1	5	ns
I_I	$V_I = V_{CC}$ or GND			±5	μA

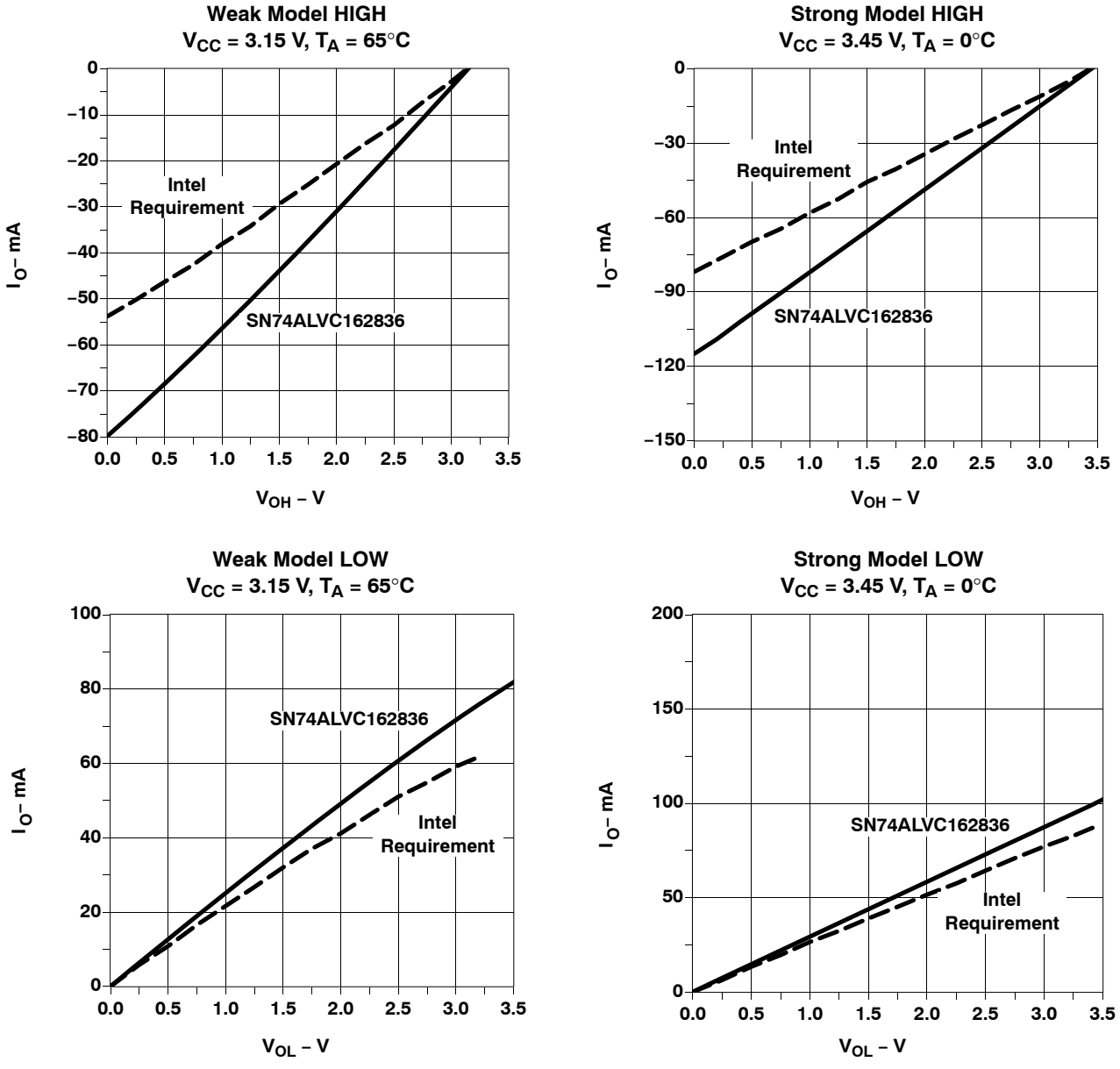
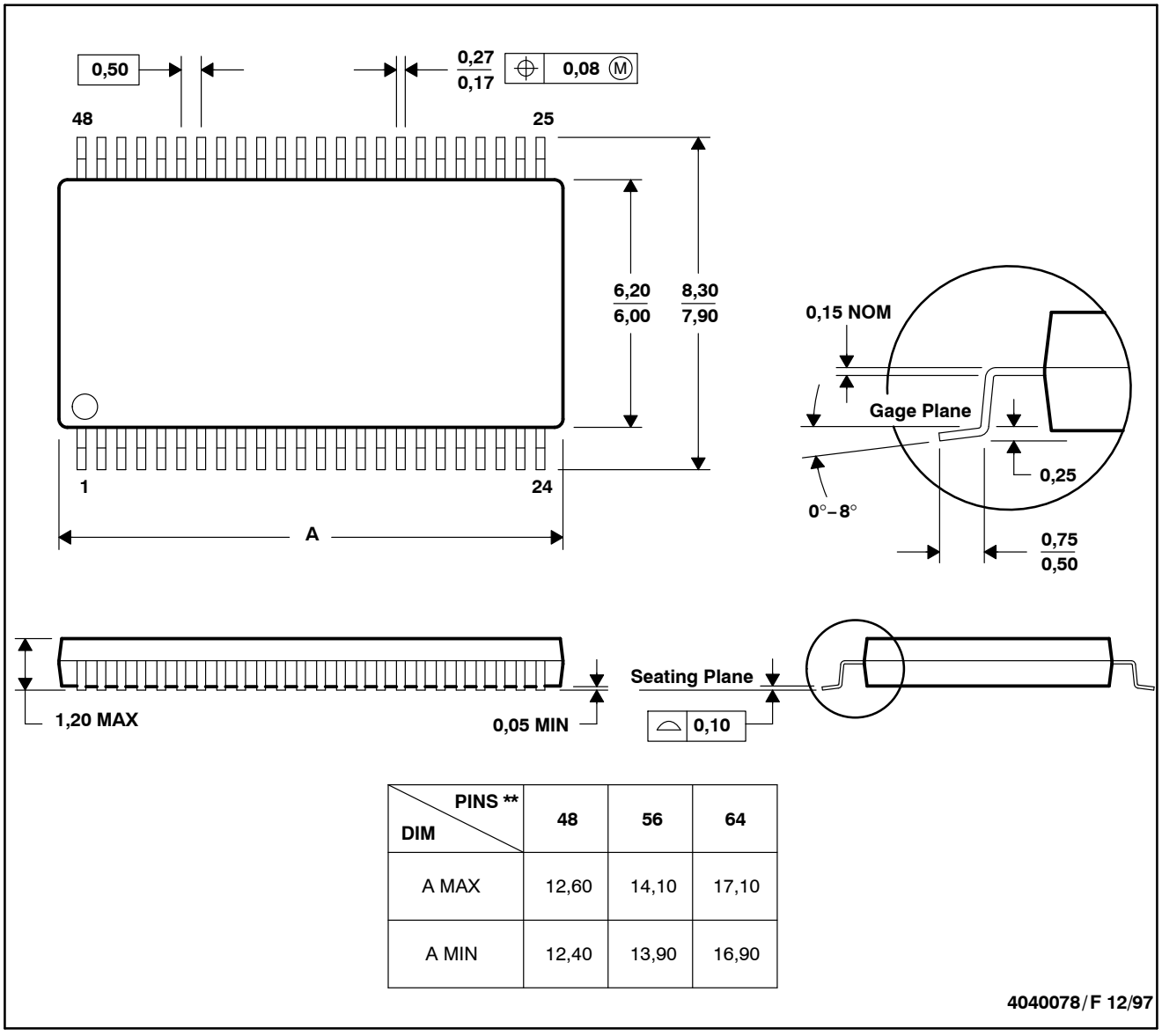


Figure 15. IV Characteristics for SN74ALVC162836 Register Output

All of the devices considered are available in the JEDEC standard SSOP (DL), TSSOP (DGG), and TVSOP (DGV) packages.[8] The mechanical data for the TSSOP (DGG) is shown in Figure 16.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48-PIN SHOWN



PINS ** / DIM	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion, which should not exceed 0,15.
D. Falls within JEDEC MO-153

Figure 16. Package Outline

Benefits of Alternative Solutions

Evaluating an alternative buffer/driver IC solution is a way of differentiating the DIMM design from the standard reference design to provide a competitive edge. Tables 10 and 11 include many of the factors to be considered.

Table 10. Features

DEVICE	PINS	BITS	LE LOGIC	SERIES RESISTOR
ALVC16334	48	16	$\overline{LE}$ = REGE	No
ALVC162334	48	16	$\overline{LE}$ = REGE	Yes
ALVC16835	56	18	LE ≠ REGE	No
ALVC162835	56	18	LE ≠ REGE	Yes
ALVC162836	56	20	$\overline{LE}$ = REGE	Yes

Table 11. Benefits

DEVICE	DRIVE	EXTERNAL LOGIC	SERIES-DAMPING RESISTOR	UNUSED INPUTS
ALVC16334	High	No added inverter cost	External resistor necessary for impedance match	Minimum pullups
ALVC162334	High	No added inverter cost	Better impedance match No external resistor cost	Minimum pullups
ALVC16835	Low	Added inverter cost	External resistor necessary for impedance match	Additional pullups
ALVC162835	Low	Added inverter cost	Better impedance match No external resistor cost	Additional pullups
ALVC162836	High	No added inverter cost	Better impedance match No external resistor cost	Minimum pullups

After reviewing the factors shown in Tables 10 and 11, the devices in Table 12 should be considered for application component selection.

Table 12. Application Component Selection

DIMM SIZE IN MEGABYTES	COMPONENT SELECTION
64	ALVC162334 × 2
128	ALVC162334 × 2
256	ALVC162334 × 2 + ALVC162836 × 1
512	ALVC162334 × 2 + ALVC162836 × 1

Differentiating the DIMM design from the standard reference design by considering the components listed in Table 12 can help provide a more cost-effective design. By choosing a component that has improved matching of bit density to the number of signals to be buffered/registered, a number of pullup resistors can be eliminated from the board. By choosing a component that uses an $\overline{LE}$ control input, which logically is the same as the REGE signal, an inverter can be eliminated from the design. These improvements save board space, simplify board layout and trace routing, decrease costs, and increase the reliability of the DIMM. Selecting a component with improved output drive characteristics simplifies the design engineer's job of ensuring signal integrity and meeting timing requirements.

Conclusion

The PC100 design originated before the availability of the SN74ALVC16334, SN74ALVC162334, and SN74ALVC162836 devices. The SN74ALVC16835 and SN74ALVC162835 were the only parts available that fit the application at the start of the project. TI has since offered these additional components for use in the PC SDRAM registered DIMM. With respect to performance, cost effectiveness, and design optimization, the ’334, ’2334, and ’2836 devices represent an optimal choice over the ’835 and ’2835.

Glossary

A

ALVC Advanced low-voltage CMOS

C

CMOS Complementary metal-oxide semiconductor

D

DIMM Dual in-line memory module

DQM Data mask

E

ESD Electrostatic discharge

I

I_I Input current

I_{OH} High-level output current

IV Current vs. voltage

J

JEDEC Joint Electronic Device Engineering Council

L

LE Active-high latch enable

$\overline{LE}$ Active-low latch enable

P

PC Personal computer

R

REGE Register enable

S

SDRAM Synchronous dynamic random-access memory

SOT Small outline transistor

T

TI™ Texas Instruments Incorporated

t_{pd} Propagation delay time

t_{PLH} Propagation delay time, low-to-high level output

TSSOP Thin shrink small-outline package

Acknowledgment

The authors of this application report are Ji Park, Stephen M. Nolan, and David Yaeger.

References

1. Intel PC SDRAM Registered DIMM Specification (Revision 1.0), February 1998
2. JEDEC Letter Ballot # 42.5-96-146A
3. TI SN74ALVC16334 16-Bit Universal Bus Driver With 3-State Outputs, literature number SCES128B, May 1998
4. TI SN74ALVC162334 16-Bit Universal Bus Driver With 3-State Outputs, literature number SCES127B, May 1998
5. TI SN74ALVC16835 18-Bit Universal Bus Driver With 3-State Outputs, literature number SCES125B, May 1998
6. TI SN74ALVC162835 18-Bit Universal Bus Driver With 3-State Outputs, literature number SCES126C, May 1998
7. TI SN74ALVC162836 20-Bit Universal Bus Driver With 3-State Outputs, literature number SCES129A, May 1998
8. TI *Semiconductor Group Package Outlines*, literature number SSYU001D, 1998

SSTL for DIMM Applications

SCBA014
December 1997

TEXAS INSTRUMENTS

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Introduction

The stub series-terminated logic (SSTL) interface standard is intended for high-speed memory interface applications and specifies switching characteristics such that operating frequencies up to 200 MHz are attainable. The primary application for SSTL devices is to interface with SDRAMs.

Texas Instruments (TI™) is the first logic vendor to design and produce a device that meets the SSTL switching standard. Currently, customers are successfully using the only available SSTL device, TI's SSTL16837, to interface to SDRAMs on dual in-line memory modules (DIMMs). As operating frequencies increase and as the demand for faster memory interfaces continues to grow, a wide acceptance of the SSTL interface standard is anticipated. With this in mind, TI is committed to providing the required functionality to meet and exceed customer expectations.

This application report discusses the SSTL interface standard and, in particular, the SSTL16837. This device is not only the first SSTL-compliant device on the market, but is also the only SSTL device currently being manufactured. (TI released the SSTL16837 to production in 2Q97 and plans to release the SSTL16847 in 1Q98.) The main topics discussed in this application report are:

- Background
- Technology and design
- Uniqueness of device
- Features
- Typical design applications
- Laboratory testing technique
- Results
- Competition analysis
- SPICE/IBIS models
- Package information
- Frequently asked questions
- Conclusion
- Glossary
- References

Background

The problem is simple. Designers are constantly trying to get the most out of their designs in the most cost-effective means. As faster versions of a particular CPU become available, the designer will often try to improve the throughput of an existing design simply by increasing the CPU clock frequency.[1]

After a certain point, the speed of the system's main memory...becomes the limiting factor in the throughput of the system.... [1]

Of course, this problem can be fixed through the use of fast main memory. The only question remaining is what speed of main memory must be used to support the fastest possible operation.[1]

These issues resulted in JEDEC defining the first official SSTL switching standard. This standard (JC-16-97-04) specified a supply voltage equal to 3.3 V and was accepted by JEDEC in early 1997.

The standard specified a particular termination scheme with appropriate values for the resistors and capacitor. Two resistors in parallel are used to establish a voltage level such that differential voltage swings can be utilized and two may be utilized and two different resistor value configurations are acceptable. Class I specifies an acceptable value of 50 ohms for the terminating resistor

R_T, and Class II specifies an acceptable value of 25 ohms. The standard states that for each value of R_T, a capacitive load equal to 10 pF or 30 pF can be used. Additionally, a series resistor R_S is specified at 25 ohms.

Figure 1 illustrates a simplified output buffer/driver, Class II environment for a SSTL device.

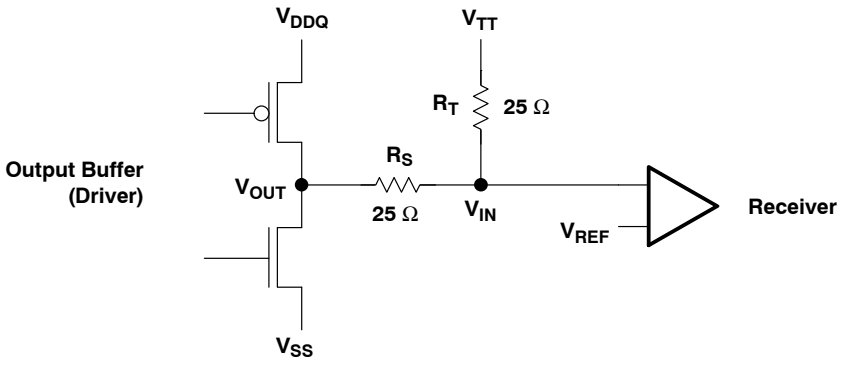

Figure 1. SSTL Simplified Output Buffer/Driver, Class II Environment

Core supply voltages are migrating from 5 V to 3.3 V. As this trend continues, manufacturers have begun to use 2.5-V supply levels and are beginning to consider supply voltages of 1.8 V. Memory supply-voltage levels generally tend to lag core-supply voltages, and although memory is still predominantly at a 5-V supply level, memory is beginning to migrate to 3.3 V eventually reaching the 2.5-V and 1.8-V supply-voltage levels. The need for a 2.5-V specification for SSTL was foreseen and as a result, JEDEC defined a 2.5-V SSTL specification (JC-16-97-58). The primary differences between the 3.3-V and the 2.5-V SSTL specifications are provided in Table 1.

Table 1. Convention for 3.3-V Versus 2.5-V SSTL Device Identification

PARAMETER	V_{CC} = 3.3 V	V_{CC} = 2.5 V
V_{REF}	1.5	1.25
V_{IH}(min)	V_{REF} + 0.2	V_{REF} + 0.18
V_{IL}(max)	V_{REF} – 0.2	V_{REF} – 0.18

As noted in Table 1, the values of V_{REF} and the corresponding differential input ranges vary from 3.3 V to 2.5 V. For the 3.3-V specification, the reference voltage is 1.5 V with the magnitude of the differential from the reference voltage to an input high or low level being 200 mV. The 2.5-V specification utilizes a reference voltage of 1.25 V with the magnitude of the differential from the reference voltage to an input high or low level being 180 mV.

Technology and Design

The SSTL16837 is a 3.3-V BiCMOS device with differential inputs. To reduce the power consumption of the device, all of the data inputs, as well as the output-enable pin, are CMOS. For speed considerations, the latch-enable and clock-input pins are BiCMOS. The output circuitry is a totem-pole CMOS design, but is converted to SSTL levels by using the appropriate configuration and values of the resistors R_S and R_T, as shown in Figure 1.

Uniqueness of Device

The SSTL16837 is a 20-bit universal bus driver (UBD) with 3-state outputs. As a UBD, it can operate in three different modes: transparent, latch, and flip-flop. In the transparent mode, the device operates as a flow-through buffer when the latch-enable pin is not activated. In the latch mode, input data is latched if the latch-enable pin is activated and the clock is held at a high or low level. In the flip-flop mode, input data is stored in the flip-flop on the low-to-high transition of the clock.

The SSTL16837 was designed to reduce power consumption. A bias generator was specifically added to the circuitry to adjust for variances in process, temperature, and V_{CC}. Additionally, the device pinout is arranged for reduced noise, e.g., control inputs (the reference voltage, the output enable, the latch enable, and the clock) are positioned so that package parasitics would be reduced and less power consumed. The clock input was centered to minimize the clock-to-Y propagation delay variances in all output pins.

The SSTL16837 promotes uniformity across ac specifications. More specifically, although only one input pin for the clock exists, the internal implementation uses four clocks to reduce the distance required for the signal to travel from the clock to the various internal circuits. Each clock was strategically placed by its own set of five bits, thereby further reducing potential skew and enhancing device consistency and signal uniformity.

In addition to the SSTL16837, TI is developing a second device that conforms to SSTL specifications; the SSTL16847 is a 20-bit buffer with 3-state outputs that is optimized at a supply voltage equal to 3.3 V.

Features

The SSTL interface standard was created specifically for high-speed interfacing to SDRAMs. As such, the SSTL16837 features a maximum frequency specification of 200 MHz. In attaining this frequency, the input high and low voltage levels (V_{IH} and V_{IL}) are V_{REF}+200 mV and V_{REF}−200 mV, respectively. This 400-mV input voltage swing allows much faster operation of the device than is normally possible using the standard 1.2-V difference in LVTTL levels where V_{IH} and V_{IL} equal 2 V and 0.8 V, respectively.

The SSTL16837 supports both SSTL and LVTTL switching levels. Although the data sheet provides specifications where SSTL levels are used for the input and output levels, the device can operate under any combination of SSTL/LVTTL levels as inputs and outputs. When the device is operated using the SSTL level as the output level, it functions noticeably faster than when LVTTL levels are used. When LVTTL levels are used for the outputs, the device's propagation delay is increased by approximately 2 ns. Regardless of whether SSTL or LVTTL is used as the input switching level, V_{REF} still must be established and provided on the appropriate input pin. Irrespective of the input and output switching levels however, the characteristic high-level and low-level output drive current of 20 mA is maintained.

The SSTL16837 was designed and optimized to operate with a supply voltage of 3.3 volts, and it is to this value that the data sheet specifications apply. However, laboratory testing shows the device also operates at a supply voltage of 2.5 V, with only a minimal amount of degradation in the propagation delay values. (The results are discussed in the *Results* section). The power supply was reduced to 1.8 V and the SSTL16837 continued to function correctly. (A standard for 1.8 V has not been defined in the electronics industry, but a calculated estimation of appropriate switching levels was used when conducting the laboratory tests.) These results also are discussed in the *Results* section.

All SSTL16837 totem-pole outputs have a dedicated V_{DDQ} supply that (as stated in the SSTL_3 JEDEC standard), can be lower than or equal to V_{DD}, but never greater than V_{DD}. This feature allows for the internal circuitry supply voltage to be raised to 3.6 V for maximum speed performance, while lowering V_{DDQ} to prevent the device from dissipating large amounts of power in the output stage.

Typical Design Applications

As a universal bus driver, the SSTL16837 is used for buffering address lines to memory and can be operated in a transparent, latch, or flip-flop mode. Various factors influence whether buffering is required, including drive strength of the core logic, frequency, capacitive load, physical length from the driver to the receiver, and the resulting reflection that may occur. Buffering address and data lines ensures adequate current is supplied to the receiver and assists in quieting noisy circuits. The flip-flop mode is commonly used to ensure the minimum skew between address lines.

Although the SSTL switching standard is still relatively new and the number of observed applications is limited, the SSTL16837 ususally resides directly on the DIMM. In some systems, however, it is located on the motherboard. Current applications use one SSTL device per DIMM to drive up to 18 SDRAMs.

The SSTL16837 can operate at both LVTTL and SSTL levels on the input and output ports. Although a switching level for a given range of frequencies is not specified by JEDEC, the general trend is to use the LVTTL switching level for systems that use frequencies less than 100 MHz. For systems with frequencies greater than 125 MHz, SSTL is more commonly used. Systems implementing frequencies between 100 MHz and 125 MHz commonly use either LVTTL or SSTL.

Laboratory Testing Technique

To demonstrate the operation of TI's SSTL device, testing the SSTL16837 with V_{CC} equal to 3.3 V, 2.5 V, and 1.8 V was desired. For this particular device, the worst-case readings are obtained at high $V_{CC,}$ high temperature, and high capacitive loading. The resultant V_{CC} values were then set to 3.6 V and 2.7 V, with C_L set to 30 pF and with the temperature at 70°C. (Since a standard for the 1.8-V switching level has not been identified, V_{CC} was set to 1.8 V for that level.) As the level of V_{CC} varied, appropriate changes were made to V_{REF}, V_{TT}, V_{IH}, and V_{IL}. For all tests, R_S and R_T remained constant at 25 ohms meeting SSTL Class II specifications), and T_A was held constant at 70°C. Table 2 summarizes the laboratory setup that was implemented.

Table 2. Laboratory Testing Setup Parameters

PARAMETER	$V_{CC} = V_{DDQ} = 3.6$ V $V_{REF} = 1.5$ V $T_A = 70°C$ $V_{IL} = 1.37$ V $V_{IH} = 1.68$ V $C_L = 30$ pF	$V_{CC} = V_{DDQ} = 2.7$ V $V_{REF} = 1.35$ V $T_A = 70°C$ $V_{IL} = 1.17$ V $V_{IH} = 1.53$ V $C_L = 30$ pF	$V_{CC} = V_{DDQ} = 1.8$ V $V_{REF} = 0.9$ V $T_A = 70°C$ $V_{IL} = 0.72$ V $V_{IH} = 1.08$ V $C_L = 30$ pF
V_{DD}	3.6 V	2.7 V	1.8 V
V_{REF}	1.5 V	1.35 V	0.9 V
V_{TT}	1.5 V	1.35 V	0.9 V
V_{IH}	1.68 V	1.53 V	1.08 V
V_{IL}	1.37 V	1.17 V	0.72 V
R_S	25 Ω	25 Ω	25 Ω
R_T	25 Ω	25 Ω	25 Ω
C_L	30 pF	30 pF	30 pF
T_A	70°C	70°C	70°C

Results

Using the conditions provided in Table 2, data was taken for high-to-low and low-to-high transitions for propagation delay from the input to the output (A to Y), for propagation delay from the clock to the output (CLK to Y), for propagation delay from the latch enable to the output (LE to Y), and for enable and disable times (OE to Y). Additionally, timing specifications also were measured for setup and hold times under a variety of conditions, as specified in the SSTL16837 data sheet and provided in Table 3. Finally, data taken was for levels of the output high and low voltages, V_{OH} and V_{OL} respectively, under steady-state conditions.

The results obtained when V_{CC} was set to 3.6 V were well within the data-sheet maximum specification values; for propagation delay, the laboratory results were approximately 1 ns faster than shown in the data sheet. For enable time, the laboratory results were approximately 1.5 ns faster and for disable time, the laboratory results were approximately 1.5 ns faster. Setup times measured in the laboratory under the above conditions decreased from 200 ps to 700 ps and hold times decreased by 400 ps.

The SSTL16837 was designed and optimized to operate with a supply voltage of 3.3 V. Even when the supply voltage was reduced to 2.5 V, however, the speed did not degrade substantially. The propagation delays increased by approximately 300 ps, the enable time increased by approximatley 1 ns, and the disable time decreased by approximately 500 ps. (In most instances, an increase in disable time would be expected; however, the decrease in disable time may have been due to differential voltage levels between the input and output trip points.) Table 3 lists setup-time and hold-time values measured in the laboratory under the above conditions.

The propagation delay times slightly more than doubled when V_{CC} was set to 1.8 V when compared to the 3.6-V supply voltage values. The enable time increased around 65% and the disable time increased by around 50%. Table 3 lists setup-time and hold-time values measured in the laboratory under the above conditions.

The results obtained from the laboratory, with their appropriate testing conditions, are summarized in Table 3.

Table 3. Results of Laboratory Testing

PARAMETER	$V_{CC} = V_{DDQ} = 3.6$ V $V_{REF} = 1.5$ V $T_A = 70°C$ $V_{IL} = 1.37$ V $V_{IH} = 1.68$ V	$V_{CC} = V_{DDQ} = 2.7$ V $V_{REF} = 1.35$ V $T_A = 70°C$ $V_{IL} = 1.17$ V $V_{IH} = 1.53$ V	$V_{CC} = V_{DDQ} = 1.8$ V $V_{REF} = 0.9$ V $T_A = 70°C$ $V_{IL} = 0.72$ V $V_{IH} = 1.08$ V
t_{PLH} A→Y	3.3 ns	3.64 ns	6.3 ns
t_{PHL} A→Y	2.41 ns	2.95 ns	5.35 ns
t_{PLH} CLK→Y	1.9 ns	2.1 ns	4.21 ns
t_{PHL} CLK→Y	2.02 ns	1.9 ns	4.74 ns
t_{PLH} LE→Y	2.79 ns	3.19 ns	7.47 ns
t_{PHL} LE→Y	2.48 ns	2.87 ns	6.15 ns
t_{PLZ} OE→Y	4.13 ns	3.66 ns	6.15 ns
t_{PZL} OE→Y	3.73 ns	4.69 ns	6.12 ns
t_{PHZ} OE→Y	4.65 ns	4.04 ns	6.78 ns
t_{PZH} OE→Y	4.06 ns	5.1 ns	6.64 ns
t_{su} A before CLK↑ and LE low	1.3 ns	0.44 ns	0.9 ns
t_{su} A before LE↓ and CLK high	1.1 ns	0.96 ns	1.08 ns
t_{su} A before LE↓ and CLK low	1.3 ns	1.89 ns	2 ns
t_h A after CLK↑ and LE low	0.6 ns	0.36 ns	0.7 ns
t_h A after LE↓	0.6 ns	0.46 ns	0.72 ns
V_{OH}	2.88 V	2.19 V	1.38 V
V_{OL}	0.44 V	0.37 V	0.79 V

Competition Analysis

TI is commited to being the market leader for SSTL and is striving to be the vendor of choice for design engineers who require SSTL logic to meet the requirements of their systems. TI has released a device to production, has a second SSTL device scheduled to be released, and is conducting research to determine and define the next sequence of SSTL devices.

SPICE/IBIS Models

SPICE and IBIS models are available for the SSTL16837. The SPICE model is a level-13 model, consists of the input and output stages, and can be obtained by contacting your local TI sales representative. The IBIS model consists of the input and output stages and can be obtained by accessing http://www.ti.com/sc/docs/asl/models/ibis.htm.

Package Information

The SSTL16837 and the SSTL16847 are 64-pin devices in a thin shrink small-outline package (TSSOP) DGG package. A pinout of the SSTL16837 is shown in Figure 2.

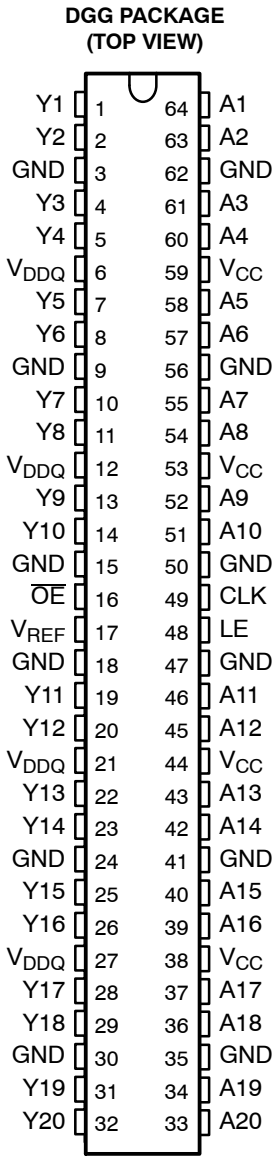

Figure 2. SSTL16837 Pinout

The DGG package has a lead pitch of 0.5 mm and measures nominally 17 millimeters in length by 8.1 millimeters (including pin length) in width; this conforms to JEDEC MO-153.

Frequently Asked Questions

Question: How do I get a copy of the SSTL16837 data sheet and samples?

Answer: The SSTL16837 data sheet can be obtained by accessing http://www.ti.com/sc/docs/psheets/pids.htm. Samples of the SSTL16837 can be obtained by contacting your local TI sales representative.

Question: How do I get a copy of the SSTL16837 SPICE and IBIS models?

Answer: The SPICE model for the SSTL16837 can be obtained by contacting your local TI sales representative. The IBIS model can be obtained by accessing http://www.ti.com/sc/docs/asl/models/ibis.htm.

Question: Are there any plans to release other SSTL devices?

Answer: Yes. TI currently is designing the SSTL16847, which is a 20-bit buffer/driver. It conforms to the SSTL interface standard, has 20-mA drive, and is planned to be released to production in 1Q98. Furthermore, TI is conducting market research to determine the next series of required SSTL devices.

Question: Why is SSTL considered a high-frequency switching standard?

Answer: The SSTL switching standard was defined for interfacing with SDRAMs at high frequencies. Features such as the usage of differential inputs and a specifically prescribed bus-termination scheme, which reduces the output voltage swing required for a high or low state, allows SSTL devices to operate at high frequencies.

Question: Can I run the SSTL16837 device at LVTTL levels?

Answer: Yes, the SSTL16837 device operates at LVTTL levels, both on the input switching level and on the output switching level. When LVTTL levels are used for the output switching level, however, the device's propagation delay is increased by approximately 2 ns.

Question: What does the future hold for SSTL, specifically double data rate (DDR) SDRAMs?

Answer: SSTL is envisioned to be the switching standard of the future for interfacing with high-speed memory. As SSTL continues to grow and become more widely used, designers may find that implementing SSTL in their designs is necessary to remain competitive. The DDR scheme utilizes both the rising and the falling edges of the clock, allowing data to be processed at twice the typical speed. This arrangement is expected to be widely used in systems since it essentially doubles the throughput.

Conclusion

The SSTL standard specifies a method of interfacing with high-speed SDRAMs. It employs a reduced voltage swing on the inputs by specifying a reference voltage with a 400-mV total differential voltage from a high-level input to a low-level input, and a unique termination scheme on the output. SSTL is envisioned to be the switching standard of the future for interfacing with SDRAMs.

Although designed and optimized for a supply voltage of 3.3 V, the SSTL16837 also can operate at supply voltage levels of 2.5 V and 1.8 V. Additionally, only a slight degradation in performance from 3.3 V to 2.5 V was observed.

The SSTL16837 and the SSTL16847 are address drivers and can be used to buffer address lines when interfacing to SDRAMs.

Glossary

DDR	Double data rate
DIMM	Dual in-line memory module
IBIS	I/O buffer information specification
JEDEC	Joint Electron Devices Engineering Councils
LVTTL	Low-voltage transistor-transistor logic
SDRAM	Synchronous dynamic random access memory
SPICE	Simulation program with integrated circuit emphasis
SSTL	Stub series-terminated logic
TI	Texas Instruments
TSSOP	Thin shrink small-outline package
TTL	Transistor-transistor logic
UBD	Universal bus driver

References

1. Handy, Jim, *The Cache Memory Book*, Academic Press, Inc., Harcourt Brace & Company, Publishers, 1993.
2. *Stub Series-Terminated Logic for 3.3 Volts* (SSTL_3) JC-16-97-04
3. *Stub Series-Terminated Logic for 2.5 Volts* (SSTL_2) JC-16-97-58
4. *Semiconductor Group Package Outlines*, 1997, literature number SSYU001C

TI Logic Solutions for Memory Interleaving with the Intel™ 440BX Chipset

SCAA001
May 1999

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Abstract

Increasing performance requirements of personal computers that necessitate a larger number of SDRAMs and DIMMs can be met by an FET-switch muliplexer. Four devices for memory interleaving for the 440BX and other core-logic chipsets incorporate internal pulldown resistors, damping resistors, and make-before-break features that increase speed while maintaining minimal simultaneous-switching noise.

Introduction

Rapid advancements in hardware and software are emerging to meet the performance needs within the personal computer (PC) industry. To meet the needs of increasing memory requirements, a large number of SDRAMs are needed. Consequently, a larger number of DIMMs are needed, adding heavy loading to the memory controller and to the data lines. To reduce the loading and maintain signal integrity and reliability of the system, an FET-switch multiplexer is recommended for this application. Texas Instruments (TI™) offers four such devices for memory interleaving for the Intel™ 440BX logic chipset and for other core-logic chipsets that need interleaving capability. This report discusses TI's logic solutions using SN74CBT16292, SN74CBTLV16292, SN74CBT162292, and SN74CBTLV162292 devices.

Background

Designing a reliable, high-performance memory system forces designers to consider every detail of the system. Up to 384-Mbytes of system memory can be achieved by using 64-Mbit technology and 168-pin, 8-byte, registered SDRAM DIMMs on three double-sided DIMMs. To achieve a larger memory system with the same type of memory device, a fourth DIMM should be introduced. But, this increases loading. To reduce the loading, an FET-switch multiplexer is recommended. An FET switch on the data line splits the load and reduces it by 50%. In order to design a simple, cost-effective, reliable system, several factors must be considered during FET-switch selection. In the following section, significant information about the SN74CBT16292, SN74CBTLV16292, SN74CBT162292, and SN74CBTLV162292 devices is discussed, as well as applications of this switch on the DIMM.

Device Information

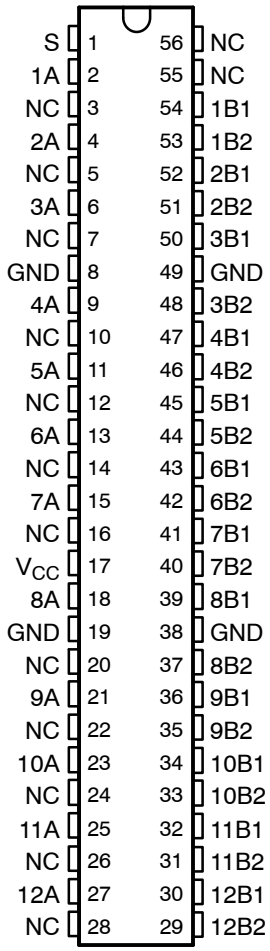
The devices discussed are members of the TI Widebus™ family, which are manufactured using TI's enhanced-performance implanted CMOS (EPIC™) submicron process. Each of these devices is a 12-bit 1-of-2 FET multiplexer/demultiplexer with 500-Ω internal pulldown resistors (R_{INT}). The pinout is the same for each device (see Figure 1). SN74CBT16292 and SN74CBT162292 are designed for 4-V to 5.5-V V_{CC} operation. SN74CBTLV16292 and SN74CBTLV162292 are designed for 2.3-V to 3.6-V V_{CC} operation. The low on-state resistance (4 Ω) of the switch allows connections to be made with minimal propagation delay. When the select (S) input is low, port A is connected to port B1 and port B2 is pulled down through R_{INT} to ground. When S is high, port A is connected to B2 and R_{INT} is connected to port B1 (see Table 1 and Figure 2).

All four devices have the same function. They are different from each other with respect to special features that are discussed in the following paragraphs.

Special Features

Internal pulldown resistors

On all four of these devices, ports B1 and B2 have an internal 500-Ω pulldown resistor connected to GND through a switch. When port B is disconnected from port A, instead of floating, port B is connected to GND through the 500-Ω resistor. If unused inputs are not connected to GND or $V_{CC,}$ they follow any stray noise on that pin, creating unpredictable circuit performance. Termination of unused inputs by connecting them with the internal pulldown resistor increases system reliability and minimizes power dissipation.



NC – No internal connection

Figure 1. Pinout for SN74CBT16292, SN74CBT162292, SN74CBTLV16292, and SN74CBTLV162292 Devices

Table 1. Function Table for SN74CBT16292, SN74CBT162292, SN74CBTLV16292, and SN74CBTLV162292 Devices

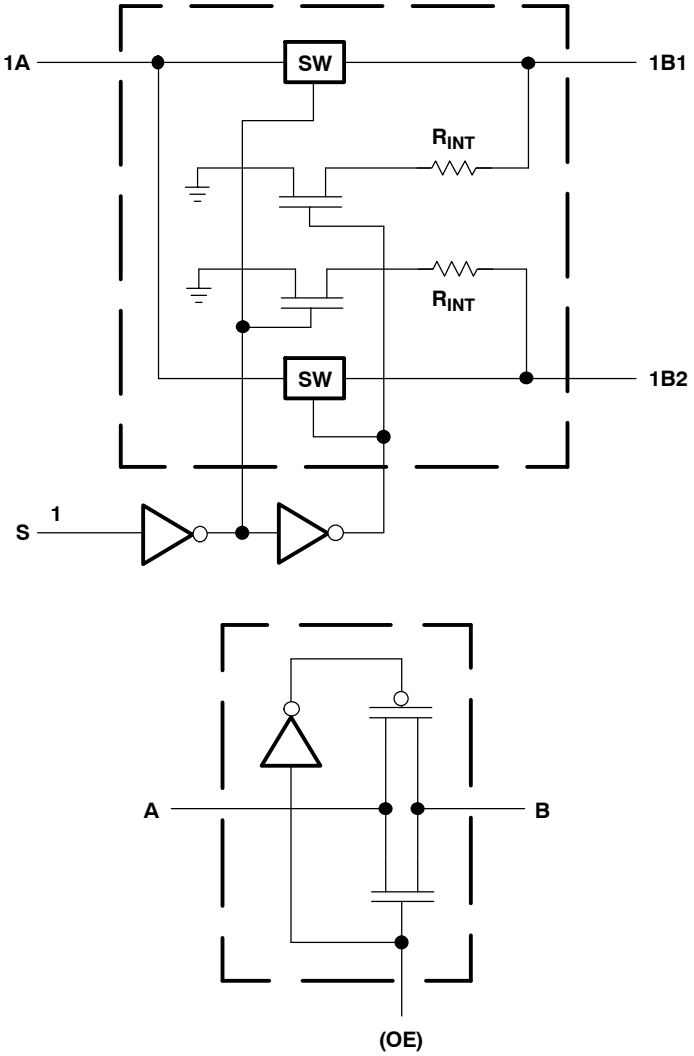
S INPUT	FUNCTION
L	A port = B1 port R_{INT} = B2 port
H	A port = B2 port R_{INT} = B1 port

Damping resistors

SN74CBT162292 and SN74CBTLV162292 have a 25-Ω internal damping resistor connected to port A inputs/outputs. This series termination resistor matches line impedance with the transmission line to reduce noise due to line reflection. It controls signal overshoot and undershoot and maintains noise at a minimum value. If a designer is concerned about the signal integrity, a series damping resistor can be added externally, if it is not incorporated into the device. By using the SN74CBT162292 or SN74CBTLV162292 devices, no external resistors are required.

Make-before-break feature

This unique make-before-break feature is available on all four of these devices. Figure 2 is the logic diagram of CBTLV16292. When S is low, 1A is connected to 1B1 and R_{INT} is connected to 1B2 through the load n channel. When S is high, 1A is connected to 1B2, and R_{INT} is connected to 1B1 through the load n channel. During this transition, the pass p channel or n channel will turn on first, then the load transistor will turn off. This feature causes port 1B1 and 1B2 (outputs) always to be connected either to GND through R_{INT} or to the input, preventing the output from floating and ensuring system reliability. The interval between these two events is known as make-before-break time (t_{mbb}). Figure 3 shows the make-before-break switching, where t_{mbb} is approximately 1.75 ns. The maximum value for t_{mbb} can be 2 ns, which means that the maximum interval between switching on the pass transistor and switching off the load transistor can be 2 ns maximum, which is very low.



Simplified Schematic of Each FET Switch

Figure 2. Logic Diagram for SN74CBTLV16292

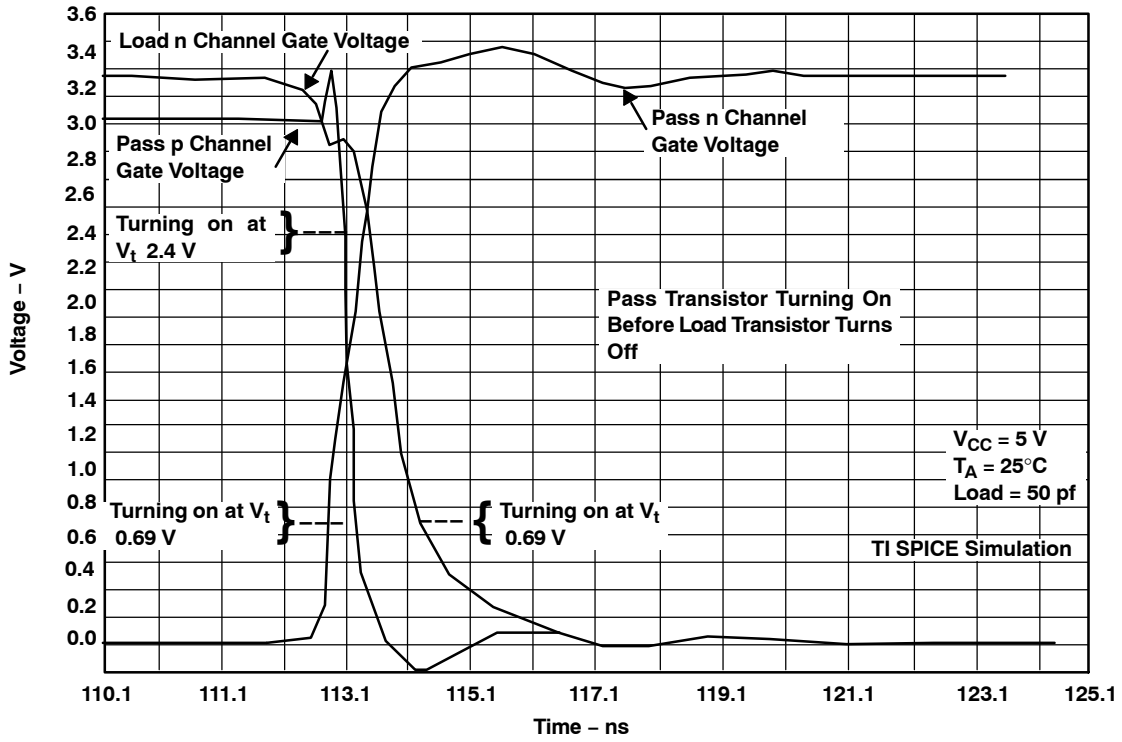


Figure 3. Make-Before-Break Switching for CBTLV16292

Tables 2 and 3 summarize the features and benefits of the CBT16292, CBT162292, CBTLV16292, and CBTLV162292 devices.

Table 2. Features of the CBT Devices

DEVICE	PINS	V_{CC} NOMINAL	I/O VOLTAGES	SERIES RESISTORS	INTERNAL PULLDOWN RESISTORS
CBT16292	56	5 V	3.3 V or 5 V	No	Yes
CBT162292	56	5 V		Yes	Yes
CBTLV16292	56	3.3 V	3.3 V only	No	Yes
CBTLV162292	56	3.3 V		Yes	Yes

Table 3. Benefits of the CBT Devices

DEVICE	SERIES DAMPING RESISTOR	UNUSED INPUTS	V_{CC}
CBT16292	External resistor necessary for impedance match	Connected to ground through 500-Ω pulldown resistor	
CBT162292	No external resistor required	Connected to ground through 500-Ω pulldown resistor	
CBTLV16292	External resistor necessary for impedance match	Connected to ground through 500-Ω pulldown resistor	3-V V_{CC} allows same power plane as memory
CBTLV162292	No external resistor required	Connected to ground through 500-Ω pulldown resistor	3-V V_{CC} allows same power plane as memory

Performance

Speed

In memory-interleaving applications, t_{en} and t_{dis} of the bus switches determine the speed of data transfer. All four of these devices have very fast enable and disable times. Figure 4 shows the enable time vs load capacitance for the four devices. The graph shows a very fast enable time over a wide range of load capacitance. At 25-pF to 30-pF load, which closely matches the DIMM loading, all the devices have t_{en} of 3 ns to 4 ns.

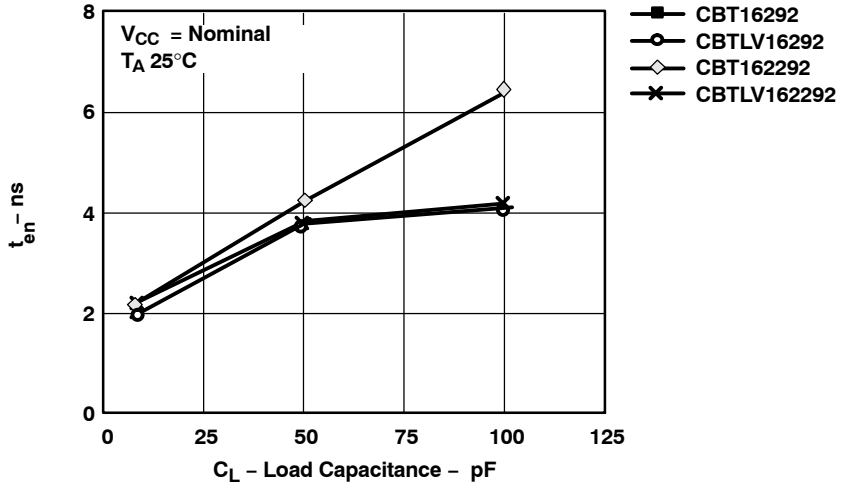


Figure 4. t_{en} vs C_L

Figure 5 shows the disable time over a wide range of load capacitance. The graph shows that, at a load of 25 pF to 30 pF, t_{dis} is between 3 and 4 ns.

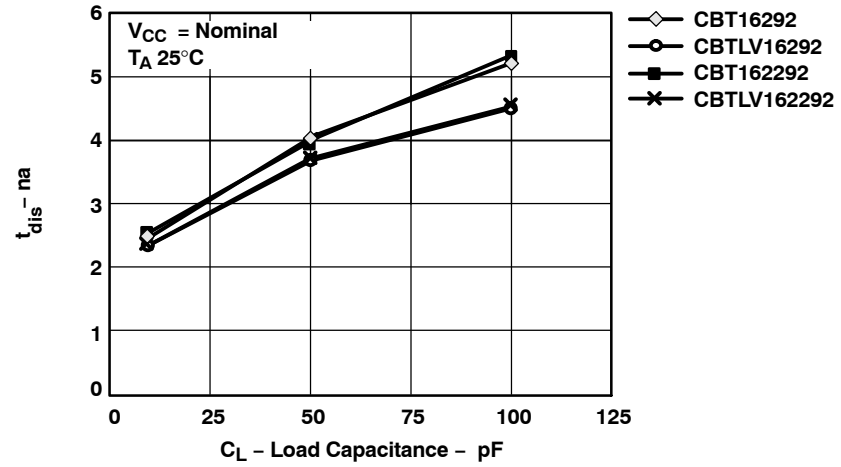


Figure 5. t_{dis} vs C_L

Simultaneous-switching noise

The effects of simultaneously switching multiple outputs of a single device can be examined using a standard procedure. The method of measuring simultaneous switching consists of holding one output low and switching all other outputs from the high state to the low state. Because of the package mutual inductance, transient current flows through the package and into the output pin that is being held low. This causes a rise in voltage and the output begins to ring. The peak of this ringing is called output low peak voltage (V_{OLP}). This is the most common and critical measure of ground bounce. Output low valley voltage (V_{OLV}) is the lowest point the low output reaches, which is usually a negative voltage.

In a similar way, a single output is held high and all other outputs are switched from the low state to the high state. Due to the package mutual inductance, the high output voltage drops, causing the outputs to ring. This valley is called output high valley voltage (V_{OHV}) and the peak is called output high peak voltage (V_{OHP}).

When V_{OLP} goes above 0.8 V, the device enters the threshold region and can switch from the low state to the high state. If V_{OHV} drops below 2 V, the device can switch from high to low. Table 4 shows the simultaneous switching data for the four CBT devices under discussion. Table 4 shows that these devices maintain a safe value for both V_{OLP} and V_{OHV}. Figures 6 through 13 show the simultaneous-switching plots for CBT16292, CBT162292, CBTLV16292, and CBTLV162292.

Table 4. Simultaneous-Switching Data

OPERATING CONDITION	DEVICE	V_{OLV} (mV)	V_{OLP} (mV)	V_{OHV} (mV)	V_{OHP} (mV)
V_{CC} = Nominal T_A = 25°C C_L = 50 pF	CBT16292	–0.12	0.44	3.64	4.36
	CBT162292	–0.08	0.24	3.44	4.00
	CBTLV16292	–0.14	0.28	3.14	3.44
	CBTLV162292	–0.06	0.24	2.98	3.24

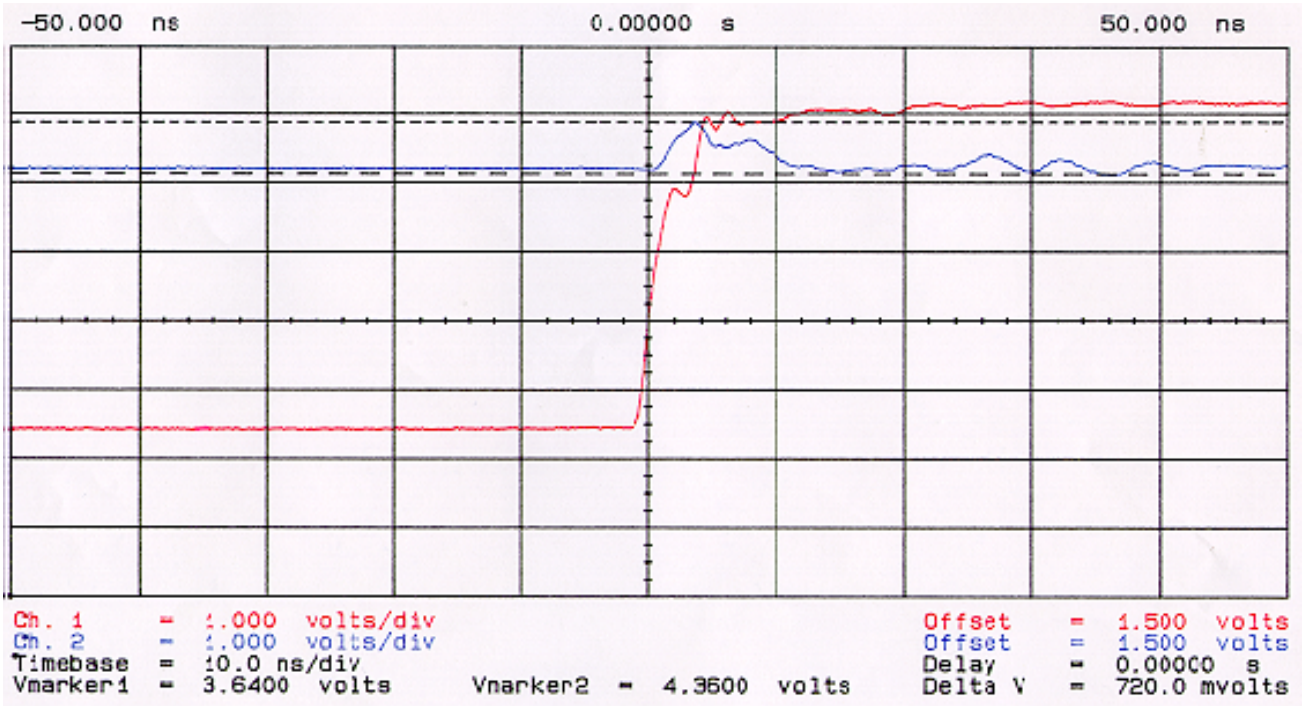


Figure 6. Simultaneous-Switching Plot for CBT16292 (V_{OHV}, V_{OHP})

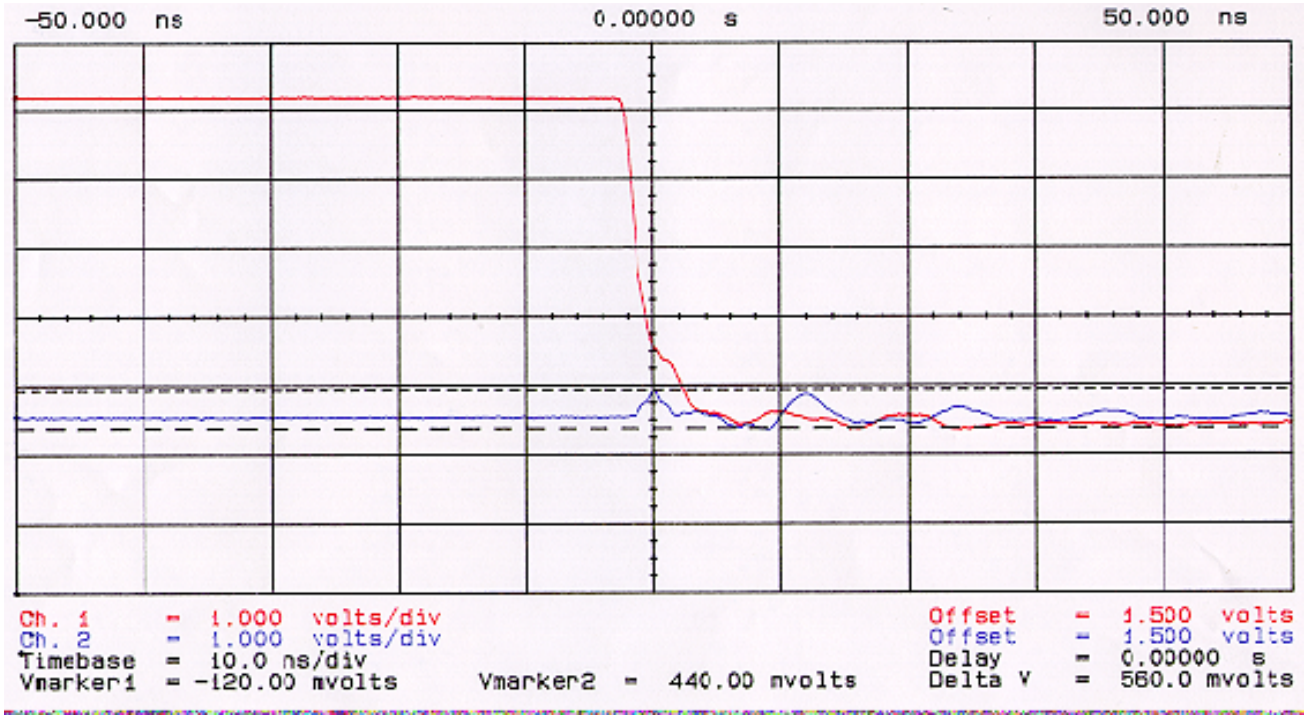


Figure 7. Simultaneous-Switching Plot for CBT16292 (V_{OLV}, V_{OLP})

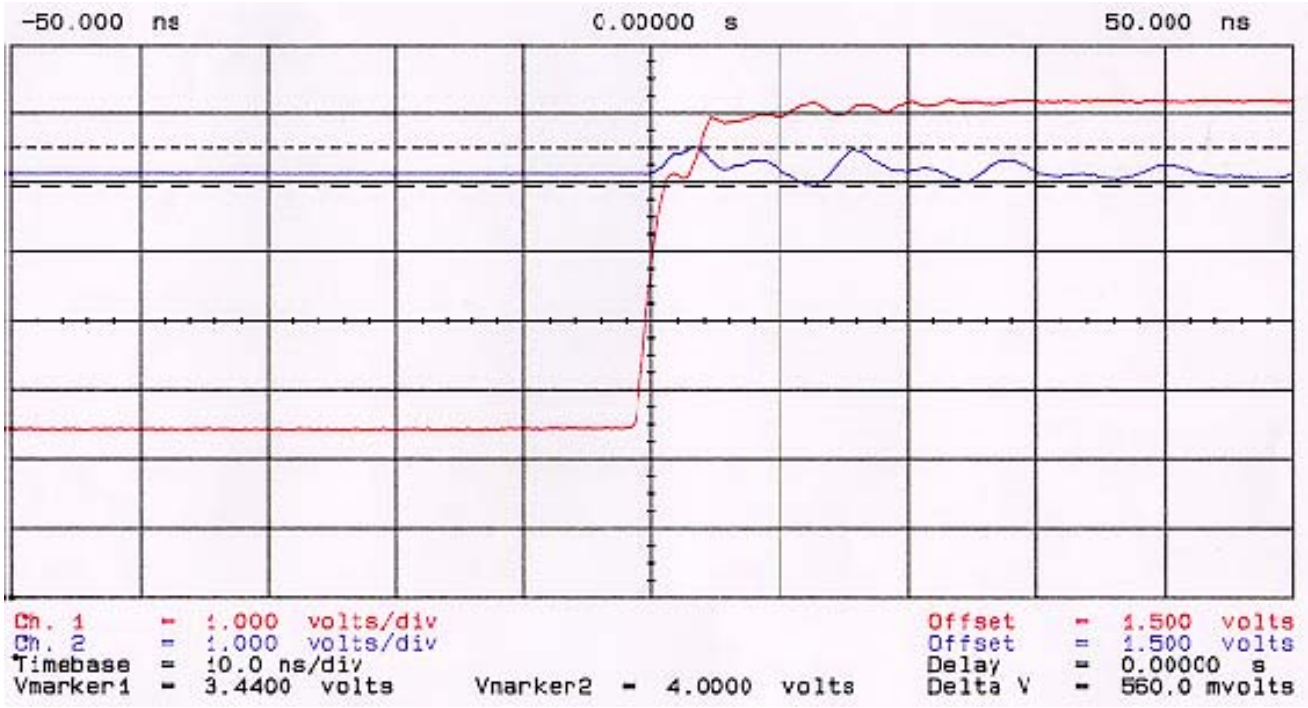


Figure 8. Simultaneous-Switching Plot for CBT162292 (V_{OHV}, V_{OHP})

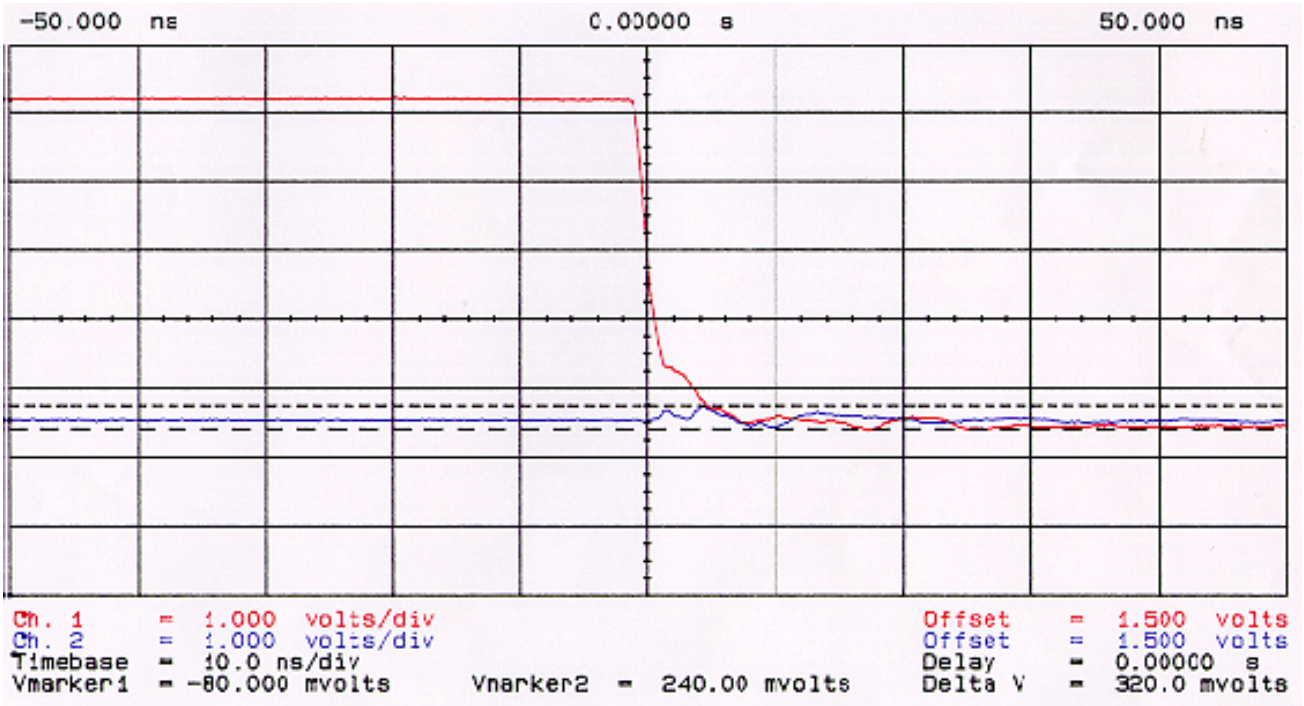


Figure 9. Simultaneous-Switching Plot for CBT162292 (V_{OLV}, V_{OLP})

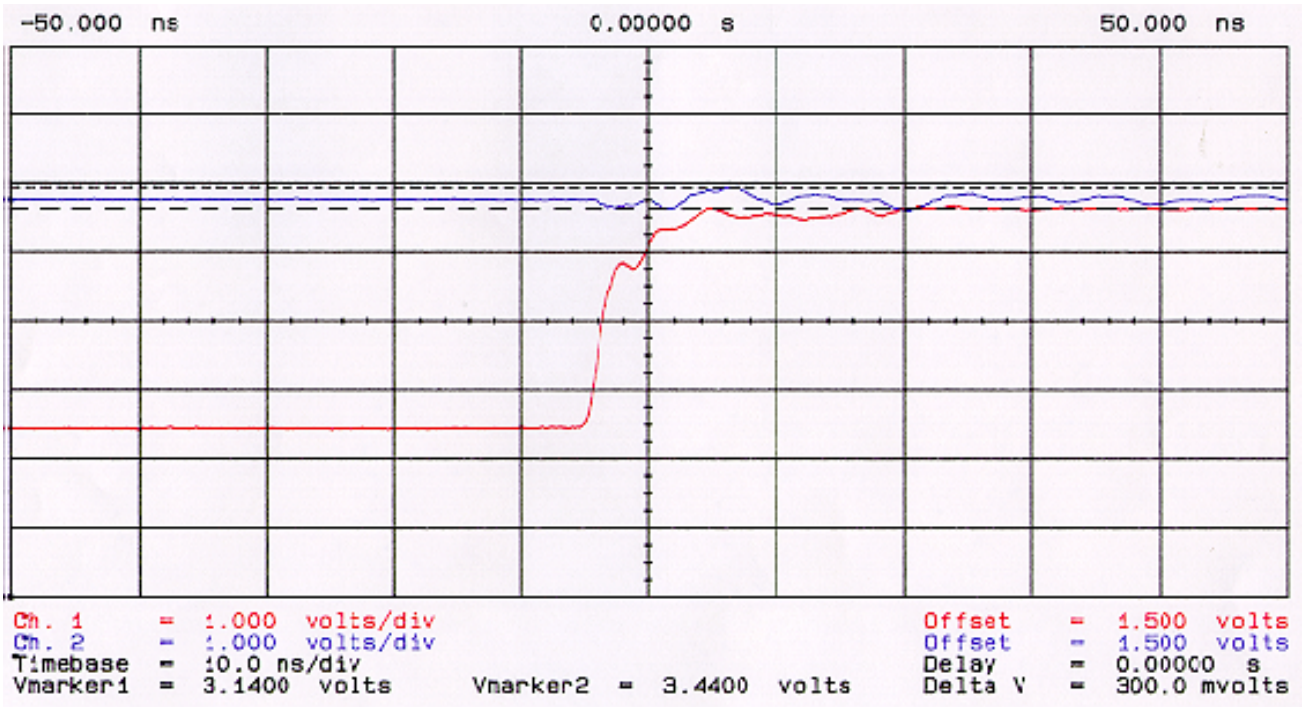


Figure 10. Simultaneous-Switching Plot for CBTLV16292 (V_{OHV}, V_{OHP})

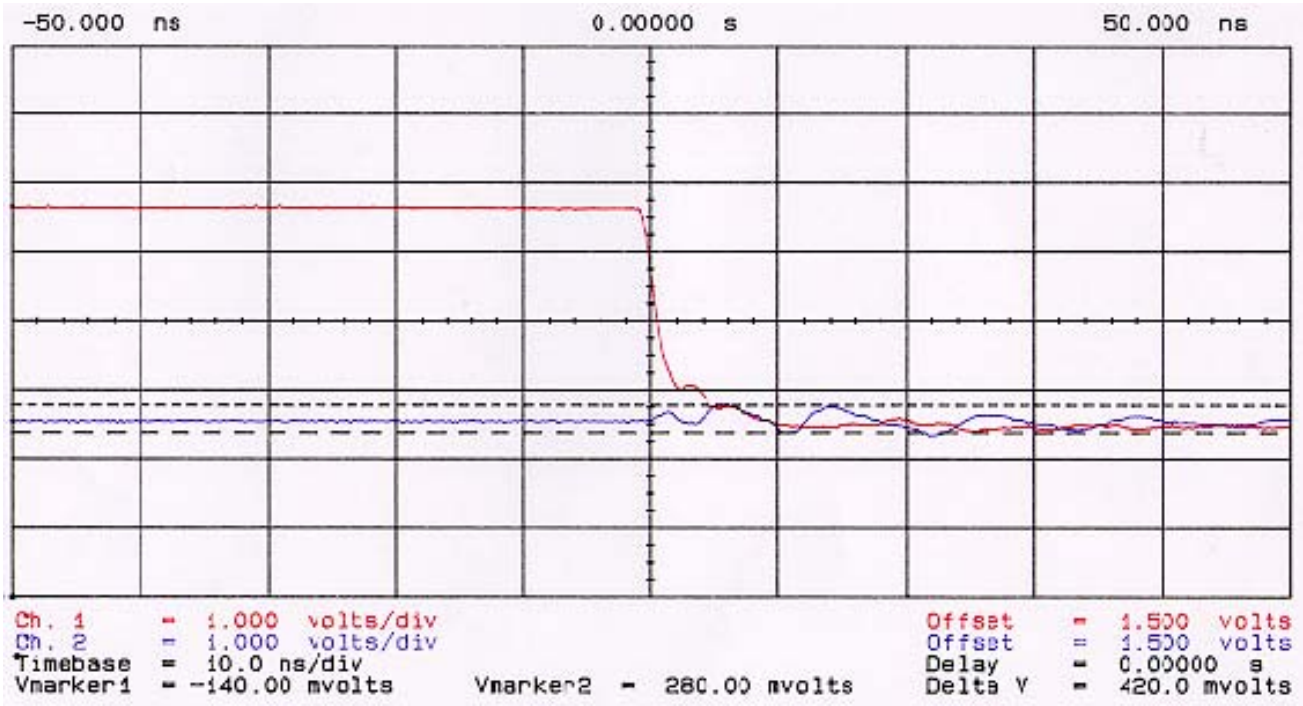


Figure 11. Simultaneous-Switching Plot for CBTLV16292 (V_{OLV}, V_{OLP})

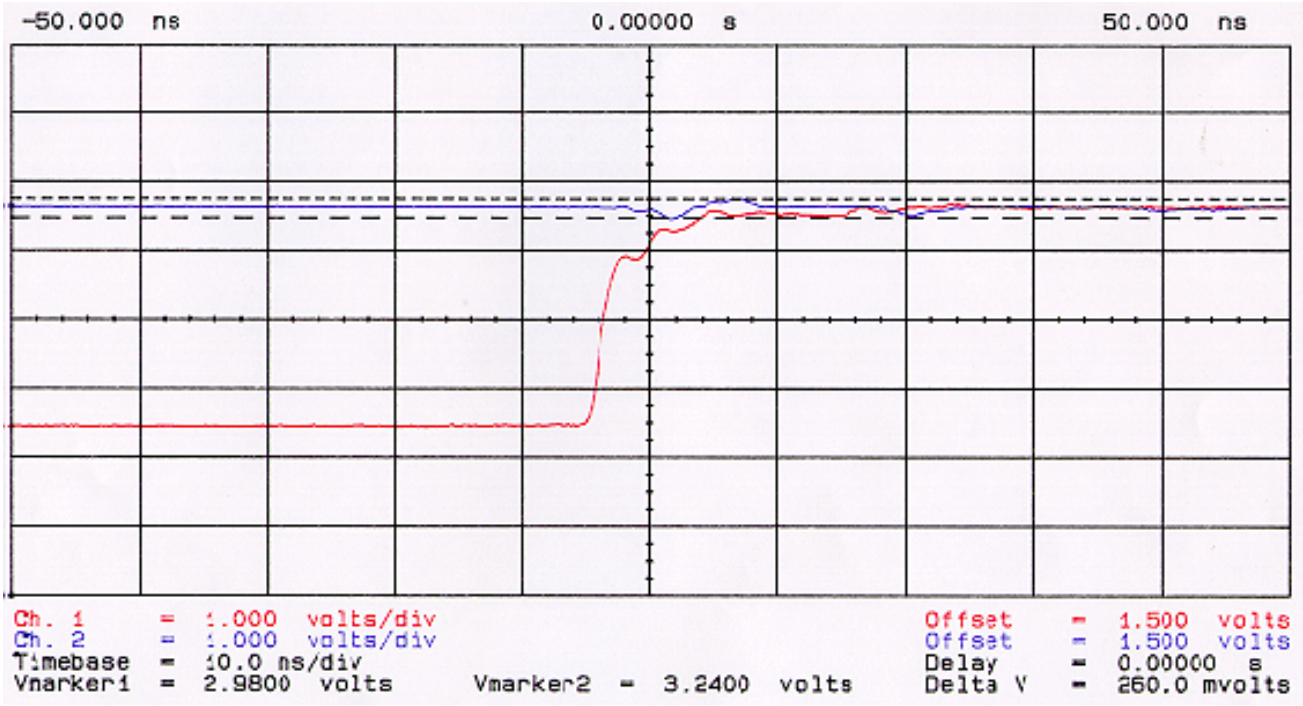


Figure 12. Simultaneous-Switching Plot for CBTLV162292 (V_{OHV}, V_{OHP})

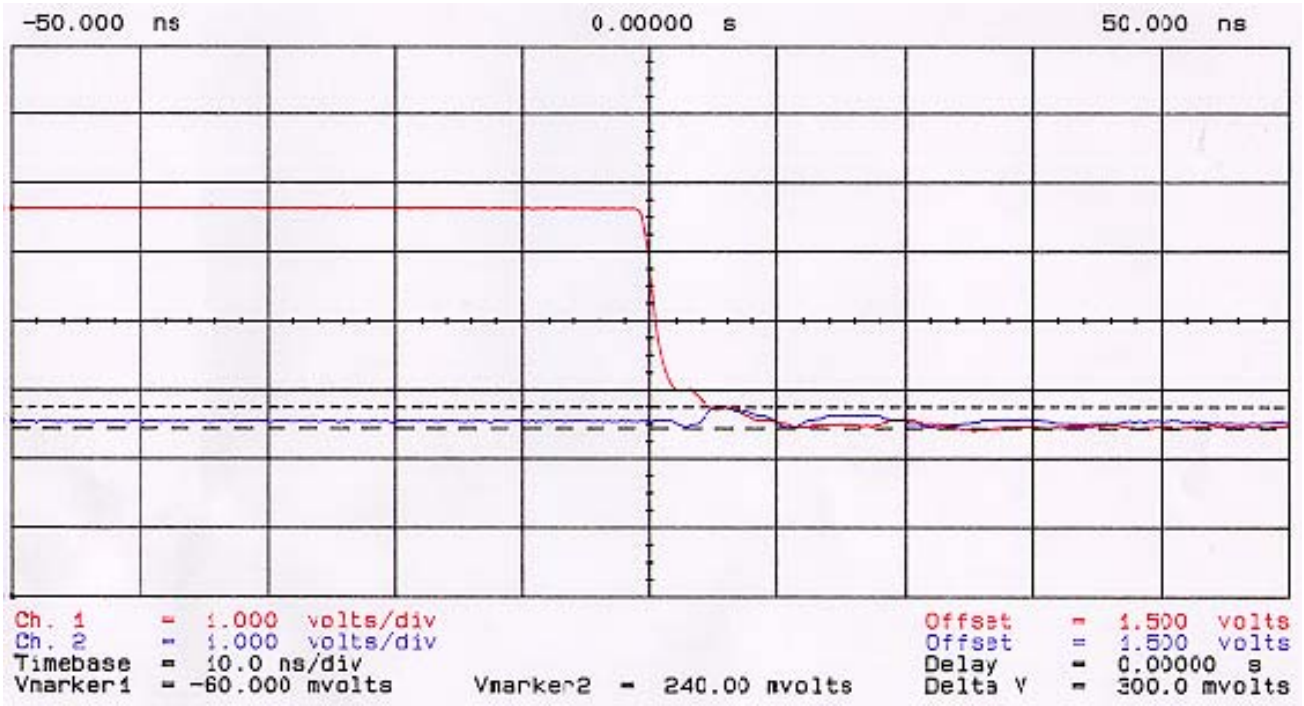


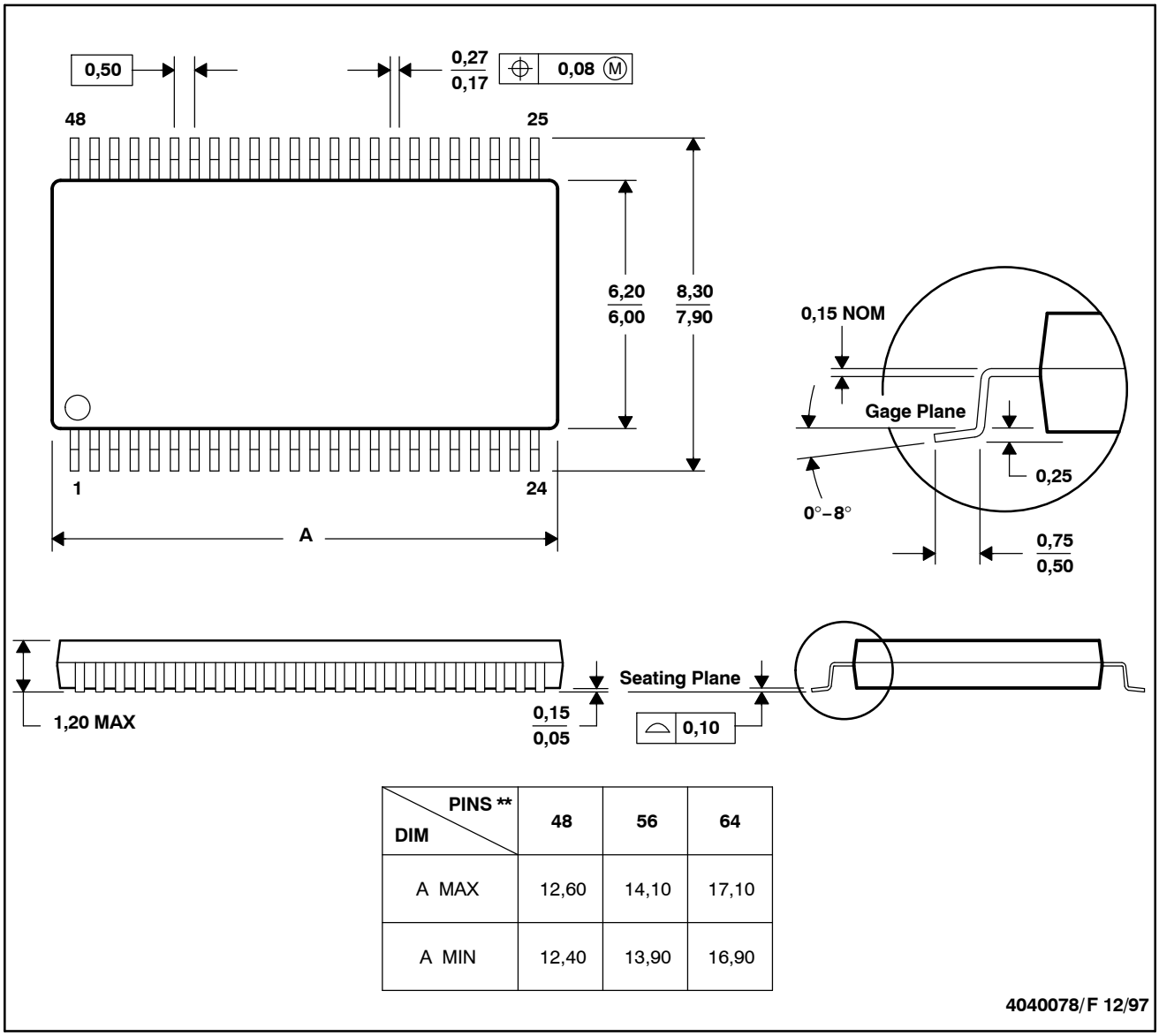
Figure 13. Simultaneous-Switching Plot for CBTLV162292 (V_{OLV}, V_{OLP})

Package Information

All of the devices discussed in this application report are available in the JEDEC-standard TSSOP (DGG) and TVSOP (DGV) packages. The mechanical data are shown in Figures 14 and 15.

DGG (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

48 PINS SHOWN



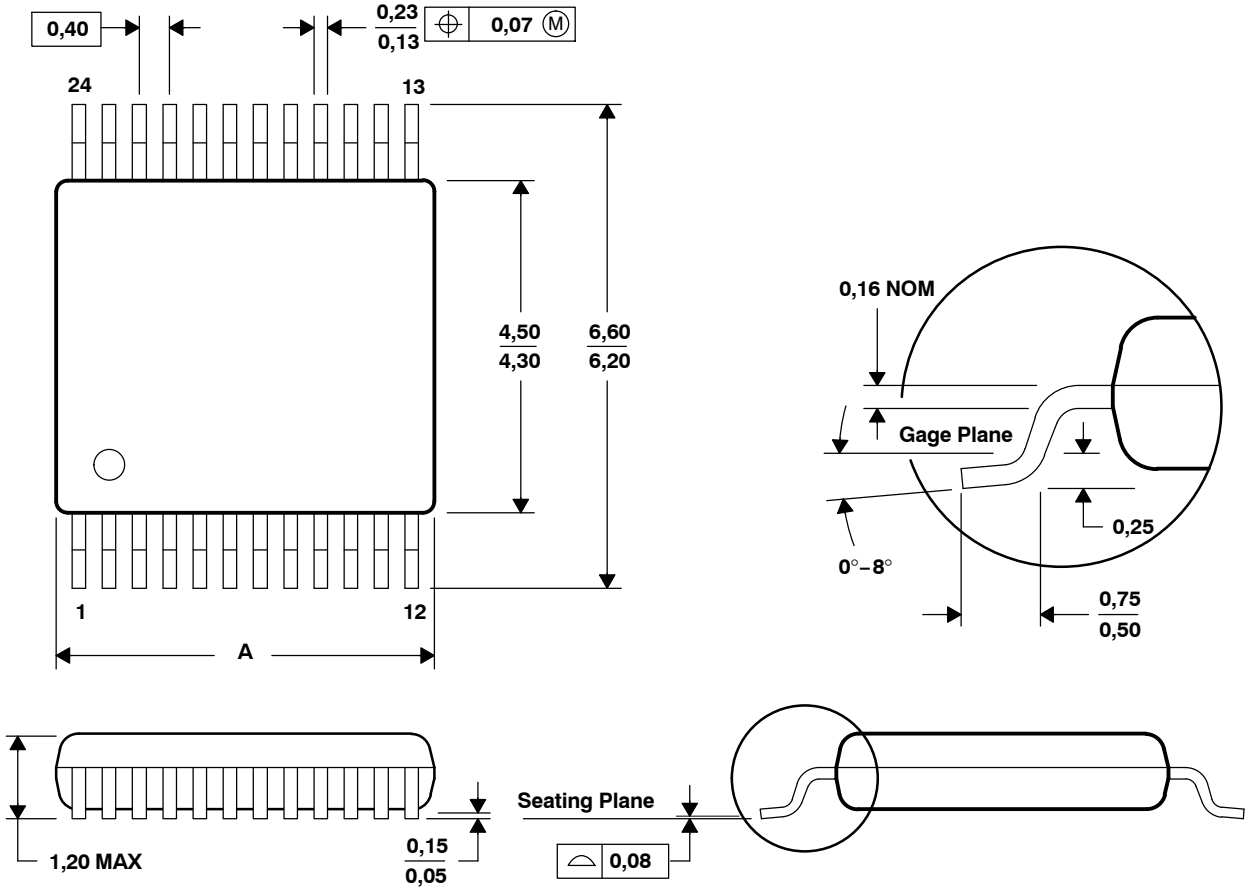
DIM \ PINS **	48	56	64
A MAX	12,60	14,10	17,10
A MIN	12,40	13,90	16,90

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

Figure 14. Package Outline Diagram (DGG)

DGV (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

24 PINS SHOWN



DIM \ PINS **	14	16	20	24	48	56
A MAX	3,70	3,70	5,10	5,10	9,80	11,40
A MIN	3,50	3,50	4,90	4,90	9,60	11,20

4073251/C 08/98

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

Figure 15. Package Outline Diagram (DGV)

Applications

High-performance desktop computers and servers utilizing Intel Pentium II or Pentium III processors and the 440BX chipset require large amounts of memory support to run complex applications. Currently, with three double-sided DIMMs using 64-Mbit technology, a total memory size of 384 Mbyte is possible. To support 512 Mbytes, a fourth DIMM must be added. The 82443BX integrates a memory controller that supports a 64/72-bit DRAM interface and operates the interface at 66 MHz or 100 MHz, while supporting up to four double-sided DIMMs. To meet the tight 100-MHz timing requirements for a four-DIMM configuration, the CBT16292 bus switch is recommended.

The BX controller supplies two copies of memory address (MA) for effectively driving the address load and optimizing strict timing requirements placed on it by the 100-MHz address bus. The controller also supplies the FET-enable signal (FENA) to enable CBT switches. For the data bus to offset heavy loading to the data-in/data-out (DQ) line with the additional fourth DIMM, the CBT16292 (12-bit to 24-bit mux/demux with internal 500-Ω pulldown resistors) is recommended. This reduces the loading to the data bus. To the memory controller it looks like there are only two DIMMs instead of four. Figure 16 shows the application of the CBT16292. With error correction code (ECC), six devices are needed to buffer the 72-bit signals. This task also can be accomplished by using CBT162292, CBTLV16292, or CBTLV162292 devices.

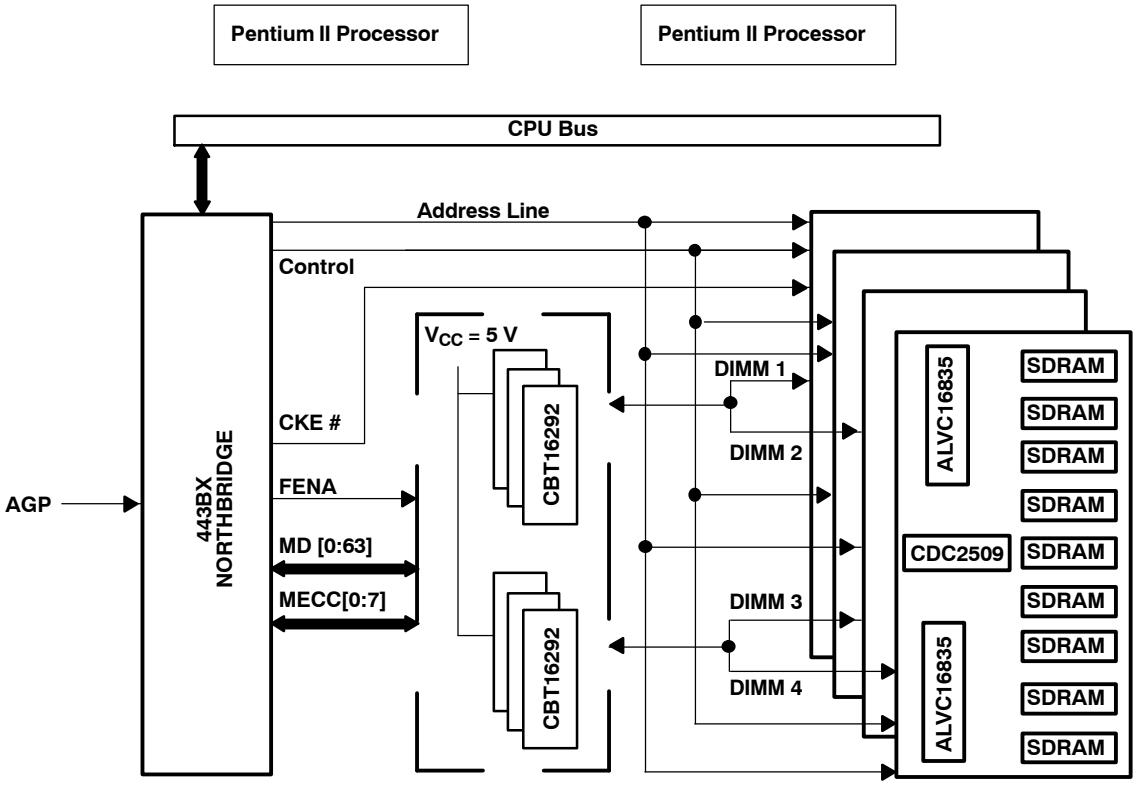


Figure 16. CBT16292 in a Four-DIMM Memory-Switching Application

Figure 16 shows that the CBT16292 plays an integral part in the overall memory solution. Layout and routing should be taken into account. Determining the optimal line length depends on different simulation methods that can accommodate strict timing requirements of a 100-MHz bus. Figure 17 is an example of a typical motherboard layout integrating CBT16292 for four DIMMs. This layout also shows that, by using the CBT16292, the design is more effective because there can be equal load distribution, which can minimize skews.

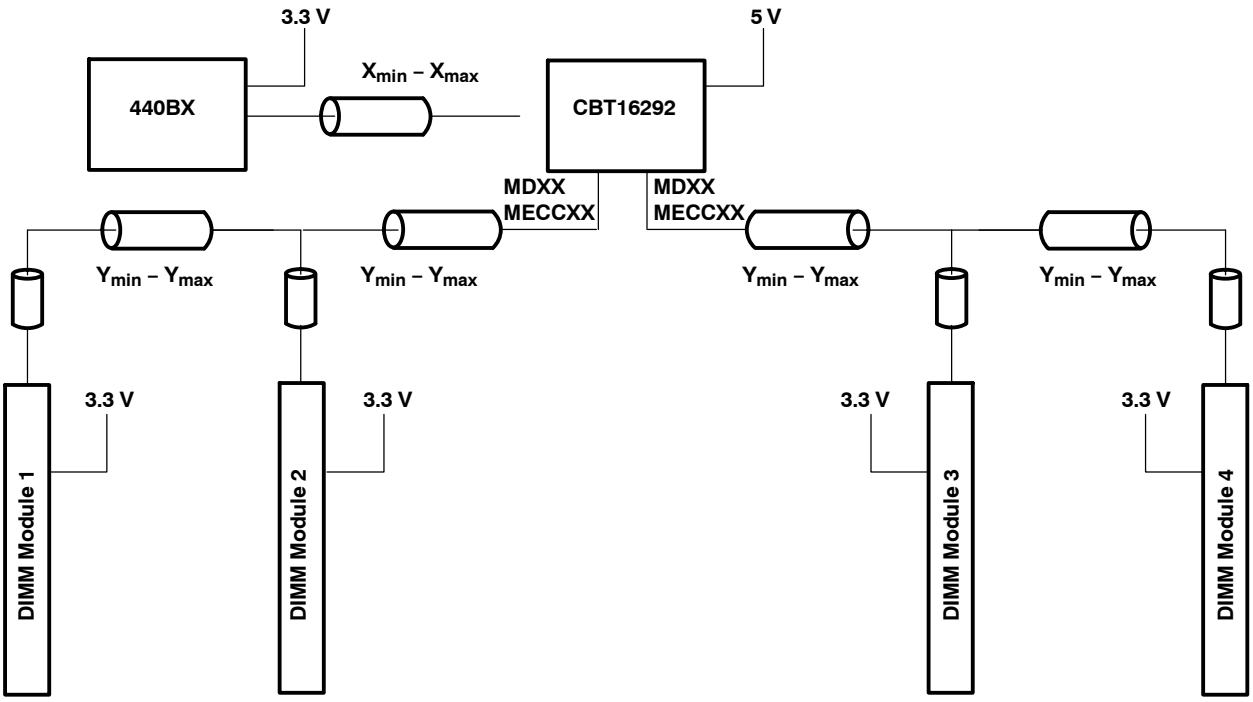


Figure 17. Typical Motherboard Layout Using CBT16292

To further optimize the layout and design shown in Figure 17, the CBTLV16292 and CBTLV162292 also are available. By using these 3.3-V FET-switch parts, all three parts of the memory solution are on the same power plane, and performance is not sacrificed.

Conclusion

TI's CBT16292, CBT162292, CBTLV16292, and CBTLV162292 bus-switch solutions allow successful 100-MHz system integration. TI's '16292 solutions reduce loading, increase reliability, and ease overall timing when integrating the devices with Intel's 440BX chipset.

Acknowledgment

The authors of this application report are Ji Park, Nadira Sultana, and Chris Cockrill.

Glossary

C

CBT	Crossbar technology
CMOS	Complementary metal-oxide semiconductor

D

DIMM	Dual in-line memory module
DRAM	Dynamic random-access memory
DQ	Data-in/data-out line

E

ECC	Error correction code

F

FET	Field-effect transistor
FENA	FET select signal

M

Mbyte	Megabyte
MA	Memory address

P

PC	Personal computer
pF	Picofarad

S

SDRAM	Synchronous dynamic random-access memory

T

TI	Texas Instruments
t_{en}	Enable time
t_{dis}	Disable time
TSSOP	Thin shrink small-outline package
TVSOP	Thin very small-outline package

V

V_{OLP}	Output low peak voltage
V_{OLV}	Output low valley voltage
V_{OHV}	Output high valley voltage
V_{OHP}	Output high peak voltage

Insert Tab Here

Basic Design Considerations for Backplanes

SZZA016
June 1999

TEXAS INSTRUMENTS

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Contents

List of Illustrations

Abstract

This paper describes the design issues relevant to backplane design. Designing a high-performance backplane can be extremely complex, where issues such as distributed capacitance, stub lengths, signal integrity, noise margin, rise time, flight time, and propagation delay need to be defined and optimized to achieve good signal integrity on the backplane board. This application report is based on a GTL+ backplane driver used to study the effects of these issues. Guidelines that should be followed by backplane designers for optimal board design are detailed. The information in this application report should enable the design engineer to successfully design a high-performance backplane using GTL+.

Introduction

The basic backplane is a parallel-data-transfer topology used in a multipoint transfer scheme. This application report discusses some of the basic design issues encountered in such a system. The effects of distributed capacitance on termination resistance and flight time are examined. The backplane lines are viewed from a dc perspective. Various effects of the stubs and connectors are discussed.

Topology

Figure 1 is an example of a simple point-to-point data transfer. A driving device at point A drives a 51-Ω transmission line. A termination resistor (R_T) is placed at point B along with a receiving device. The transmitter is an open-drain device. The transmission line is a 25.4-cm or 10-in. (l), 51-Ω (Z_o) stripline with a 138-pF/m or 3.5-pF/in. characteristic capacitance (C_o). Using the equation $t_{pd} = Z_o C_o$ yields a 7.03-ns/m or 178-ps/in. propagation delay (t_{pd}) and a total flight time [$t_{(flight)}$] (time for the signal to propagate down the transmission line) from A to B ($l \times t_{pd}$) of 1.785 ns.

$$t_{(flight)} = \left(\frac{t_{pd}}{\text{unit length}}\right)\text{length of line} \quad (1)$$

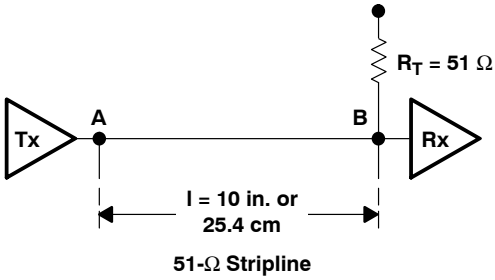

Figure 1. Point-to-Point Application

In Figure 2, the point-to-point configuration is a multipoint layout with a 1-in. spacing (d) on the stripline. There is one transmitter (Tx) and ten receivers (Rx). In a multipoint system, any position can assume the role of transmitter, with the remaining positions being receivers. The 51-Ω stripline is terminated on both ends of the transmission line. The termination resistance (R_T) is calculated later, but is less than 51-Ω when all card slots are filled, i.e., the backplane is fully loaded.

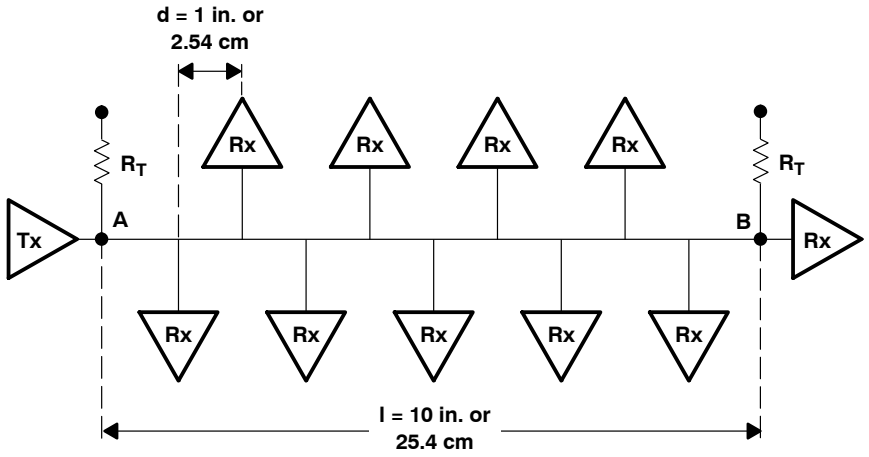

Figure 2. Multipoint Application

Distributed Capacitance

Figure 3 is a simplified version of Figure 2, with receivers replaced by capacitors. The values of the capacitors are discussed later in this report, but are assumed to be 12 pF. In this report, it is assumed that the spacing between card slots is within the rise/fall time of the driver signal and that all slots are populated with cards. The capacitance (C_d) can then be distributed uniformly at an equivalent rate of capacitance per inch.

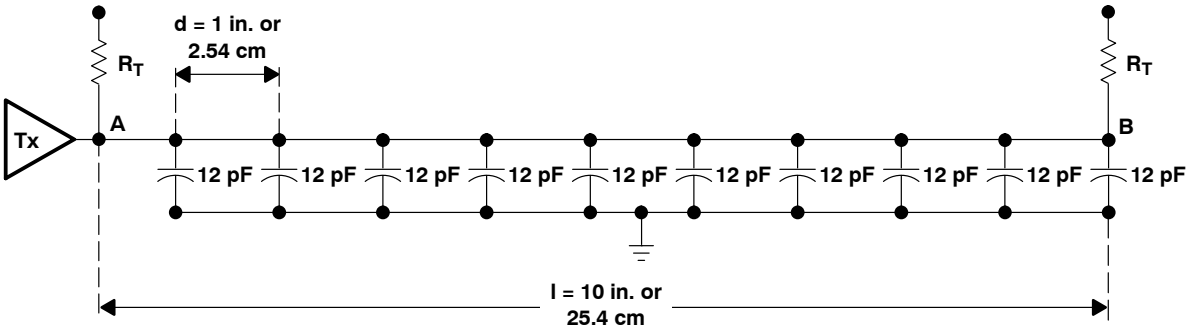

Figure 3. Equivalent Multipoint Application

When all slots are filled, the 10-in. transmission line has 12-pF capacitance distributed at 1-in. intervals. The distributed capacitance (C_d) affects both the propagation delay and the characteristic impedance of the stripline. The results are a new effective impedance, $Z_{o(eff)}$, and a new effective propagation delay, $t_{pd(eff)}$. The applicable equations are:

$$Z_{o(eff)} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} \quad (2)$$

$$t_{pd(eff)} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}} \quad (3)$$

The effects of the term $\sqrt{1 + \frac{C_d}{C_o}}$ on Z_o and t_{pd} are shown in Figures 4 and 5. The effective impedance and t_{pd} are graphed in terms of characteristic impedance and t_{pd}. As an example, consider a 50-Ω line (Z_o) with a t_{pd} of 180 ps/in. (7.09 ns/m) used in a system where the C_d/C_o ratio is 3. From the graph in Figure 4, the effective impedance is 0.5 of the characteristic impedance, or $Z_{o(eff)} = 0.5 \times Z_o = 25\ \Omega$. Figure 5 shows that, for the same C_d/C_o ratio, $t_{pd(eff)} = 2 \times 180 = 360$ ps/in. (14.18 ns/m) for the loaded line.

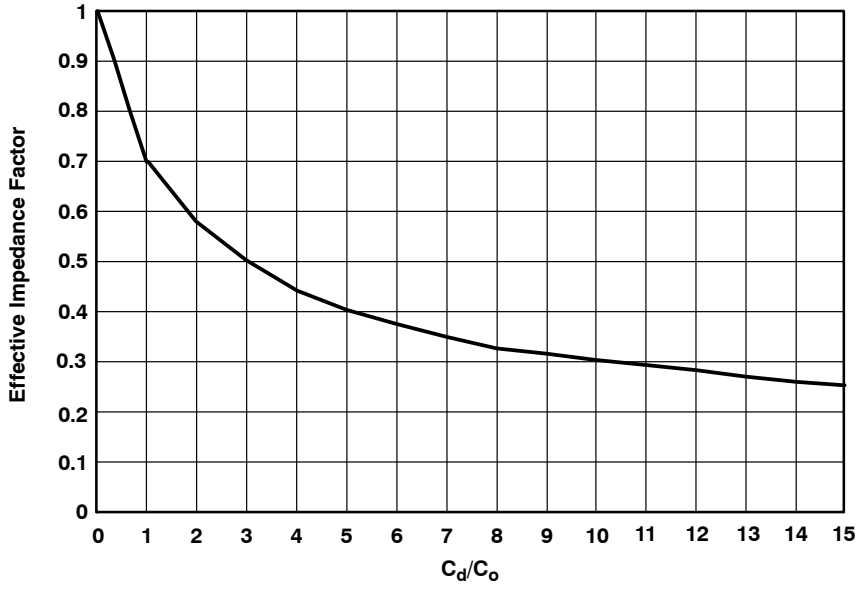

Figure 4. Effective Impedance vs C_d/C_o

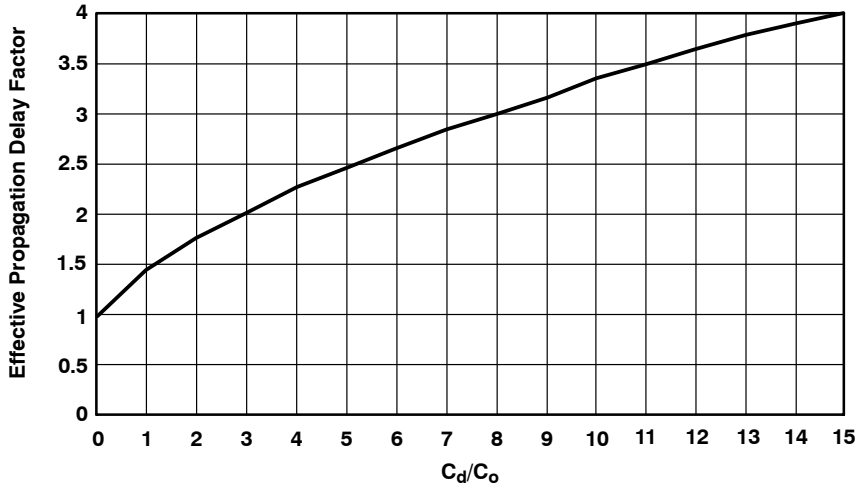

Figure 5. Effective t_{pd} vs C_d/C_o

If the loads (capacitors in Figure 3) are equally spaced by (d) inches, the distributed capacitance equals the total capacitance at each point (C_t) divided by the separation, or $C_d = C_t/d$. In our example, C_d = 12/1 or 12 pF/in. (472 pF/m). The term $\sqrt{1 + \frac{C_d}{C_o}}$ = 2.1. The C_d/C_o ratio is 3.43. The C_d/C_o ratio can be used with Figures 4 and 5 to see the changes in the normalized (characteristic) values of the transmission line. Using equation 2, the value of the effective impedance, $Z_{o(eff)}$ and, thus, the termination resistance (R_T), is 24.2 Ω. Using equation 3, the effective $t_{pd(eff)}$ is 375.6 ps/in. (14.79 ns/m). Using equation 1, the flight time is 3.76 ns from point A to B.

$$R_T = Z_{o(eff)} = \frac{Z_o}{\sqrt{1 + \frac{C_d}{C_o}}} \qquad t_{pd(eff)} = t_{pd}\sqrt{1 + \frac{C_d}{C_o}}$$

$$R_T = \frac{51}{2.1} = 24.2 \qquad t_{pd(eff)} = 178.5\ (2.1) = 375.6\ \text{ps/in.}$$

$$t_{(flight)} = \text{length} \times \frac{t_{pd}}{\text{unit length}}$$

$$t_{(flight)} = 10\ \text{in} \times 375.6\ \text{ps/in.} = 3.76\ \text{ns}$$

Figure 6 shows a typical connection scheme between the backplane stripline and the driving/receiving device on the daughter cards. Point C is the connection to the backplane stripline, while point D is the connection to a transceiver integrated circuit. The total capacitance (C_t) at point C is the sum of each of the elements in the connection chain.

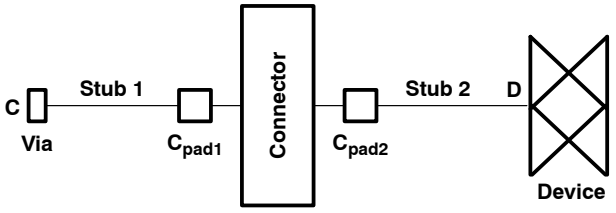

Figure 6. Typical Connection Scheme to Backplane

In Figure 6, the stub lines (stub 1 and stub 2) are 51-Ω microstrip with a characteristic capacitance of 2.6 pF/in. (102 pF/m). The connection via connects the stripline to the upper trace (microstrip) and has an approximate capacitance of 0.5 pF. Stub 1 has a length of 1/16 in. and connects to the surface-mount pad for the connector (C_{pad1}), approximately 0.5 pF. The SPICE model for this connector has the connector capacitance (C_{con}) at 0.74 pF. C_{pad2} is the surface-mount pad for the connector on the daughter card. The daughter-card stub (stub 2) length is 1 in., while the device input/output capacitance (C_{io}) is listed at 7 pF. The capacitance in this chain is:

$$C_t = C_{via} + C_{stub1} + C_{cpad1} + C_{con} + C_{cpad2} + C_{stub2} + C_{io} \qquad \textbf{(4)}$$

$$C_t = 12\ \text{pF}$$

Where:

C_{via} = capacitance of via = 0.5 pF
C_{stub1} = capacitance of stub 1 = 0.0625 × 2.6 = 0.16 pF
C_{cpad1} = capacitance of $C_{pad1} = C_{pad2}$ = 0.5 pF
C_{stub2} = capacitance of stub 2 = 1 × 2.6 = 2.6 pF
C_{con} = capacitance of connector = 0.74 pF
C_{io} = input/output capacitance of device = 7 pF

The total capacitance (C_t) of 12 pF is placed at point C on the backplane. This is where the capacitance value used for each receiver in Figure 3 was determined.

Figure 7 shows the results of an HSPICE simulation of the circuit in Figure 3, with 51 Ω used for the (R_T) pullup terminations to 1.5 V. The transmitter (driver) is a high-drive GTL device operating at a clock frequency of 50 MHz. The effects of the reflections, due to termination mismatch, can be clearly seen.

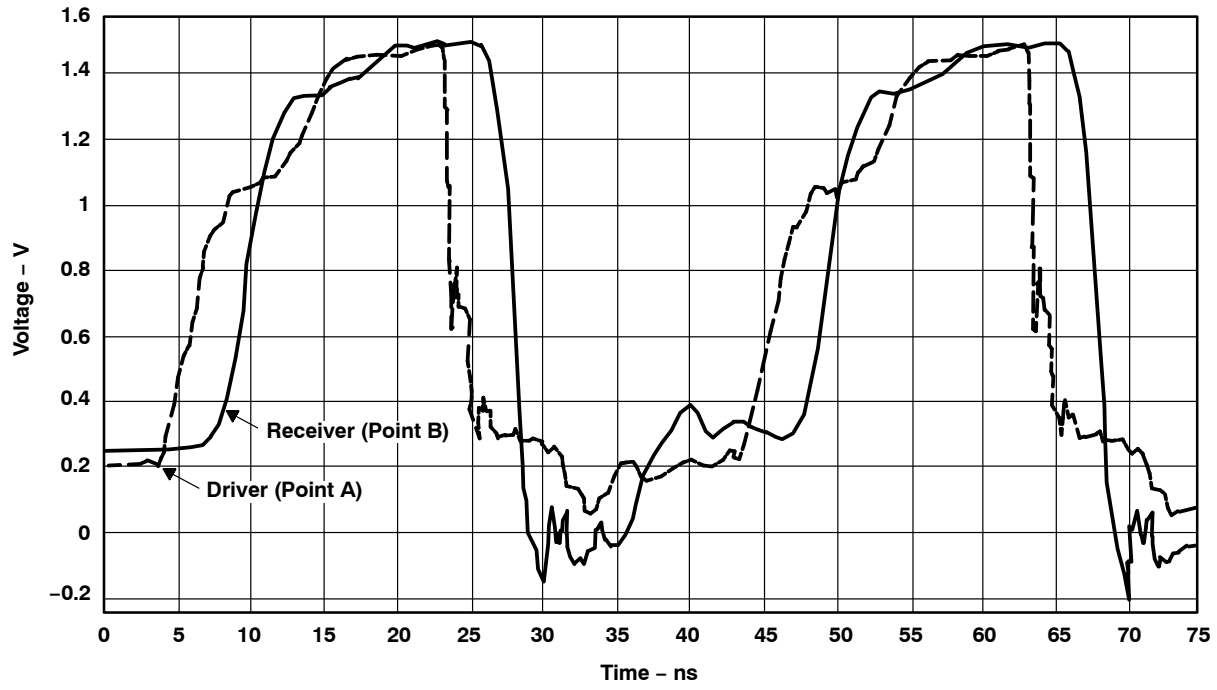

Figure 7. Mismatched Line Termination

Figure 8 shows the same waveforms when the termination resistors are changed to the calculated value of 24.2 Ω. The improvement in signal integrity is due to the matching of the termination resistors to the loaded impedance of the stripline. The delay between the two signals is measured at the threshold level for the GTL device (1 V). The SPICE simulation reveals that the flight time from point A to point B is the same as calculated in the previous discussion.

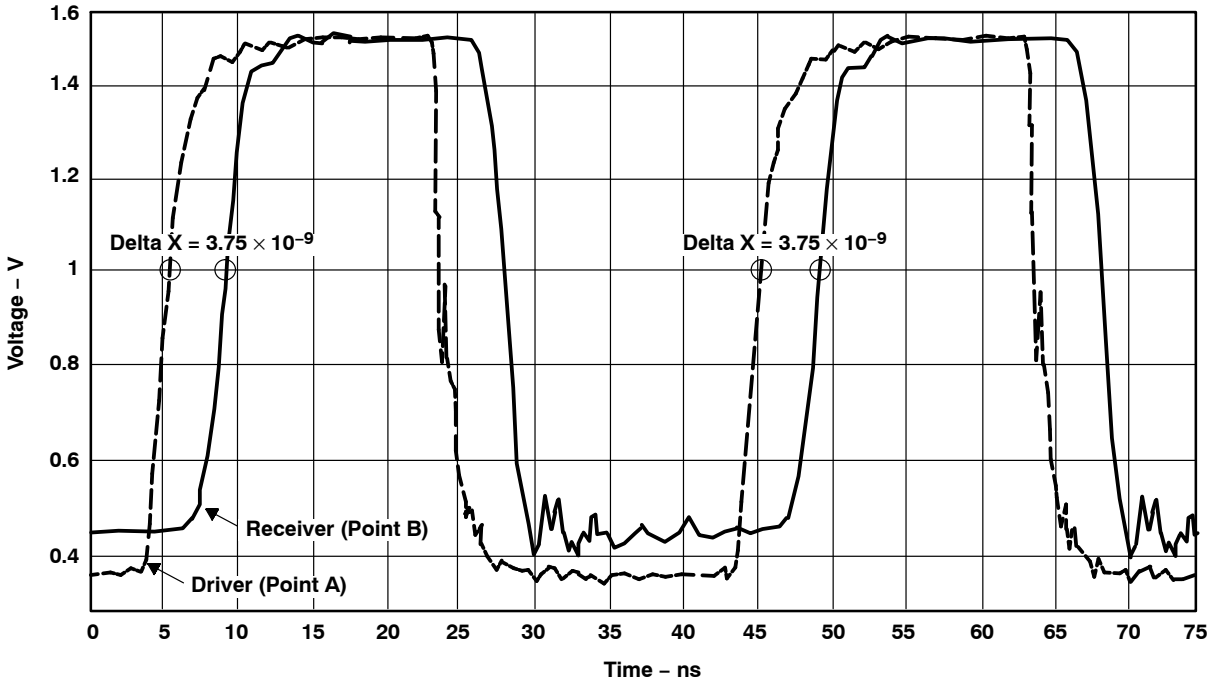

Figure 8. Matched Line Termination

Table 1 shows the effects of distributed capacitance on various microstrips and striplines used in backplane design. In this example, the distributed capacitance is 12 pF/in. In a loaded backplane, microstrip lines have a faster effective t_{pd} than striplines of the same impedance (Z_o), but have lower *effective* impedance, which requires a lower termination resistance. The designer must balance the required signal propagation time with the GTL driver capabilities when deciding which type of line to use and what characteristic impedance to choose.

Table 1. Comparison of Backplane Lines (Loaded Backplane, C_d = 12 pF/in.)

TYPE LINE Er = 4.5	Z_o (Ω)	C_o/in. (pF)	t_{pd}/in. (ps)	$Z_{o(eff)}$ (Ω)	$t_{pd(eff)}$/in. (ps)
Microstrip	140	1	140	38.8	505
Microstrip	70	2	140	26.5	370
Microstrip	50	2.8	140	21.7	322
Microstrip	30	4.67	140	15.9	265
Stripline	140	1.29	180	43.6	578
Stripline	70	2.58	180	29.5	428
Stripline	50	3.6	180	24	375
Stripline	30	6	180	17.3	312

DC Effects

Figure 9 is the dc circuit equivalent of Figure 2. The driver (transmitter) is replaced by its on resistance (R_{device}), and the transmission line is replaced by its dc resistance (R_{line}). The current I3 is the sum of currents I1 and I2. The voltage V_{OL1} when the output is low at the driver, is the product of R_{device} and I3. The voltage V_{OL2} is the low level seen at the last receiver and is V_{TT} minus the product of R_T and I2.

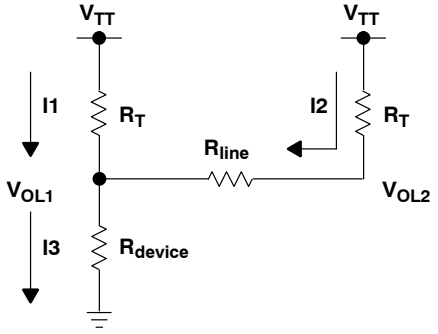

Figure 9. DC Equivalent of Single Backplane Line

In our example, R_T = 24.2 Ω, R_{line} = 2.2 Ω, and V_{TT} = 1.5 V. The basic equation starts with:

$$I3 = \left(\frac{V_{TT}}{R_T // R_T + R_{line}}\right) + R_{device} \quad (5)$$

Where:

$R_T // R_T + R_{line}$ = parallel resistance of the upper branch

The following equations can be derived from equation 5:

$$V_{OL1} = \frac{(V_{TT})(R_{device})(2R_T + R_{line})}{(R_T)(R_T + R_{line}) + (R_{device})(2R_T + R_{line})} \quad (6)$$

$$V_{OL2} = V_{OL1} + \frac{(R_{line})(V_{TT} - V_{OL1})}{R_T + R_{line}} \quad (7)$$

$$R_{device} = \frac{(R_T)(V_{OL1})\left(R_T + R_{line}\right)}{(V_{TT} - V_{OL1})(2R_T + R_{line})} \quad (8)$$

For the GTL16612A device used in Figure 8, the R_{device} value was estimated to be 4 Ω. Using equation 6, V_{OL1} = 0.361 V, and using equation 7, V_{OL2} = 0.456 V. The dc analysis can help provide the designer with best-case (V_{OL1}) and worst-case (V_{OL2}) signal levels expected at the receivers on a backplane when the termination resistance has been determined. The V_{OL} levels affect noise margins at the receivers, which is illustrated by Figure 8. The signal at point B is the last receiver on the backplane. The low level of this signal is higher than that of point A. At lower values of R_T and on longer backplanes (higher values of R_{line}), this difference becomes greater. The drive capability (R_{device}) of the transmitter will also affect the levels of the waveforms.

Stubs

The effects of stubs are largely manifested in the driver stub. These effects are in two distinct categories: flight time and rise time.

The longer the stub, the longer it takes for a signal to propagate down it, and this results in increased flight time from the driver to the backplane line (stub delay).

One of the interesting effects of the stub is the faster rise time observed at the driver circuit. The inductance of the stub and connector form an L-C-R network between the driver and load (backplane). Figure 10 is a simplified equivalent circuit.

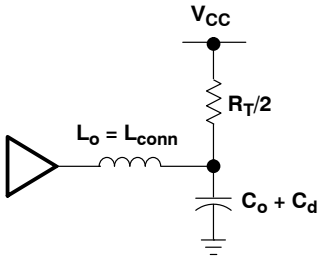

Figure 10. Thevenin Equivalent of Load

The longer the stub length or the higher the stub impedance (Z_o), the larger the value of inductance that is seen by the driver [the sum of the stub line inductance (L_o) and the connector inductance (L_{conn})], and, thus, the faster the rise time of the driving waveform. The faster rise time causes increased ring back (increased reflections) and worsens the signal integrity of the system.

Figure 11 shows the results of simulation data taken on rise time when only the impedance of the stubs was changed. The termination resistance was changed with each new value of stub impedance because this changes the distributed capacitance on the backplane. S1 is the rise time measured at the driver. S2 is the rise time measured at the beginning of the backplane. S3 is the measured rise time when the signal leaves the backplane at the last receiver slot. S4 is the measured rise time at the last receiver. The higher-impedance stubs (higher inductance) result in a faster driver rise time and, thus, faster rise times at all points along the backplane.

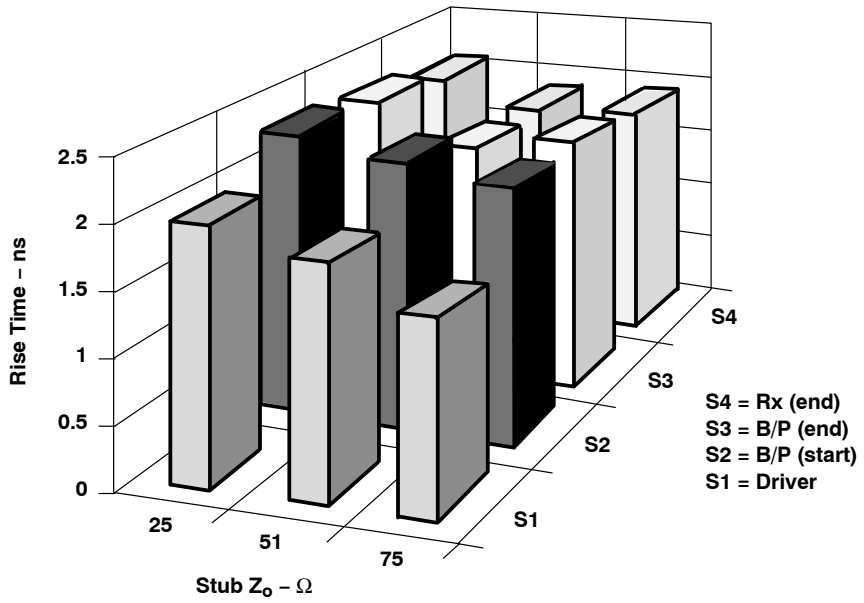

Figure 11. Rise Time vs Stub Z_o at Various Points on the Backplane

Figure 12 demonstrates the effects of stub length on stub delay and driver rise time. For this graph, the stub impedance was fixed at 51 Ω, and only the lengths and termination resistance were changed. The capacitance of the different stub lengths changed the distributed capacitance on the backplane. Figure 12 shows that, as the stub length is increased, the stub delay increases and the driver rise time decreases.

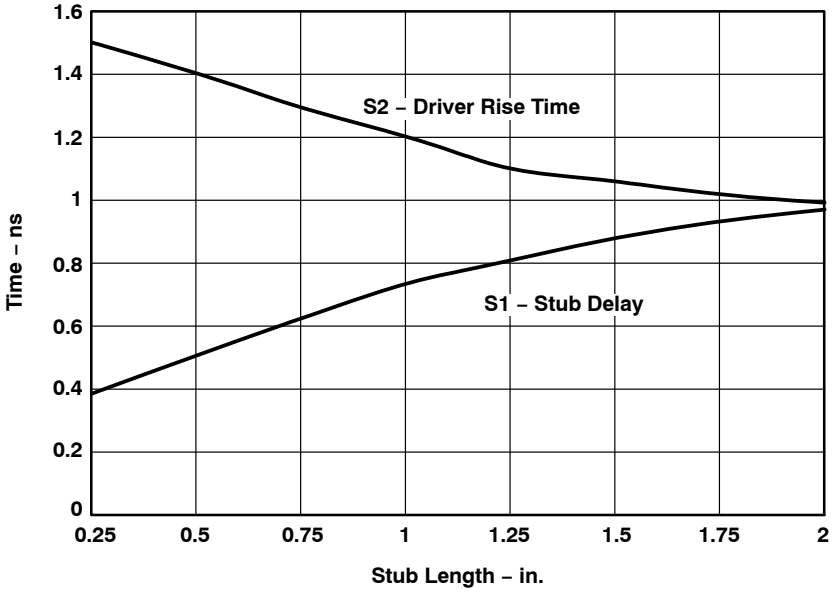

Figure 12. Effects of Stub Length on Stub Delay and Rise Time

Figure 13 shows the effects of stub lengths on the termination resistance. Figure 13 demonstrates that longer stub lengths result in lower termination resistance.

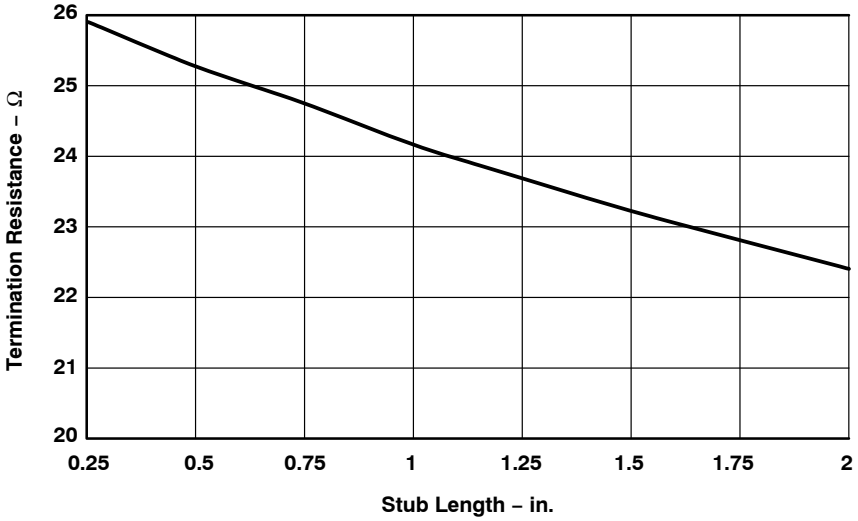

Figure 13. Effect of Stub Length on Termination Resistance at S1

In all three cases, minimum stub lengths are desired. This results in reduced stub propagation delay, less change in rise time, and minimum change in termination resistance. A design goal for stub length would be 1 in. or less.

Figure 14 illustrates the results of simulations for flight time in a backplane. Various stub impedances, coupled with a fixed 50-Ω connector, were used in the system simulations depicted in Figure 2. The stub lengths were held constant and the termination resistance was calculated based on the distributed capacitance. The driver's rise time (20% to 80%) was set to 1.5 ns. The measurements were made from the delay between the driver and the last receiver. This plot indicates that there is a range of stub impedances that results in minimum system flight time. The higher-impedance stubs have a larger value of inductance that produces longer stub delays, which resulted in a longer flight time. The lower-impedance stubs have larger values of capacitance that resulted in increased distributed capacitance on the backplane. This increased the effective propagation delay on the backplane and increased the flight time.

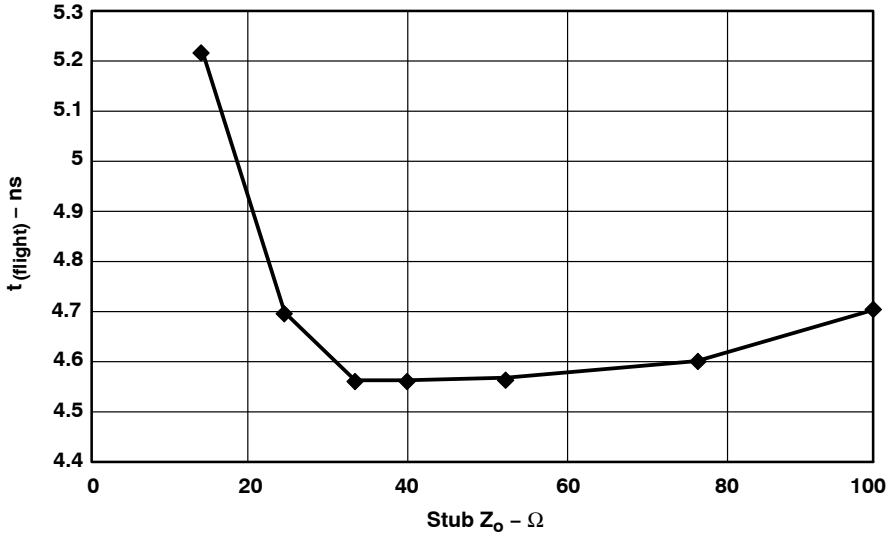

Figure 14. System Flight Time vs Stub Impedance

Conclusion

The capacitance loading effects on a transmission line used in a backplane system must be accounted for from both a signal-integrity standpoint and a system-timing standpoint. Minimizing the distributed capacitance on the backplane lines can be accomplished by selecting low-capacitance, low-inductance connectors; using devices with low I/O capacitance; and by keeping stub lengths short.

The selected drivers used in the system must be capable of driving the lower-than-characteristic impedance terminations on a loaded backplane, and should be able to maintain the minimum required V_{OL} levels along the backplane.

The summation of the flight time (from the driver to the farthest receiver on the backplane), the driving device's internal propagation delay, and the receiving device's setup time can limit the maximum operating frequency of a clock-synchronous system to well below the maximum limit of the driving device. To maximize the frequency of this system, the designer should minimize flight time and use devices with low propagation delay and setup time.

Acknowledgment

The authors of this application report are Ernest Cox, Ramzi Ammar, and Shankar Balasubramaniam.

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Johnson, Howard and Graham, Martin. 1993. *High-Speed Digital Design*, Prentice-Hall, Inc.

Glossary

Characteristic capacitance, C_o	Capacitance per unit length of a transmission line in free space
Characteristic impedance, Z_o	Impedance of a transmission line as defined by $Z_o = \sqrt{\frac{L_o}{C_o}}$
Characteristic inductance, L_o	Inductance per unit length of a transmission line in free space
C_{io}	Input/output capacitance of a transceiver integrated device
Effective impedance, $Z_{o(eff)}$	Impedance of a transmission line when external capacitance is added at fixed intervals along the line: $Z_{o(eff)} = \sqrt{\frac{L_o}{C_o + C_d}}$
Flight time, $t_{(flight)}$	Time for a signal to propagate between two points on a transmission line when the distance (l) between the points is known: $t_{(flight)} = 1 \times t_{pd}$
Propagation delay, t_{pd}	Delay per unit length of a signal traveling down a transmission line, expressed by the formula $t_{pd} = Z_o C_o$
Termination resistance, R_T	Resistance that matches the effective impedance of a transmission line in order to minimize reflections: $R_T = Z_{o(eff)}$

Fast GTL Backplanes With the GTL1655

SCBA015
February 1999

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Abstract

This application report describes the physical principles of fast bus systems and the problems that can arise in their development. Transmission-line theory is the basis for comparing various specifications of TTL, BTL, and GTL integrated circuits.

The SN74GTL1655 universal bus transceiver (UBT™) is presented as an optimum solution for the design of backplanes for future high-speed bus systems. Comprehensive measurement results of tests on the SN74GTL1655 are included.

Introduction

Since the 1970s, bus systems have been used in every microprocessor system. In the early systems, the delay time of the driver was in the range of 15 ns to 20 ns, and the frequency of the system clock was about 1 MHz. The speed of the total system was determined primarily by the delay time of the active electronics, for example, the processor, gates, and bus drivers.

With increasing clock rates, the bus became more and more the bottleneck that limited the performance of the total system. To circumvent this limitation, numerous improvements have been introduced in modern bus systems:

Pipelining	By pipelining, instructions and data are continually transmitted from the memory to the processor.
Cache memory	To avoid having the fast processor continually waiting for the slow main memory (DRAM, EPROM), an intermediate storage of the current data is implemented in a fast cache memory.
Block transfer	The transfer of individual words of data is replaced by the transmission of complete data blocks.
Multimaster	Every device connected to the bus can initiate the transmission of data. The cumbersome and slow route of transferring data exclusively via the CPU is, therefore, no longer necessary.
Bus width	The bus width has grown from 8 bits to 64 bits, and larger.
Clock rate	The clock rate of the backplane has increased into the range of many tens of megahertz, e.g., with a PCI bus to 33 MHz or 66 MHz. The processor itself operates internally at far higher clock rates, e.g., at 400 MHz. The memory is connected by a dedicated bus that operates at very high clock rates, e.g., up to 400 MHz.

The first sections of this application report deal exclusively with general physical principles and conditions. The engineer developing a bus system must be concerned with these in order to achieve high data rates on the bus.

Then, circuit solutions based on TTL, BTL, and GTL logic families are compared. Particular attention is devoted to the GTL transceiver circuit having increased drive capability and support for live insertion.

Finally, SN74GTL1655 is presented and examined in detail.

Physical Principles

In data sheets, the delay times of driver circuits are commonly given with a load circuit of 50 pF and 500 Ω at the outputs. However, this load circuit does not correspond well to the actual effective loads in current application. Rather, it is intended to match the conditions existing with IC testers. In particular, a load of this kind corresponds in no way to reality with bus systems. If the connecting line between two components is compared with the relationship on a bus line, significant differences will be found to exist.

Does a Line Behave Like a Capacitive Load?

The conditions shown in Figure 1 represent a typical connecting line between two components. If the connecting line is 20 cm long, then there will be a very small capacitive load of 12 pF. As shown in Figure 2, modules are connected to a bus line with a spacing between them of 2 cm, and these contribute an additional capacitive loading of 20 pF/2 cm (= 10 pF/cm) (see Table 1). A typical bus line on the backplane wiring of a 19-inch rack having a length of 40 cm, therefore, has a total capacitance of 424 pF (10.6 pF/cm × 40 cm).

The development engineer needs to know the effect of the capacitive load on the signal delay of drivers under the previously mentioned conditions (C_L = 12 pF, or C_L = 424 pF). The delay times given in data sheets assume a load of 50 pF.

However, now the line no longer can be considered a capacitive load, but instead must be treated from the point of view of transmission-line theory. With the bus line described previously, a signal delay of 10 ns (25 ns/m × 0.4 m) from one end of the line to the other is observed. If a pulse edge is applied at the beginning of the line having a rise time of 2 ns, the signal proceeds 8 cm (2 ns/25 ns/m) within this rise time. During this pulse edge, nothing happens over the length of the rest of the bus line (32 cm). Therefore, during this time, the capacitance of a 32-cm line (340 pF) will not have been charged. The capacitance of this part of the line has no influence on the waveform or the signal delay of the driver circuit.

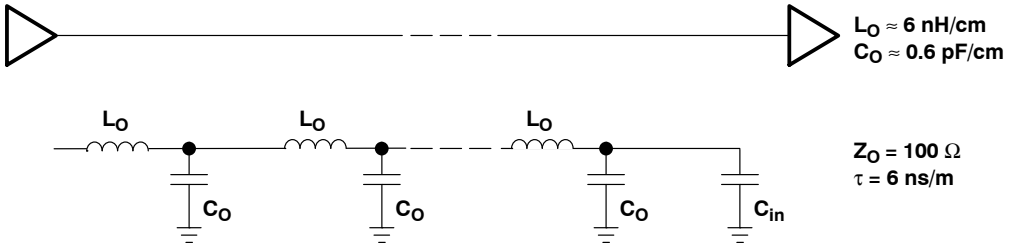

Figure 1. Physical Relationships on a Connecting Line Between Two Components

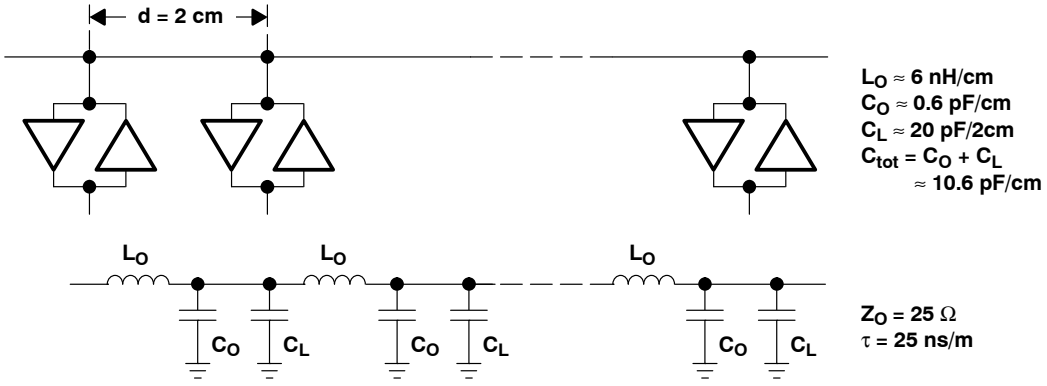

Figure 2. Physical Relationships on a Bus Line

Table 1. Additional Capacitive Loading of a Bus Line by a Module

CONTRIBUTOR	CAPACITANCE (pF)
Capacitance of the connector plug	≈5
Capacitance of the feedline from the driver input/output	≈5
Capacitance of the driver input/output	≈10
Capacitive loading from a module (total)	≈20

To illustrate this situation, Figure 3 shows a comparison between the waveform on a line with that from a load consisting of a lumped capacitance. It can be seen clearly in the diagram on the left that the length of a line and, therefore, its capacitance, has no influence on the waveform. To better observe the various loads, the rising edge is shown shifted by 10 ns. In the diagram on the right, instead of a line, a capacitor having the equivalent total capacitance value has been connected to the output of the test circuit. In this case, the output edge takes the form of a capacitor-charging curve. If the two measurement results are compared, it is clear that signals on a line behave very differently than in the case of a capacitive load. Therefore, an analysis using transmission-line theory is necessary.

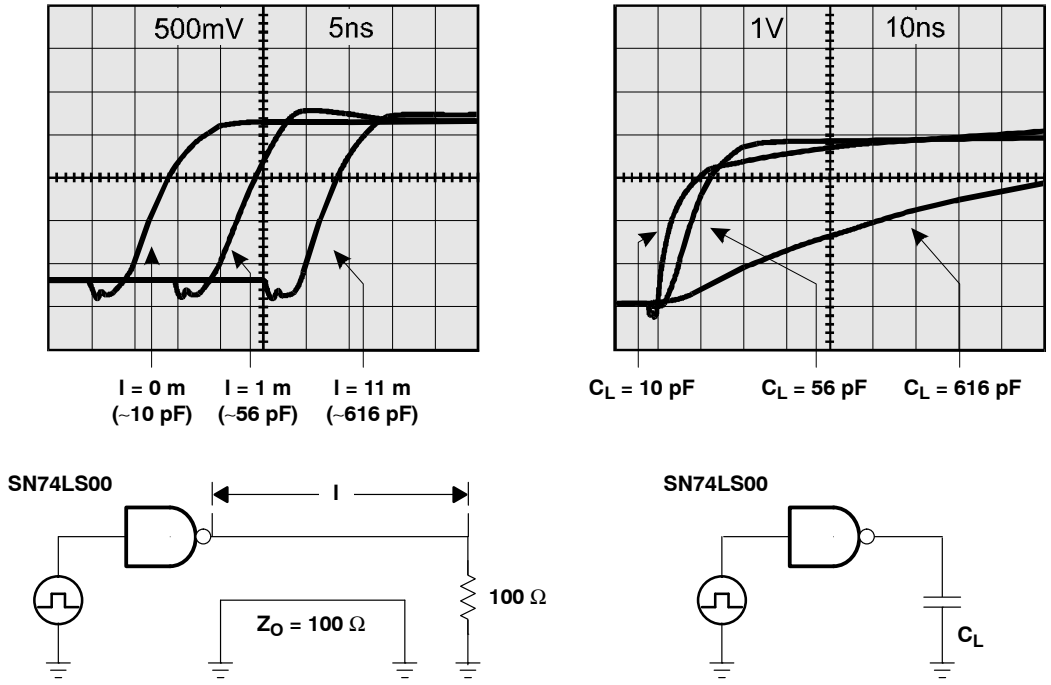

Figure 3. Waveform on a Line Compared to the Waveform With a Load Capacitor

Transmission-Line Theory in Practice

With lines of more than a certain length, the behavior of signals must be analyzed using transmission-line theory. There is a simple rule that applies in this situation:

> *If the rise time or fall time of a signal is shorter than twice the line propagation delay time, transmission-line theory must be used.*

In practice, transmission-line theory must be used for a bus line with a propagation delay of 25 ns/m and a signal with an edge rise time of 2 ns, from a line length of 4 cm (2 ns/25 ns/m × 2). Because buses usually are longer than 4 cm, transmission-line theory is a necessary basis for examining the physical characteristics of bus lines.

With the frequencies and lengths of lines that now are used commonly in bus systems, the transmission-line theory can be simplified by neglecting any resistive component of the impedance. Equations 1 and 2 can be used for lossless lines with sufficient accuracy. Typical values for the characteristic properties of point-to-point lines between two components and bus lines are given in Table 2.

$$Z_O = \sqrt{\frac{L'}{C'}} \quad (1)$$

$$\tau = \sqrt{L' \times C'} \quad (2)$$

Where:

Z_O = impedance of the line (Ω)
τ = propagation delay of the line (ns/m)
L' = inductive component of the line (nH/cm)
C' = capacitive component of the line (pF/cm)

Table 2. Typical Characteristic Properties of Lines

	L′ (nH/cm)	C′ (pF/cm)	Z_O (Ω)	τ (ns/m)
Point-to-point line between two components	5 to 10	0.5 to 1.5	70 to 100	≈5
Bus line	5 to 10	10 to 30	20 to 40	10 to 20

If a signal edge is fed into the beginning of the line (see Figure 4), a signal amplitude is created that can be calculated from the simple voltage divider consisting of the internal resistance of the signal generator and the impedance of the line (Equation 3). The termination resistor R_T can have no influence on the edge, since at this point the edge changes the voltage only at the beginning of the line, and at the end of the line no voltage change occurs.

$$U_i = U_G \frac{Z_O}{Z_O + R_G} \quad (3)$$

Where:

U_i = amplitude of the incident wave (V)
U_G = open-circuit voltage of the signal generator (V)
R_G = output resistance of the signal generator (Ω)
Z_O = impedance of the line (Ω)

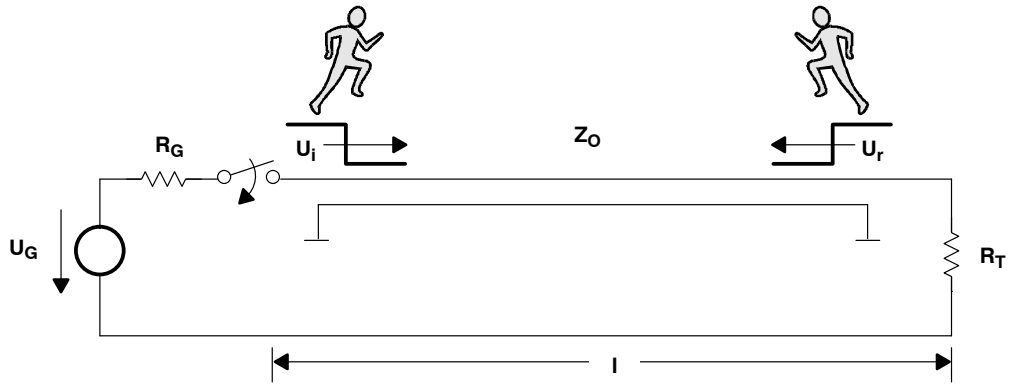

Figure 4. Wavefronts on Lines

This voltage edge now runs from the beginning of the line to the end. This first wave is called the incident wave. When the voltage wave reaches the end of the line, a reflected voltage wave is generated, the amplitude of which can be calculated from the reflection factor ρ, as shown in Equations 4 and 5.

$$\rho = \frac{R_T - Z_O}{R_T + Z_O} \quad (4)$$

$$U_r = U_i \times \rho \quad (5)$$

Where:

U_r = amplitude of the reflected wave (V)
U_i = amplitude of the incident wave (V)
ρ = reflection factor
R_T = termination resistor at the end of the line (Ω)
Z_O = impedance of the line (Ω)

Using Equations 3, 4, and 5, results at the end of the line can be predicted:

$R_T = 0 \Rightarrow \rho = -1$ (see Figure 5a)

The incident wave is inverted and reflected at the end of the line. Incident and reflected waves therefore cancel out each other, and no voltage increase is seen at the end of the line.

$R_T = Z_O \Rightarrow \rho = 0$ (see Figure 5b)

No line reflections occur. The end of the line is perfectly terminated.

$R = \infty \Rightarrow \rho = +1$ (see Figure 5c)

The incident wave is fully reflected at the end of the line. A doubling of the amplitude can be seen at the end of the line.

A detailed analysis follows in *The End of the Line: The Reflected Wave*.

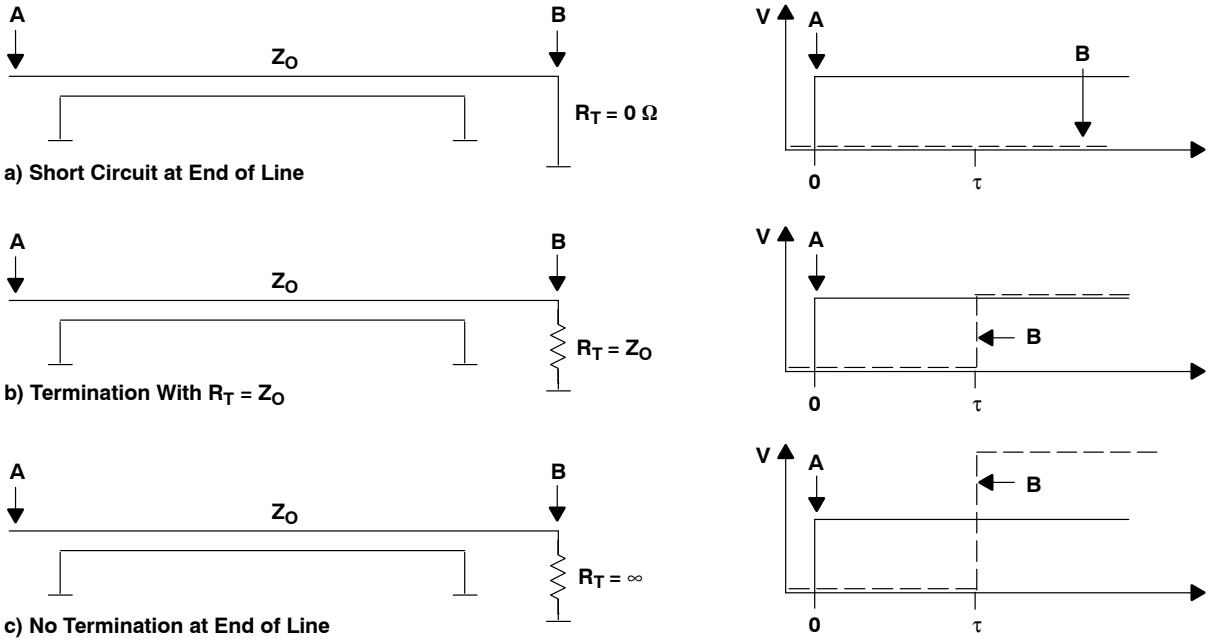

Figure 5. Signals at the End of the Line

Effects on Bus Lines

Beginning of the Line: The Incident Wave

A fundamental characteristic of bus drivers is their output resistance. Together with the line impedance, this forms a voltage divider (Equation 3) and is thus responsible for the amplitude of the incident voltage wave.

If the driver can generate an incident voltage edge that has an amplitude above (below) the defined voltage threshold for the high logic state (low logic state), the logic level of all inputs that are connected on the bus will be changed over with the incident wave. For TTL-compatible bus systems, the rising edge of the incident voltage wave must exceed 2 V, and the falling edge must fall below 0.8 V. To calculate the maximum signal delay on the bus, for an incident-wave-switching system, only the simple line propagation delay needs to be added to the delay time of the driver circuit (see Table 3).

Table 3. Signal Delay Using Figure 6 as an Example

	SWITCHING WITH THE INCIDENT WAVE	SWITCHING WITH THE REFLECTED WAVE
A⇒B	$t_{pd\ Driver} + t_{pd\ Receiver}$ = 5 ns + 5 ns = 10 ns	$t_{pd\ Driver} + t_{pd\ Line} + t_{pd\ Line} + t_{pd\ Receiver}$ = 5 ns + 10 ns + 10 ns + 5 ns = 30 ns
A⇒C	$t_{pd\ Driver} + t_{pd\ Line} + t_{pd\ Receiver}$ = 5 ns + 10 ns + 5 ns = 20 ns	$t_{pd\ Driver} + t_{pd\ Line} + t_{pd\ Receiver}$ = 5 ns + 10 ns + 5 ns = 20 ns
Worst case	20 ns	30 ns

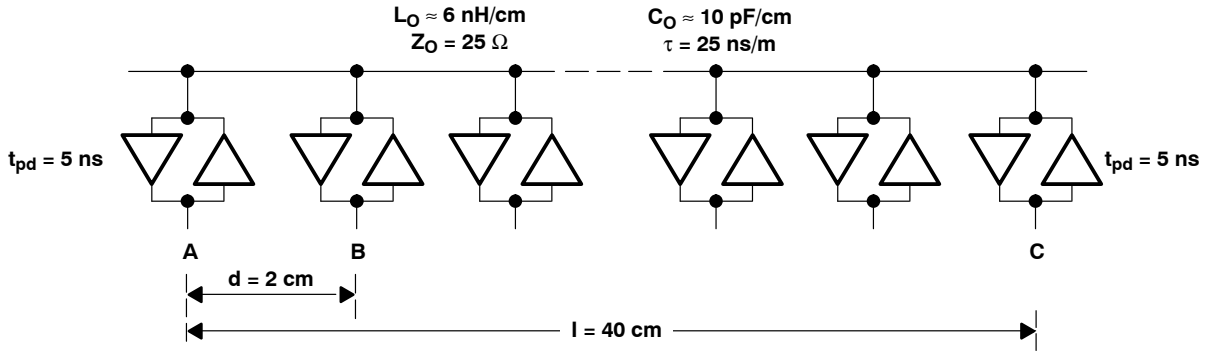

Figure 6. Example of a Bus Line

However, if the amplitude of the incident wave is insufficient, it is necessary to wait until the reflected wave returns from the end of the line to the beginning. Only then will a valid logic level have been reached on the entire bus line. In the example of Figure 6, according to Table 3, the signal delay time of 30 ns maximum results. Thus, when compared with switching with the incident wave, the signal delay time of the system is increased by 10 ns, or 50%.

This demonstrates one of the basic problems of bus systems. Since the amplitude of the incident wave depends on the voltage divider between the output resistance of the driver and the impedance of the line (≈25 Ω), a driver is needed with a particularly low output impedance. Only then is it possible to switch over a bus line with the incident wave. This is made more difficult by the fact that only two bus drivers are situated at the beginning or end of the line. Most drivers sit in the middle of the bus line, and from there must effectively drive two lines, one to the left and one to the right (see Figure 7). In this case, the resulting load impedance for drivers in the middle of the bus line is effectively halved (≈12.5 Ω).

Taking into account the voltage-divider rule for the incident wave, with TTL-compatible systems, an output resistance of < 10 Ω is needed for the rising edge, and < 4 Ω for the falling edge; the assumption here is that V_{OH} = 3.5 V, V_{OL} = 0 V. Even the most modern bus-driver families (such as the ABT family) do not have an output resistance that meets this requirement. For such applications, Texas Instruments (TI™) offers special TTL-compatible circuits featuring the low output resistances that are needed: the incident wave switching (IWS) devices from TI, SN74ABT25xxx, for example, the SN74ABT25245. All other circuits that have the required low-resistance outputs were developed for new bus systems that are not TTL compatible. Examples of these new bus systems include backplane transceiver logic (BTL) and Gunning transceiver logic (GTL).

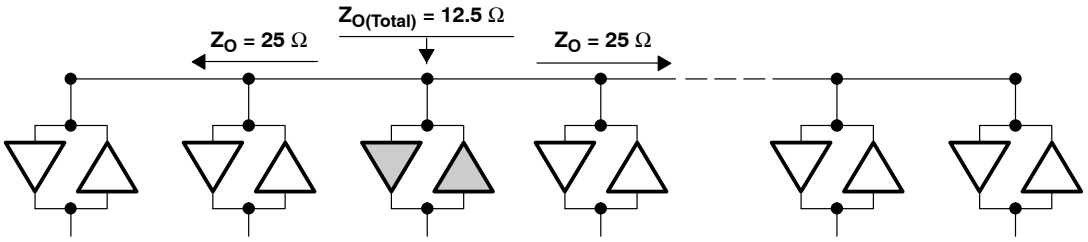

Figure 7. Load on a Driver in the Middle of the Bus is 0.5 × Z_O

End of the Line: The Reflected Wave

As explained in *Transmission-Line Theory in Practice*, a voltage wave is reflected at the end of a line, and this reflected wave moves back to the beginning of the line. The amplitude of the reflected wave is determined by the amplitude of the incident wave and the reflection factor (Equation 5). This reflection factor is determined by the line impedance and the termination resistance (Equation 4). Therefore, the termination resistance has a major influence on the waveform of a bus line.

For the case of no termination resistance at the end of the line ($R_T = \infty$), as shown in Figure 8a, the reflection factor is $\rho = 1$. The amplitude of the reflected wave is, therefore, exactly the same as the amplitude of the incident wave. In practice, this means that a low-resistance driver that generates an incident wave of 3 V, generates a reflected wave that also has an amplitude of 3 V. This results in an overshoot at the end of the line of 6 V ($V_{incident} + V_{reflected}$ = 3 V + 3 V). The worst-possible case would be a very low-resistance CMOS driver with an incident wave of 5 V, which would then give rise to an overshoot of 10 V at the end of the line.

If the value of the termination resistance is assumed to be exactly the same as that of the line impedance, a reflection factor of $\rho = 0$ (Figure 8b) results. In this case, no reflection of the arriving wave occurs; thus, it is an ideal line termination. However, this method cannot be used with TTL and CMOS-compatible bus systems, because the impedance of the line would make it necessary to have a termination resistor of 25 Ω. With bidirectional lines, it would be necessary to connect this termination resistor at both ends, and each driver then would have to drive a load of 12.5 Ω. The maximum current through these resistors would be 280 mA (3.5 V/12.5 Ω) per line. Because, in practice, a bus often has more than 100 lines, the maximum total current of the bus termination would be >28 A. For this reason, with TTL systems, one operates with other terminating networks (Figure 8c to 8f), and, in such cases, accepts a mismatch ($R_T > Z_O$).

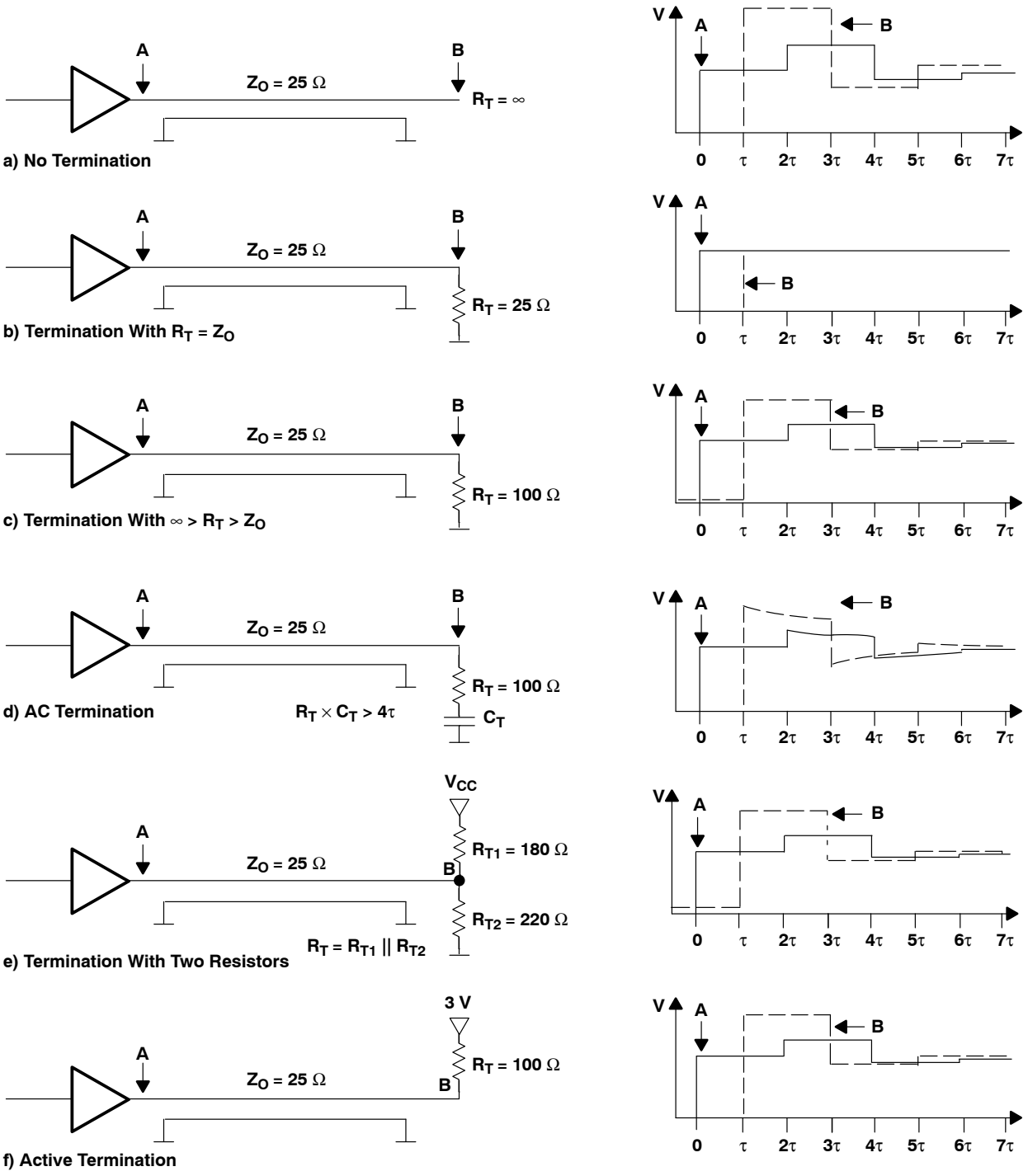

Figure 8. Termination Methods With TTL and CMOS Circuits

New Bus Systems Are Needed

The cause of most problems with bus lines is the distributed capacitive loading on the line by the modules connected to it. The impact on TTL and CMOS buses is:

- Very low signal speed on the line (about 25 ns/m, instead of 5 ns/m)
- The impedance of the line is reduced from about 80 Ω to about 25 Ω.
- As a result of the low impedance, an adequate amplitude of the incident wave is possible only with extremely low-resistance drivers.
- Correct termination is not possible because, otherwise, excessively high currents would flow through the terminating resistors.

It is not possible to solve these problems adequately with the circuit techniques commonly used with TTL- and CMOS-compatible circuits. With the commonly used techniques, it always would be necessary to accept a compromise in the circuit layout.

To develop a new bus system meeting the requirements imposed by the situation mentioned above requires the following:

- The capacitance of a module must be reduced, and also the capacitance of the I/O pins of the bus-driver circuit.
  - Because of the reduced capacitive component of the bus line, the impedance is reduced only to about 30 Ω.
  - The smaller capacitive component also results in less degradation of the signal speed (to about 20 ns/m).
- The drivers must be of low resistance to switch the bus with the incident wave.
- The signal amplitude must be reduced to allow correct termination of the line impedance. For example, with a signal amplitude of 1 V, a termination resistor of 30 Ω could be considered, since the current flowing will be only 33 mA per signal line.

The two bus systems that meet these basic physical requirements are BTL and GTL.

BTL Bus

The specification of the BTL bus was conceived especially for large backplane systems. The basic circuit layout of a BTL bus is shown in Figure 9.

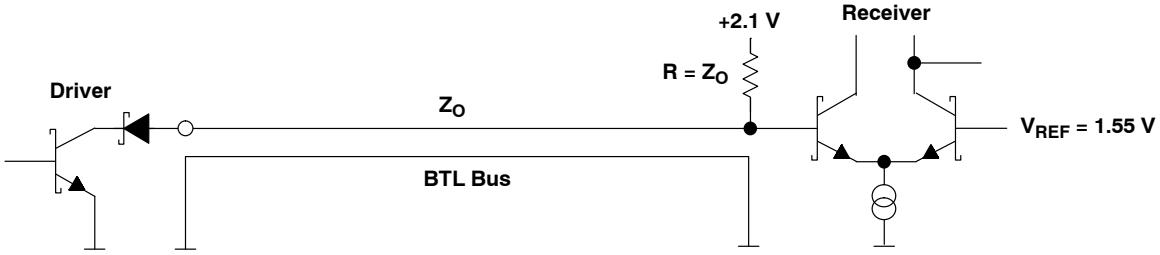

Figure 9. Circuit Concept of the BTL Bus

The outputs of a BTL driver are provided with open-collector pins. The maximum capacitance of an I/O pin was fixed at 5 pF. To attain this goal, a diode is connected in series with the output transistor. The series connection of the capacitance of the transistor with the capacitance of the diode results in a reduction of the total capacitance. This circuit results in a low level of 1 V.

To allow switching of the bus lines with the incident wave, the specification for the drive capability was fixed at I_{OL} = 100 mA.

The high level is generated with the help of a terminating resistor connected to 2.1 V at the end of the line. With bidirectional lines, a termination resistor must be provided at both ends of the line. As a result of the low signal amplitude of 1.1 V, the bus line can be correctly terminated with BTL systems. The maximum output current (I_{OL} = 100 mA) allows driving a terminating resistor of as low as 11 Ω (1.1 V/100 mA). If the BTL driver is in the middle of the bus line, the lower limit for the impedance is 22 Ω. This is sufficient for all bus systems that are used, particularly when the impedance and the signal speed are kept high, as a result of the limitation in the I/O capacitance.

By definition, the threshold voltage lies at 1.55 V, exactly midway between the low and high levels.

In large systems, it is essential that it be possible to remove and reinsert boards during system operation (live insertion). To meet this requirement, the precharge function has been implemented in BTL circuits. By means of this function, the capacitance of the pin, the stub line, and the I/O pin on the insertable board can be charged to the threshold voltage (1.55 V) before this pin comes in contact with the signal line on the backplane. Thus, it is possible to prevent signals on the backplane wiring from being so seriously interfered with that the data is corrupted.

The most serious disadvantage of the BTL bus is its high power consumption. If the transistor of a driver stage is operated to the limits of its specification, at the low level, a current of 100 mA can flow, with a voltage drop of 1 V. This results in the output stage dissipating 100 mW. If a 16-bit bus driver is used, in the worst case, 1.6 W may be consumed in the output transistors alone. With small surface-mounted components, this power consumption makes it necessary to use packages with a special heatsink.

GTL Bus

As shown in Figure 10, the basic circuit layout of the GTL bus is very similar to that of BTL. In this case, there also is a system with open-drain drivers and correct bus termination. The voltage levels of the logic states are 0.4 V in the low-logic state, and 1.2 V in the high-logic state. The signal amplitude is reduced to 0.8 V, whereby the threshold voltage lies exactly between the low and high levels, also at 0.8 V.

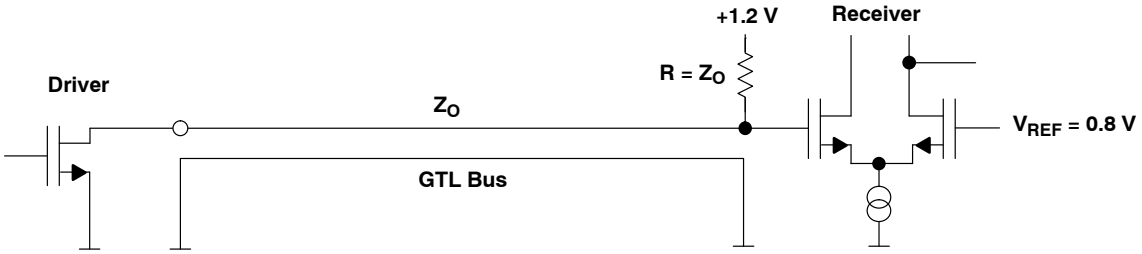

Figure 10. Circuit Concept of the GTL Bus

In contrast to the BTL circuits, the drive capability of the output transistor is 40 mA. Therefore, the lower limit of the termination resistance (also of the line impedance) is 20 Ω (0.8 V/40 mA). For a driver connected to the middle of a bus line, the limit for the impedance of the line is 40 Ω. To attain impedance of the bus lines of 40 Ω, the capacitive component of the line must not be too high. Therefore, GTL is not the first choice when driving extensive backplane wiring with many modules.

Since the GTL bus was conceived for smaller buses on a circuit board, for example a memory bus between CPU and memory modules, the specification does not include the precharge function. The reason is that, when the bus is on a circuit board, there is no question of withdrawal and reinsertion during operation.

Comparison Between BTL and GTL

The structure of the two bus concepts (BTL and GTL) is similar. Both operate with open-collector/open-drain outputs and correct line termination. The most obvious difference is the definition of the logic voltage levels (Figure 11). The characteristics are listed and compared in Table 4. For large backplane wiring systems, the BTL circuits have the better characteristics, whereas the GTL bus features significantly lower power consumption. The target applications, which were in mind when designing each of these bus systems, are apparent: BTL for large backplane systems, and GTL for smaller buses on a circuit board.

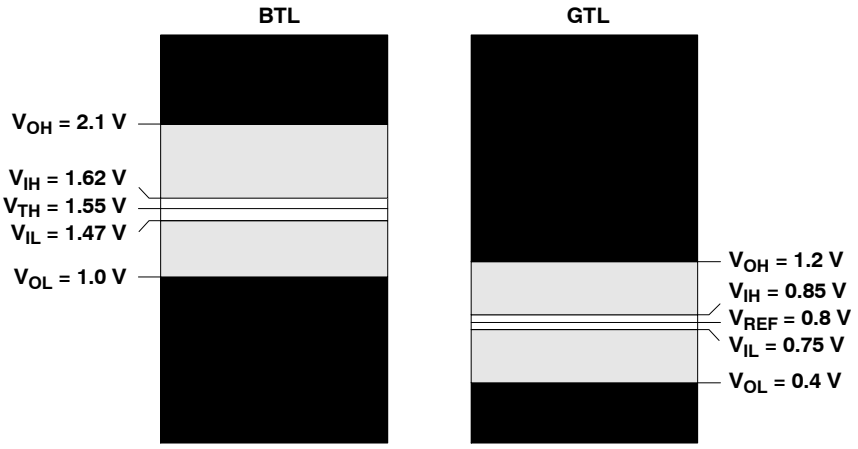

Figure 11. Comparison of the Logic Voltage Levels of BTL and GTL

Table 4. Comparison of the Characteristics of BTL and GTL

CHARACTERISTICS	BTL	GTL
Capacitance of an I/O pin	5 pF	Not defined, typically 5 to 9 pF
I_{OL}	100 mA	40 mA
Maximum power consumption of an output driver	100 mW	16 mW
Minimum Z_O for point-to-point connection	11 Ω	20 Ω
Minimum Z_O for a bus system	22 Ω	40 Ω
Precharge for withdrawing and reinserting boards during operation	Yes	No

New Backplane Solution: The GTL1655 From TI

It would be ideal to have a bus concept that combines all the desirable characteristics of both BTL and GTL. Meanwhile, TI offers a new generation of GTL drivers, that is compatible with existing GTL systems, but provides both the advantages of BTL and also the positive aspects of GTL drivers. A comparison is given in Table 5.

- The logic levels are compatible with GTL buses, and also bus systems with GTL+ levels. GTL+ represents a modification of the GTL specification that uses different termination voltage (V_{TT}) and reference voltage (V_{REF}) (see Table 6).
- Low capacitive loading of the bus (typical 6 pF)
- High drive capability (100 mA)
- Switching of a 12.5-Ω unidirectional line with the incident wave
- Switching of a 25-Ω bidirectional line with the incident wave
- Built-in precharge function

Table 5. SN74GTL1655 Compared With BTL and GTL

CHARACTERISTICS	BTL	GTL	GTL1655
Capacitance of an I/O pin	5 pF	< 9 pF	6 pF
I_{OL}	100 mA	40 mA	100 mA
Maximum power consumption of an output driver	100 mW	16 mW	50 mW
Minimum Z_O for point-to-point connection	11 Ω	20 Ω	12.5 Ω
Minimum Z_O for a bus system	22 Ω	40 Ω	25 Ω
Precharge for withdrawing and reinserting boards during operation	Yes	No	Yes
Variable edge rate at the GTL output	No	No	Yes
Bus hold	No	Yes	Yes

The individual characteristics of the SN74GTL1655 are discussed in detail in the following sections.

Features of the SN74GTL1655

Functional Description: SN74GTL1655 – a Universal Bus Transceiver

The SN74GTL1655 is described as a universal bus transceiver, i.e., a bus driver for a wide variety of applications.

The function of this component can be controlled and changed in accordance with the signals and static voltage levels applied to the various control inputs.

By means of the control inputs OE, $\overline{\text{OEAB}}$, $\overline{\text{OEBA}}$, LEAB, and LEBA, one of the following three operating modes for the SN74GTL1655 can be selected:

- Transparent mode

  The SN74GTL1655 behaves like a bidirectional bus driver, for example, the ’245.

- Level-sensitive storage (latch) mode

  The SN74GTL1655 behaves like a level-sensitive register (latch), for example, a ’373. However, in this case, it can be used bidirectionally.

- Edge-triggered storage (flip-flop) mode

  The circuit behaves like an edge-triggered register, for example, a ’374. In this mode, it can be used bidirectionally.

The operating mode can be set separately for each direction of transmission. An example of a typical application is shown in Figure 12.

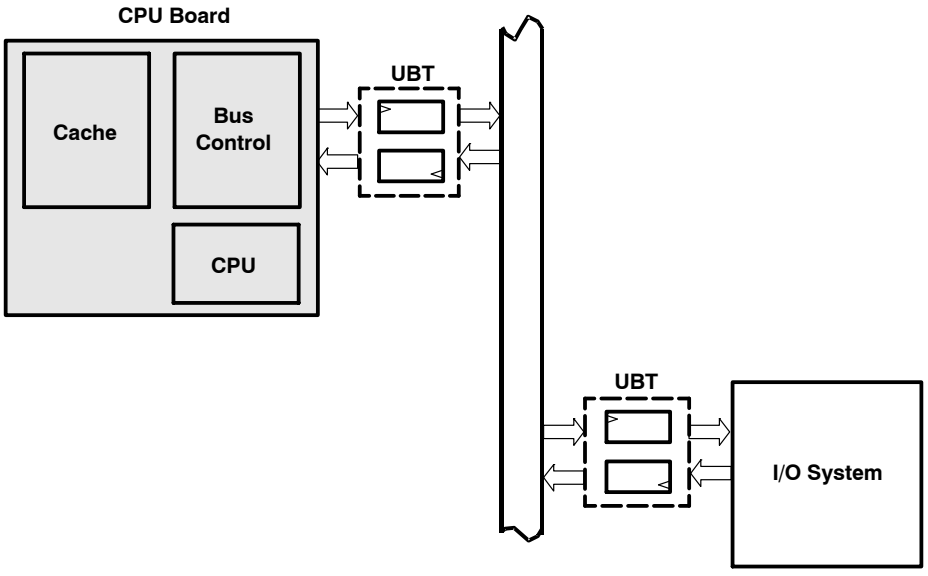

Figure 12. Typical Bus Application for a Universal Bus Transceiver

SN74GTL1655: The Link Between a GTL/GTL+ Backplane and an LVTTL Module

The SN74GTL1655 converts LVTTL-level signals (A port) into GTL or GTL+ -level signals (B port), and *vice versa*. The user decides, by choosing the termination voltage and the reference voltage, which level will be provided on the B-port side (see Table 6). The A port is, in every case, compatible with LVTTL.

This conversion is useful when continuing to work with LVTTL levels on the module, while the GTL and GTL+ levels, specially developed for this application, are transmitted on the backplane. The low-voltage TTL and GTL/GTL+ signal levels are shown in Figure 13. The SN74GTL1655 needs 3.3 V as the operating voltage.

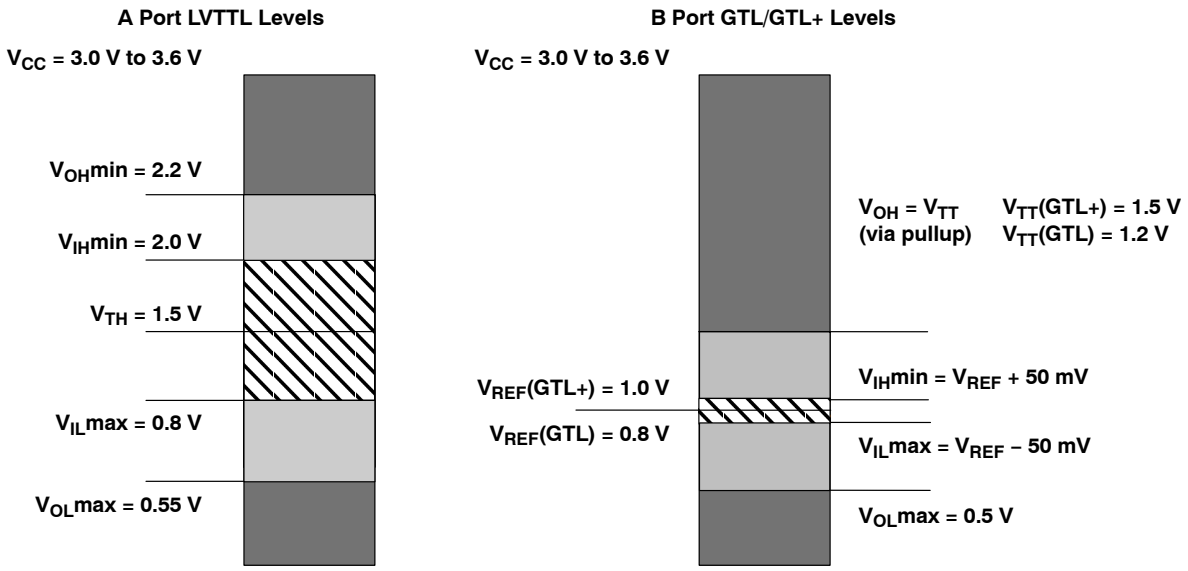

Figure 13. LVTTL and GTL/GTL+ Signal Levels of the SN74GTL1655

Table 6. Choice of the GTL/GTL+ Level (Using V_{TT} and V_{REF})

LEVEL		MIN	TYP	MAX	UNIT
GTL	V_{TT}	1.14	1.2	1.26	V
	V_{REF}	0.74	0.8	0.87	
GTL+	V_{TT}	1.35	1.5	1.65	V
	V_{REF}	0.87	1	1.1	

Termination Voltage, V_{TT}

There are various rules and techniques regarding proper line termination that should be observed for a successful development using GTL1655.

The termination voltage (V_{TT}) should be derived from a voltage regulator. The current requirements, e.g., up to 100 mA per output, must be observed. There are various voltage regulators available that meet these requirements. Depending on the application, the regulators should be situated either directly on the backplane or on the module boards connected to it.

If several signal lines are switched simultaneously, considerable current fluctuations may occur at the termination voltage. For this reason, bypass capacitors should be provided close to the termination resistors (Figure 14).

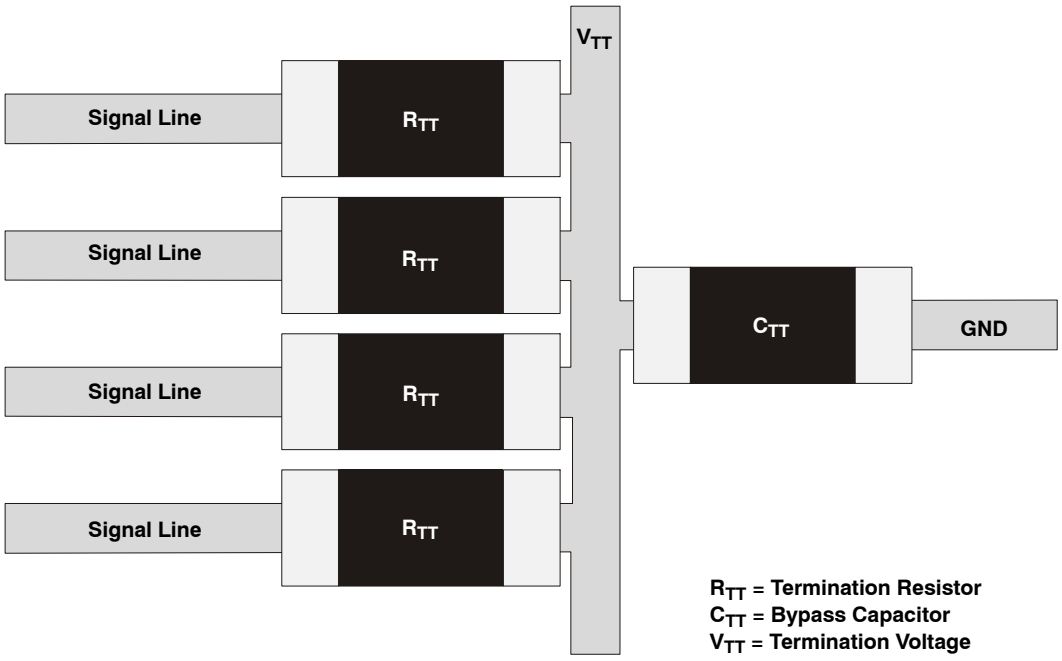

Figure 14. Proposed Layout of Termination Resistors and Bypass Capacitor on a Circuit Board

Since the bypass capacitor should have the lowest possible inductance, it is recommended that ceramic capacitors in surface-mount packages be used. The value of capacitance can be calculated from Equation 6.

$$C = I\frac{\Delta t}{\Delta U} \tag{6}$$

I = 50 mA For bidirectional lines with a termination resistor at both ends of each line, a maximum of one-half the output current of a GTL1655 (I_O = 100 mA) can flow through one of the two termination resistors.

ΔU = 10 mV In this example, the collapse of the termination voltage V_{TT} must not exceed 10 mV.

Δt = 4 ns The collapse of the termination voltage V_{TT} should be postponed for at least 4 ns.

$$C = I\frac{\Delta t}{\Delta U} = 50\ \text{mA} \times \frac{4\ \text{ns}}{10\ \text{mV}} = 20\ \text{nF} \tag{7}$$

If 82-nF ceramic capacitors are used, a bypass capacitor should be provided for every four signal lines. A proposed layout for the four termination resistors and the bypass capacitor on a circuit board is shown in Figure 14.

Reference Voltage, V_{REF}

The GTL or GTL+ reference voltage (V_{REF}) can be derived, using a simple voltage divider and a bypass capacitor (0.01 to 0.1 μF), from the termination voltage. The circuit shown in Figure 15 has the advantage that V_{REF} follows voltage fluctuations of the termination voltage, V_{TT}. In this way, the maximum possible signal-to-noise ratio (SNR) always is ensured, even with an unstable termination voltage. Since only a very small current (maximum 10 μA) flows in the V_{REF} pin of the SN74GTL1655, the pin can be connected to the voltage divider without adversely affecting the GTL/GTL+ reference voltage.

Ensure that the bypass capacitor is placed as close as possible to the V_{REF} pin of the SN74GTL1655.

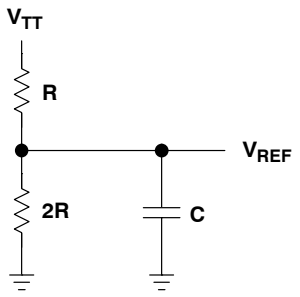

Figure 15. Suggested Connection of V_{REF} Pin

Static Characteristics of the SN74GTL1655

An understanding of the static characteristics of a component is necessary for a circuit development to be successful. The input and output characteristics of the SN74GTL1655 were, therefore, measured under laboratory conditions.

Input Characteristics

In principle, the input characteristics appear identical on both sides (A and B ports) of the device.

In Figure 16, the input protection diode is easily recognized; it is found both at the inputs of the LVTTL side (A port) and also at the inputs of the GTL/GTL+ side (B port) of the device. The diode circuit provides protection against high negative voltage spikes, which can occur as the result of electrostatic discharges or line reflections. In such cases, the diode conducts and prevents more sensitive components from being destroyed.

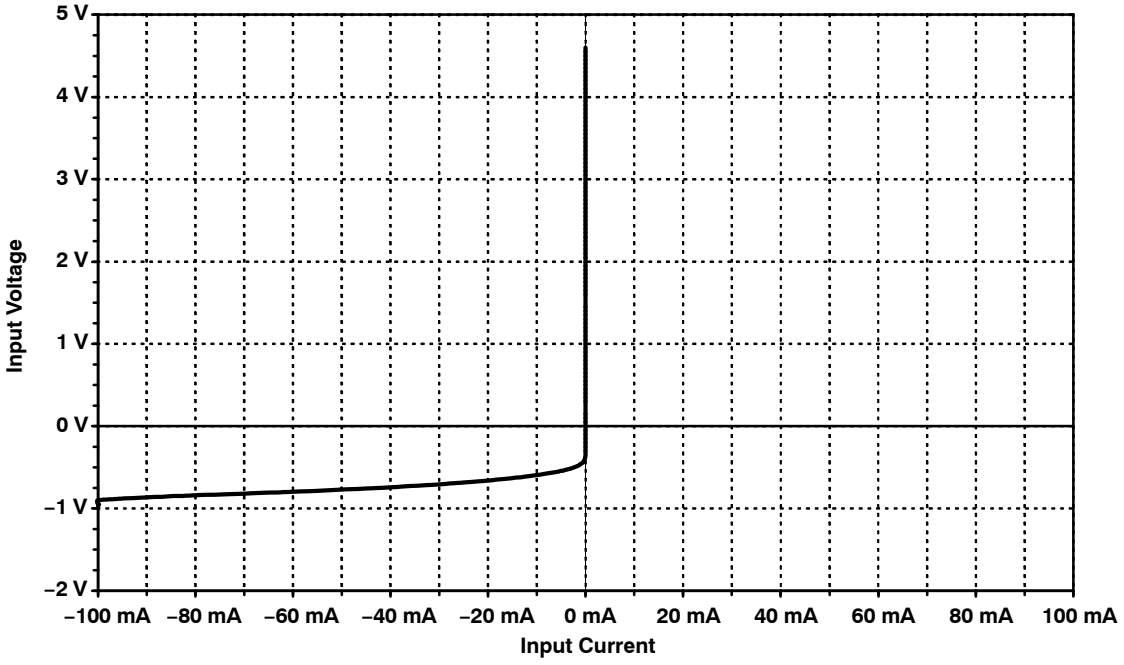

Figure 16. Input Characteristics of the SN74GTL1655

Bus-Hold Circuit

If the input characteristics of the LVTTL side (A port) are recorded in small increments, and over a narrow range of current, then the curve shown in Figure 17 results. This curve clearly demonstrates the effectiveness of the bus-hold circuit.

To change the logic state stored by the bus-hold circuit, a current of about 250 µA must be overridden.

This circuit is useful when, for example, all drivers on the bus are in a high-impedance state. Thus, an undefined state can be prevented.

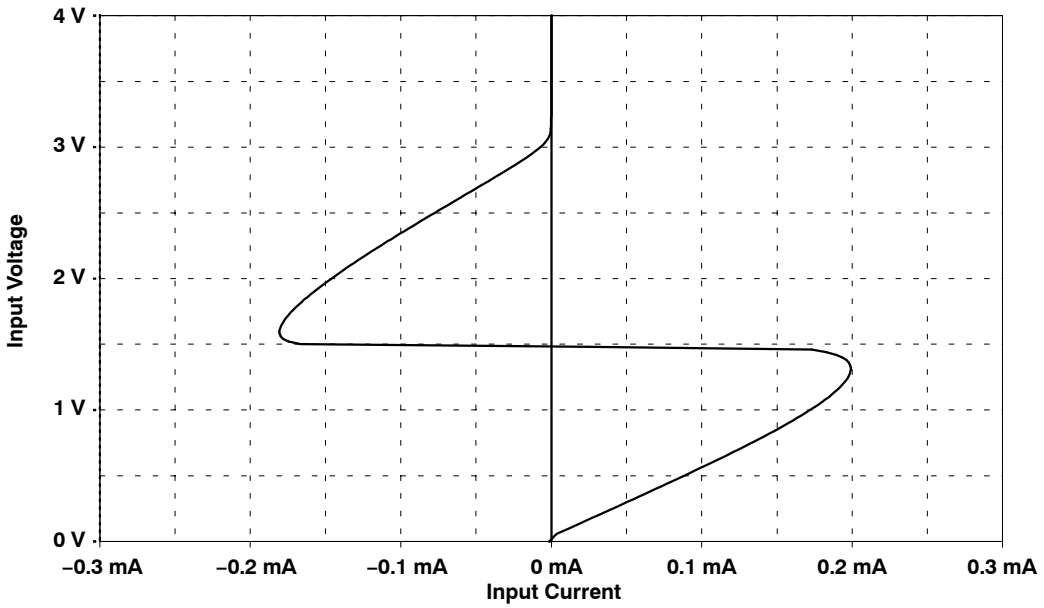

Figure 17. Bus-Hold Characteristics at the LVTTL Input of the SN74GTL1655

There is no bus-hold circuit on the GTL/GTL+ side (B port). A bus-hold circuit on the GTL/GTL+ side would defeat the principle of operation of the open-drain outputs, which take on the high-impedance state to allow the bus to achieve a logic high state (via the pullup resistors).

GTL/GTL+ Output Characteristics

Because the SN74GTL1655 has been conceived as an interface between LVTTL partial systems and a GTL/GTL+ backplane, the output characteristics of both sides are shown here. The characteristics for the various logic states of the output stage are shown in a single voltage-current diagram.

The principle of the GTL bus is based on open-drain drivers, as shown in Figure 18.

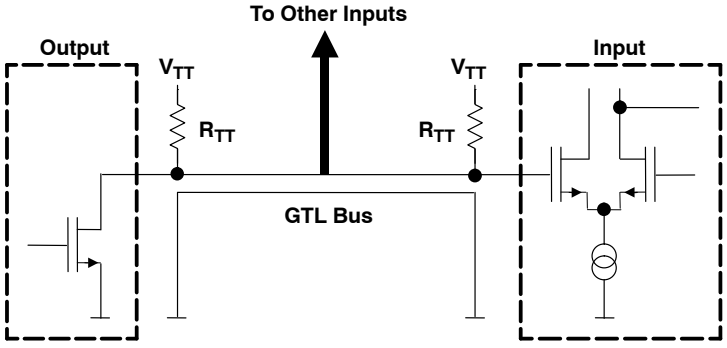

Figure 18. GTL/GTL+ Bus: An Open-Drain Bus

The device actively drives only the low state on the bus; whereas, for the high state, the required current flows directly from the termination voltage source, V_{TT}. The current is limited only by a pullup resistor (R_{TT}), which usually is of very low resistance. According to the specification, the pullup resistor must not be less than the minimum value of 25 Ω. A primary purpose of resistor R_{TT} is to provide an optimum termination of the bus to avoid line reflections (see *Transmission-Line Theory in Practice*).

Figure 19 shows that in the low state, the output resistance of the GTL/GTL+ output stage is in the range of a few ohms.

In the high state, the output transistor is blocking. The output is thus at a very high impedance as shown in Figure 19. Because of the bidirectionality of the SN74GTL1655, the input protection diode also can be seen at the output, if the output is at high impedance. The outputs and inputs of the device are connected together and routed to a single pin.

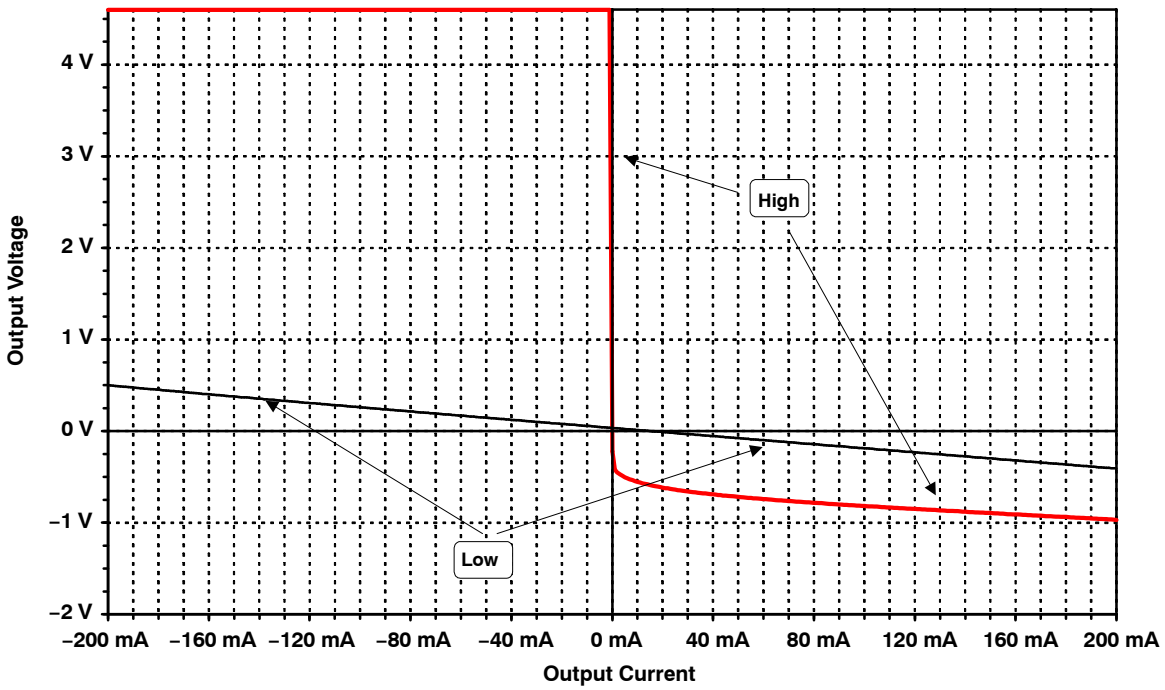

Figure 19. Output Characteristics of the GTL/GTL+ Side of the SN74GTL1655

LVTTL Output Characteristics

The output characteristics of the LVTTL output side of the SN74GTL1655 are shown in Figure 20, recorded with a supply voltage V_{CC} = 3.3 V. The output resistance for the low state is around 10 Ω, and in the case of the high state, a value of about 25 Ω is typical.

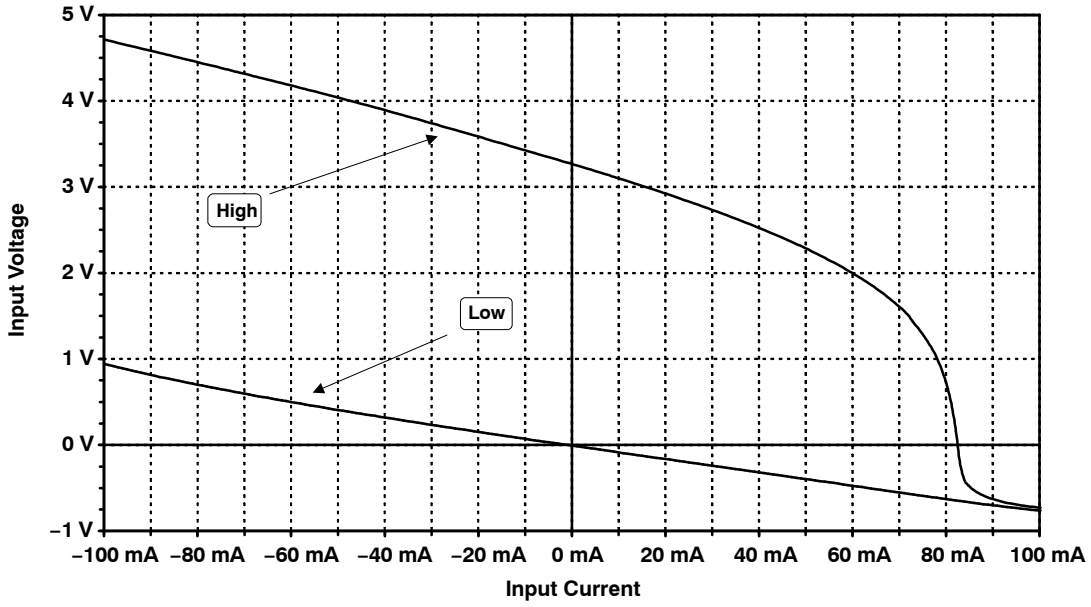

Figure 20. Output Characteristics of the LVTTL Side of the SN74GTL1655

Edge-Rate Control (ERC)

In the GTL/GTL+ output stage, a circuit is included that allows two different values of edge rate to be set. With the use of the edge-rate control input, V_{ERC}, different rise and fall times can be set, to allow the optimum configuration under various loading conditions of the backplane. If V_{ERC} is connected to the supply voltage (V_{CC}), the outputs are switched with longer rise and fall times than when it is connected to GND.

In two series of measurements, the voltage at the control input V_{ERC} was varied to determine the influence of the edge-rate control circuit on the behavior of the signal.

As shown in Figure 21, the measurements on the SN74GTL1655 were made with a single device under no-load conditions, using GTL+ voltage levels. During the measurement, only the 25-Ω pullup resistor was at the GTL+ output. There were LVTTL signals from a signal generator at the A port of the device, each having different rise and fall times: t_r, t_f = 2 ns and t_r, t_f = 10 ns.

Additional measurement results on the SN74GTL1655 test board are presented in a later section, which explains the behavior with a bus under realistic conditions.

The measurement results for falling edges are shown in Figures 22 and 23; Figures 24 and 25 show the curves for rising edges.

Using the definition of edge rate (slew rate) $dV/dt = (V_{OH} - V_{OL}) / t_r, t_f$, a slew rate results in the range of 0.6 V/ns to 0.7 V/ns. As a comparison, these values are significantly less than those of standard TTL devices, which are usually about 1 V/ns, or more.

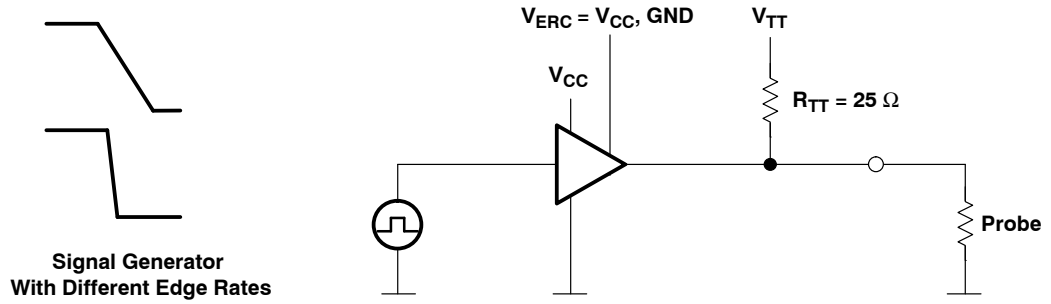

Figure 21. Setup for Measuring Edge Rate at the GTL/GTL+ Side of the SN74GTL1655

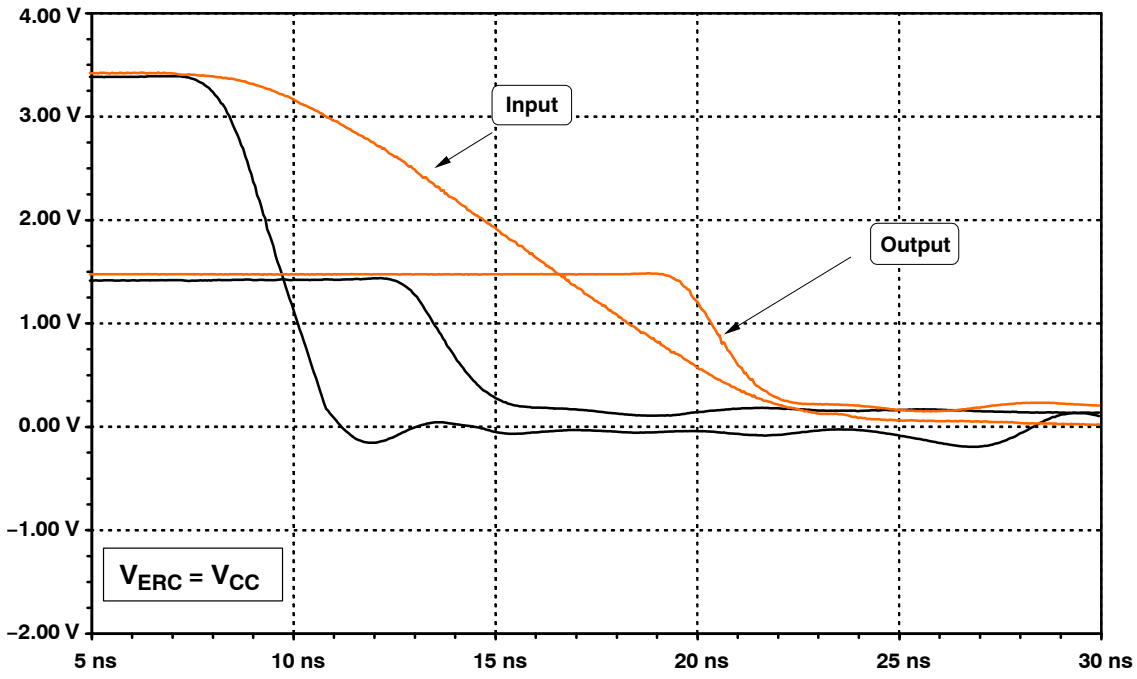

Figure 22. Falling Edge, $V_{ERC} = V_{CC}$ (Slow Edge Rate), Input Signals t_f = 2 ns, 10 ns

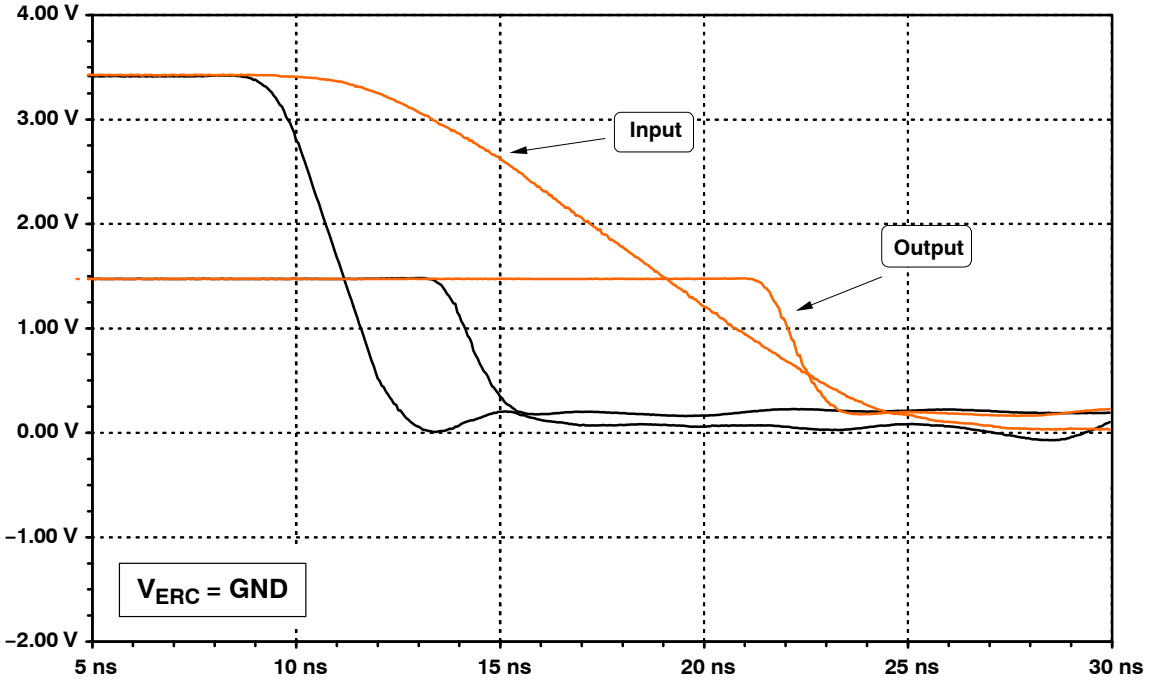

Figure 23. Falling Edge, V_{ERC} = GND (Fast Edge Rate), Input Signals t_f = 2 ns, 10 ns

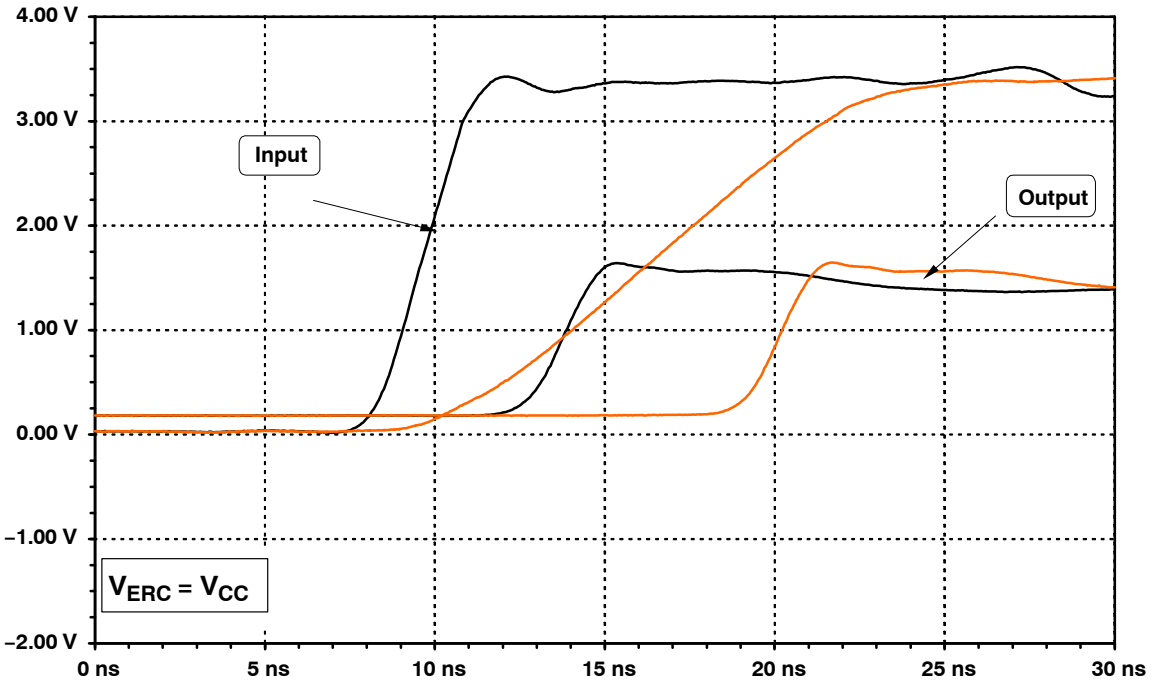

Figure 24. Rising Edge, $V_{ERC} = V_{CC}$ (Slow Edge Rate), Input Signals t_f = 2 ns, 10 ns

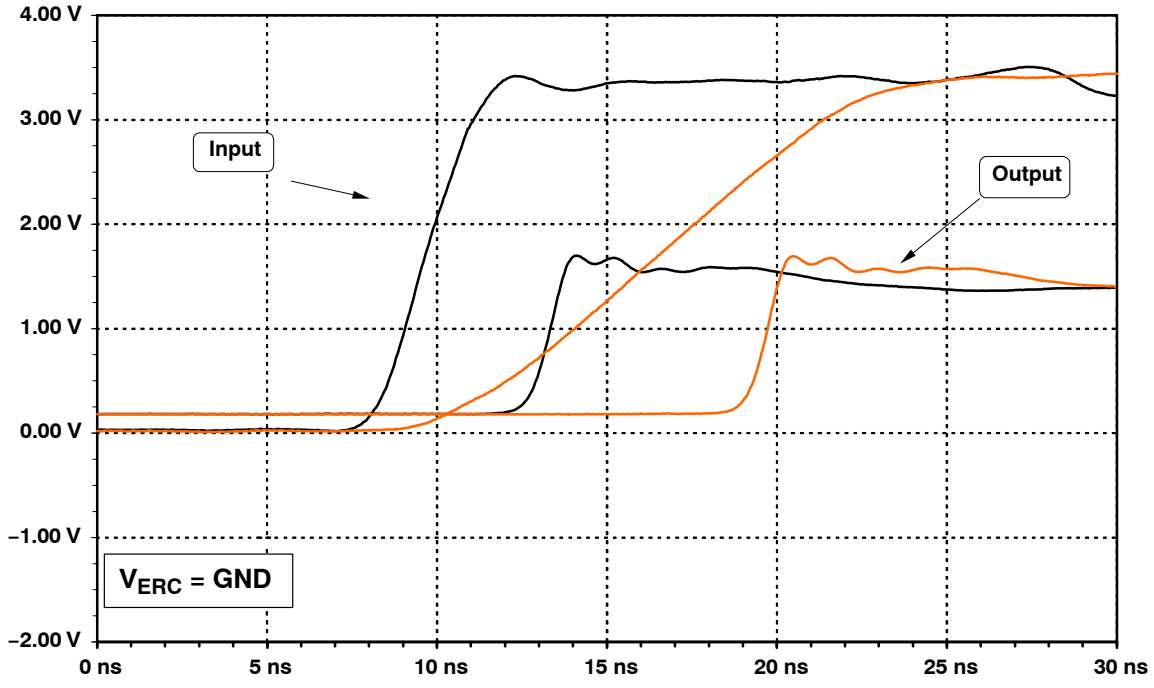

Figure 25. Rising Edge, V_{ERC} = GND (Fast Edge Rate), Input Signals t_f = 2 ns, 10 ns

Removal and Insertion Under Voltage and Partially Switched-Off Systems

If it is possible to remove and reinsert plug-in boards in a system, while it remains in operation (live insertion), special precautions must be taken with the signal lines.

- The outputs of the boards to be inserted or removed must be at a high impedance when the boards are inserted or removed.

- Before inserting a board, all pins must be charged to the threshold voltage (1.5 V with TTL compatible systems, or $V_{CC}/2$ with CMOS-compatible systems). Thus, destructive voltage spikes on the signal line, in excess of the threshold voltage range, which might otherwise corrupt the data on the bus, can be avoided.

This principle is shown in Figure 26. The data pins are charged to the switching threshold (V_{TH}). As a maximum, the switching threshold can be reached when inserting; however, it can no longer be exceeded as a result of a voltage spike.

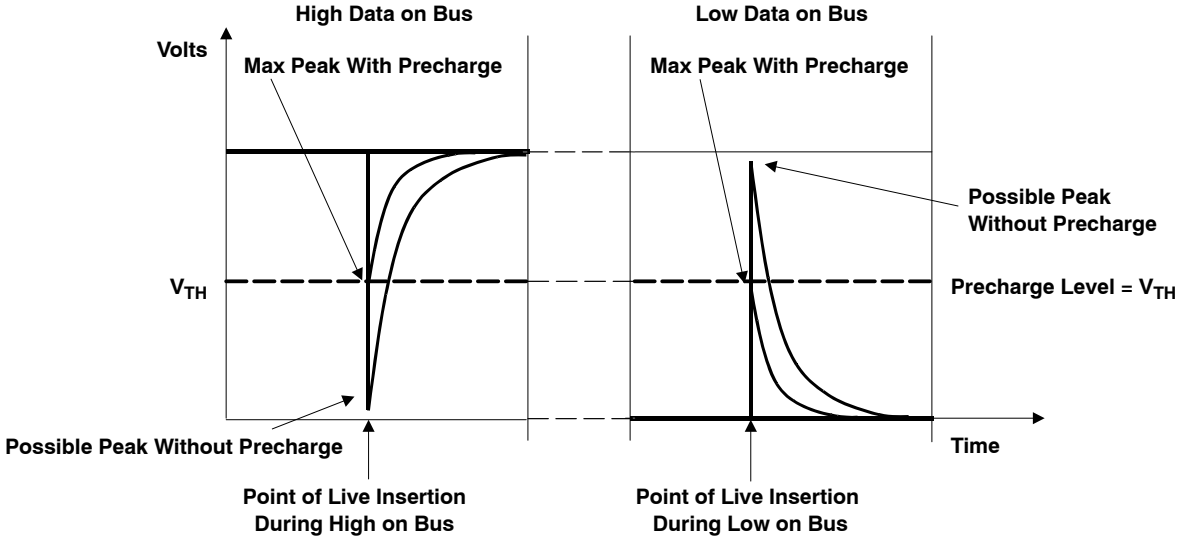

Figure 26. Influence of the Precharge Function on the Bus Signal

The SN74GTL1655 has the characteristics discussed above, which are necessary for the successful development of a live-insertion application.

Using the OE control input, it is possible to set the outputs of the SN74GTL1655 on both sides simultaneously to a high-resistance state. As a result of the integrated power-up 3-state circuit, the device is definitely inactive at a V_{CC} of less than 1.5 V.

To ensure that there is also a definite high-resistance state at a supply voltage between 1.5 V and the operating voltage, it is recommended that OE be connected to V_{CC} via a pull-up resistor.

High-impedance outputs can be precharged to a definite voltage level by means of the bias input (BIAS V_{CC}). Disturbances to the active bus arising from insertion (charging / discharging of the input / output capacitance) will thus be kept to a minimum.

In a similar fashion, in modern applications, particular parts of a system are switched off from the source of power without having first removed them from the complete system. This is a partial switching off of the system, or a partial power down.

If a device is used in a partial power-down application, the inputs and outputs for V_{CC} = 0 V must be at high impedance, and thus be able to tolerate active bus signals.

The property of being partial-power-down compatible is reflected in the parameter I_{OFF}, which specifies the maximum leakage current in an input or output.

I_{OFF} is defined as:

- The device is disconnected from the operating voltage (V_{CC} = 0 V), and
- A logic level is applied to the input or output.

With the SN74GTL1655, the maximum value of I_{OFF} is 100 μA.

Refer to the TI application report *Live Insertion,* literature number SDYA012, which discusses this subject in detail.

Measurements on the GTL1655 Test Board

A GTL1655 test board has been constructed to examine the characteristics of the SN74GTL1655 in a practical application. The principle of this board is shown in Figure 27.

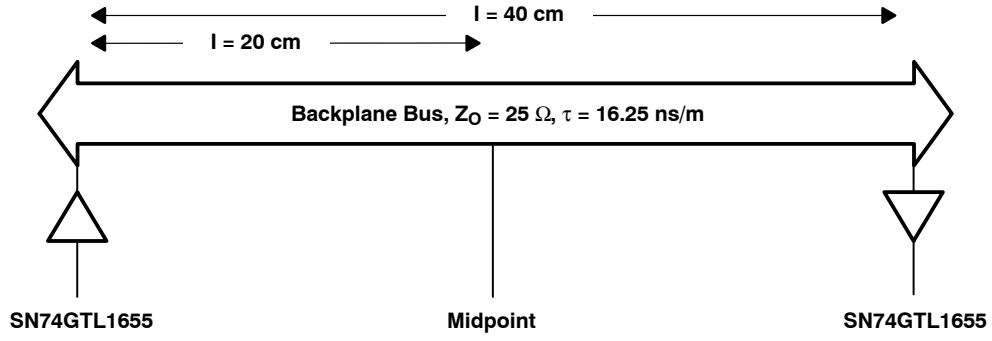

Figure 27. Principle of Construction of the GTL/GTL+ Bus on the GTL1655 Test Board

This bus consists of a straight connecting line, 40 cm long, between two SN74GTL1655 devices.

In practice, a backplane wiring system provides the option for multiple plug-in modules. The bus impedance is reduced as a result of the additional input capacitances of the modules that are connected to it (see Figure 2). This effect can be approximated by connecting capacitors between the bus line and ground at intervals of 2 cm.

Both sides of the bus are provided with termination resistors, which are connected to V_{TT}. The termination voltage is set at 1.5 V. A 1-V reference voltage (V_{REF}) was chosen. In this way, GTL+ signals are transmitted on the bus.

The termination resistors for this setup were chosen to match the line impedance, which, for a fully loaded backplane, results in Z_O = 25 Ω. This case provides optimum line termination, with a reflection factor very close to ρ = 0.

For the measurements, the slew rate of the GTL output stage was varied by means of the edge-rate control input V_{ERC}. The measurements were carried out under two different bus conditions: a fully loaded bus (with distributed capacitors) and the bus unloaded (without capacitors). The clock frequencies used were 10 MHz, 50 MHz, and 160 MHz, the last being the maximum value specified in the data sheet.

For the case of a fully loaded bus, the result is a line impedance of about 25 Ω, and a delay time on the line of about 7 ns.

With the bus unloaded, i.e., operated without capacitors connected to it, the line impedance is about 30 Ω, and the delay time on the line reaches a value below 3 ns.

The measurement results presented in Figures 28 through 51 show:

- The LVTTL input signal of the SN74GTL1655 that drives the bus line, together with the LVTTL output signal of the SN74GTL1655 receiver that is situated at the end of the GTL bus. For this, the load of the receiver was varied. The diagrams show the curves for $R_L = \infty$ (unloaded output) and for $R_L = 50\ \Omega$.
- Waveforms on the GTL bus line:
  - The GTL output signal of the SN74GTL1655 that drives the bus line, i.e., the signal at the beginning of the line
  - The bus signal in the middle of the GTL bus
  - The signal at the end of the GTL bus line, which also is applied to the input of the SN74GTL1655 receiver device.

All curves are shown together for the frequencies 10 MHz, 50 MHz, and 160 MHz, and for the two different edge-rate settings (with $V_{ERC} = V_{CC}$ and $V_{ERC} = GND$).

For these measurements, care was taken to ensure that the timing relationships between them remained constant. A summary of the measurement results is given in Table 7.

Table 7. Measurement Results on the GTL1655 Test Board

	SIGNAL	BUS LINE UNLOADED (WITHOUT CAPACITORS)		BUS LINE LOADED (WITH CAPACITORS)	
		SLOW EDGE RATE $V_{ERC} = V_{CC}$	FAST EDGE RATE $V_{ERC} = GND$	SLOW EDGE RATE $V_{ERC} = V_{CC}$	FAST EDGE RATE $V_{ERC} = GND$
f = 10 MHz	Input/output LVTTL level	Figure 28	Figure 30	Figure 40	Figure 42
	Beginning, middle, end of GTL Bus	Figure 29	Figure 31	Figure 41	Figure 43
f = 50 MHz	Input/output LVTTL level	Figure 32	Figure 34	Figure 44	Figure 46
	Beginning, middle, end of GTL Bus	Figure 33	Figure 35	Figure 45	Figure 47
f =160 MHz	Input/output LVTTL level	Figure 36	Figure 38	Figure 48	Figure 50
	Beginning, middle, end of GTL Bus	Figure 37	Figure 39	Figure 49	Figure 51

Measurement Results With an Unloaded Backplane (Z_O = 30 Ω, R_T = 25 Ω)

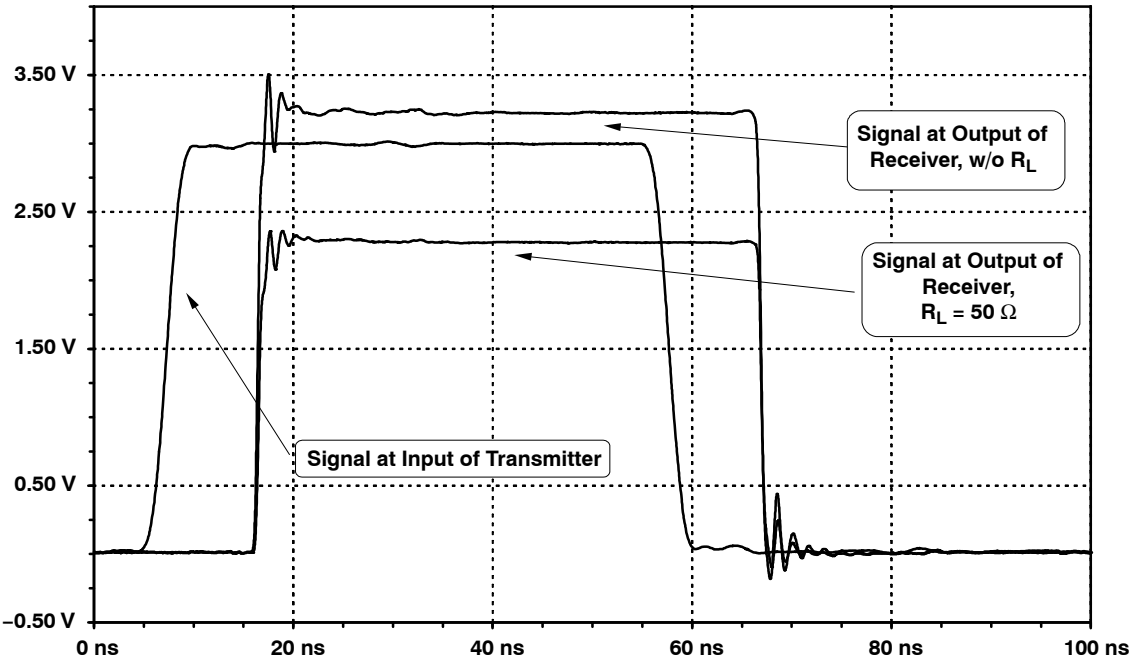

Figure 28. LVTTL Input and Output Signal, Unloaded-Bus Case, f = 10 MHz, V_{ERC} = V_{CC} (Slow Edge Rate)

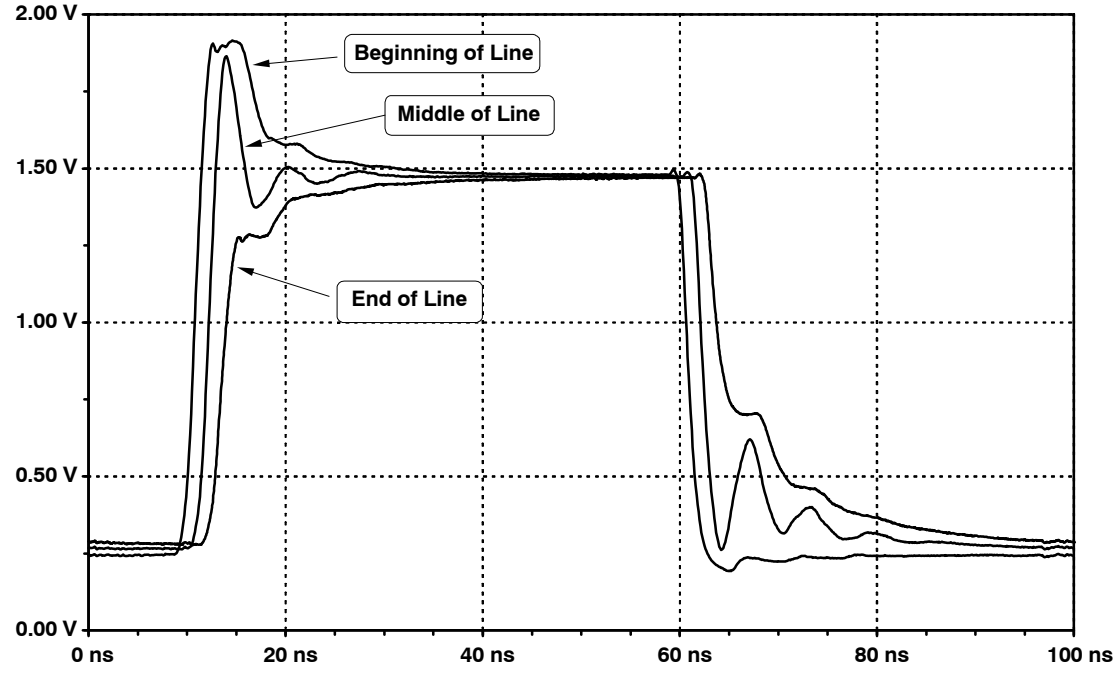

Figure 29. Waveform of GTL Bus Signal, Unloaded-Bus Case, f = 10 MHz, V_{ERC} = V_{CC} (Slow Edge Rate)

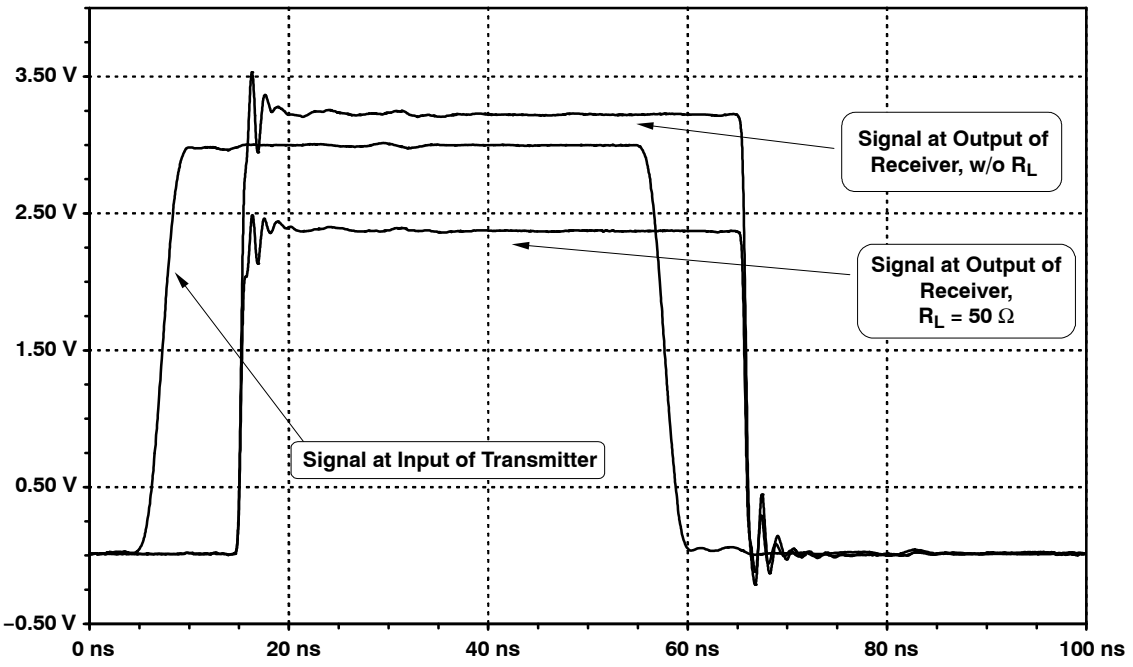

Figure 30. LVTTL Input and Output Signal, Unloaded-Bus Case, f = 10 MHz, V_{ERC} = GND (Fast Edge Rate)

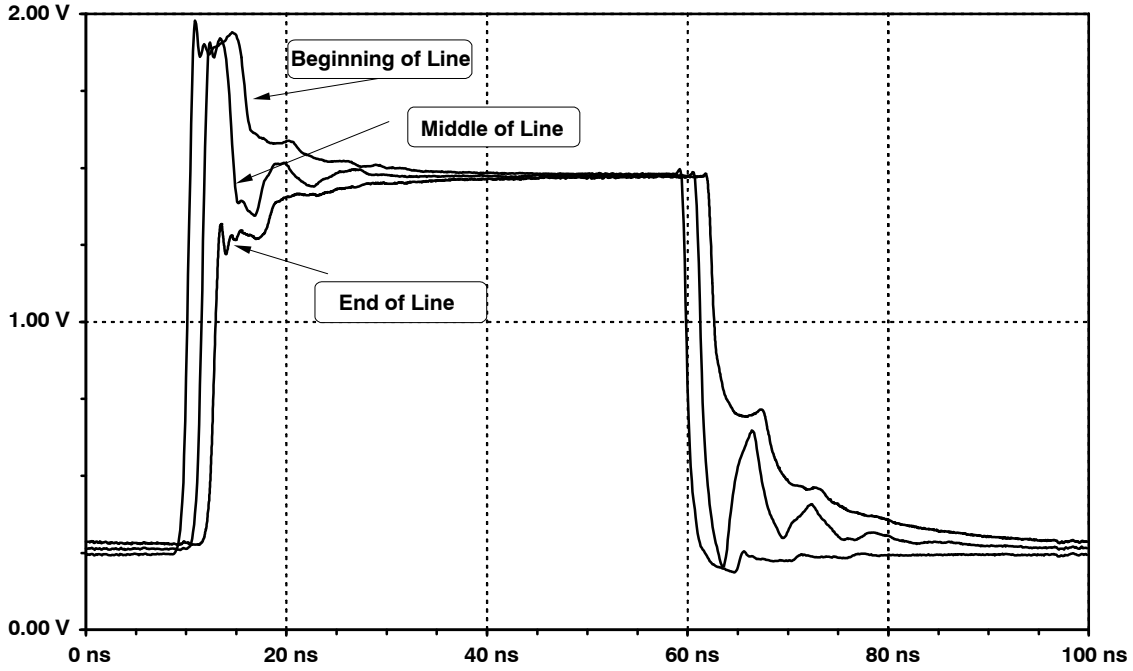

Figure 31. Waveform of GTL Bus Signal, Unloaded-Bus Case, f = 10 MHz, V_{ERC} = GND (Fast Edge Rate)

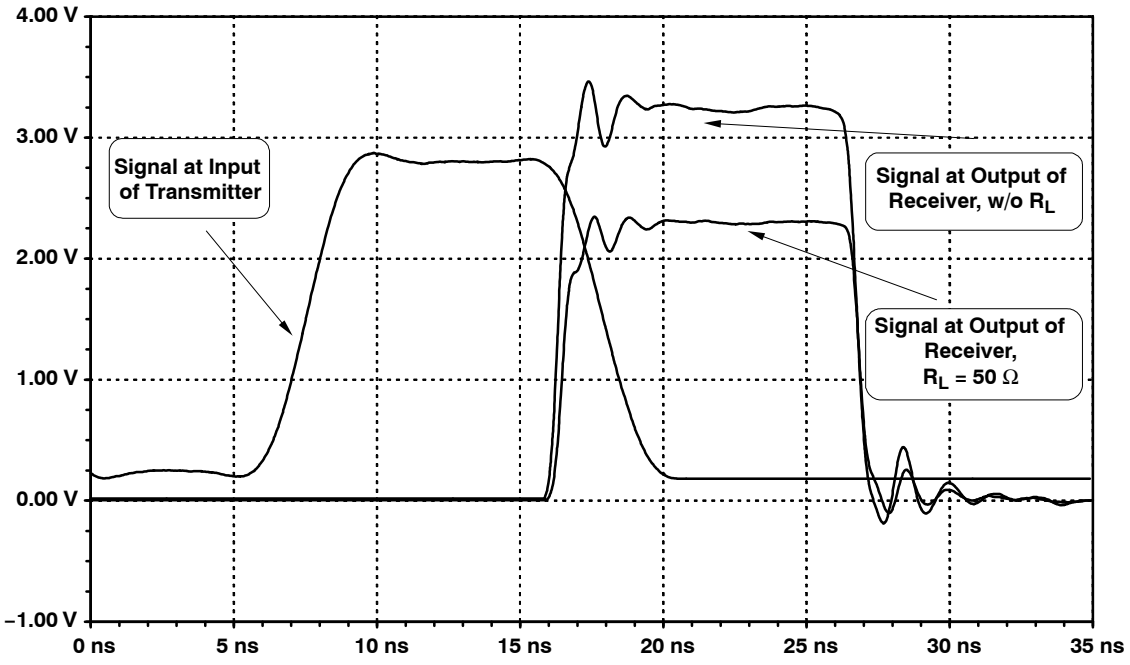

Figure 32. LVTTL Input and Output Signal, Unloaded-Bus Case, f = 50 MHz, $V_{ERC} = V_{CC}$ (Slow Edge Rate)

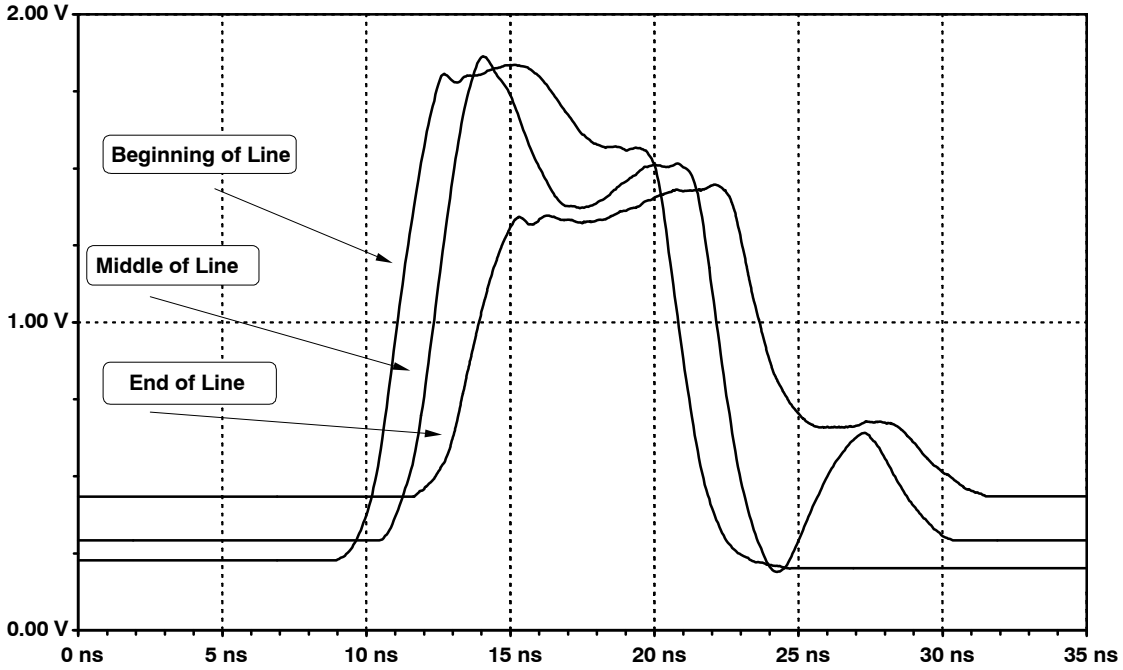

Figure 33. Waveform of GTL Bus Signal, Unloaded-Bus Case, f = 50 MHz, $V_{ERC} = V_{CC}$ (Slow Edge Rate)

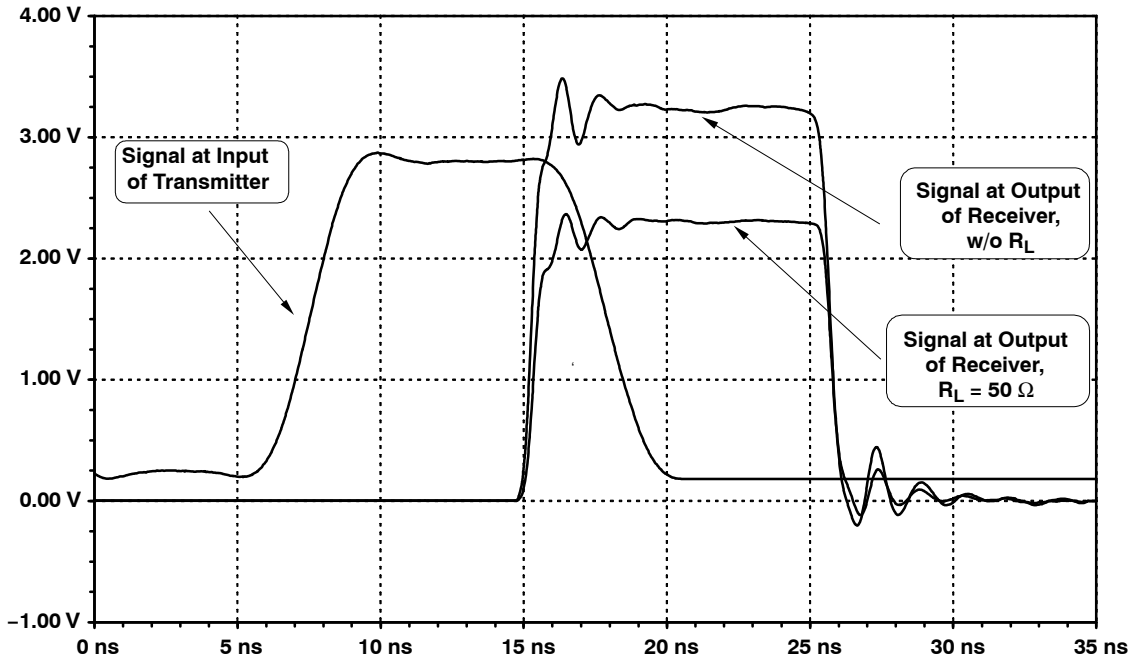

Figure 34. LVTTL Input and Output Signal, Unloaded-Bus Case, f = 50 MHz, V_{ERC} = GND (Fast Edge Rate)

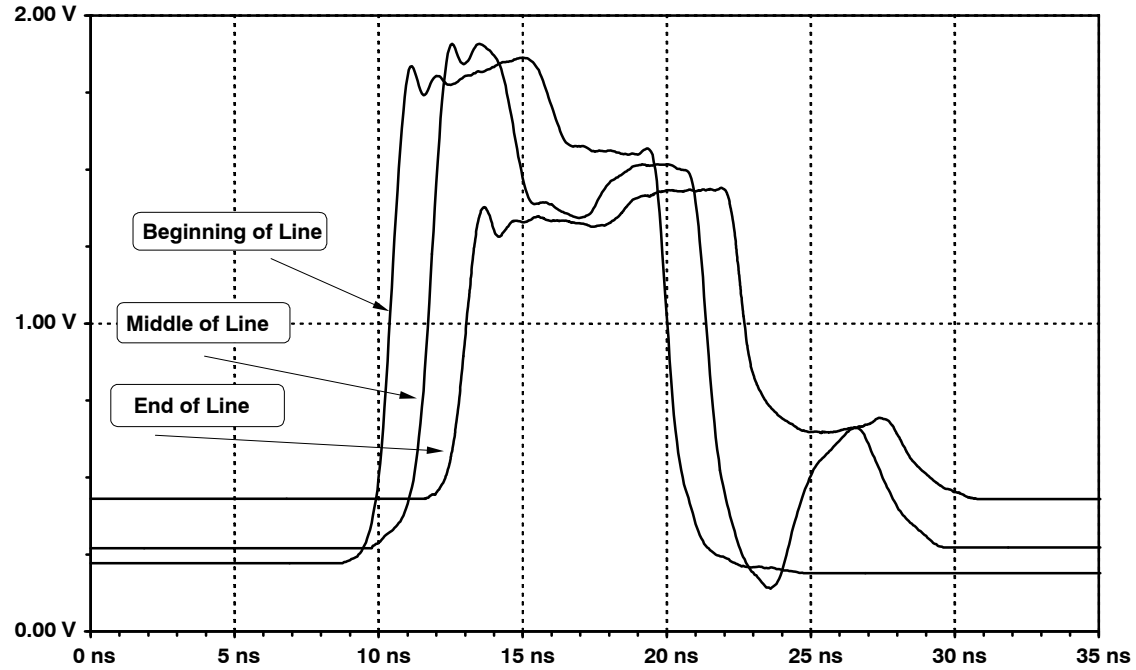

Figure 35. Waveform of GTL Bus Signal, Unloaded-Bus Case, f = 50 MHz, V_{ERC} = GND (Fast Edge Rate)

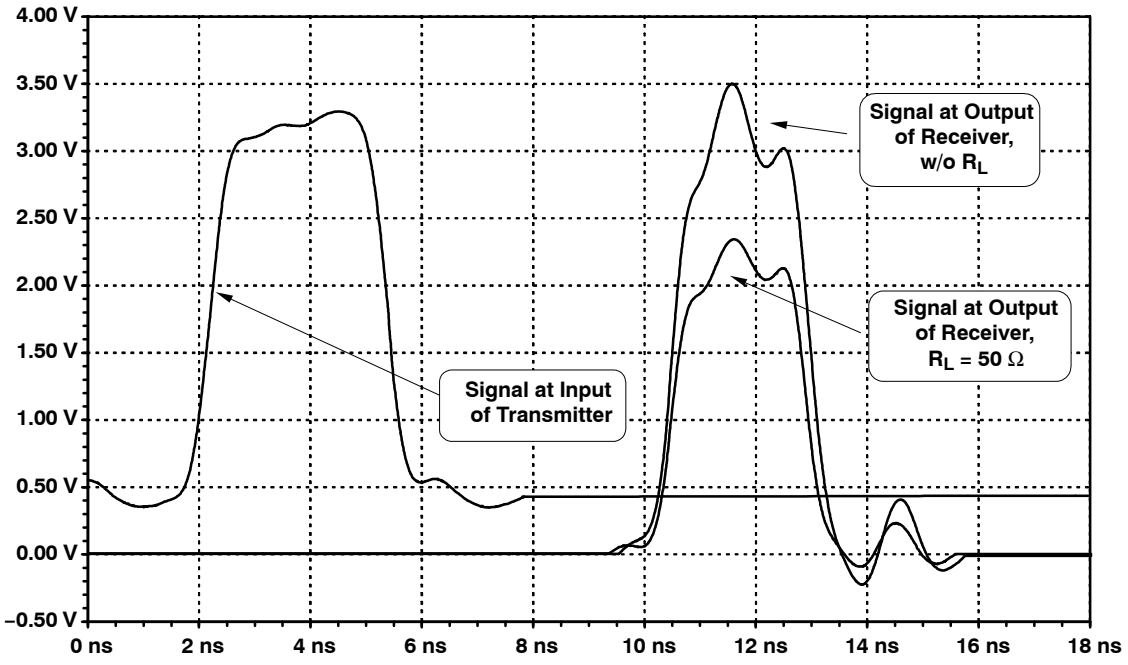

Figure 36. LVTTL Input and Output Signal, Unloaded-Bus Case, f = 160 MHz, $V_{ERC} = V_{CC}$ (Slow Edge Rate)

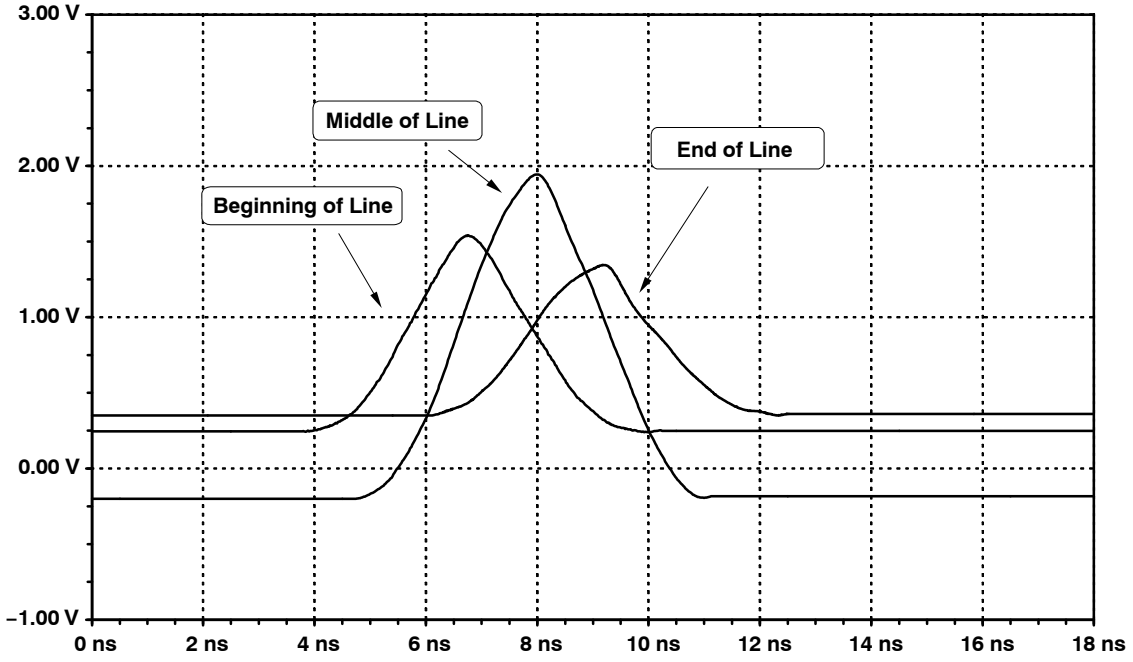

Figure 37. Waveform of GTL Bus Signal, Unloaded-Bus Case, f = 160 MHz, $V_{ERC} = V_{CC}$ (Slow Edge Rate)

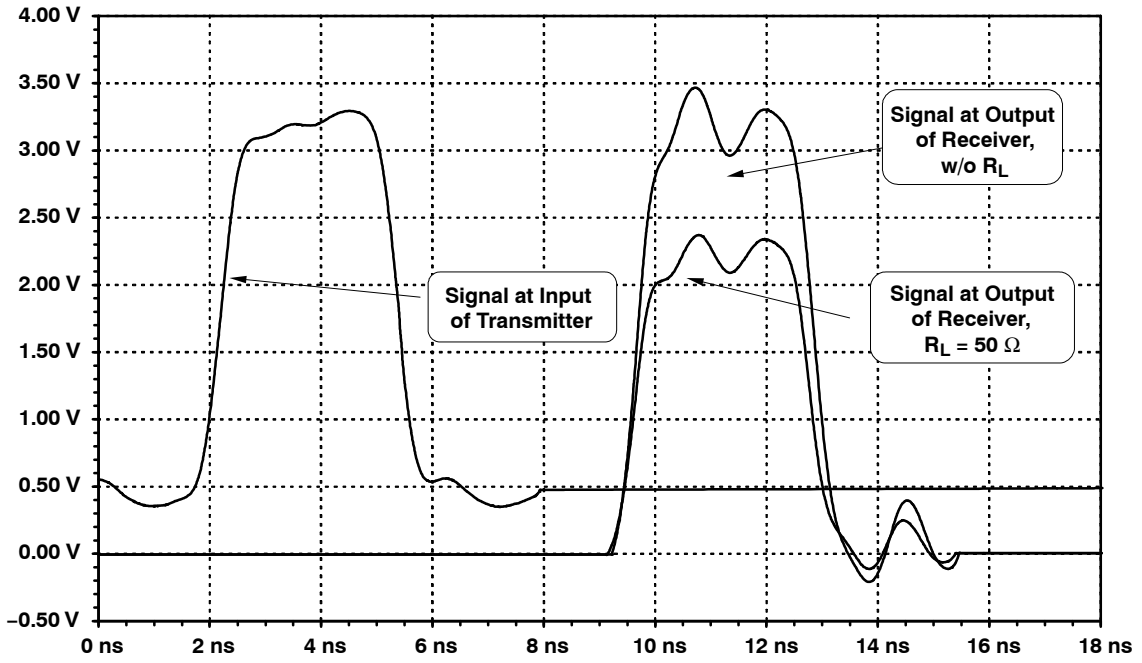

Figure 38. LVTTL Input and Output Signal, Unloaded-Bus Case, f = 160 MHz, V_{ERC} = GND (Fast Edge Rate)

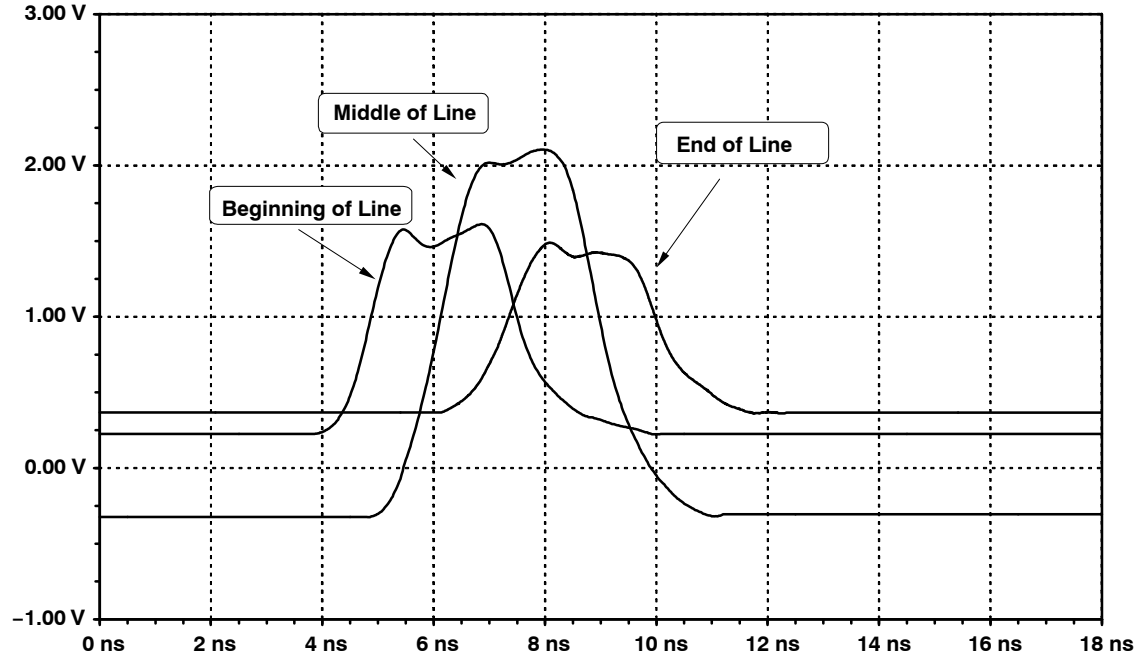

Figure 39. Waveform of GTL Bus Signal, Unloaded-Bus Case, f = 160 MHz, V_{ERC} = GND (Fast Edge Rate)

Measurement Results With a Loaded Backplane (Z_O = 25 Ω, R_T = 25 Ω)

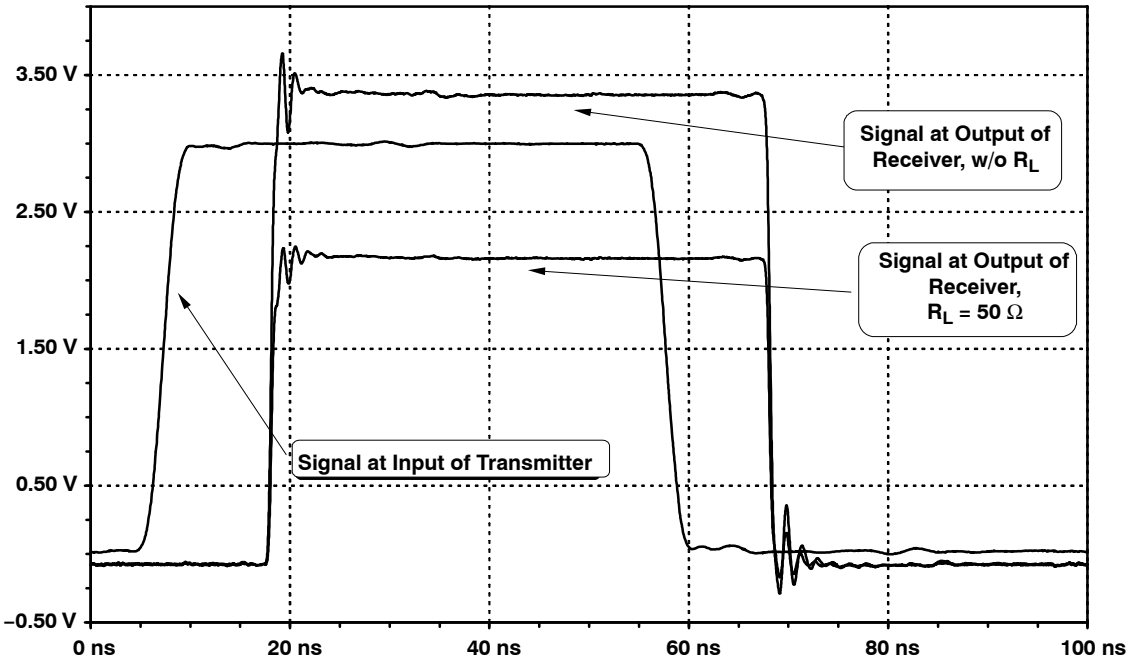

Figure 40. LVTTL Input and Output Signal, Loaded-Bus Case, f = 10 MHz, V_{ERC} = V_{CC} (Slow Edge Rate)

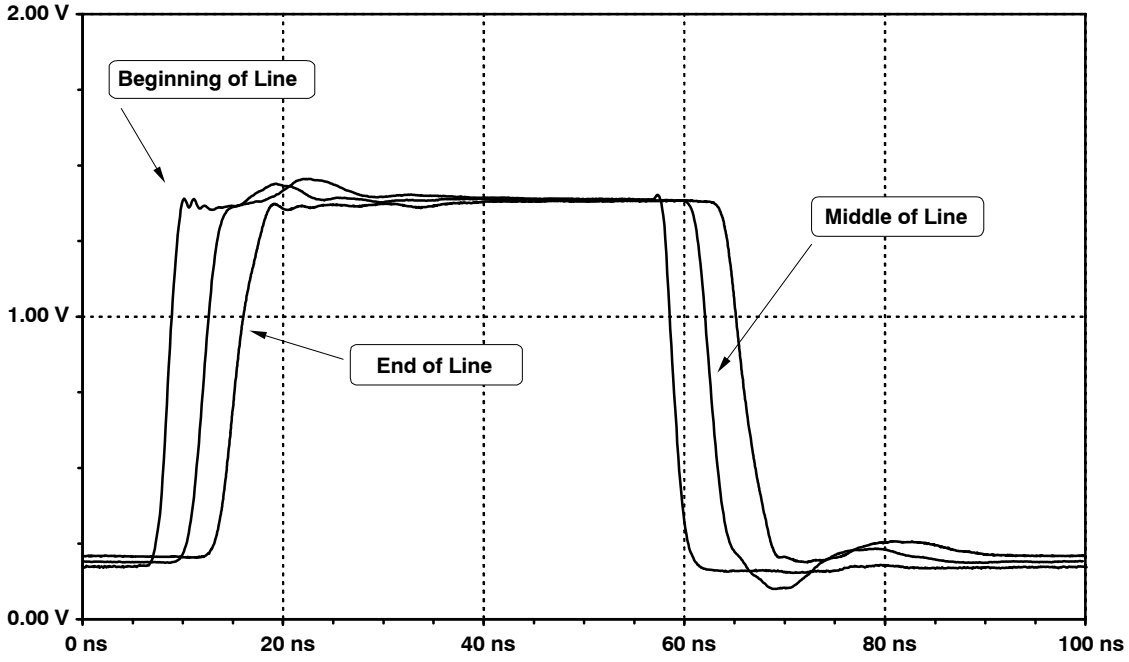

Figure 41. Waveform of GTL Bus Signal, Loaded-Bus Case, f = 10 MHz, V_{ERC} = V_{CC} (Slow Edge Rate)

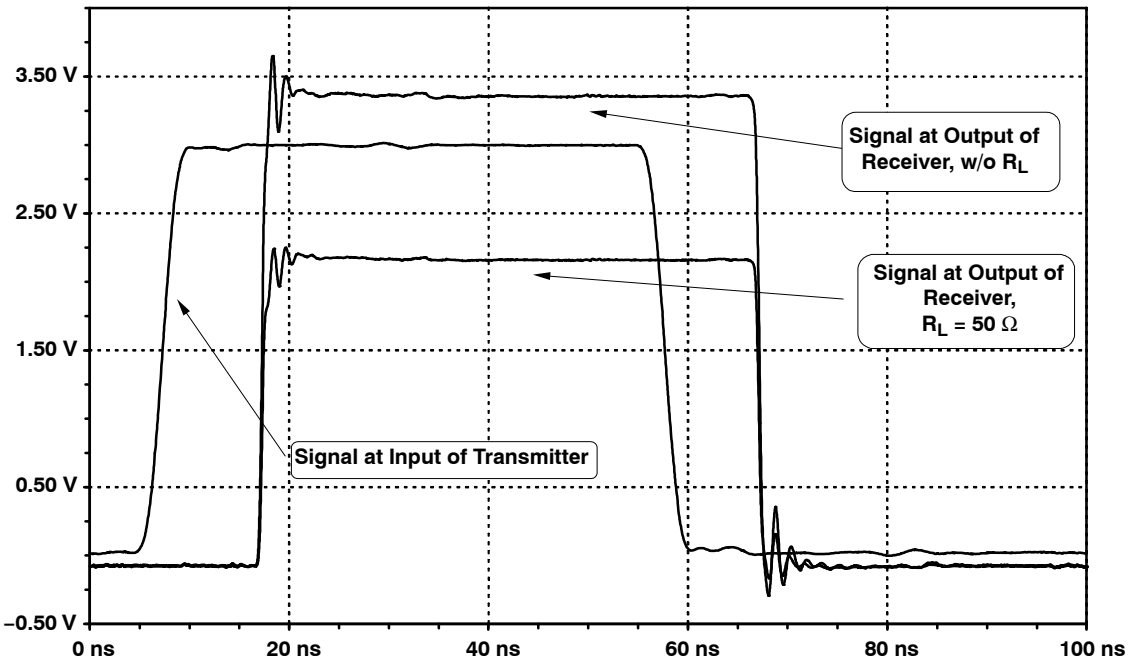

Figure 42. LVTTL Input and Output Signal, Loaded-Bus Case, f = 10 MHz, V_{ERC} = GND (Fast Edge Rate)

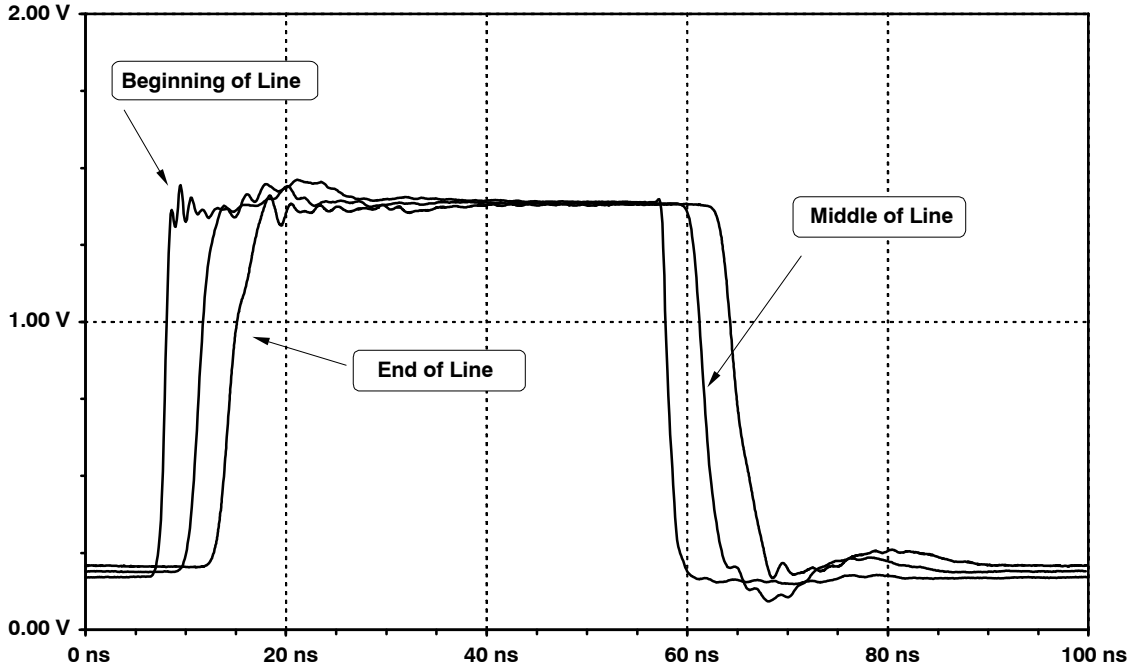

Figure 43. Waveform of GTL Bus Signal, Loaded-Bus Case, f = 10 MHz, V_{ERC} = GND (Fast Edge Rate)

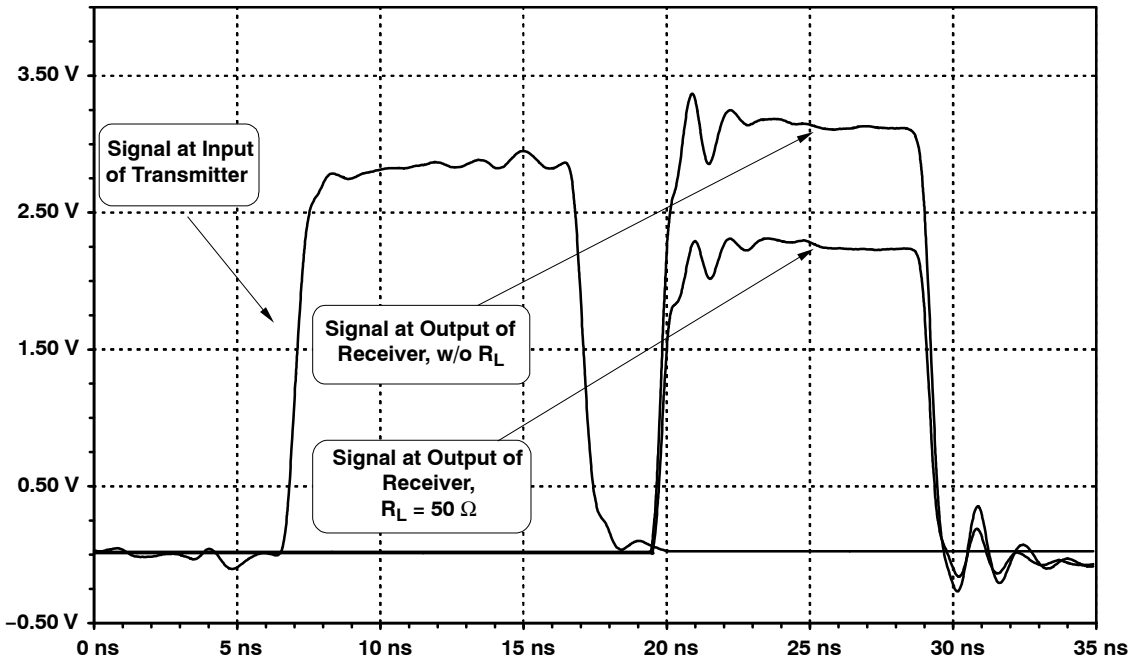

Figure 44. LVTTL Input and Output Signal, Loaded-Bus Case, f = 50 MHz, V_{ERC} = V_{CC} (Slow Edge Rate)

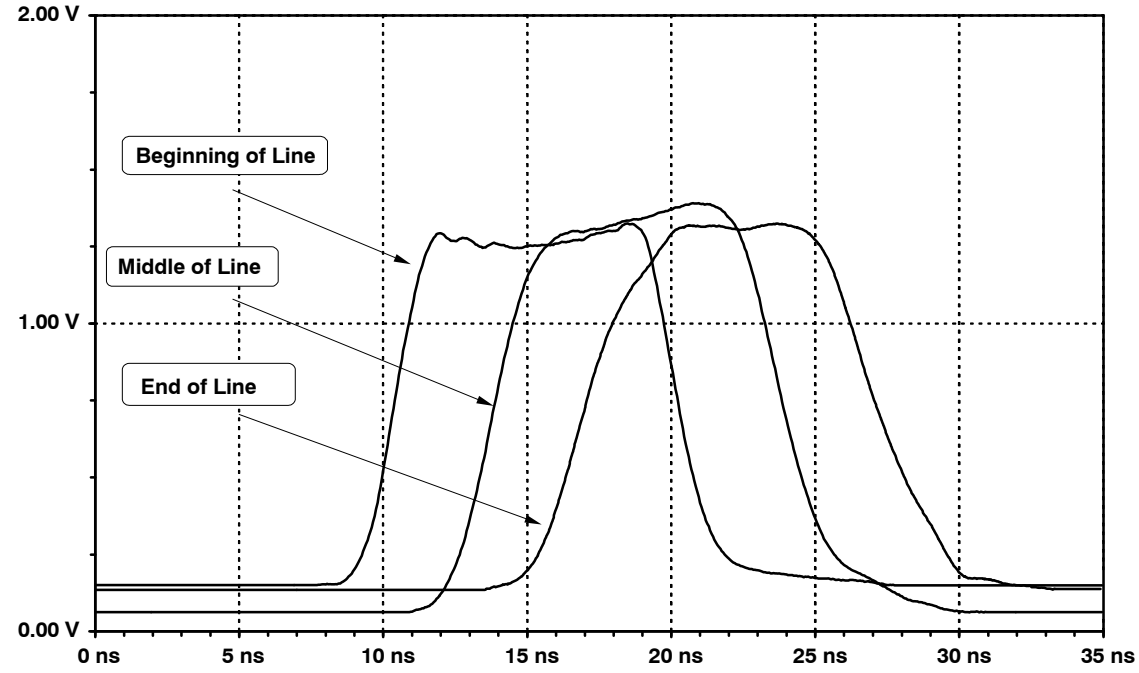

Figure 45. Waveform of GTL Bus Signal, Loaded-Bus Case, f = 50 MHz, V_{ERC} = V_{CC} (Slow Edge Rate)

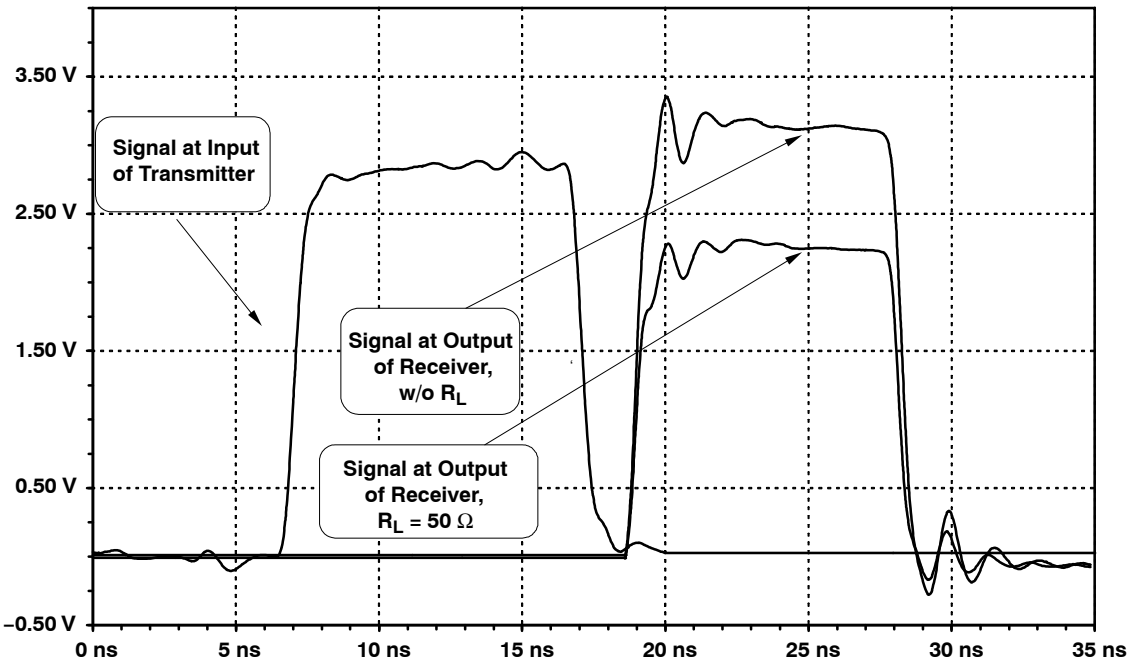

Figure 46. LVTTL Input and Output Signal, Loaded-Bus Case, f = 50 MHz, V_{ERC} = GND (Fast Edge Rate)

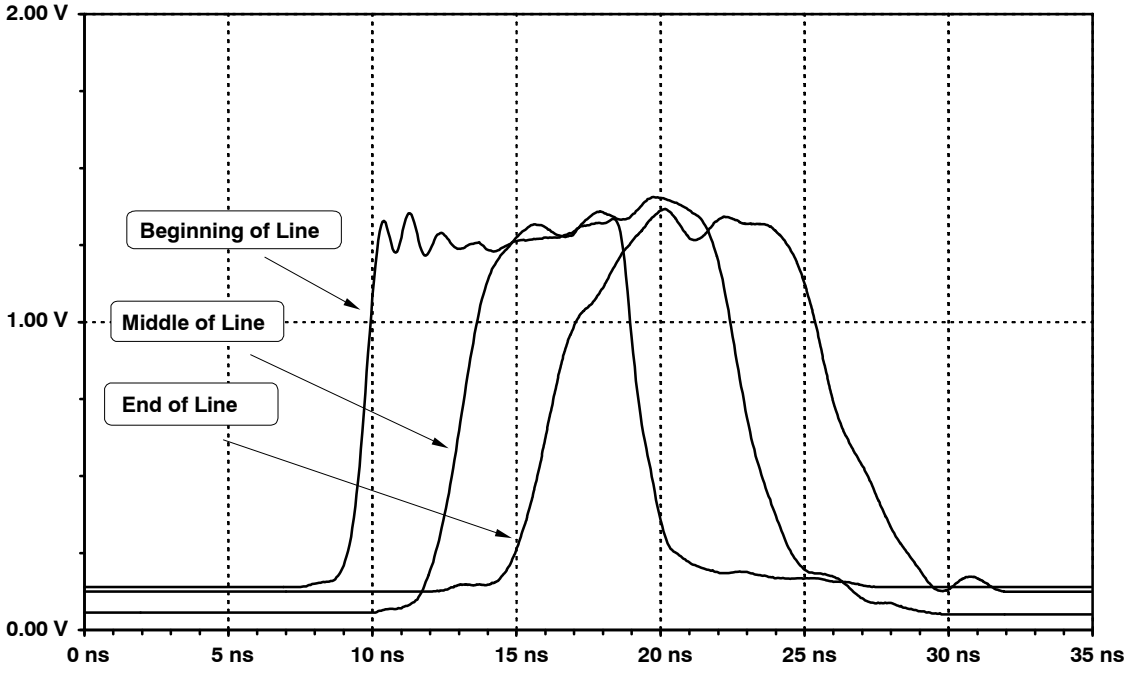

Figure 47. Waveform of GTL Bus Signal, Loaded-Bus Case, f = 50 MHz, V_{ERC} = GND (Fast Edge Rate)

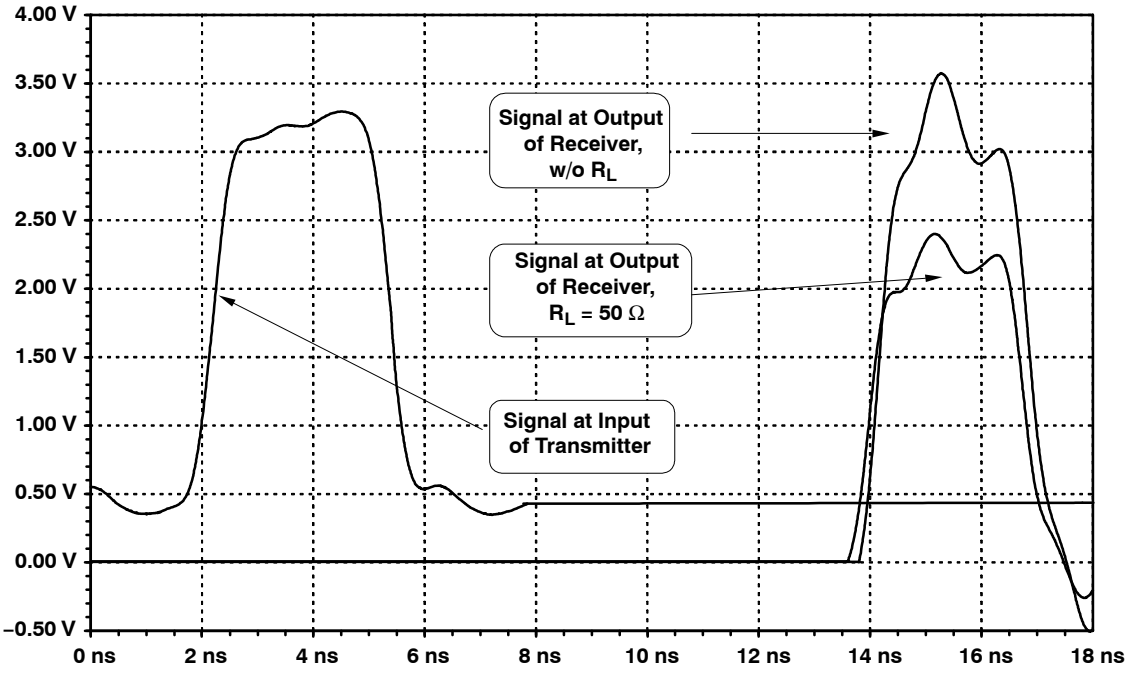

Figure 48. LVTTL Input and Output Signal, Loaded-Bus Case, f = 160 MHz, $V_{ERC} = V_{CC}$ (Slow Edge Rate)

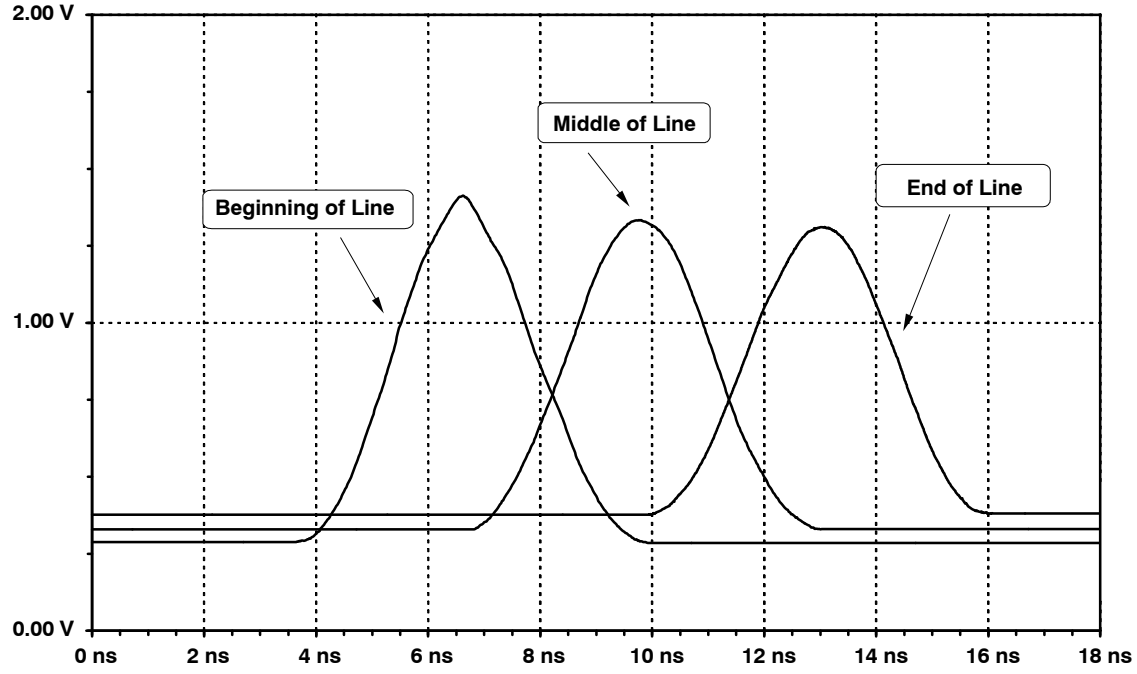

Figure 49. Waveform of GTL Bus Signal, Loaded-Bus Case, f = 160 MHz, $V_{ERC} = V_{CC}$ (Slow Edge Rate)

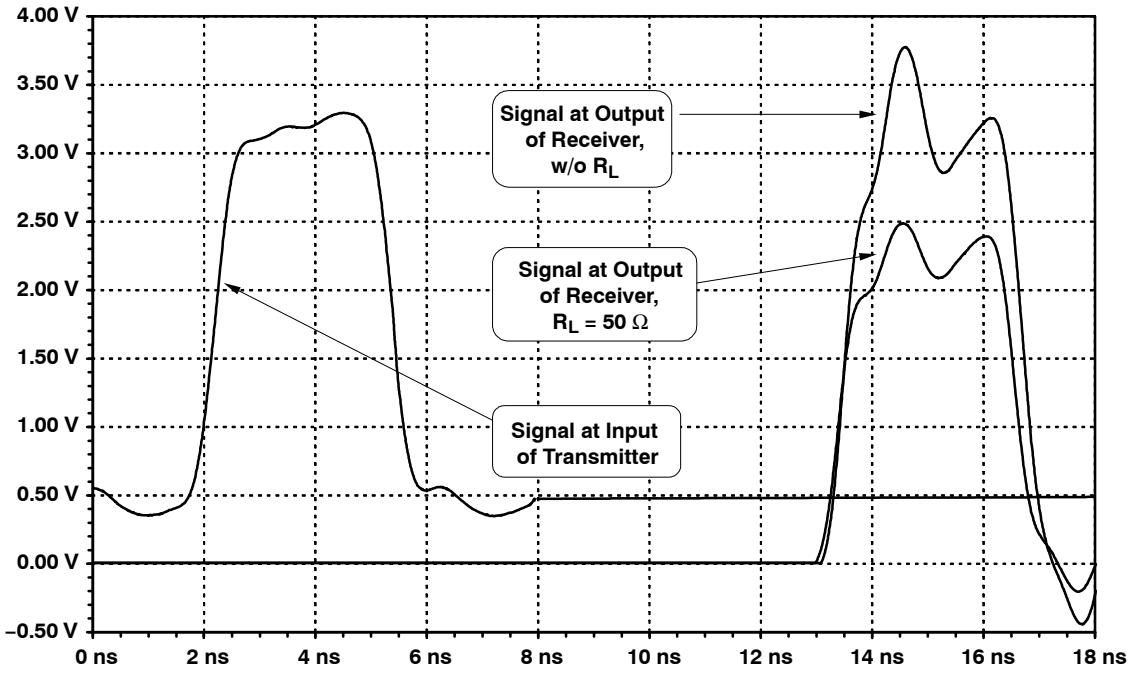

Figure 50. LVTTL Input and Output Signal, Loaded-Bus Case, f = 160 MHz, V_{ERC} = GND (Fast Edge Rate)

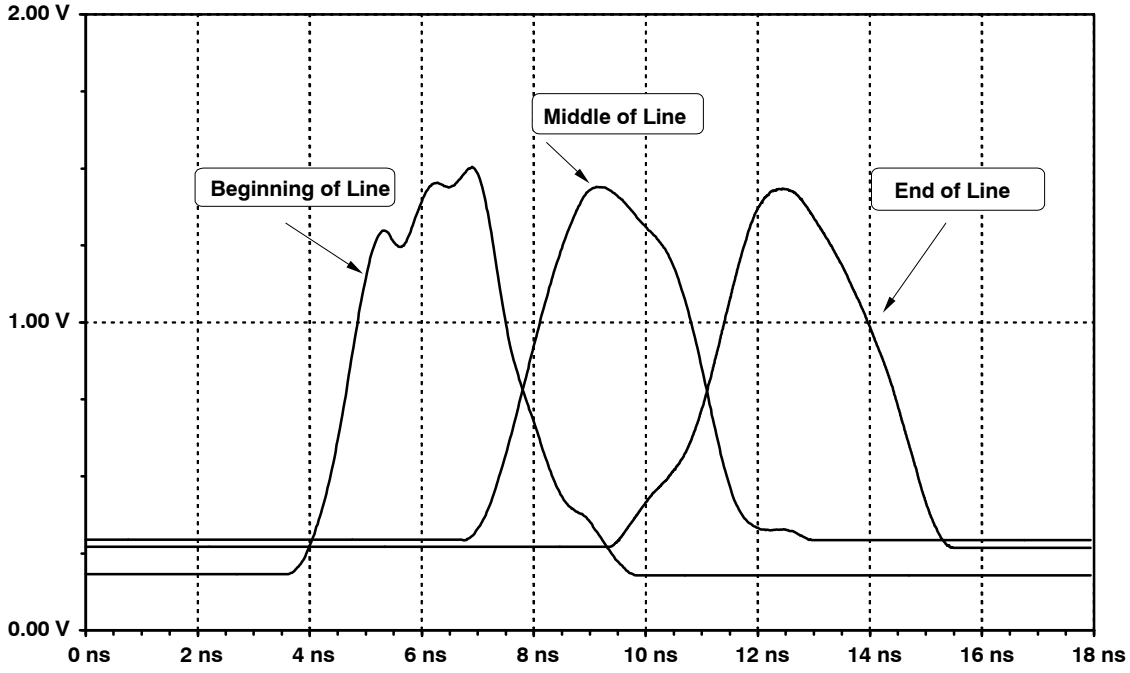

Figure 51. Waveform of GTL Bus Signal, Loaded-Bus Case, f = 160 MHz, V_{ERC} = GND (Fast Edge Rate)

Summary

The SN74GTL1655 from TI provides engineers developing fast and complex bus systems with a high-performance bus driver that is particularly suitable for the design of modern low-voltage systems.

Very high signal-propagation speeds are possible, as a result of the increased drive capability of 100 mA, compared with standard GTL circuits (40 mA), and the programmable edge rate. Bus lines with low line impedances of about 25 Ω can be used with the SN74GTL1655.

This device allows optimum termination of low-impedance bus lines, and thus prevents the interference and signal distortion that otherwise can occur as a result of line reflections. Because of the reduced signal-voltage amplitude, improved signal integrity is achieved.

The power-up 3-state and precharge functions provided by the SN74GTL1655, and also the bus-hold cells at the input of the LVTTL side, allow the design of modern high-speed systems requiring minimum development effort.

Acknowledgment

The authors of this application report are Peter Forstner and Johannes Huchzermeier.

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Glossary

BTL	Backplane Transceiver Logic
GND	Ground potential
GTL	Gunning Transceiver Logic
I/O	Input/Output
Live insertion	Removal and reinsertion of modules during operation
LVTTL levels	3.3-V logic levels, compatible with TTL logic levels
Partial power down	Switching off parts of a system that is in operation without removing them from a system
Precharge	Charging I/O pins to the threshold voltage
TTL	Transistor-Transistor Logic
V_{CC}	Supply voltage

High-Performance Backplane Design With GTL+

SCEA011
June 1999

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Abstract

Results from a system that demonstrates the performance of GTL+ devices in a backplane are provided. The Texas Instruments (TI™) GTL16622A is the example used in the design of the physical backplane. The TI backplane demonstration system is a useful tool for designers in understanding issues related to loading effects, termination, signal integrity, and data-transfer rate in a high-performance backplane environment. Simulation results are compared to laboratory measurements to validate the performance of TI GTL+ devices, and simulation results for the new TI GTL16612A in a very high-performance backplane are provided.

Introduction

High-performance backplane is becoming common terminology in the rapidly evolving data-communications market. Designers are developing innovative methods for multiplexing data to achieve higher throughput on the system bus or backplanes. High-speed backplanes that can handle large amounts of data are extremely important to high-performance systems.

The backplane is a physical and electrical interconnection between various modules in a system. Each module in the backplane communicates with other modules through the backplane bus. The backplane traces and the load capacitance affect signal integrity.

The discussion of the backplane demonstration system in this application report describes the various issues that should be considered while designing a backplane. The type of termination, backplane topology and layout, connector capacitance and stub lengths, along with the effect of the number of loads, all are investigated in this report. This report explains a demonstration backplane and its elements, followed by results that have been obtained using the TI GTL+ devices. HSPICE, a simulation tool, is used to model the performance of the system and to compare it to the hardware.

Background

In the past, increased throughput was achieved by increasing the frequency, or clock rate, or by increasing the bit width of the bus. Logic families that were used as backplane drivers included Advanced BiCMOS Technology (ABT), Fast CMOS Technology (FCT), Advanced CMOS Technology (ACT) and Backplane Transceiver Logic (BTL). These backplane drivers do not perform well in backplanes operating at frequencies over 33 MHz, but are sufficient for lower throughput requirements. With the trend toward higher system bandwidth requirements, into the hundreds of multimegabits per second, using a technology that supports these higher performance requirements is essential.

These increased speeds and performance requirements in designs created a need for higher-speed devices. Newer technologies developed by TI have helped to create devices that can drive these high-performance backplanes.

GTL/GTL+

Gunning Transceiver Logic (GTL), a technology invented by William Gunning at Xerox Corporation and standardized by JEDEC, was a low-swing input/output (I/O) driver technology that helped address these high-performance requirements. This technology was further modified by Intel™ and TI by increasing the voltage swing to create the GTL+ switching standard (see Figure 1). Subsequently, the standard was used by TI and Fairchild to create stand-alone devices to drive backplanes.

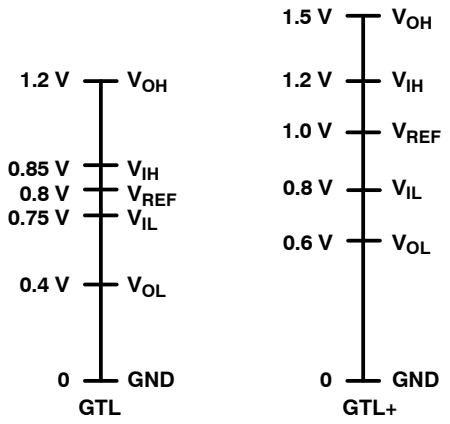

Figure 1. GTL/GTL+ Switching Levels

GTL+ achieves high performance with the help of the low signal voltage swing.[1] The typical swing for GTL+ is from 0.6-V low (V_{OL}) to 1.5-V high (V_{OH}) maximum. TI uses tighter threshold regions, V_{IH} at 1.05 V, V_{IL} at 0.95 V, and V_{OL} at 0.55 V, to provide better signal integrity in its stand-alone devices. This report demonstrates the performance of the newest TI GTL+ devices operating at clock rates of 100 MHz, providing bit rates of up to 10 Gbit/s in a 100-bit-wide backplane bus.

The TI GTL family offers edge control, which reduces signal noise and electromagnetic interference (EMI). The basic GTL output structure is an open-drain transistor, whereas the input is a differential receiver.[2] Also, the GTL I/Os have been designed to minimize their capacitance, an extremely important factor for distributed-load high-performance backplanes.

Backplane Design Considerations

This section covers the electrical elements of the backplane. The backplane bus connects the different modules in a backplane. The wires and traces on the bus and the traces on the modules are electrical elements that are a connection point for the various electrical modules. It is necessary to understand these electrical elements (such as impedance, capacitance, inductance, termination, connectors, stub lengths, vias, and driver and receiver characteristics) to design a successful backplane.

All of the above parameters contribute to the performance of the backplane. Backplanes can be categorized as low performance, medium performance, or high performance. A low-performance backplane can be modeled as a lumped load; medium- and high-performance backplanes must be viewed as a distributed load, by applying transmission-line theory.

With a low-performance backplane, the backplane driver sees the load as a lumped capacitance. The capacitive load in many cases is still distributed; however, it is modeled as a lumped load. This lumped model is used where the rise time of the signal is small compared to the transition time along the backplane. Here, only the final state matters, and bus performance is not the highest concern. The lumped capacitance is charged or discharged by the driver (see Figure 2) and is controlled by the RC time constant. The low-to-high signal transition is indicated by $1 - e^{-t/RC}$ and the high-to-low signal transition is of the form $e^{-t/RC}$. This lumped capacitance is referred to in the industry as a lumped load.

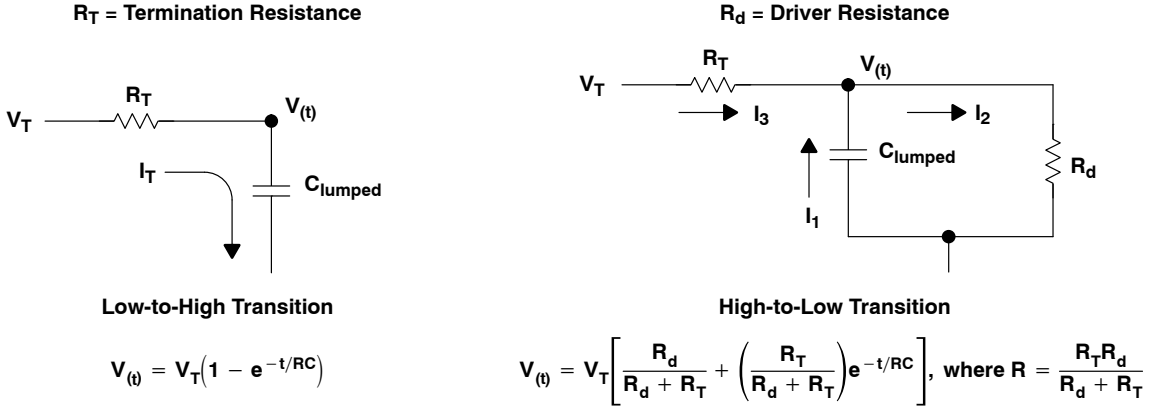

Figure 2. Lumped-Load Effects

Medium- and high-performance backplanes can be modeled as a distributed load. This is because performance drives a multidrop architecture, where the capacitance is distributed over the length of the backplane. To design an optimized medium- or high-performance backplane, a few concepts must be understood. These include the characteristic impedance of the backplane, (Z_o), the characteristic delay per unit length (τ_o), and the reflection coefficient (ρ), defined as the ratio of the amplitude of the reflected wave to the incident wave.

Figure 3 shows the transmission line as a distributed inductance and capacitance. The backplane driver charges the capacitance and is delayed by the inductance along the line. The signal sees the line as a characteristic impedance, given as:

$$Z_o = \sqrt{(L_o/C_o)} \quad (1)$$

Where:

L_o, C_o = distributed inductance and capacitance per unit length

The current flowing into the transmission line is of the form:

$$I = V_{in}/Z_o \quad (2)$$

The transition time or the time it takes for the signal to travel along the transmission line is:

$$\tau_o = \sqrt{(L_o/C_o)} \quad (3)$$

The intrinsic per-unit delay along the line is multiplied by the distance to give the overall delay across the line.

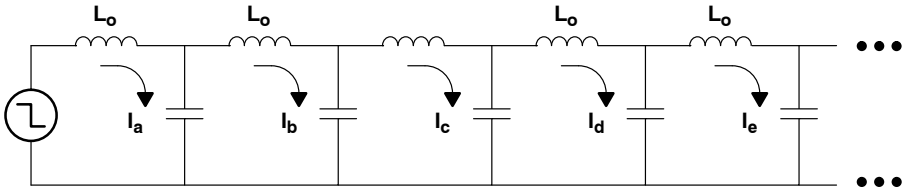

Figure 3. Transmission Line

The connectors on the backplane connect the backplane traces to branch transmission lines called stubs. These stubs are the communication ports between the backplane and the plug-in modules. These stubs, which have inductance and capacitance, change the overall impedance of the transmission line, and affect the signals that feed into the plug-in modules. This lumped capacitance changes the impedance and delay constants along the line by the following relationships:

$$Z_L = Z_o/\sqrt{(1 + C_d/C_o)} \quad (4)$$

$$\tau_d = \tau_o\sqrt{(1 + C_dC_o)} \quad (5)$$

Where:

C_d = added capacitance per unit length
C_o = intrinsic capacitance (as defined previously)

A point on the backplane where the impedance changes is called a discontinuity. A discontinuity on a backplane can occur if the drivers are placed too far from the backplane, there is improper termination, or the driver and receiver characteristics are not properly matched. At each point where a voltage wave that travels down the backplane meets a discontinuity, some of the signal is reflected, while the rest is transmitted along the backplane. The reflection coefficient determines the amount of signal that is reflected and is defined as the ratio of the reflected wave to the incident wave.

Figures 4 and 5 show the effects described above by using the GTL16622A to drive lumped and distributed loads, respectively. The lumped load consists of 25 Ω to 1.5 V, 30 pF to GND, whereas, the backplane (distributed load) consists of 16 slots separated by 0.875 in. Each load is approximately 14 pF.

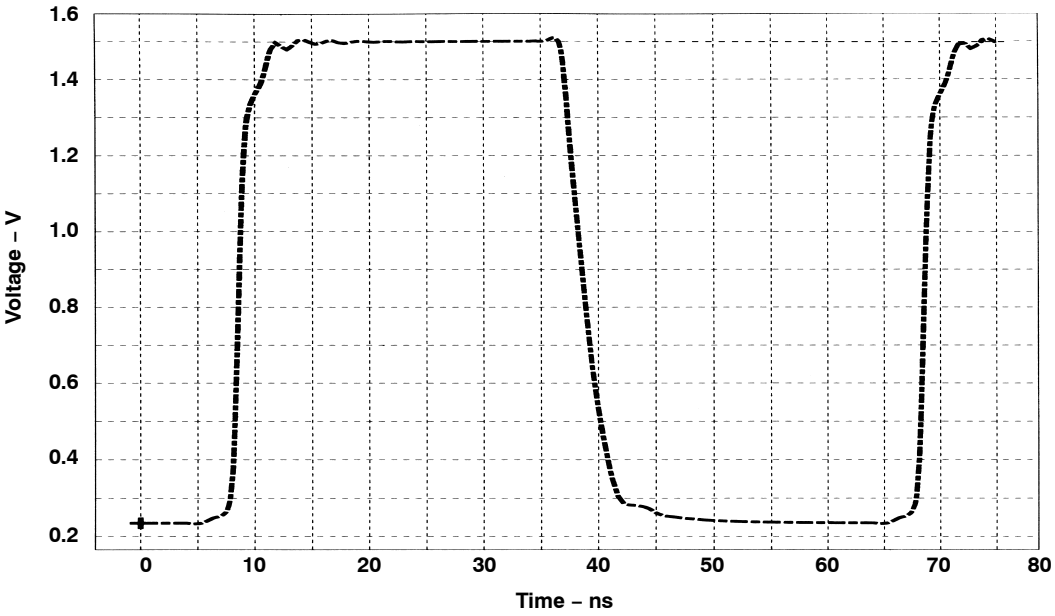

Figure 4. GTL16622A H-SPICE Simulation (Lumped Load, 33 MHz)

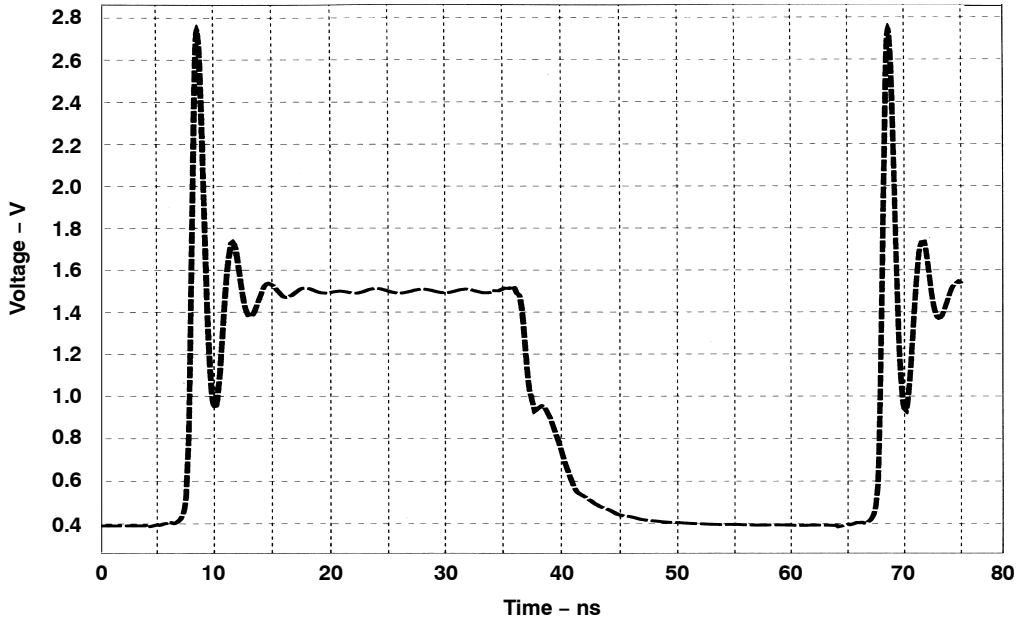

Figure 5. GTL16622A H-SPICE Simulation of a Backplane (Distributed Load, 33 MHz)

The added capacitance and inductance in the distributed load cause reflections that result in problems that include reduced noise margins.[3] In this case, the signal on the bus must settle before being sampled, hence, the bus settling time is required before valid data can obtained. Table 1 shows the comparison for the noise margins obtained for GTL and GTL+. GTL+ provides a wider noise margin than GTL, an important factor for designing signal-integrity-critical applications. In high-performance backplane designs, termination voltage, bus impedance, termination resistance, stub lengths, and driver and receiver characteristics must be controlled carefully to achieve good signal integrity, so that valid data can be presumed at the incident wave of the signal.

Table 1. Noise-Margin Comparison

DEVICE TYPE	NOISE MARGIN (mV)	
	UPPER	LOWER
GTL	350	350
GTL+	450	400

Another issue to consider in backplane design is crosstalk. Crosstalk, an effect of capacitive coupling in backplanes, can also result in false switching. Crosstalk between signal lines can be approximated as being inversely proportional to the distance between the signal lines and directly proportional to the distance between the signal lines and the ground plane. The most popular technique used to avoid crosstalk is fine-line technology that increases the distance between the signal lines while decreasing the distance between the signal line and the reference plane.

Backplane Demonstration System

The TI backplane demonstration board represents a typical industry backplane. The following section explains the elements of the demonstration backplane.

Architecture

Backplane Driver/Receiver (GTL16622A)

The GTL16622A 18-bit LVTTL-to-GTL/GTL+ bus transceiver translates between GTL/GTL+ signal levels and LVTTL or 5-V TTL signal levels. The device supports mixed-mode signal operation (3.3-V and 5-V signal) on the A port and control pins and is hot insertable with an output drive capability of 50 mA.[4] The device is used as both the driver and the receiver on the individual plug-in modules in the backplane.

Backplane Motherboard

The TI backplane demonstration board was constructed after studying various backplane loads. The 36-bit backplane consists of 14-in. traces with 16 slots separated by 0.875-in. pitch. Figure 6 shows the physical layout of the backplane board and its elements. The power supplies are represented as PS1 (5 V) and PS2 (3 V) and connectors by points P1 to P16. The connectors host the driver/receiver cards.

The clock drivers are U1, U2, and U3. U1 and U2 each distribute the clock to eight loads, while U3 is configured to supply the data at one-half the clock rate. The crystal oscillator (X1) supplies the clock and the data to the backplane board. The crystal oscillator can be changed to configure the clock rates at any frequency. The frequencies that have been used to test the demonstration board are 50 MHz, 66 MHz, 80 MHz, and 100 MHz. One of the plug-in cards is a driver, while the remaining cards are receivers. The GTL16622A is used as both driver and receiver. The position of the driver card on the backplane can be varied to study the loading effects and signal integrity on the backplane.

The 1.5-V termination voltage (V_{TT}) for GTL+ is from a 5-V regulated power supply. The 3.3-V power supply provides power to the GTL device on board. The voltage reference, V_{REF}, is generated from V_{TT}, using a simple voltage-divider circuit with an appropriate bypass capacitor (0.1 μF) placed as close as possible to the V_{REF} pin.[2] TI recommends placing the voltage-divider circuitry on each daughter card, because this eliminates the noise introduced by the backplane trace.

The intrinsic, unloaded, backplane trace impedance is 50 Ω and has a loaded impedance of 25 Ω with 16 loaded slots. The backplane is dc terminated using a 25-Ω resistor to V_{TT} to match the loaded impedance of the backplane. The 36-bit backplane is used to transmit data from the driver to each receiver card at the frequency of the crystal oscillator.

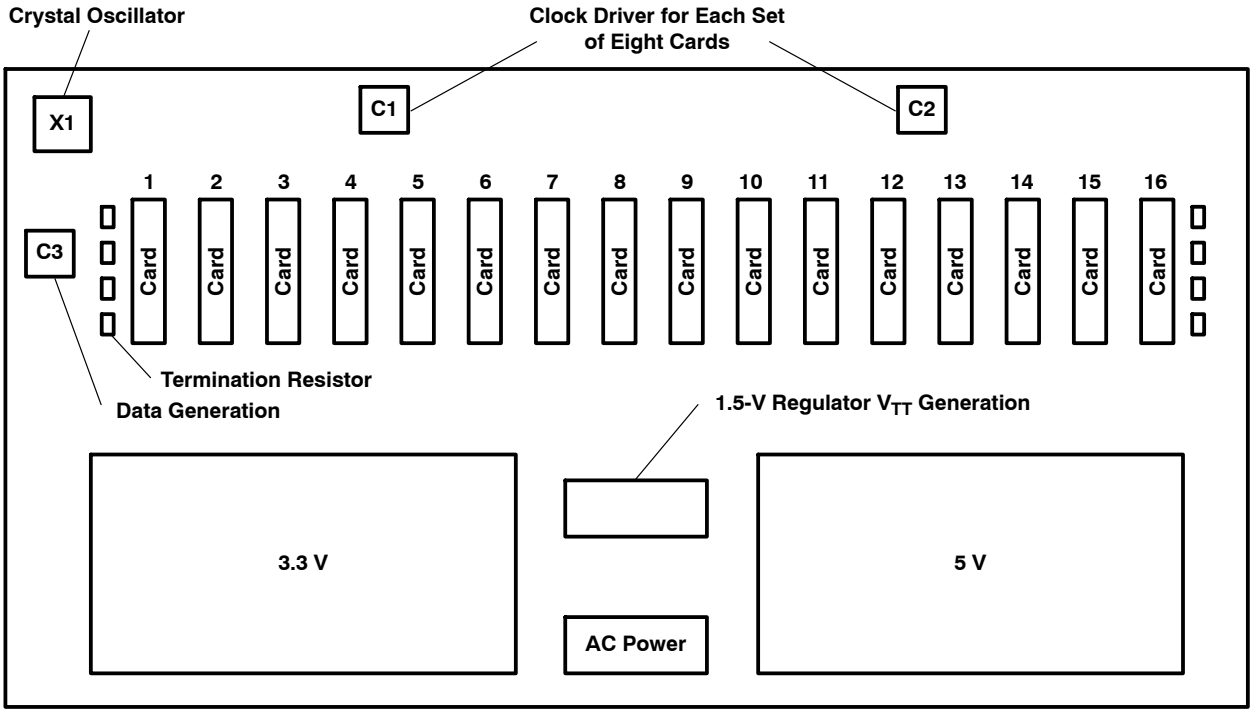

Figure 6. Backplane Demonstration Board Physical Layout

Interconnect and Impedance Calculations

Figure 7 is a graphical summary of the network that provides the physical dimensions of the backplane. Each element introduces additional capacitance on the board, which increases the loading on the backplane, eventually affecting signal integrity. The physical representation of the demonstration backplane shows the slots separated by 0.875 in. of backplane trace (B). There is a 0.0625-in. stub between the backplane trace and the connector (C), followed by approximately 1 in. of microstripline card stubs (D), and a total stub length of 1.0625 in. (as shown in the impedance calculator in Figure 8).

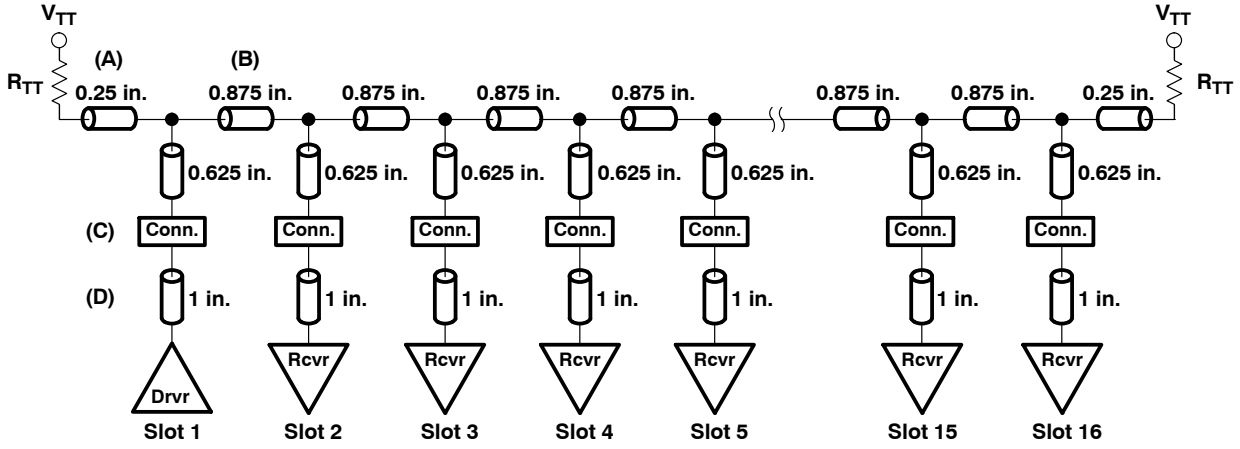

Figure 7. Backplane Physical Representation

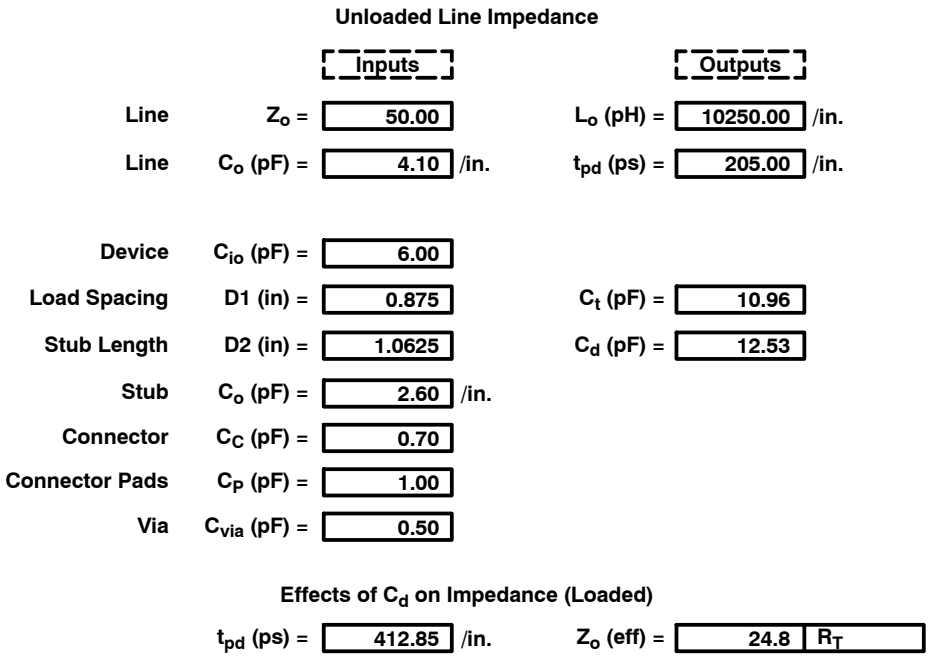

Figure 8. Impedance Calculator

The impedance calculator is a spreadsheet that is created using the previous equations to show the effects of distributed capacitance. The spreadsheet shows that the initial impedance of the 50-Ω backplane trace introduces a delay of 205 ps/in. (see equation 3) and has a C_o of 4.1 pF/in. The introduction of backplane loads increases the distributed capacitance (C_d) to 12.53 pF/in., which increases the propagation delay (t_{pd}) to 412.85 ps/in. and reduces the backplane impedance to 24.83 Ω (see equation 4). The backplane loading is a factor of the input/output capacitance of the driver or receiver (C_{io}), stub capacitance, via capacitance, and connector capacitance. Both ends of the backplane trace are terminated by a stub (A), using a 25-Ω pullup resistor to the termination voltage (V_{TT} = 1.5 V).[5]

Results

Laboratory data were taken using the demonstration backplane and compared to HSPICE simulation results to validate the performance of the GTL16622A on the backplane. Figure 7 is the reference to give the position of driver and receiver cards in the backplane. Results for TI's newest addition, the GTL16612A, demonstrate the throughput capability in a very high-performance backplane.

Laboratory

Figure 9 shows the laboratory results for the GTL16622A, with all 36 bits switching on the fully loaded backplane board with the driver card in slot 1. The worst-case signal was observed in the receiver card closest to the driver card (slot 2), while the best-case signal was seen in the receiver card farthest from the driver (slot 16). The throughput obtained at 50 MHz is 1.8 Gbit/s.

Figure 9. GTL16622A Signal Integrity (Laboratory Results)

Simulation

Figure 10 shows the HSPICE simulation results for the GTL16622A, which correlate closely with results observed in the laboratory with the demonstration hardware. The simulation results are observed after modeling the backplane using HSPICE for single-bit switching.

Figure 10. GTL16622A Signal Integrity (HSPICE Simulation Results)

The slot closest to the driver (slot 2) shows the worst-case ringing because it sees the fastest rise time of the IC driver compared to the slots that are farther away from the driver. The worst-case signal at slot 2 also is due to the effect of reflected energy that is maximum in the receiver closest to the driver.[3]

Correlation

Figure 11 shows laboratory versus simulation results for the GTL16622A on the demonstration board. The results shown are for the receiver at slot 2 (closest to the driver card). Here, as the frequency is increased, the time available for the data to be sampled decreases, making good signal integrity necessary at these high frequencies.

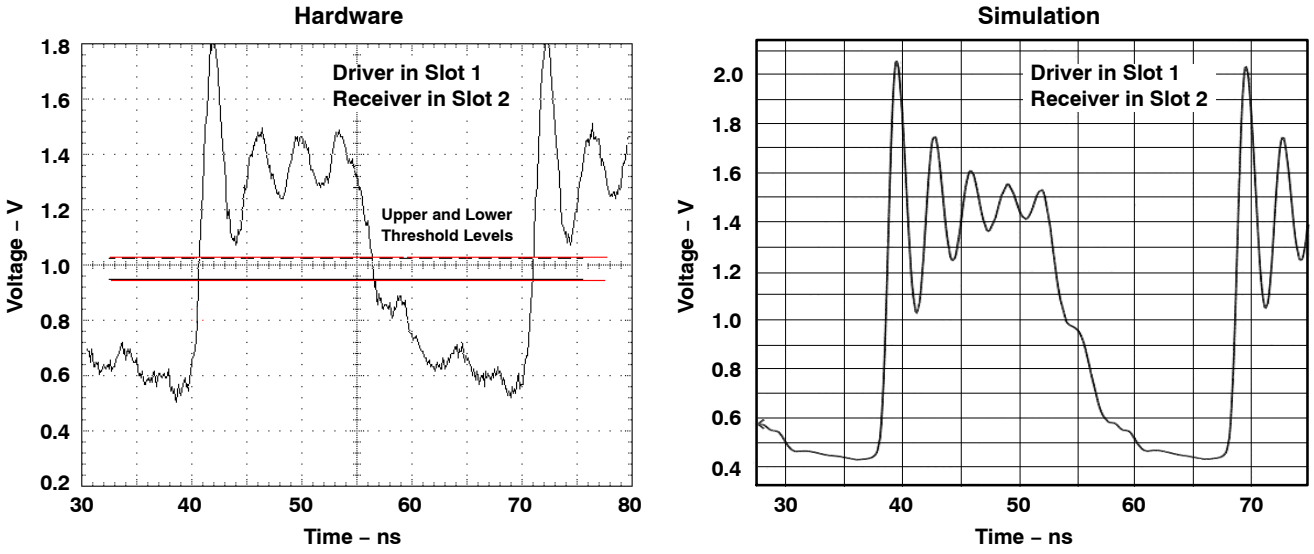

Figure 11. GTL16622A Signal Integrity (Hardware vs Simulation at 66 MHz)

Moving Forward With the GTL16612A

TI has continued to improve the characteristics and features of the GTL family to provide higher throughput rates at backplane frequencies up to 80 MHz. These higher frequencies allow designers to transmit increased amounts of data on their board, achieving high bit rates in their systems. The newest device in the GTL family, the GTL16612A, an improved version of the GTL16612, is capable of operating at frequencies as high as 80 MHz. The features of this device include output edge control (OEC™) on the rising and the falling edge, and optimization for high-performance distributed-load applications. Simulation results that provide a comparison between the GTL16622A and the GTL16612A are shown in Figures 12 and 13 at 50 MHz and 66 MHz, respectively.

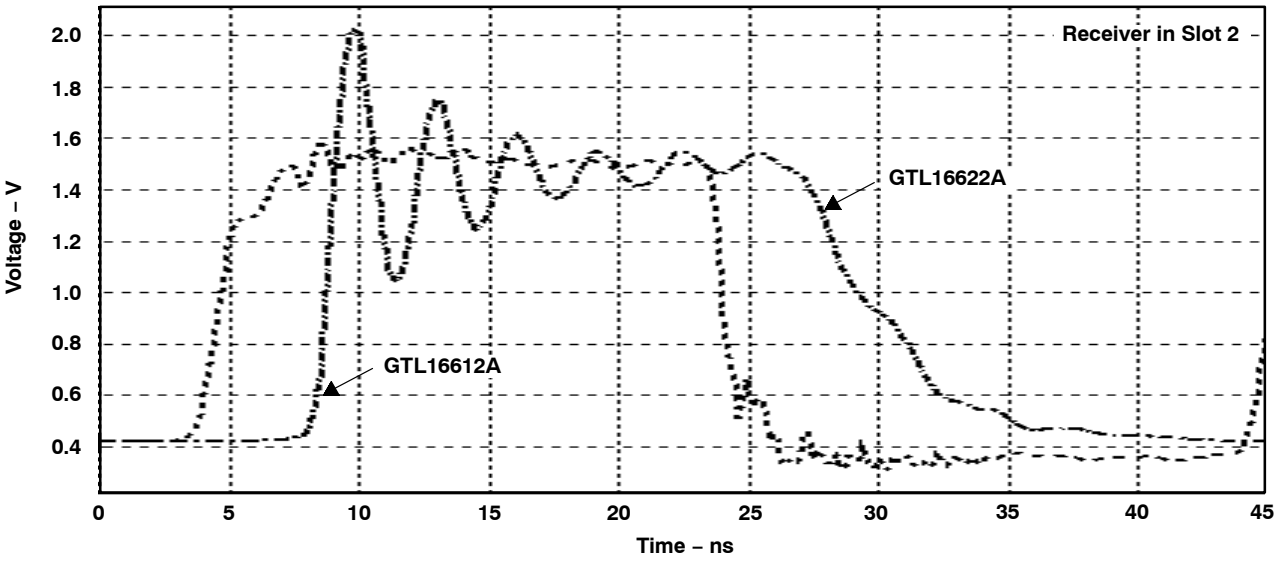

Figure 12. GTL16622A vs GTL16612A (50 MHz)

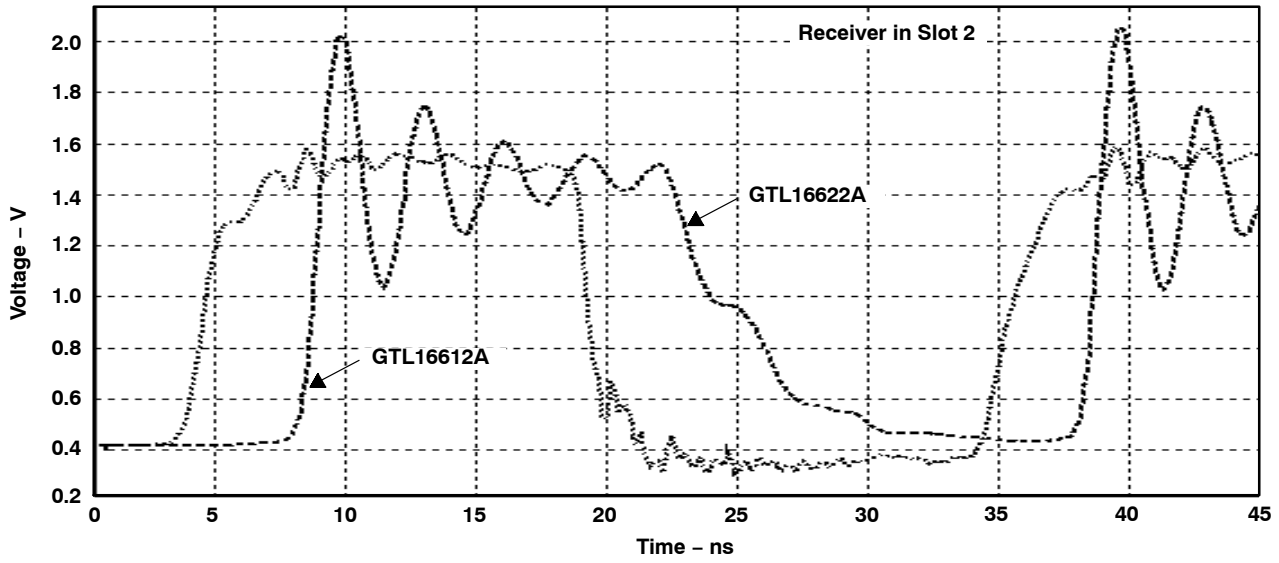

Figure 13. GTL16622A vs GTL16612A (66 MHz)

OEC is a trademark of Texas Instruments Incorporated.

Figure 14 shows simulation results for the GTL16612A operating at high clock rates of 80 MHz and 100 MHz. The innovative design of the 18-bit device provides for extremely high throughput on a backplane if the timing requirements of the board can be met.

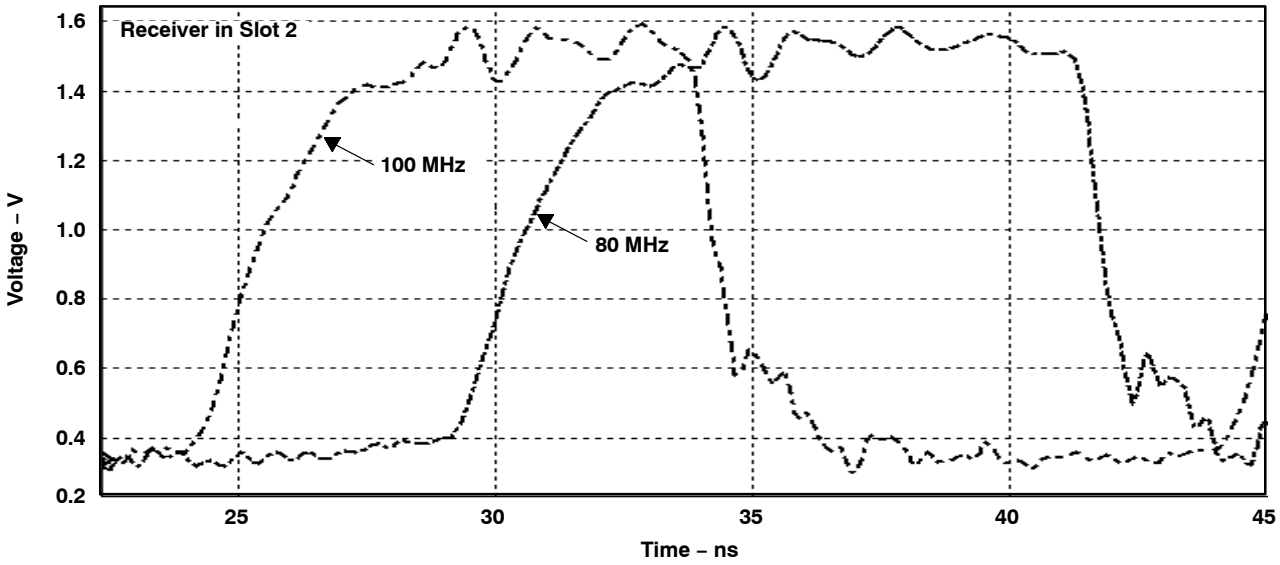

Figure 14. GTL16612A Simulation Results at 80 MHz and 100 MHz

Summary

The demonstration board has clarified backplane design issues and has provided unique insight into the capability of the GTL+ technology. With the escalation of requirements for high-speed data transfer, and a transition from low and medium performance to high performance, the backplane will be a critical component in the performance equation. The TI GTL16622A has served as a backplane driver for medium- and high-performance applications, while the new GTL16612A overcomes the problems in a very high-performance backplane to provide good signal integrity. Clearly, GTL+ is the next-generation technology, capable of accurately moving large amounts of data on the backplane with high speeds, while achieving the bit rates that will be required by new designs.

Acknowledgment

The authors of this application report are Shankar Balasubramaniam, Ramzi Ammar, and Ernest Cox.

The authors recognize the contributions and assistance provided by Adam Ley, Gene Hintershcer, and Mac McCaughey.

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4 Texas Instruments, SN74GTL16622A data sheet, literature number SCBS673.

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Glossary

Incident-wave switching	Voltage transition that is strong enough to switch the input of the receiver on the first edge of the wave. This implies that subsequent reflections do not change the state of the receiver to its previous state.
Noise margin	Difference between the driver or receiver threshold voltage and the voltage on the bus. A noise margin comparison for the GTL/GTL+ technologies is shown in Table 1. The increased noise margin for GTL+ is preferred because it can result in better signal integrity.
Stub	Path on the board between the driver/receiver card and the backplane. This includes the trace on the board, the connectors, and the lumped capacitance of the driver or the receiver. The length from the driver/receiver to the backplane is the stub length.
Throughput	Data rate that is achieved on the bus or the backplane. It can be calculated on a parallel-bus architecture as the product of the number of bits and the frequency of transmission.

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12-mm Tape-and-Reel Component-Delivery System

SLZA001
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Abstract

The design advances of component pick-and-place automated equipment for board assembly increasingly are pushing the margins of the tape-and-reel packing configurations. The continuing drive for faster assembly reduces the index time and tends to amplify the forces acting on the tape-and-reel component-delivery system. The magnified forces, when combined with a high carrier-tape width-to-component mass ratio, may cause component placement problems, reduced yield, and subsequent degradation of board-assembly manufacturing efficiency. Texas Instruments (TI™) has initiated an improved component-packing method for the 8-/14-/16-pin TSSOP PW packages to ensure that customer processes remain efficient. This application report describes the improved tape-and-reel configuration on a 12-mm carrier-tape width that performs better in end-user assembly operations and aligns more closely with modern industry standards.

Background

The tape-and-reel component-delivery system consists of a carrier tape and a cover tape sealed on the carrier tape (see Figure 1). This composite tape is wound onto a 330-mm-diameter reel. The reeled components are loaded on end-user assembly machines, and the components are indexed and removed from the carrier tape cavity as needed for the board-assembly operations. Multiple reels are loaded on the same machine to allow fully automated component placement during the board-assembly process.

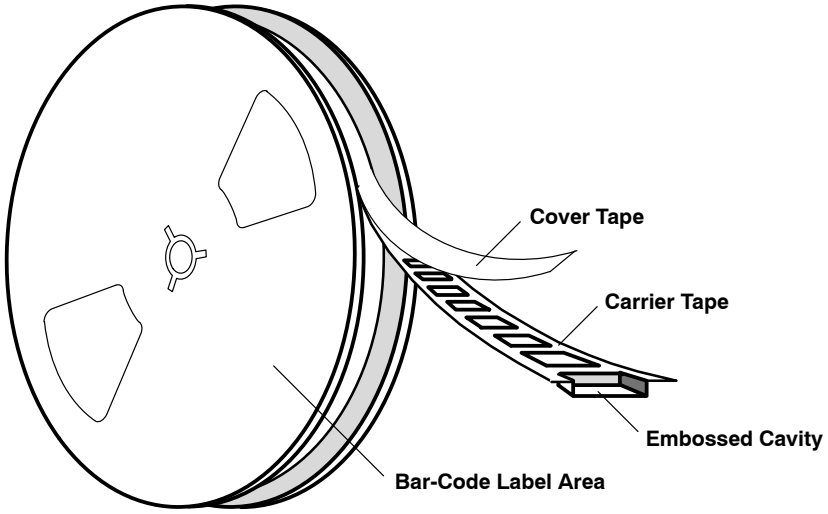

Figure 1. Tape-and-Reel Packing

Tape-and-reel component-delivery systems are designed based on the component package dimensions: length, width, and height. The package dimensions determine the corresponding A_0, B_0, and K_0 dimensions of the carrier-tape cavity (see Figure 2). These basic dimensions influence the width (W) and pitch (P_1) of the carrier tape.

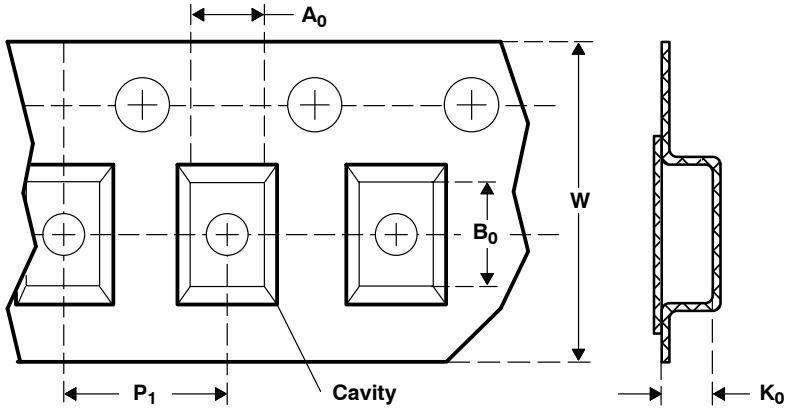

Figure 2. Carrier-Tape Dimensions

When the TSSOP PW 8-/14-/16-/20-/24-pin packages were initially released in TI-Japan, the tape-and-reel component-delivery system used the same width (16 mm) carrier tape for the entire device family. Initially, most of these products were used in the Japanese market. Over the years, as sales volume increased, the use of these devices outside Japan became more prevalent. Recent data indicates the market outside Japan is at parity with the internal Japanese market as shown in Table 1.

Table 1. Market Distribution of 8-/14-/16-Pin PW Package (November 1997 Data)

PINS	JAPAN (%)	ASIA/US/EUROPE (%)
8	10	90
14/16	57	43
Total	51	49

Summary of Component and Industry-Standard Information

This application report pertains to the TI devices in the TSSOP 8-/14-/16-pin packages designated as PW. The package outline dimensions and tape-and-reel industry guidelines are in Table 2.

Table 2. PW-Package Outline Dimensions and Corresponding Industry Guidelines

PACKAGE	PINS	COMPONENT		CURRENT		JIS c0806	
		LENGTH (mm)	WIDTH (mm)	TAPE WIDTH (mm)	TAPE PITCH (mm)	TAPE WIDTH (mm)	TAPE PITCH (mm)
PW	8	3.00	6.40	16	8	8	4
	14	5.00	6.40	16	8	12	8
	16	5.00	6.40	16	8	12	8

The customer receives a 330-mm diameter reel containing 2000 components. The tape-and-reel configuration is shown in Figure 3.

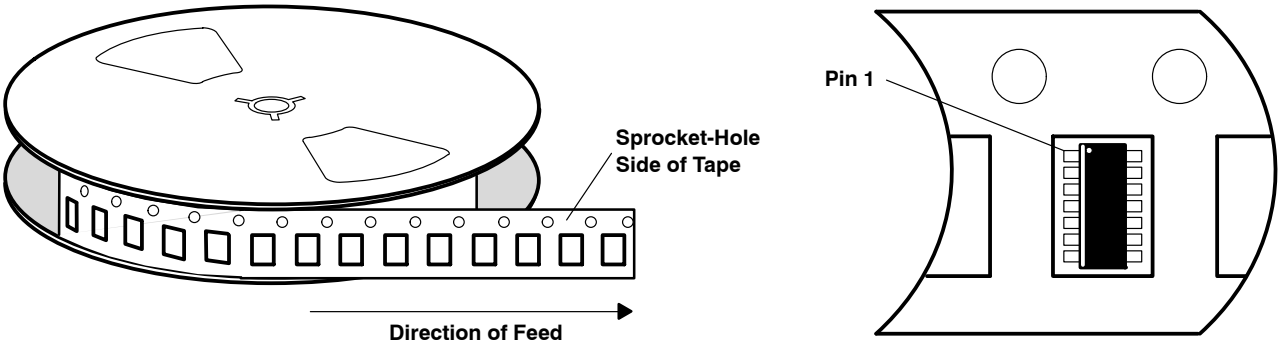

Figure 3. Typical Tape-and-Reel Configuration

Industry Trends Toward Standardization

Table 3 shows the tape widths and pocket pitch used by several semiconductor manufacturers for shipping their devices.

Table 3. Industry Shipping Configurations

COMPANY	TAPE WIDTH (mm)	POCKET PITCH (mm)
FSC	12	8
Hitachi	16	8
Motorola-Japan	12/16	8
Motorola-U.S.	12	8
Pericom	12	8
National-Japan	12/16	8
TI†	12	8
TI-Japan	16	8
Toshiba	16	8

† Beginning April 1, 1998, for all TI except Japan; TI-Japan began conversion on July 1, 1998.

Device Feeder Technology

A tape feeder moves the cavity of the carrier tape into a fixed location for the component to be picked up by the vacuum head. Indexing the carrier tape, peeling the cover tape, and exposing the component for pick-up occur simultaneously. These actions cause rapid acceleration and deceleration of the component inside the carrier-tape cavity. These actions can cause low-mass components to tilt or be ejected from the cavity, making it impossible for the vacuum head to pick up the component. Figure 4 illustrates a typical feeder configuration.

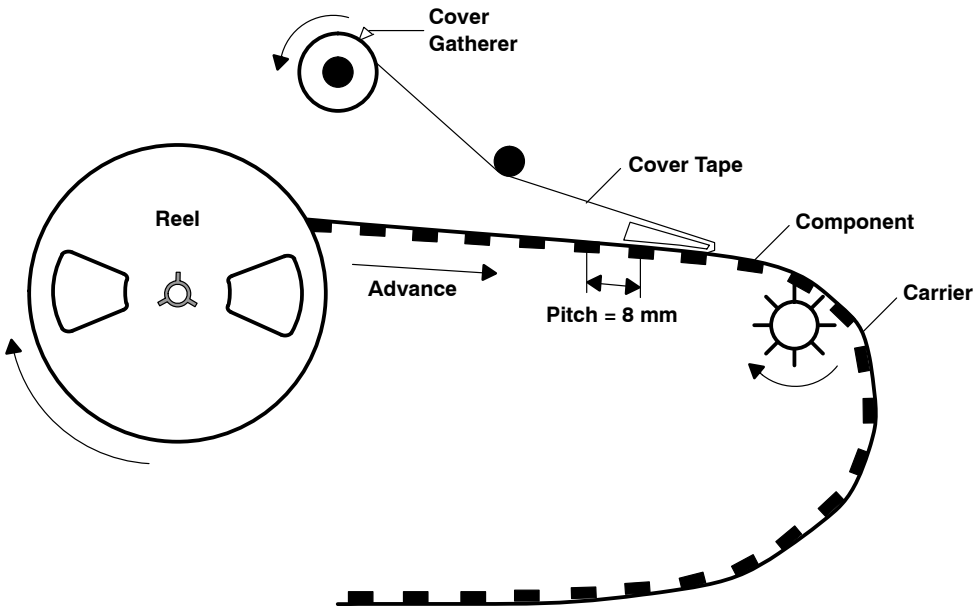

Figure 4. Typical Tape-and-Reel Feeder Configuration

Automated Board-Assembly Technology

Carrier-tape feeder designs vary among manufacturers. In most cases, end users rely on the tape-and-reel component-delivery system to compensate for the multiple feeder designs.

Key elements to smooth transfer of the components from the carrier-tape cavity to the designated place on the board are the index time, cover-tape removal tension, design of the blade used to lift and route the cover tape away from the carrier tape, and the function and design of the feeder cavity cover (if used).

Low-mass components are more prone to bounce and jostle in reaction to flexural motions generated by the high-speed, rapid indexing of the feeder, and pick-and-place actions of the vacuum head on the carrier tape. The formed cavity of the carrier tape provides strength to the middle portion of the tape. The outer portions of the tape remain flat, which provides the area for vertical flexing. The wider the tape, relative to the pocket, the greater the deflection. The flexing is illustrated in Figure 5.

$$\text{Deflection} = \frac{\text{Load} \times \text{Tape Width}^3}{4 \times \text{Young's Modulus} \times \text{Cavity Breadth} \times \text{Cavity Depth}^3}$$

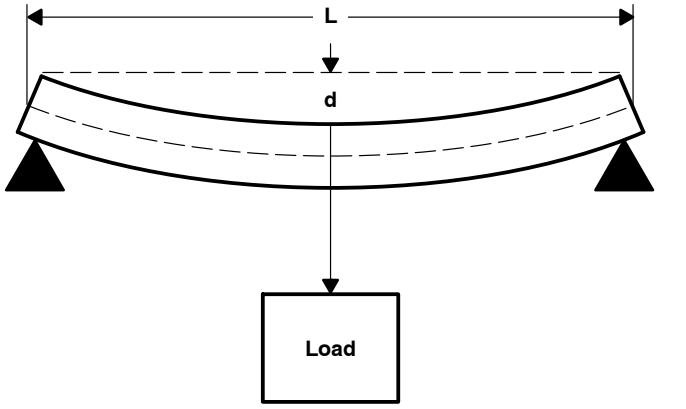

Figure 5. Carrier-Tape Flexing

The amplitude of the deflection is directly proportional to the cube of tape width. Reducing this value decreases the flexing potential. Figure 6 illustrates the improved performance that the reduced tape width provides.

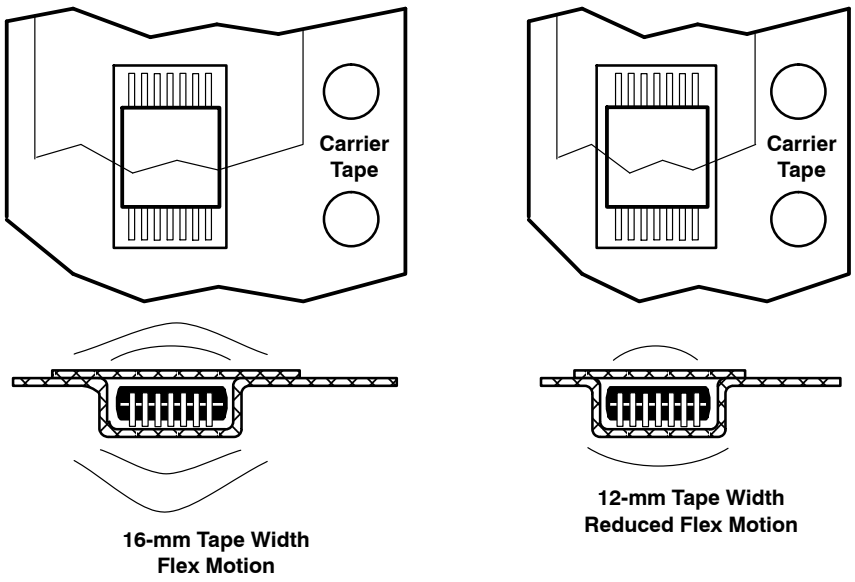

Figure 6. 16-mm and 12-mm Carrier-Tape Widths

Assume that load, cavity breadth, cavity depth, and Young's modulus are identical for both tape widths. The carrier-tape deflection is directly proportional to the cube of the widths. Therefore, the reduction can be estimated to be 57.8%.

- For 16-mm tape, the calculations are:

  Width = 16 mm
  Load (pick-up head) = 0.01 N
  Cavity breadth = 3.8 mm
  Cavity depth = 1.6 mm
  Young's modulus = 0.5 N/mm^2
  Deflection $= \frac{0.01 \times 16^3}{4 \times 0.5 \times 3.8 \times 1.6^3} = 1.312$ mm

- For 12-mm tape, the calculations are:

  Width = 12 mm
  Load (pick-up head) = 0.01 N
  Cavity breadth = 3.8 mm
  Cavity depth = 1.6 mm
  Young's modulus = 0.5 N/mm^2
  Deflection $= \frac{0.01 \times 12^3}{4 \times 0.5 \times 3.8 \times 1.6^3} = 0.555$ mm

NOTE:
These values are assumptions, and are given for explanatory purposes only. Actual conditions vary, depending on material suppliers and assembly equipment manufacturers.

Survey of Customer Experience

While limited data is available from customers receiving components in 12-mm tape, some customers receiving units in 16-mm tape widths reported that 35–40% of the components fell out of the tape. No issues related to this topic have been reported since converting to 12-mm tape.

A key customer recorded the process with a high-speed camera. Their analysis of the 16-mm tape configuration is summarized in the following paragraph:

> *The tape is too wide and thus flexible. The feeder mechanism is allowing the part to be jostled in the pocket. As the tape is ratcheted and advanced (electrical solenoid), the device is jostled 'up' in the pocket and is being caught in the cover of the feeder mechanism so as to bind the part and bend the lead(s) during the normal advancing to the next pocket stop.*

Local feeder modifications could minimize this issue, but each time the device was set up for a new run, the above process was repeated.

Conclusion

Using a narrower-width carrier tape reduces flexural forces applied to the component during the indexing action of the feeder, which leads to a more efficient board-assembly process for the end user.

Additionally, narrower-width carrier tape proportionally reduces the amount of raw materials consumed in the component-packing process. This reduction requires less space for inventory and reduces waste.

Acknowledgments

The authors of this application report, Cles Troxtell and Bobby O'Donley, acknowledge the assistance of Mary Helmick and Edgar Zuniga.

References

Elements of Physics, Smith and Cooper, 8th Edition.

EIA-481, *Taping of Surface Mount Components for Automatic Placement*, Revision A, February 1986.

JIS c0806 (Japanese Industrial Standard), *Packaging of Electronic Components on Continuous Tapes (Surface Mounting Devices)*, 1995.

Glossary

C

Carrier tape — Formed polystyrene semirigid tape used to contain individual components for sequential pick-and-place operations in automated board-assembly processes.

Cover tape — Transparent PET material attached to the surface of the carrier tape to contain the individual component in the carrier-tape cavity during reeling, shipping, and unreeling of the tape-and-reel-packaged components.

T

Tape and reel — Method of packing components in a tape system and reeling specified lengths or quantities onto a reel for shipping, handling, and configuring for use in industry-standard automated board-assembly equipment.

Tape feeder — Industry-standard feeder mechanism designed to accept the tape-and-reel-configured components and index the taped components for precise positioning to be picked up by the vacuum head used by the automated board-assembly equipment.

JEDEC Publication 95
Microelectronic Package Standard

SZZA006
January 1999

TEXAS INSTRUMENTS

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Contents

List of Illustrations

Abstract

Many electronics companies have joined the Joint Electron Device Engineering Council (JEDEC) and the JC-11 Mechanical (Package Outline) Standardization committee to gain further understanding of industry package standards and to register their product lines. As a member of JC-11, the company receives a hardcopy of Publication 95 that generally is in the custody of the committee member. The publication is updated and maintained by the member or the alternate. The JC-11 member, or alternate, often is contacted for information, a drawing copy, or instructions for registering a package with JEDEC.

JEDEC provides free access to Publication 95 on the JEDEC web page. This document is intended to familiarize the reader with the JC-11 procedures, requirements for registration, and how to locate and use Publication 95. The available information is useful to packaging engineers, component engineers, product engineers, end users, designers, and marketing personnel.

What Is EIA/JEDEC?

EIA is the Electronic Industries Alliance (formerly the Electronic Industries Association), which provides many services and benefits to the electronics industry. EIA is the umbrella organization for many standardization activities and committees, one of which is JEDEC. The EIA web-page address is www.eia.org (see Figure 1) . JEDEC can be accessed from this page by selecting *JEDEC Solid-State Products Electronics Technology Division*.

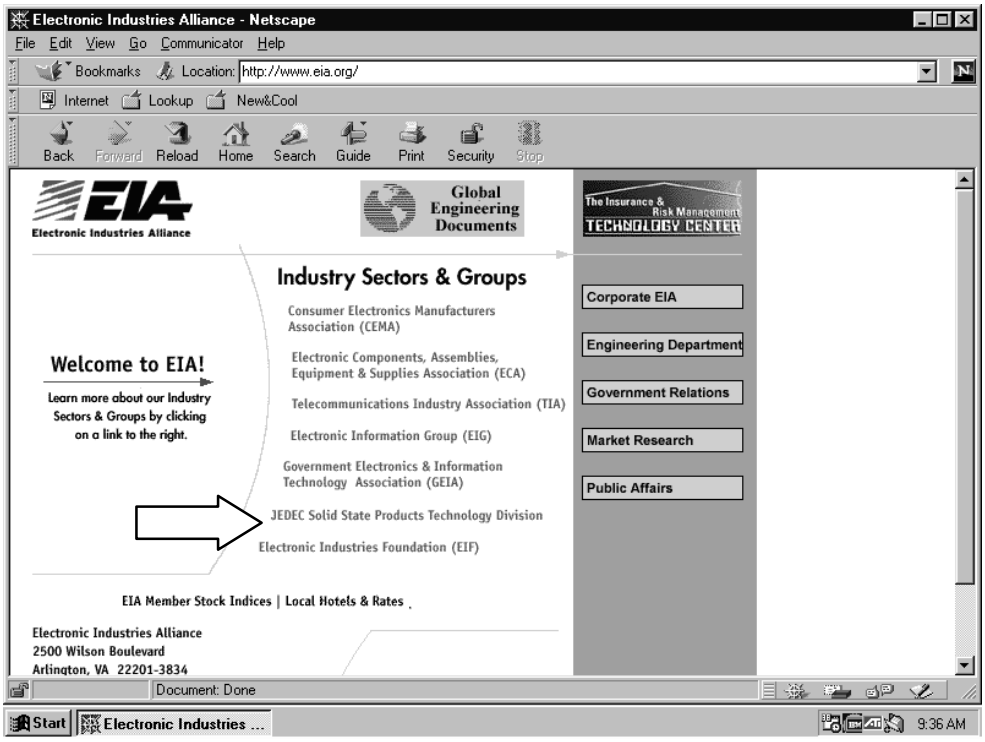


Figure 1. EIA Web Page

JEDEC became a full division of the EIA in January 1998 and now controls its own budget and operation. JEDEC has been serving the industry for many decades in standardization efforts in the areas of test methods, nomenclature, packaging, and product characterization. JEDEC is governed by a board of directors composed of representatives of various member companies. JEDEC, with its many committees, is the engineering standardization body for solid-state products in the United States, with membership of more then 300 companies. The JEDEC web-page address is www.jedec.org (see Figure 2).

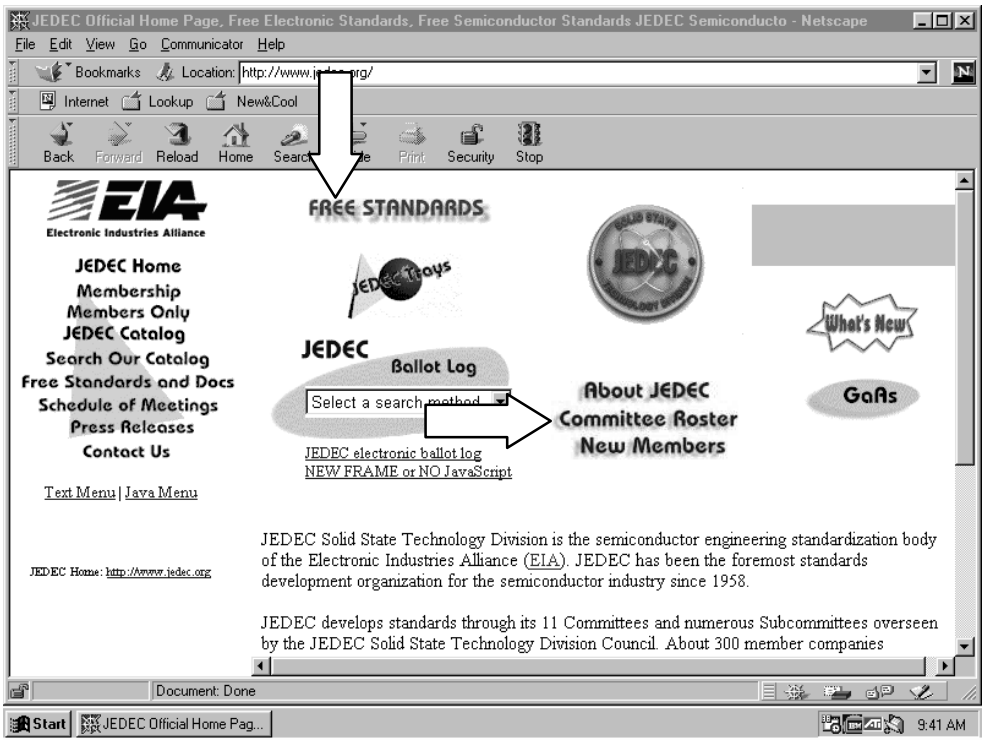


Figure 2. JEDEC Web Page

The JEDEC Committee Roster can be found on the JEDEC web page (Figure 2) by accessing Committee Roster, under the JEDEC seal. This roster provides information on the JEDEC office staff and the various JEDEC committees and chairs, with their company affiliations.

The committees within JEDEC are:

JC10 Terms, Definitions, and Symbols
JC-11 Mechanical (Package Outline) Standardization
JC-13 Government Liaison
JC-14 Quality and Reliability of Solid-State Products
JC-15 Electrical and Thermal Characterization Techniques for Electronic Packages and Interconnects
JC-16 Electrical Interface and Power-Supply Standards for Electronic Components
JC-17 Microelectromechanical Systems (MEMS)
JC-22 Diodes and Thyristors
JC-25 Transistors
JC-40 Standardization of Digital Logic
JC-41 Linear Integrated Circuits
JC-42 Solid-State Memories
JC-44 Semicustom Integrated Circuits

This document provides insight into the JC-11 Package Outline committee and Publication No. 95. The JC-11 committee meets four times a year. Due to the size of the committee, attendance is restricted to company members and alternates, or by invitation and approval of the committee chair.

What Is Publication 95?

Purpose

Publication 95 (Pub-95, JEP95), *JEDEC Registered and Standard Outlines for Solid State and Related Products*, is one of many documents published by EIA/JEDEC. Pub-95 documents several-hundred Registered Outlines, Standard Outlines, and various Design Guides endorsed by JC-11, Mechanical (Package Outline) Standardization. The publication has grown to three loose-leaf binders, which are divided into sections for easier use. The first few sections provide general information and the latter sections contain the various Registration and Standard documents. Pub-95 can be accessed from the JEDEC web page (see Figure 2) by selecting Free Standards, located just to the left of the JEDEC seal. The screen shown in Figure 3 is displayed. From this screen, scroll down and select Publication 95.

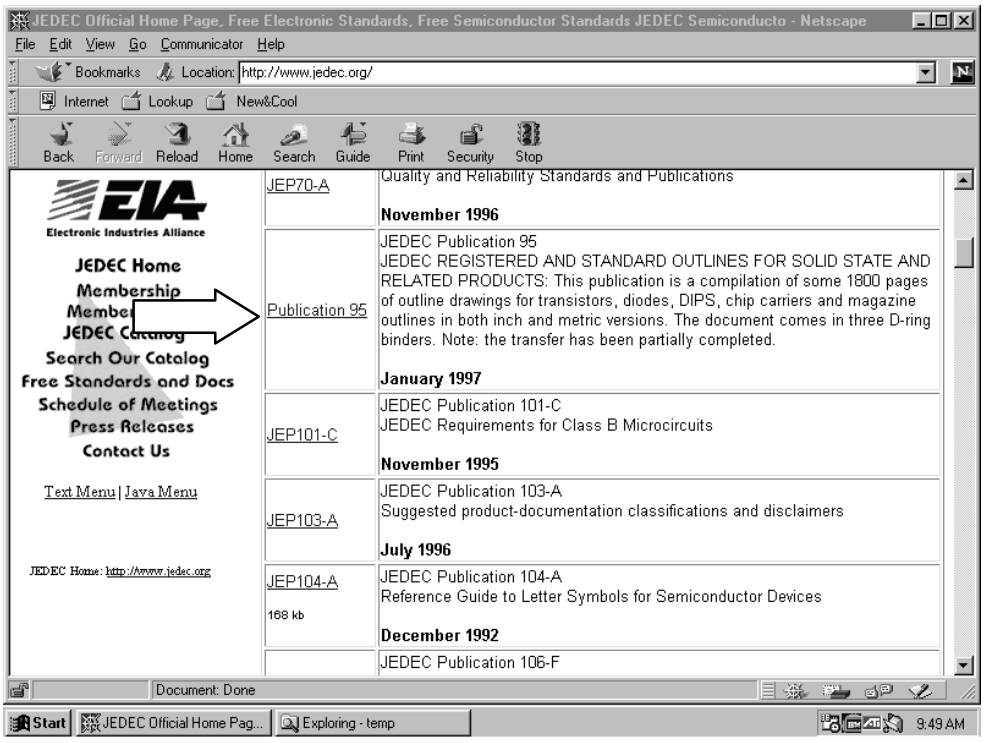


Figure 3. Access to Publication 95

The resulting screen (Figures 4 and 5) is the web page for Publication 95.

Registered Outlines vs Standard Outlines

Registered- and Standard-Outline drawings look identical, except for the outline number and the statement above the page 1 title block.

A Registered Outline has the following statement at the bottom of page 1 of the drawing:

> *This Registered Outline has been prepared by the JEDEC JC-11 committee and reflects a product with anticipated usage in the electronics industry; changes **are likely** to occur.*

See Appendix A, Figure A–1 for an example. Note the MO number near the lower right corner.

A Standard Outline has the following statement on page 1 of the drawing:

> *This Standard Outline has been prepared by the JEDEC JC-11 committee and approved by the JEDEC Council and reflects a product with wide acceptance in the electronics industry; changes **are not likely** to occur.*

See Appendix A, Figure A–2 for an example. Note the MS number near the lower right corner.

How Are Documents Controlled?

The JC-11 committee approves all additions or changes to Pub-95. Changes to Standards, or new Standards, also must have the JEDEC Board of Directors approval. Once approved, a change is forwarded to the JEDEC office in Arlington, Virginia, and the update is made to Pub-95. In 1997, Pub-95 was placed on the JEDEC web page (see Figures 4 and 5).

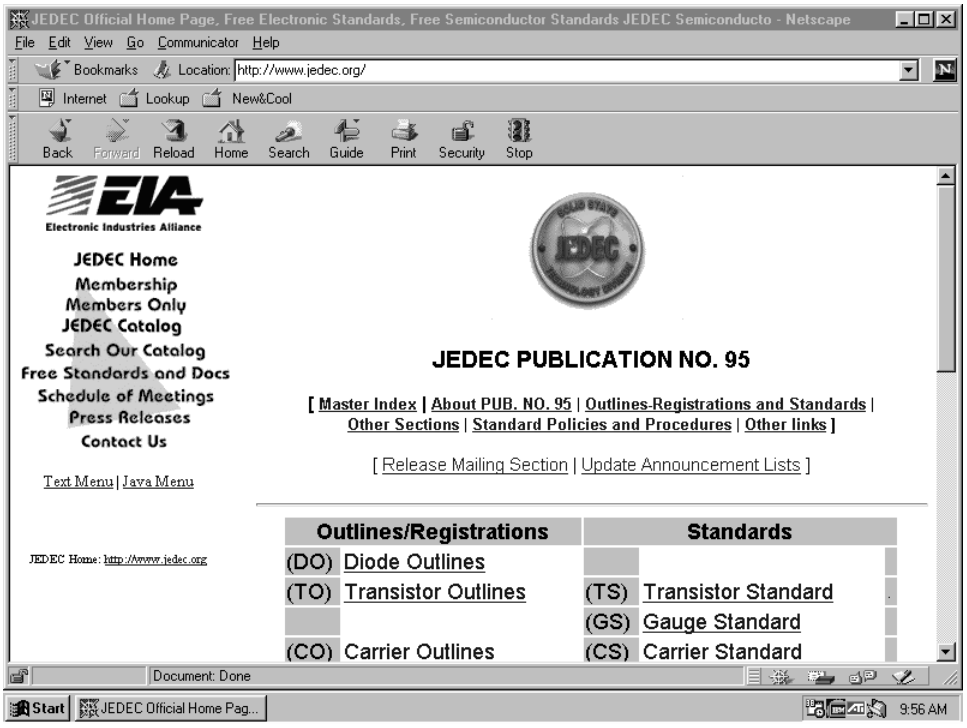


Figure 4. Publication 95 Web Page

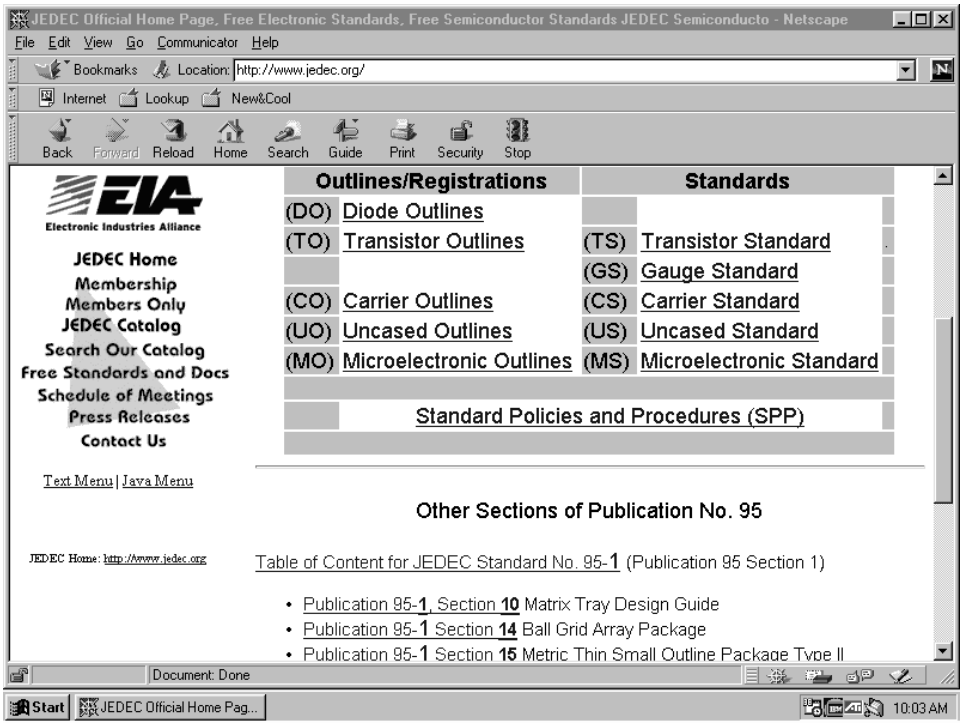


Figure 5. Publication 95 Web-Page Extension

How Are Changes Made?

Any JC-11 member company can propose a new Registration or Registration change. All proposals approved for ballot must have a two-thirds affirmative vote before being published. Organizations within a company should contact their JC-11 member for needed changes or registrations. If a company listing of committee members is not available, contact the company JEDEC board member.

A *Standard* (a Registration that is being elevated to a Standard) process includes the same JC-11 committee ballot approval and, in addition, must have unanimous JEDEC board approval to be published.

Does Our Package Outline Conform to JEDEC?

One of the first questions asked is, ‘‘Does our package conform to JEDEC?” Checking for JEDEC conformance is a manual process of finding potential similar Registrations or Standards and performing a dimensional comparison analysis.

What Is Contained in Publication 95?

Contents

Information in Pub-95 is useful to package designers, component engineers, product engineers, designers, and marketing personnel. The question that frequently is asked is, ‘‘Does our package meet or conform to JEDEC?” Package designers are concerned that new design concepts conform to the JEDEC Design Guides.

Pub-95 is divided into sections for easier reference; each section has a table of contents. The Master Index provides an overview of the entire document. The sections are:

- Guide for Outline Preparation
- Symbol List, Terminal Positions (drawings now conform to ASME Y14.5M1994)
- Outline Classifications
- JEDEC Std 95-1: Standard Practices & Procedures.
- Standard Outlines: MS (Microelectronic Standard), CS (Carrier Standard)
- Carrier Outlines (CO-nnn) -nnn denotes the sequential number assigned by the committee
- Diode Outlines (DO-nnn)
- Transistor Outlines (TO-nnn)
- Uncased Outlines (UO-nnn)
- Gauges (GS-nnn)
- Microelectronic Outlines (MO-nnn)

Requirements for Document Registration

Any member company can propose to register an outline (package) by introducing a proposal as a new business item at a regularly scheduled meeting of JC-11. The sponsor must present an outline drawing conforming to the committee requirements and to drafting standard ASME Y14.5 M1994. The sponsor is required to provide either sample outlines or company literature demonstrating company commitment.

Any member company also can sponsor the elevation of a Registration to a Standard. The outline to be raised to Standard should be well accepted by the industry and must have been registered for 2 to 3 years before being elevated to Standard. The voting process first must pass the JC-11 committee and then the JEDEC board. Normally, the Registration number is rescinded and a new Standard number assigned. The new document is published on the web in the appropriate standard section.

Definitions and Symbology

Documents to be included in Publication 95 must conform to the procedures defined in Publication 95-1 (Pub-95, Section 1). This section defines requirements, such as the guide for drawing preparation, the symbols to be used, the approved classification system, and various design guidelines. See Appendix A, Figures A–1 and A–2, for examples.

The JC-11 Committee on packaging has adopted *Dimensioning and Tolerancing Standard ASME Y14.5M-1994* as the reference document for all documents to be registered. Standard Practice & Procedure 13 (SPP-13) defines the border format and titles. Individual company drawings are not acceptable for registration.

Symbology is not standardized when comparing registrations of JEDEC vs EIAJ vs IEC47D. Each organization uses different symbols and formats. This problem is very cumbersome when one organization wishes to move a registration to another organization. Joint meetings are held routinely to address these issues.

Various Registered-Outline Types

Any member company can approach the committee to register a package. As a result, there are many types of registered outlines (see Figures 4 and 5).

A *Carrier Outline* is denoted by CO-nnn, where -nnn is the sequential number assigned by the committee. Carrier registration types include PDIP shipping tubes, PLCC shipping tubes, and trays of various types (see Figure A–3).

A *Diode Outline* is denoted by DO-nnn. Diode outlines include two- and three-lead devices, as well as axial-lead devices. Activity in this category is very low (see Figure A–4).

A *Transistor Outline* is denoted by TO-nnn. Recent outline registrations in this category include two-, three- and four-lead surface-mount packages similar to Small-Outline Packages (SOPs) or packages similar to a TO-220 surface-mount package.

An *Uncased Outline* is denoted by UO-nnn. There are only two registered outlines in this category, Beam Lead and TAB.

The largest category by far is *Microelectronic Outlines,* denoted by MO-nnn. This category includes outlines of PDIP, SOJ, SOP, SSOP, QFP, BGA, DIMM, ceramic packages, and bottom-contact (no-lead) packages. This category has more than 200 registrations.

Various Standard-Outline Types

Standard Outlines are packages that have become widely accepted in the industry and are considered to be a true standard. Very few Registrations become a Standard.

REGISTERED OUTLINE		STANDARD OUTLINE	
CO-nnn	(Carrier Outline)	CS-nnn	(Carrier Standard)
DO-nnn	(Diode Outline)	DS-nnn	(Diode Standard)
TO-nnn	(Transistor Outline)	TS-nnn	(Transistor Standard)
UO-nnn	(Uncased Outline)	US-nnn	(Uncased Standard)
MO-nnn	(Microelectronic Outline)	MS-nnn	(Microelectronic Standard)

For the more than 200 MO Registrations, there are only 29 MS Standards.

How to Access Publication 95 on the Web

Pub-95 is free access (no password required) to all viewers with web access. Anyone with computer access to the web can access a registration and print out a document. Adobe™ Acrobat™ Reader is required to view documents. Access to Pub-95 can be through the EIA web page or by going directly to the JEDEC home page. At the EIA home page:

1. Enter www.eia.org.
2. Select *JEDEC Solid-State Products Technology Division* (see Figure 1).
3. Select *Free Standards* (see Figure 2).
4. Scroll down and select *Publication 95* (see Figure 3).
5. Figure 4 shows the introduction to *JEDEC Publication No. 95*.

Find the JEDEC home page by entering the web page at www.jedec.org or, from Step 2 above, follow Steps 3, 4, and 5. From the JEDEC Publication No. 95 screen (see Figures 4 and 5), the reader can access the Master Index, Registrations or Standards, Standard Policies and Procedures, or Design Guides.

How to Find a Registration or Standard Number

Find package outline drawings in Pub-95 at web address http://www.jedec.org/download/freestd/Pub-95/, or by following the five steps in *How to Access Publication 95 on the Web*. Either method provides the same screen as shown in Figure 4. There are several options available from this screen.

Option 1

Selecting Master Index provides a numerical listing of all Registration and Standard types in Pub-95 (see Figure 6).

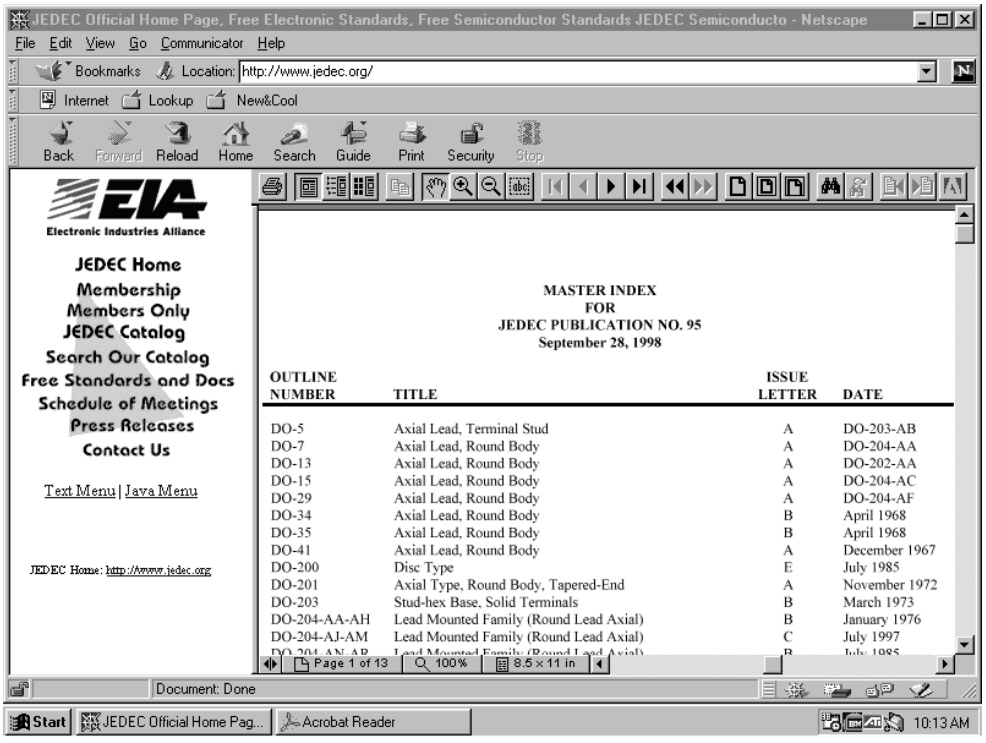


Figure 6. Master Index

Option 2

Selecting Other Sections displays a listing of the various Design Guides adopted by JC-11 (See Figure 7).

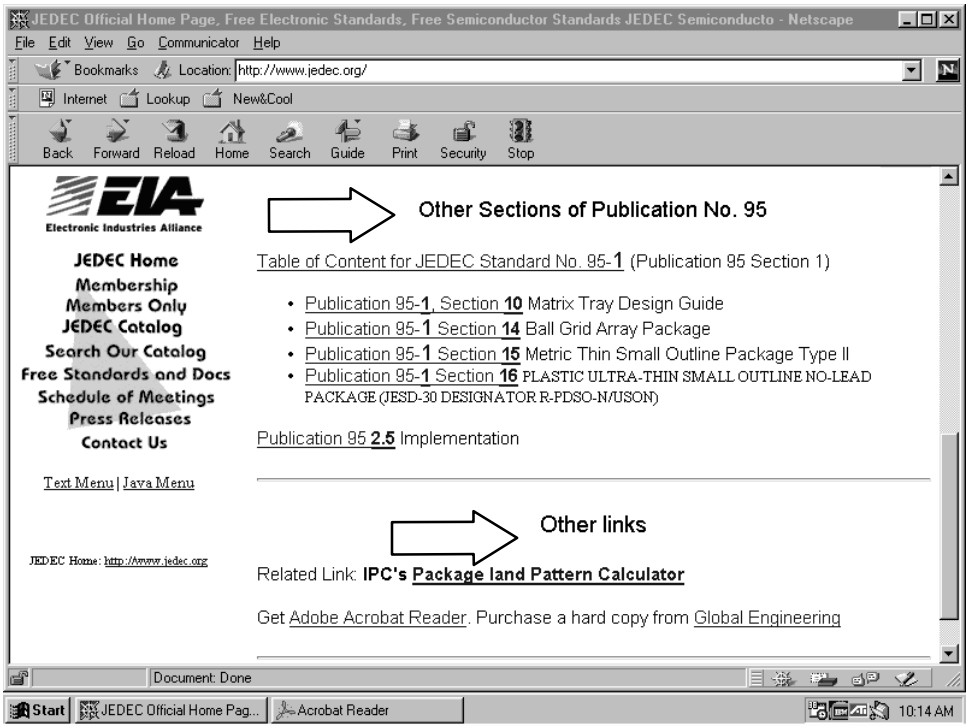


Figure 7. Other Sections (Design Guides)

Option 3

Selecting Standard Policies Procedures SPP provides a listing of the JC-11 committee operating procedures (see Figure 8).

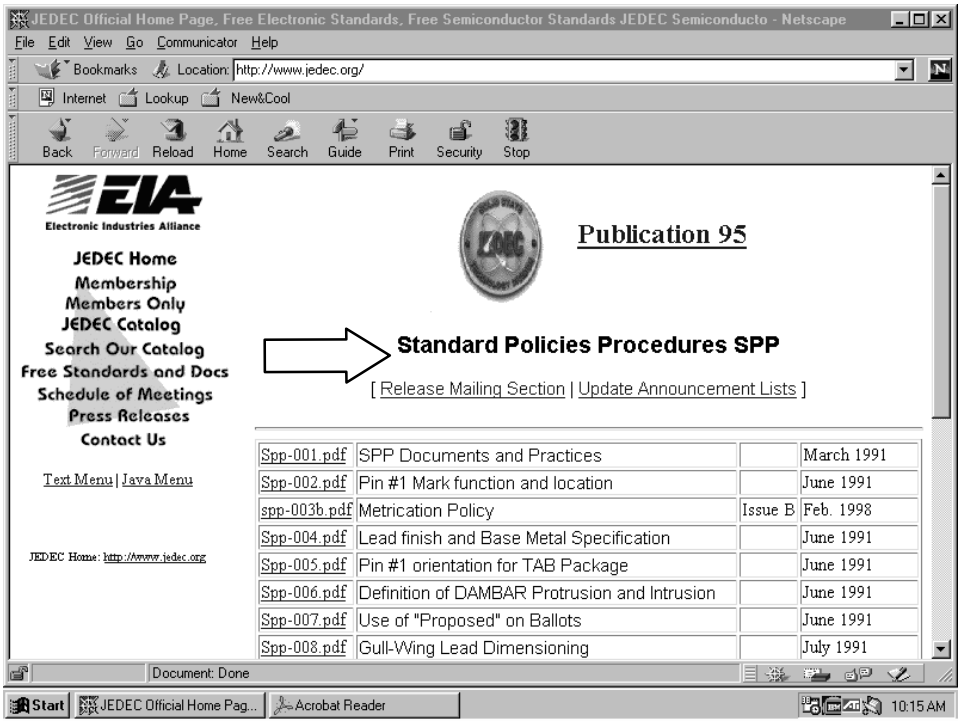


Figure 8. Standard Policies and Procedures (SPP)

Option 4

Selecting Other Links allows access to the Package Land-Pattern Calculator (see Figure 7).

Option 5

The screen shown in Figure 4 displays a comparison of Outlines/Registrations vs Standards (Mechanical Standards); for example, TO vs TS.

Search Procedure

A common question is, ‘‘Does our package meet JEDEC?’’ To determine this, a manual search through Pub-95 is required to find similar drawings and compare them to the package in question, dimension by dimension.

As an example, assume a BGA package comparison is needed. If the reader accesses the MO selection in Figure 5, the screen shown in Figure 9 is displayed.

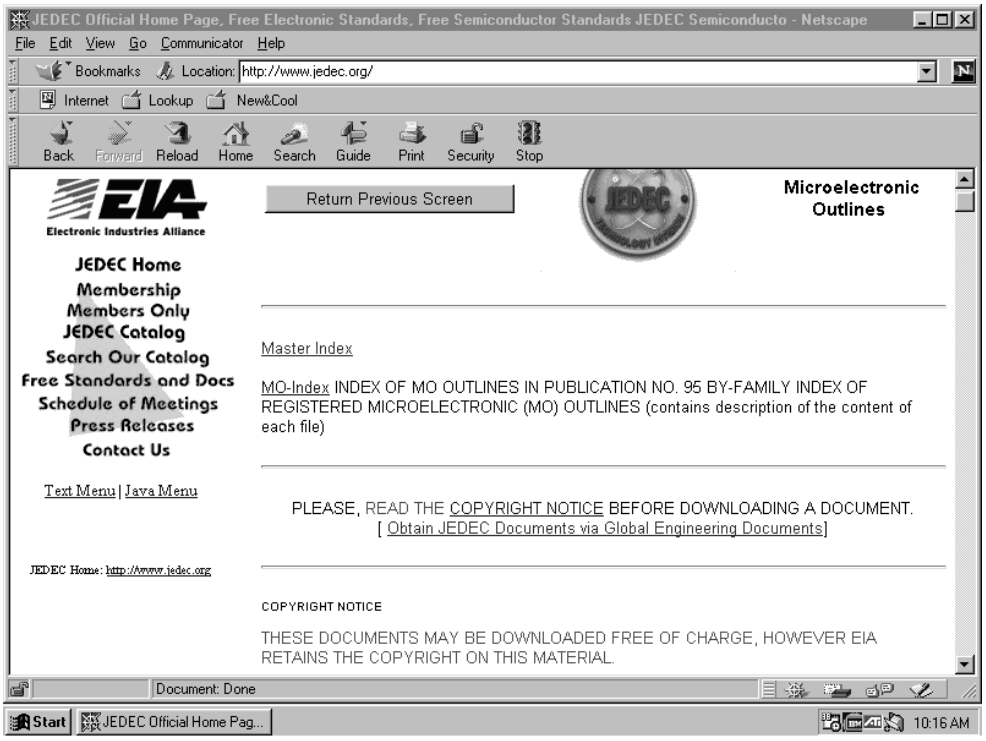


Figure 9. Microelectronic Outlines (MO)

From this screen, three basic choices are available.

1. Master Index is the same Pub-95 overall index as described earlier and shown in Figure 6. Scroll down to the list of MOs and look for BGA registrations. This is an undesirable choice because Adobe Acrobat must be activated just to display the index and then, after viewing the list, the reader must go through all the registrations to find the list of MOs. The drawings cannot be read directly.
2. Scrolling down the screen (see Figure 9) reveals a sequential numerical listing of MO registration outlines. The reader can click on the name of choice to view the drawing using Adobe Acrobat. This is a better choice, but still is not the most efficient method.
3. Selecting the MO-Index (see Figure 9) displays the By-Family Index of Registered Microelectronic Outlines (MO) in JEP-95 (see Figure 10).

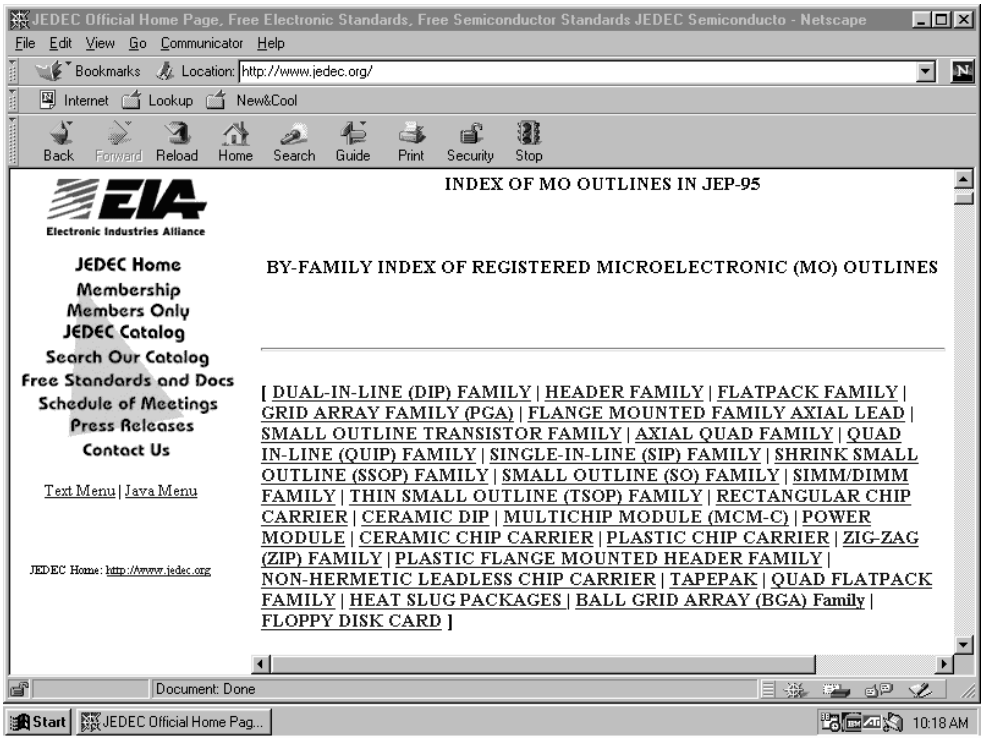


Figure 10. Index of MOs by Family

Selecting a package family name, in this case Ball Grid Array (BGA) Family, produces a screen of all outlines having this family description, both Registration MOs and Standard MSs. This, by far, is the most direct method to find similar package registrations for review (see Figure 11). To view a registration, select or click on the blue title.

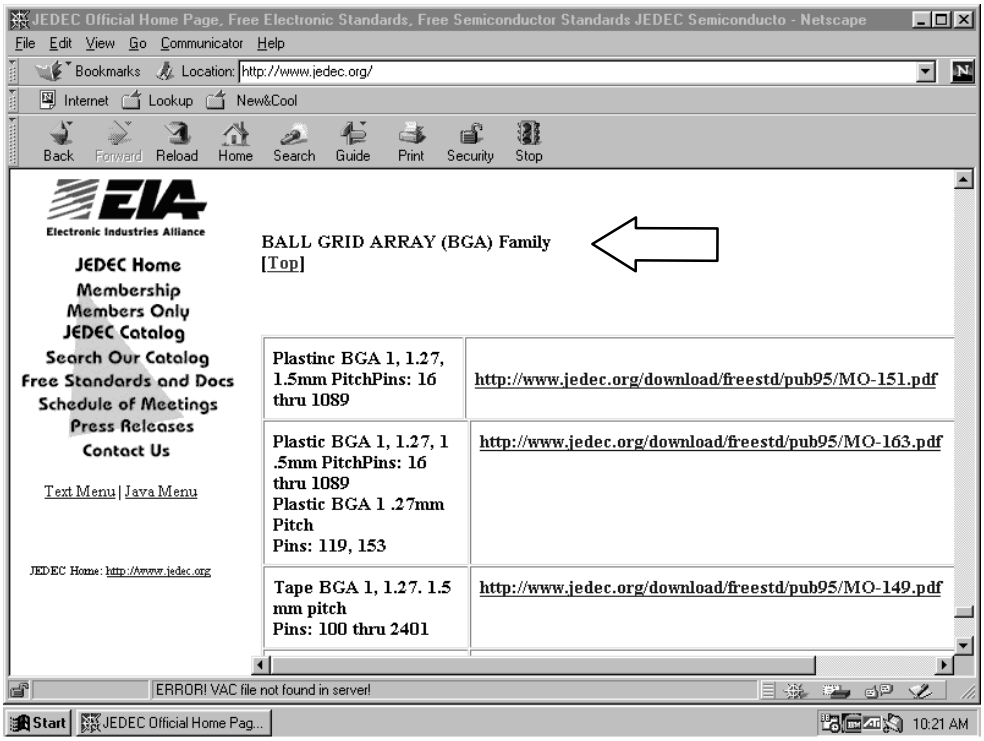


Figure 11. Listing of Ball Grid Array Registrations

In the future, search acronyms such as SSOP, QFP, and PDIP will be added to the web page. By knowing the type package, the reader can search quickly for a particular package type and screen out many by the name description.

Guides for Designers

Various Design Guides are located on the Pub-95 web page (see Figure 5). There also is a link to the IPC Package Land-Pattern Calculator.

Current Design Guides included in Pub 95-1 are:

Section 4:	Quad Flatpack
Section 10:	Generic Matrix Tray for Handling and Shipping
Section 11:	Dual Inline Plastic Family
Section 13:	Metric SOJ Package
Section 14:	Ball Grid Array Package
Section 16:	Fine-Pitch BGA (pending)

Summary

Pub-95 has been provided to member companies of JC-11 for many years. Access has been limited to committee members, alternates, or member companies willing to pay an added fee for additional copies. In the past, member-company employees had to contact the committee member to obtain information concerning package registration or registration details.

Today, anyone with web access can view a Registration or Standard and print a copy. The single most misunderstood factor with JC-11 is the difference in Registrations and Standards. This difference has been explained, and readers can now understand the difference and know how to find them efficiently by using the JEDEC web page.

Glossary

ASME	American Society of Mechanical Engineers
ASME Y14.5M-1994	Dimensioning and Tolerancing Standard endorsed by JC-11
BGA	Ball grid array package
EIA	Electronic Industries Alliance (formerly known as Electronic Industries Association)
EIAJ	Electronic Industries Association of Japan
GD&T	Geometric Dimensioning & Tolerancing drafting methodology endorsed by ASME Y14.5M-1994 and JC-11
IEC	International Electrotechnical Commission
JC-11	Committee Number 11 of JEDEC, with responsibility for establishing package-outline Registrations and Standards
JEB-xx	JEDEC Bulletin number xx
JEDEC	Joint Electron Device Engineering Council
JEDEC BOD	JEDEC Board of Directors (formerly known as the JEDEC Council)
JEDEC Standard 95-1	Section 4 of Pub-95, Design Guidelines
JEP-95	JEDEC Publication No. 95
Pub-95	Publication 95 of the JEDEC JC-11 committee
Registered	Package-outline drawing approved by the JC-11 committee
SOJ	Small-outline J-lead package
SPP	Standard Policies and Procedures of the JC-11 committee
Standard	JC-11 Registration that has attained wide use by the industry and now is recognized as an industry standard
TSSOP	Thin Shrink Small-Outline Package

Acknowledgment

John W. Yantis, P.E., is acknowledged as the author of this report. Sadly, John died in an accident prior to its publication.

John was a key contributor to TI's Logic Products packaging group for over 25 years and was a TI representative to the JEDEC JC-11 committee for packaging standardization. He was a key contributor to the JEDEC 95 Publication that this application report describes and also chaired the JC-11.10 subcommittee on Microelectronic Ceramic Packages and the JC-11.7 subcommittee on IEC Interface.

On behalf of John's family, friends, and colleagues, we acknowledge his extensive contributions in his practice of engineering and our pride in our association with him.

Bibliography

1. Publication No. 95, *Registered Outlines for Solid State and Related Products,* EIA, Arlington, VA, 1996.
2. ASME Y14.5M-1994, *Dimensioning and Tolerancing*, The American Society of Mechanical Engineers, New York, N.Y., 1995.
3. http://www.jedec.org, EIA-JEDEC, Arlington, VA, 1997

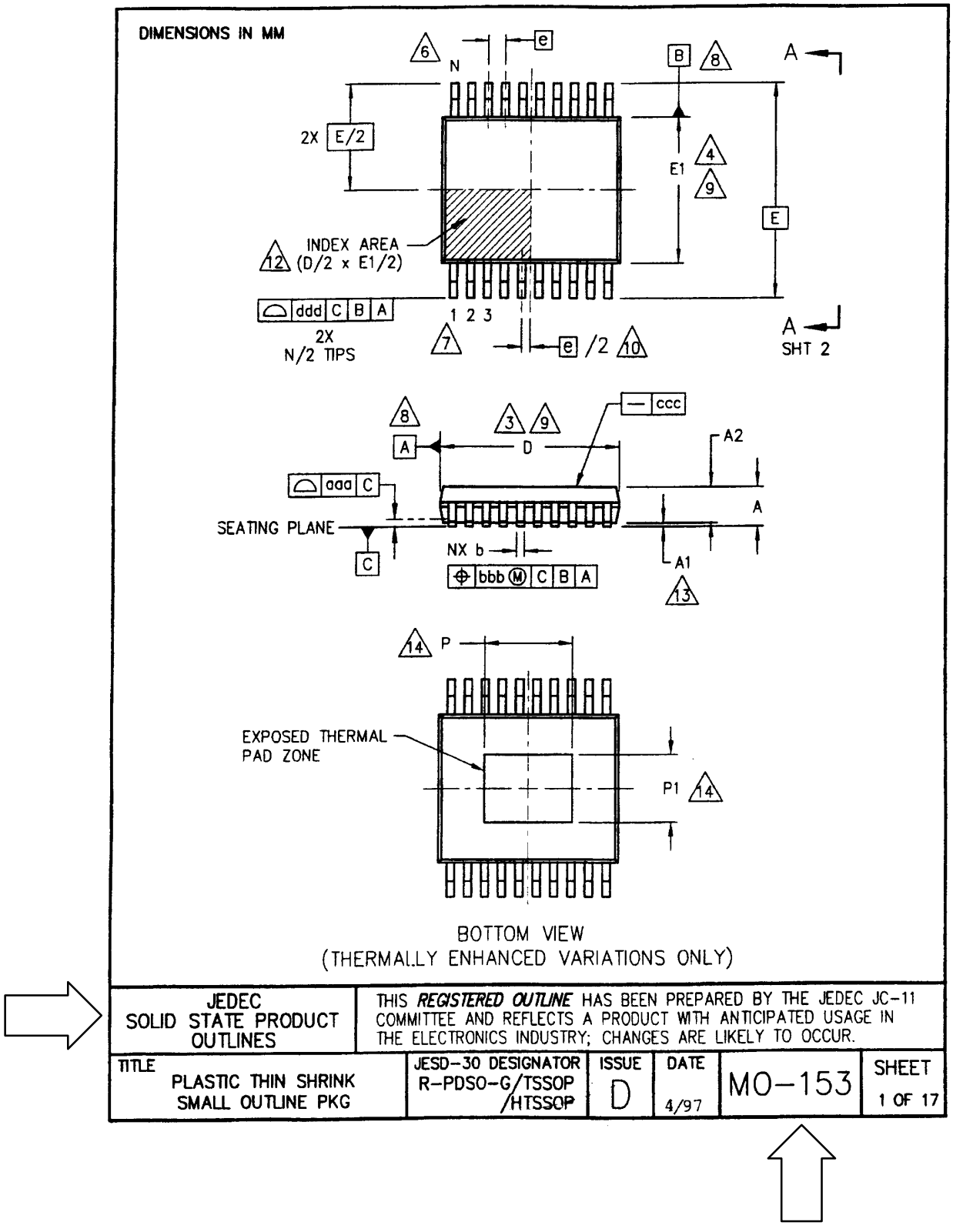


Figure A–1. Example of a Registered-Outline Drawing Top Sheet

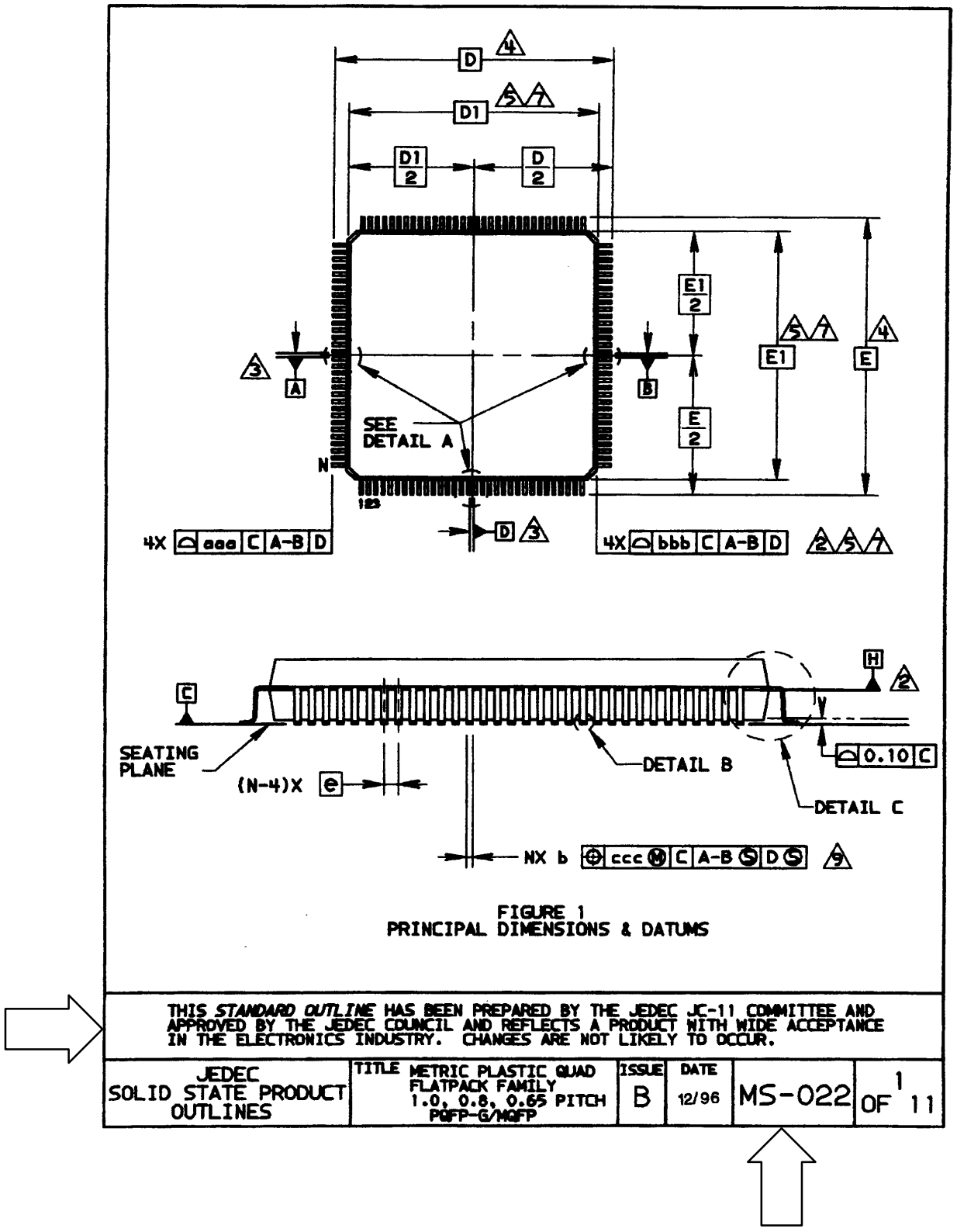


Figure A–2. Example of a Standard-Outline Drawing Top Sheet

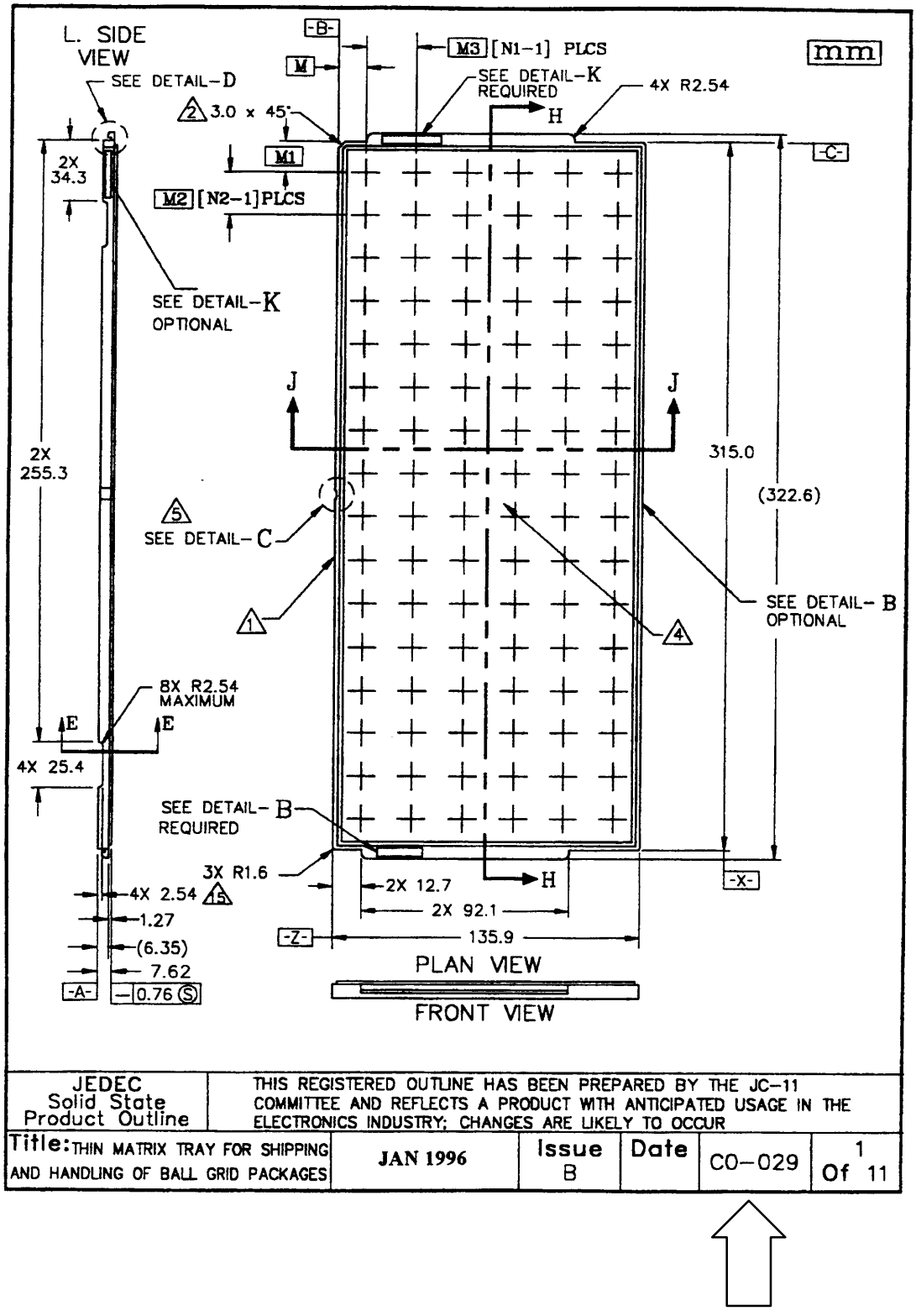
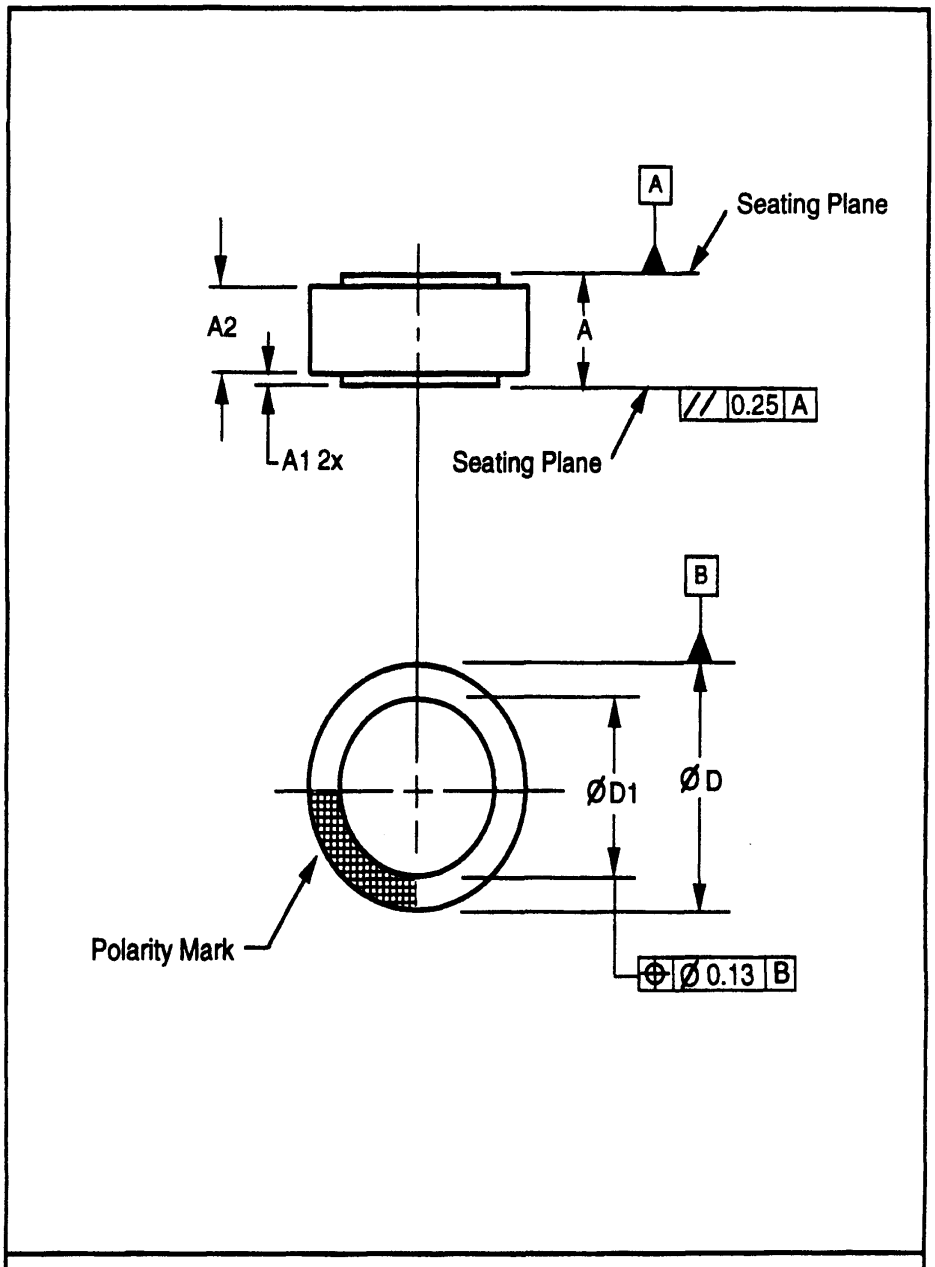


Figure A–3. Example of a Carrier Registered-Outline Drawing Top Sheet



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JEDEC SOLID STATE PRODUCT OUTLINES	TITLE: GADB-N Button Rectifier	ISSUE	DATE:		SHEET
		A	05-96	D0-217	1 OF 2

Figure A–4. Example of a Diode Registered-Outline (DO) Drawing Top Sheet

32-Bit Logic Families in LFBGA Packages:

96 and 114 Ball Low-Profile Fine-Pitch BGA Packages

SCEA014
October 1998

TEXAS INSTRUMENTS

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32-Bit Logic Families in LFBGA Packages:

96 and 114 Ball Low-Profile Fine-Pitch BGA Packages

Application Note

October 26th, 1998 by:

Sylvie Kadivar, Philips Semiconductors

Maria Balian, Texas Instruments

Ed Agis, Texas Instruments

Valentino Liva, Integrated Device Technology

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Contents

1 Introduction

With increasing systems and circuit complexity and the constant downward pressure on system prices, the requirements for bus interface solutions demand new approaches to system needs. One of the major challenges and goals of the digital processing industry is to continue decreasing the overall system costs as system complexity increases. Consequently, circuit integration and board miniaturization have become key words and key trends in present and future applications. A direct consequence of these trends is the need for wider bus interfacing. Today, as many networking, telecom and computer systems begin using DSP's and MPU's that require 32-bit, or even 64-bit wide interfacing, there is an increasing demand for 32-bit wide buffer, driver and transceiver functions. These new functions will become the standard in the years to come. To address evolving customer requirements, three suppliers, Integrated Device Technology, Philips Semiconductors and Texas Instruments have come together to define a package for 32-bit functions. Collectively Integrated Device Technology, Philips Semiconductors and Texas Instruments evaluated many customer inputs and identified a Low-Profile Fine-Pitch Ball Grid Array (LFBGA) package solution that would best serve customers' needs. Studies have shown that the LFBGA is an optimal solution for reducing the inductance, improving thermal performance and minimizing board real estate in support of integrated bus functions. Together, our objective is to provide multi-source products in a package that enables significant electrical improvements when compared to existing packages, as well as cost savings to the OEM manufacturing process. From a supplier standpoint, we can now guarantee the multi-sourcing of a package that will become the standard in the very near future.

The purpose of this document is to discuss the two new LFBGA solutions, the 96 and 114 ball LFBGA packages. Five 32-bit functions will initially be introduced in LFBGA package. Additional products will be manufactured per market interest and customer demand. A definition and description of the 96 and 114 ball LFBGA packages are discussed in this application note. Content and technical exhibits from the application note should be used to develop PCB layouts using the 96 and/or 114 ball LFBGA packages. Examples of routing, layout and mechanical dimensions are also included in this document. The initial introduction of the 32-bit logic is noted in the table below:

	Number of Balls			
LVCH Functions	Package	GND	V_{CC}	No Connection
74LVCH32244	96	16	8	NA
74LVCH32245	96	16	8	NA
74LVCH32373	96	16	8	NA
74LVCH32374	96	16	8	NA
ALVCH Function				
74ALVCH32501	114	16	8	2

Table 1.1 – Initial 32-Bit Functions

LFBGA packages offer lower inductance and parasitic capacitance than any other TSSOP, TVSOP and MillipaQ™ packages. The LFBGA package characteristics supports improvements in ground bounce, V_{CC} undershoot, pin-to-pin skew, and signal propagation delay of 20 to 50 ps.

The definition of these two packages in terms of standardization, both physical and mechanical, was developed by Integrated Device Technology, Philips Semiconductors and Texas Instruments to provide the industry pin out compatible solutions.

2 Examples of Applications with LFBGA Packages

2.1 Industry Expressed Requirements for 32-Bit Logic

With the growing trend towards increased bus widths, OEMs are looking to consolidate logic functions in an effort to effectively make use of board real estate. This requirement from customers is prevalent across many end equipments. The requirement to reduce board real estate also necessitates a packaging solution, which integrates logic as well as addresses improved thermal packaging characteristics in addition to minimizing pin-to-pin skew. The selection of the 96 and 114 Ball LFBGA addresses all of these careabouts with improved performance and standardization of pin outs agreed upon by Integrated Device Technology, Philips Semiconductors and Texas Instruments. In the initial 8 month study, consisting of 15 OEMs and several worldwide subcontractors, we found that the preferred pitch for introducing logic in either the LFBGA is a 0.8 mm with a 0.5 mm ball diameter. Both packages are being offered by Integrated Device Technology, Philips Semiconductors and Texas Instruments to support customer requirements and enable easier PCB design/layout along with a more robust solder joint based on life cycle studies.

While other solutions were looked at such as staggered depopulated balls, with a smaller pitch, as well as, a smaller ball diameter, none were considered suitable to address the current market needs for OEM's and the subcontractors. The LFBGA packages selected by IDT, Philips Semiconductors and Texas Instruments is the optimal solution as it addresses our current customer needs. More details for package comparison are noted within the other subsections of this application note.

2.2 Customer Needs and Problems Targeted

Workstations:

- Workstation buses extend to 128-, 256-bit, or wider bus structures
- Require denser and faster logic products

PCs:

- The trend is to integrate as much logic as possible into fewer packages
- Due to space constraint, PC Cards require dense integration and small package foot-prints
- PCI bus structures may require 5-V tolerance, in addition to integrating logic circuits

Datacommunication:

"Intelligent" routers and switches require more logic to support interfaces and build real time lookup tables for routing addresses with statistics.

Telecommunication:

- Base stations are becoming small and ubiquitous requiring the repackaging of many circuits into dense boards
- New complex and smaller equipment must interface with legacy equipment.

2.3 Application Examples

- PC Motherboards
- Data communications
- Telecommunications
- Back Planes
- Base stations
- Cellular and cordless telephone

2.4 Existing or Alternative Solutions: A Comparison

While other packages have been introduced to address integrated logic solutions, these packages have only had limited success, such as the 100-pin TQFPs or the 80/96-pin MillipaQ™. As a comparison, these two solutions have a reduce number of ground and V_{CC} pins leading one to believe that ground bounce and pin-to-pin skew cannot be optimally designed to address these design issues.

Comparisons of the foot print space show that the 100-pin TQFP and 80/96-pin MillipaQ™ packages takes up respectively 245% and 66% more area than the corresponding 96 ball LFBGA. For further details refer to tables 2.1 and 2.2.

The 96 ball LFBGA package provides an optimal area/bit ratio and improved pin-to-pin skews. Pin-to-pin skew is minimized by the number of pin signals connected to the same ground connection.

Package	Footprint Area (mm^2)	Area/Bit (mm^2)	Weight (g)	Total # of Balls or Pins
LFBGA-96	74.25	2.32	0.132	96
MillipaQ™ 80/96 pin	123.0	3.84	0.332	80/96
2 x TVSOP 48 pin	132.5	4.14	0.227	96
2 x TSSOP 48 pin	213.0	6.66	0.383	96
2 x SSOP 48 pin	342.0	10.7	1.180	96
TQFP 100 pin	256.0	8.00	0.660	100

Note 1: The Area/Bit is computed for 32 bits and assumes a 1.3 mm PCB spacing for two-package solution.
Note 2: The MillipaQ™ offers 32-bit logic functions with reduced ground and V_{CC}'s; such configuration compromises the signal integrity of the logic functions.

Table 2.1 – Comparison of Foot Print Size with LFBGA-96

Package	Footprint Area (mm^2)	Area/Bit (mm^2)	Weight (g)	Total # of Balls or Pins
LFBGA-114	88.00	2.44	0.167	114
2 x TVSOP 56 pin	153.0	4.25	0.271	112
2 x TSSOP 56 pin	237.3	6.59	0.423	112
2 x SSOP 56 pin	394.6	11.0	1.360	112
TQFP 120 pin	256.0	7.11	0.660	120

Note 1: The Area/Bit is computed for 36 bits and assumes a 1.3 mm PCB spacing for two-package solution.

Table 2.2 - Comparison of Foot Print Size with LFBGA-114

3 Package Descriptions

Figure 3.1 shows a cross section of the LFBGA package.

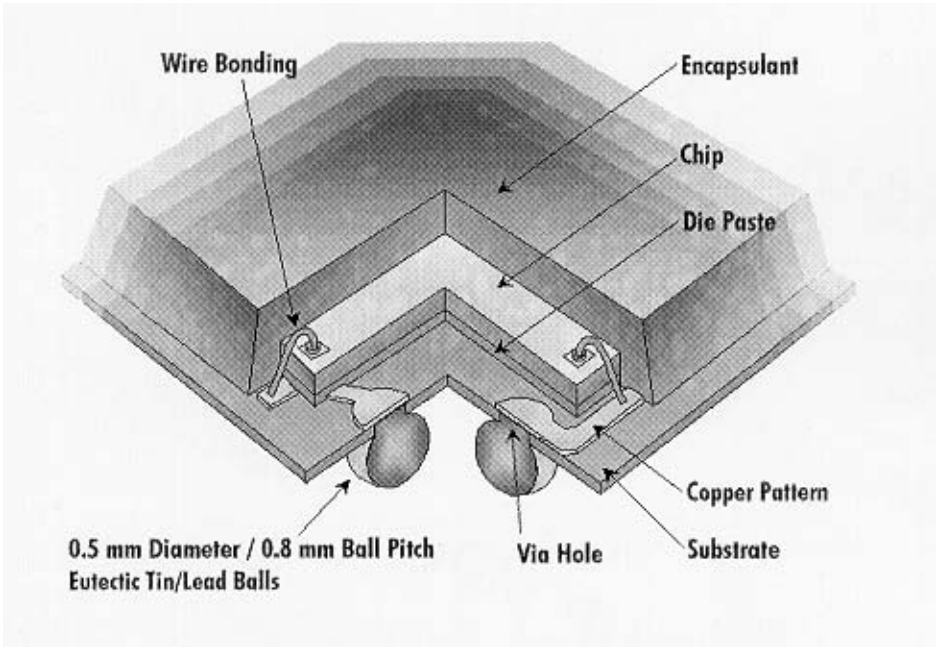


Figure 3.1 - LFBGA Cross Section

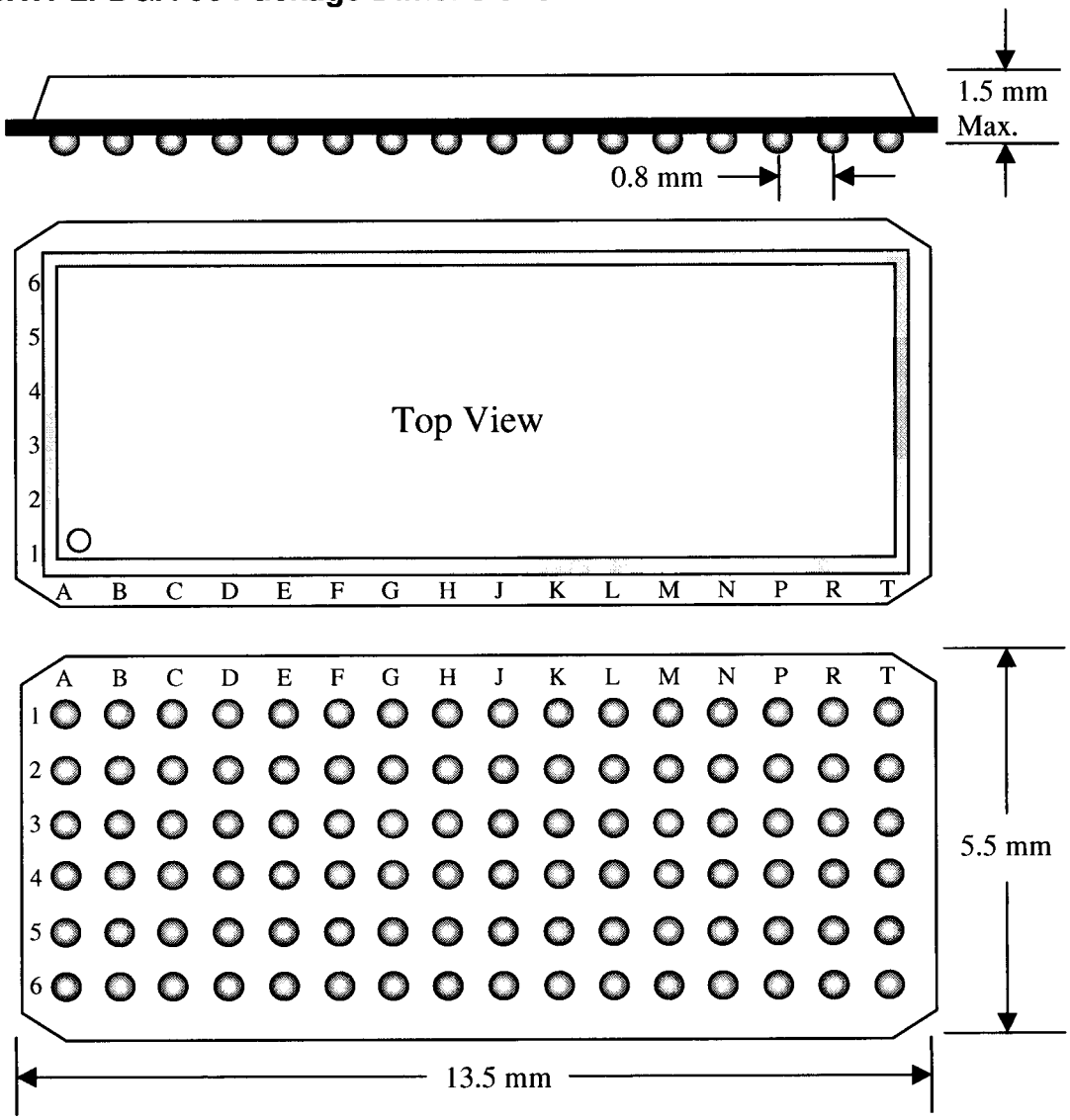
Table 3.1 summarizes the package attributes for the LFBGA.

	LFBGA-96	LFBGA-114
Ball count	96	114
Ball configuration (rows, columns)	6 x 16	6 x 19
Square/Rectangular	R	R
Ball-to-ball pitch (mm)	0.8	0.8
Ball diameter (mm)	0.5	0.5
Package body width (mm)	5.5	5.5
Package body length (mm)	13.5	16
Package thickness (mm)	1.2 min – 1.5 max	1.2 min –1.5 max
Package weight (mg)	132	167
Shipping media tape & reel (units)	1000	1000
Desiccant pack	Level 3	Level 3

Table 3.1 – LFBGA Package Attributes

3.1 LFBGA Package Characteristics

3.1.1 LFBGA-96 Package Dimensions



Ball organization: 6 x 16 = 96 balls; grid = 0.8 mm;
Footprint: 74.25 mm^2

Figure 3.2 - LFBGA-96 Package Layout

Advantages:

- Industry accepted 0.8 mm pitch industry standard; easy pad-via-to-ball routing
- Easy customer PCB layout; easy to locate near connectors
- Robust solderability due to standard 0.5 mm ball size

LFBGA-96 Pin Out Configuration:

Note: The pin out configuration below adopts the same naming convention applied in the industry to logic devices in 48-pin packages (i.e. TSSOP, SSOP, TVSOP).

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T
6	A46	A43	A40	A37	A35	A32	A29	A27	B46	B43	B40	B37	B35	B32	B29	B27
5	A47	A44	A41	A38	A36	A33	A30	A26	B47	B44	B41	B38	B36	B33	B30	B26
4	A48	A45	A42	A39	A34	A31	A28	A25	B48	B45	B42	B39	B34	B31	B28	B25
3	A1	A4	A7	A10	A15	A18	A21	A24	B1	B4	B7	B10	B15	B18	B21	B24
2	A2	A5	A8	A11	A13	A16	A19	A23	B2	B5	B8	B11	B13	B16	B19	B23
1	A3	A6	A9	A12	A14	A17	A20	A22	B3	B6	B9	B12	B14	B17	B20	B22

Gnd Vcc Control

Note: This is a topside view

Figure 3.3 – Top View Pin Assignment

Electrical:

The electrical parameters of a package are dependant upon parasitic elements, which include inductance, capacitance, and electrical or propagation delays throughout the package. The following values summarize the nominal parasitic components of the LFBGA-96 package: self inductance 2.2nH, pin-to-ground capacitance 0.2pF. One should note that the reported values for the LFBGA package are about 35% better than the TVSOP package and greater that 50% compared to the TSSOP package. Overall the LFBGA package is better than any existing industry standard package on the market today.

Figure 3.4 provides an electrical comparison of the LFBGA-96 with other industry standard packages.

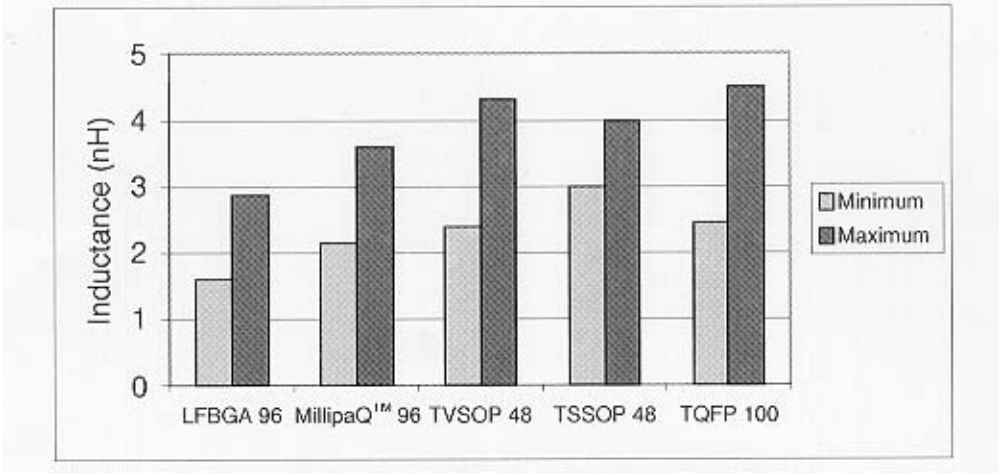
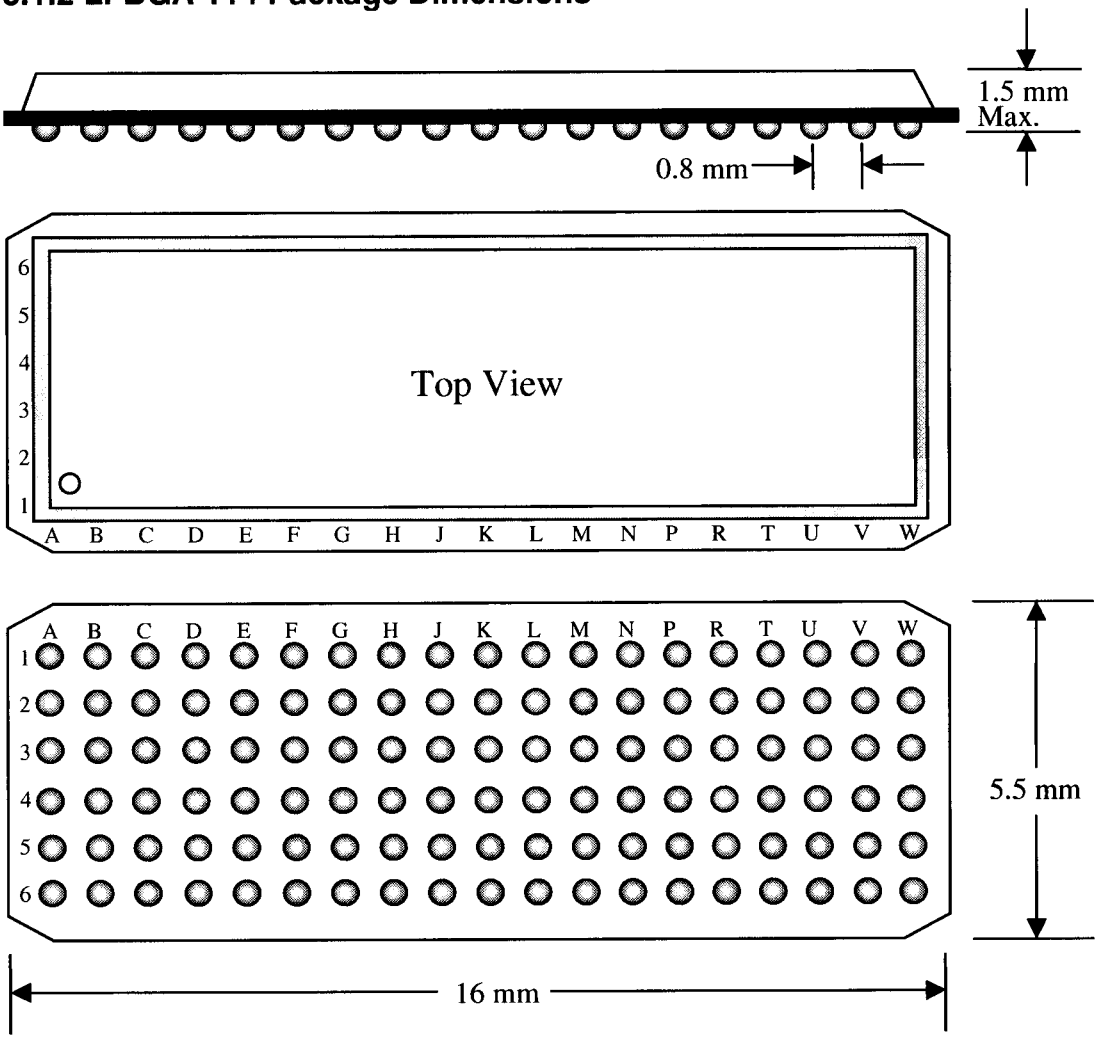


Figure 3.4 - Electrical Comparisons

3.1.2 LFBGA-114 Package Dimensions



Ball organization: 6 x 19 = 114 balls (112 used); grid = 0.8 mm;
Footprint: 88 mm^2

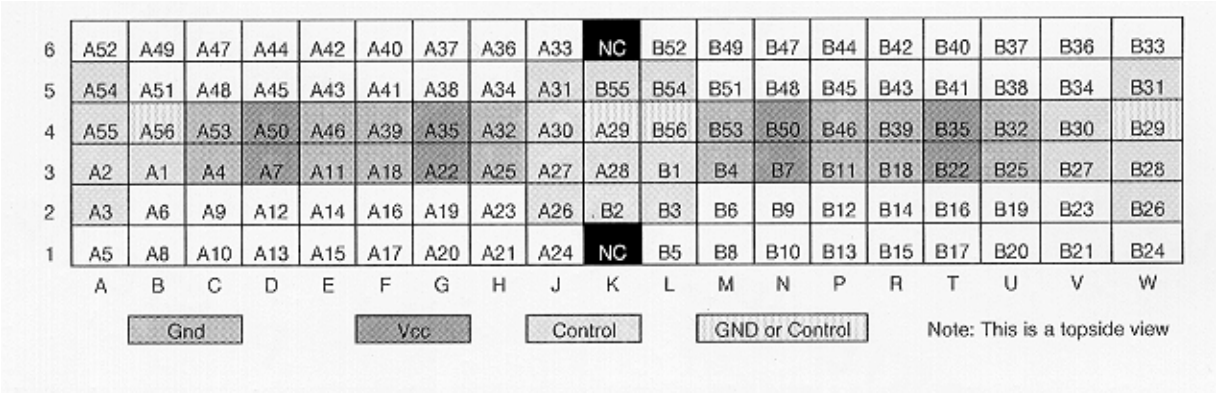
Figure 3.5 - LFBGA-114 Package Layout

Advantages:

- Industry accepted 0.8 mm pitch; easy pad-via-to-ball routing
- Easy customer PCB layout; easy to locate near connectors
- Robust solderability due to standard 0.5 mm ball size

LFBGA-114 Pin Out Configuration:

Note: The pin out configuration below adopts the same naming convention applied in the industry to logic devices in 56-pin packages (i.e. TSSOP, SSOP, TVSOP).



	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U	V	W
6	A52	A49	A47	A44	A42	A40	A37	A36	A33	NC	B52	B49	B47	B44	B42	B40	B37	B36	B33
5	A54	A51	A48	A45	A43	A41	A38	A34	A31	B55	B54	B51	B48	B45	B43	B41	B38	B34	B31
4	A55	A56	A53	A50	A46	A39	A35	A32	A30	A29	B56	B53	B50	B46	B39	B35	B32	B30	B29
3	A2	A1	A4	A7	A11	A18	A22	A25	A27	A28	B1	B4	B7	B11	B18	B22	B25	B27	B28
2	A3	A6	A9	A12	A14	A16	A19	A23	A26	B2	B3	B6	B9	B12	B14	B16	B19	B23	B26
1	A5	A8	A10	A13	A15	A17	A20	A21	A24	NC	B5	B8	B10	B13	B15	B17	B20	B21	B24

Gnd Vcc Control GND or Control Note: This is a topside view

Figure 3.6 – Top View Pin Assignment

Electrical:

The electrical parameters of a package are dependent upon parasitic elements, which include inductance, capacitance and electrical propagation delays throughout the package. One should note that the reported values for the LFBGA-114 package are about 35 % better than the TVSOP package and greater than 50 % compared to the TSSOP package. Overall the LFBGA packages are better than any existing industry standard package on the market today.

3.1.3 LFBGA Power Dissipation

The power dissipation of LFBGA is very much dependent upon the thermal conduction paths between the chip and the printed circuit board (PCB). The 96 and 114 ball LFBGA package outline is small, thereby limiting the amount of power dissipation due to convection or radiation, so the PCB becomes the major heat source for the package. The thermal performance of the packages is good when the chip overlaps the solder balls due to the fact that the balls under the chip act as thermal conduction paths to the PCB. The thermal resistance of LFBGA packages is 35% better than the TVSOP package and 30% better than the TSSOP package.

A well-designed PCB board further enhances the power dissipation of both LFBGA packages. By adding thermal vias (i.e via from the solder ball to the top buried ground plane), a significant benefit of 15 to 20% is obtained over existing PCB designs.

Note: The maximum power dissipation is calculated using a junction temperature of 150°C.

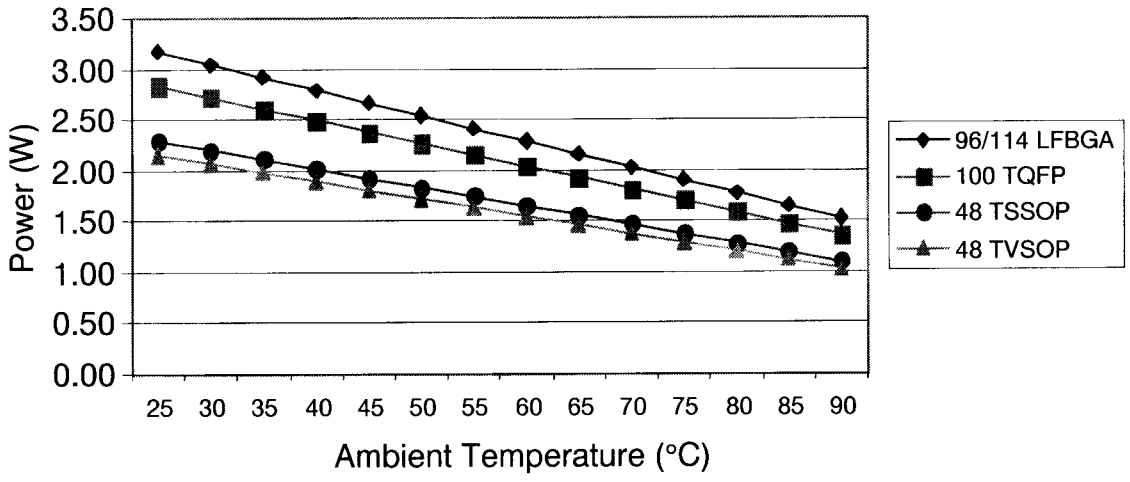
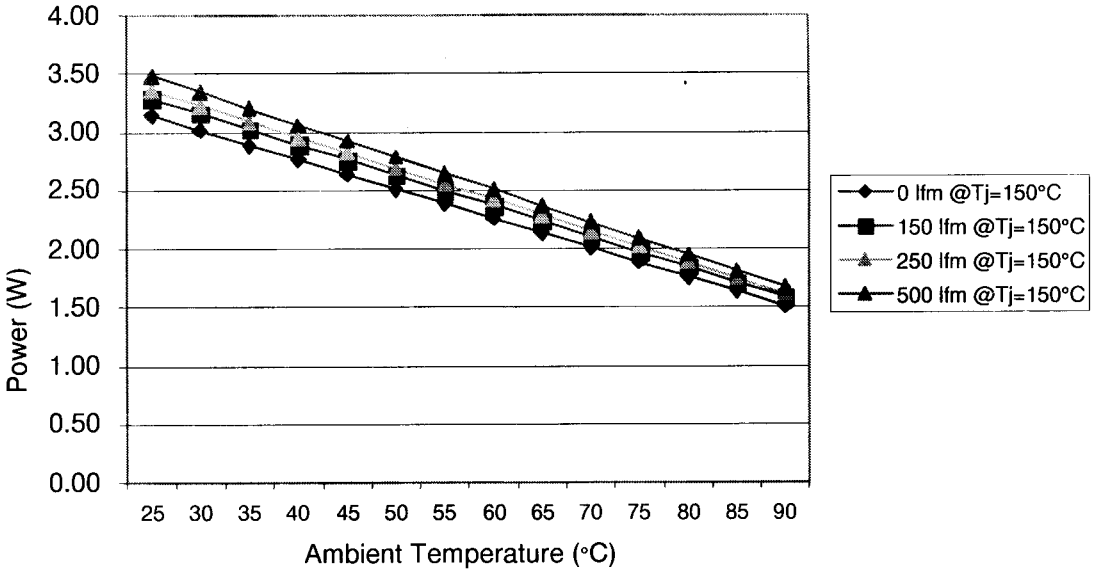


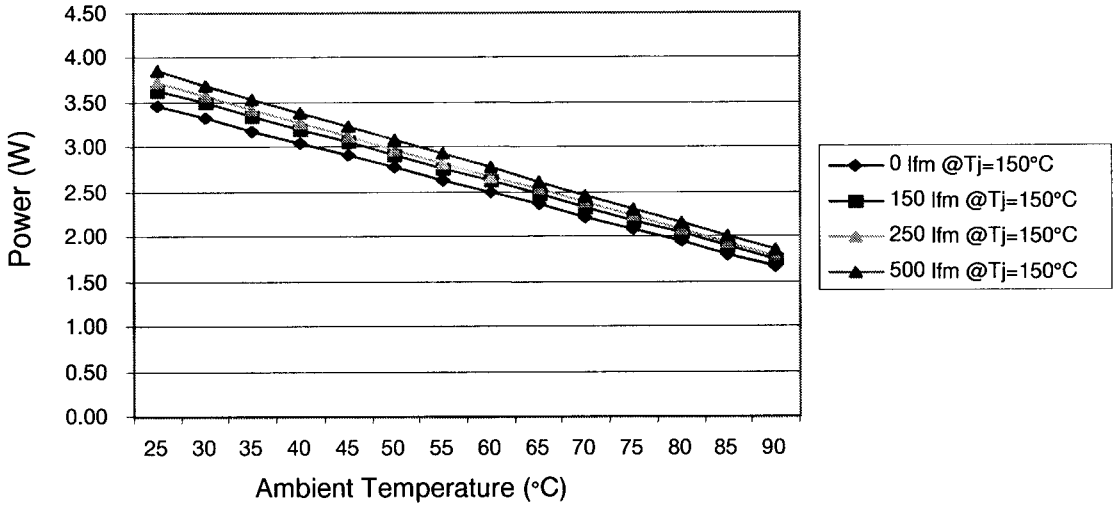
Figure 3.7 - Thermal Comparisons on Multi-Layer JEDEC Board



Note: The maximum power dissipation is calculated using a junction temperature of 150°C.

Air Velocity (ft/min)	0	150	250	500
θ_{JA} (°C/W)	39.8	38.0	37.2	35.9

Figure 3.8 – LFBGA Thermal Derating Curves without Thermal Vias Using Multilayer JEDEC Board



Note: The maximum power dissipation is calculated using a junction temperature of 150°C.

Air Velocity (ft/min)	0	150	250	500
θ_{JA} (°C/W)	36.1	34.4	33.6	32.5

Figure 3.9 – LFBGA Thermal Derating Curves with Thermal Vias Using Multilayer JEDEC Board

3.2 LFBGA vs. TVSOP, TSSOP, and MillipaQ™ footprint

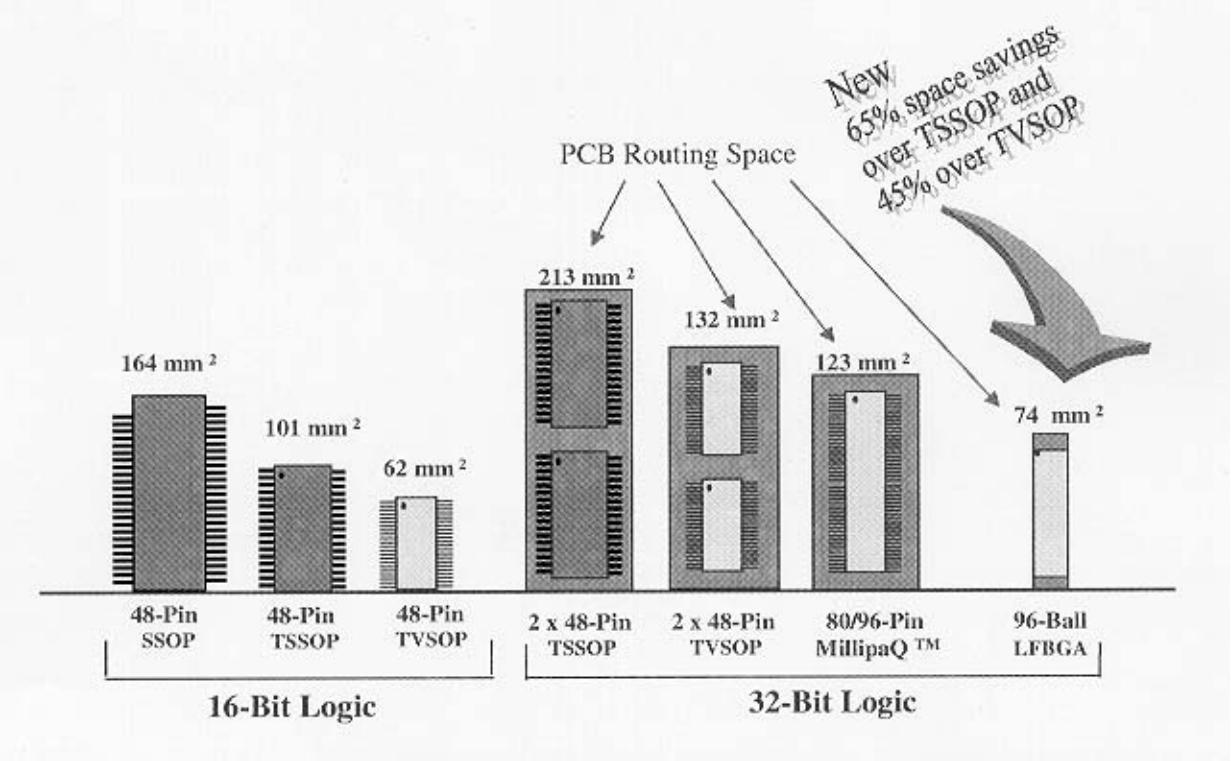


Figure 3.10 – Package Comparisons

Comparison of the normalized thermal dissipation for the TSSOP, TVSOP, and the LFBGA-96 shows that the LFBGA-96 with thermal vias exceeds by a factor of 2 the capability of 2 x 48 TSSOP packages.

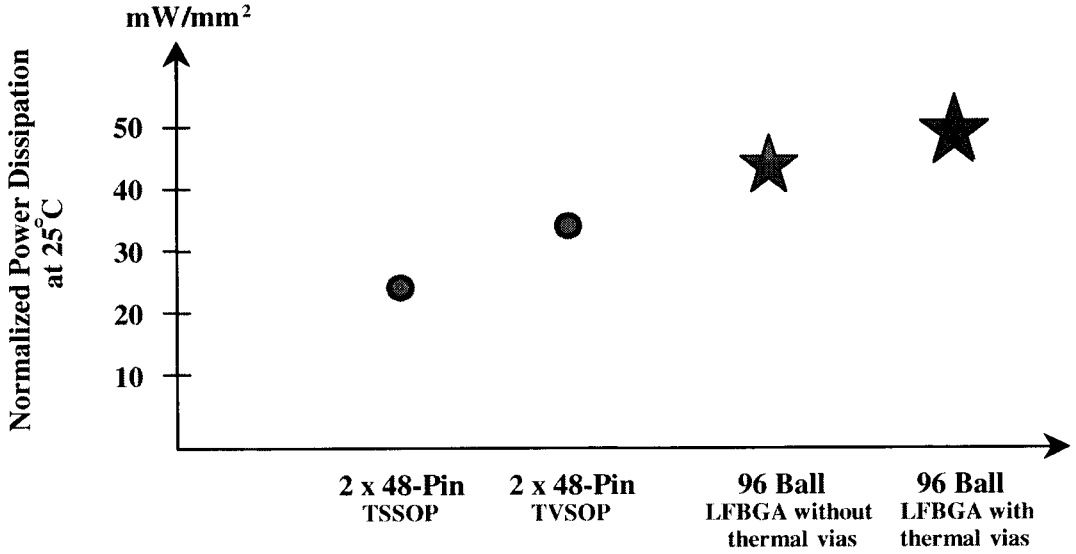


Figure 3.11 – Normalized Power Dissipation at 25°C

Note: Calculations are based on the data from figure 3.7 and figure 3.10.

3.3 Benefits to the Customer

The following table summarizes key features and corresponding benefit for logic products assembled in LFBGA packages.

Feature	Benefit
Offer the minimum foot print to industry	Uses the smallest real estate among industry standard packages. Cost savings for PC boards.
Minimize the skew parameter	Provides the user with a reliable solution in new faster bus configurations.
Minimize package propagation delay	Provides the user with additional design margin in high speed buses.
Rise time and fall time is 1ns typical	Again, t_r and t_f are optimized to meet good duty cycle at 100 MHz and 133 MHz while keeping the ground bounce under 500 mV.
Lower ground bounce	Allows more noise margin.
Selected as a JEDEC standard package	Meet mechanical and electrical specifications define by the IDT/Philips/TI working group. Can use 2.5V or other special supply from 2.5 to 3.3V.
No external components other than bypass capacitors	Low cost, low maintenance, better reliability.
Supports/enables high speed applications	LFBGA packages has less capacitance pin-to-pin inductance and ground inductance. This provides better support for high-speed applications.

Table 3.2 – Feature/Benefits of LFBGA Packages

3.4 Contribution to JEDEC Definition

The 96 and 114 ball LFBGA packages have received JEDEC (Joint Electronics Device Engineering Council) JC-11 under semiconductor package standard MO-205 and EIAJ (Electronic Industry Association Japan) registration. IDT, Texas Instruments and Philips Semiconductors have also submitted to JEDEC a proposed 96 and 114 ball LFBGA pin-out to the JC-40 council and final voting by JEDEC participants is expected by the end of 1998.

3.5 Evaluation Units

For evaluation units, contact authorized distributors or for more information refer to the following URLs:

Integrated Device Technology URL: http://www.idt.com
Philips Semiconductors URL: http://www.philipslogic.com
http://www.semiconductors.philips.com/logic
Texas Instruments URL: http://www.ti.com/sc/lfbga

4 LFBGA Package Marking, Shipping Media and Handling

The following section describes the symbolization of these new LFBGA packages.

4.1 Marking

Integrated Device Technology, Philips Semiconductors and Texas Instruments use laser marking to identify the vendor, product number, year and month of fabrication, manufacturing site, lot trace code. Each vendor adopted a specific package designator for the LFBGA packages and is reported in table 4.1:

	Integrated Device Technology	Philips Semiconductors	Texas Instruments
LFBGA-96	BF	GKE	GKE
LFBGA-114	BF	GKF	GKF

Table 4.1 – Vendor Package Designator

Marking examples for the LVCH32244 device:

IDT Marking:
Part #: LVCH322244A
Date Code, Marking Location
Lot number, Assembly Location

Logo	LVCH32244A
	X9848Y
O	Xmax10xX

Texas Instruments Marking:
Part #: CH244A
Year, Month, Site
Lot trace code

Logo	CH244A
	YMS
O	LLLL

Philips Semiconductors Marking:
Part #: LVCH32244A
Lot number, Site
Date Code

Logo	LVCH32244A
	Lot Trace
O	YYWW

Device Name	Integrated Device Technology	Philips Semiconductors	Texas Instruments
LVCH32244A	LVCH32244A	LVCH32244A	CH244A
LVCH32245A	LVCH32245A	LVCH32245A	CH245A
LVCH32373A	LVCH32373A	LVCH32373A	CH373A
LVCH32374A	LVCH32374A	LVCH32374A	CH374A
ALVCH32501	ALVCH32501	ALVCH32501	ACH501

Table 4.2 – Vendor Part Number Marked on Top of Package

4.2 Tape & Reel

The embossed Tape & Reel method is preferred by automatic pick-and-place machines. Integrated Device Technology, Philips Semiconductors and Texas Instruments offer Tape & Reel packaging for the 96 and 114 ball LFBGA packages. The packaging materials used include Carrier Tape, Cover Tape and a Reel. All material used meets industry guidelines for ESD protection and the design is in full compliance with EIA Standard 481-A, "*Taping of Surface Mount Components for Automatic Placement.*" The dimensions that are of interest to the end-user are tape width (W), pocket pitch (P) and quantity per reel. The figure below illustrates the Tape & Reel design for LFBGA package.

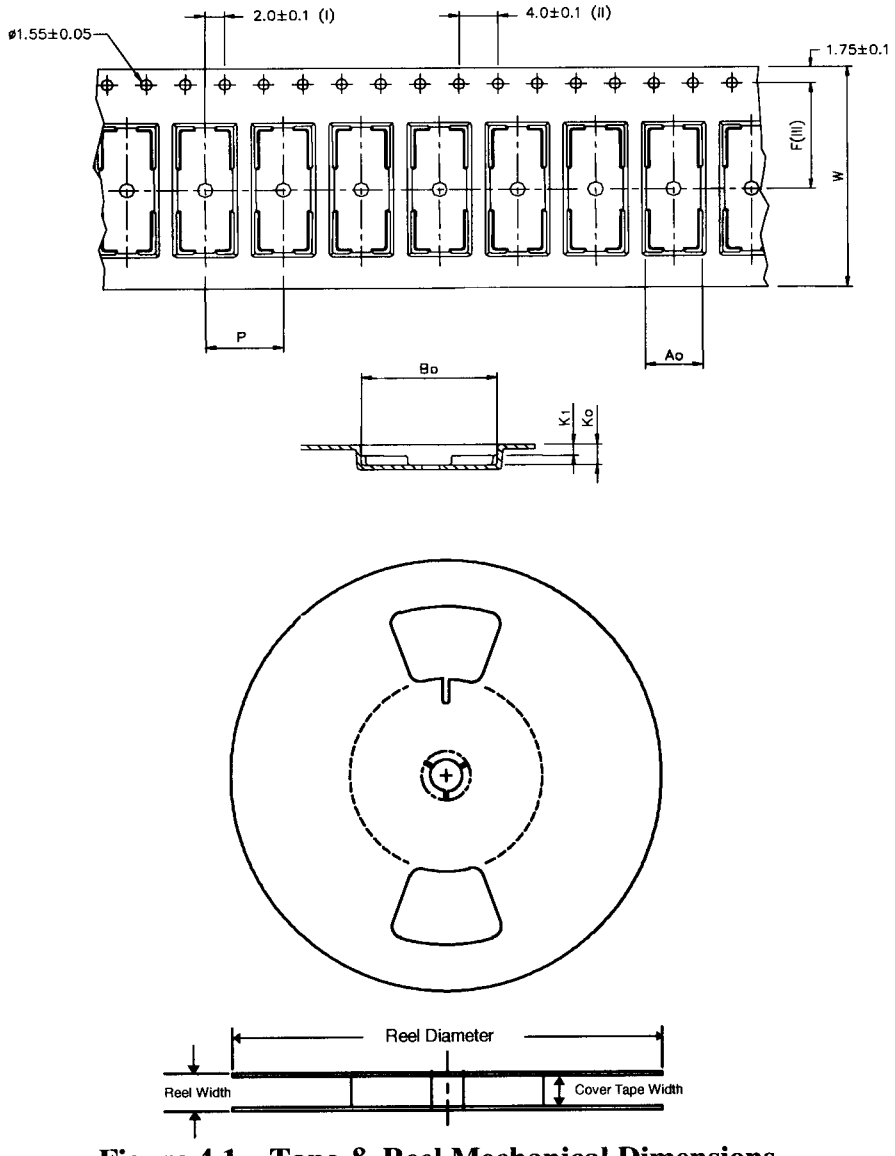


Figure 4.1 – Tape & Reel Mechanical Dimensions

Package	Cover Tape Width (W)	Pocket Pitch (P)	Reel Width	Reel Diameter	Quantity Per Reel
LFBGA-96	21.0	8.00	24.0	330	1000
LFBGA-114	21.0	8.00	24.0	330	1000

Table 4.3 – Tape & Reel Assembly Information

Package	Pocket Width (A_0)	Pocket Length (B_0)	Pocket Depth (K_0)	Pedestal Depth (K_1)	Hole to Pocket Centerline (F)
LFBGA-96	5.7	13.7	2.0	1.2	11.5
LFBGA-114	5.7	16.2	2.0	1.2	11.5

All dimensions are in millimeters

Table 4.4 – Tape & Reel Dimension for LFBGA Package

4.3 Sockets, and Socket Manufacturer (Ordering Information)

Yamaichi Socket numbers: LFBGA-96 PN# IC280-096-144
LFBGA-114 PN# IC280-114-145

Yamaichi Electronics USA, Inc.
2235 Zanker Road
San Jose, CA 95131 *Tel: (408) 456-0797*

Loranger Socket numbers: LFBGA-96 PN# 135055096U6617
LFBGA-114 PN# 169055114U6617

Loranger International Corp.
817 Fourth Avenue
Warren, PA 16365 *Tel: (814) 723-2250*
California Contact Office *Tel: (408) 727-4234*

5 PCB Manufacturing Considerations

The following section describes the assembly on PCBs of the LFBGA products.

5.1 Land Pads

The design of the land pads for LFBGA packages on the printed circuit board is critical, if the end-user wants to achieve good manufacturability and optimum reliability. An optimum design is when the diameter of the land pad is equal to the diameter of the package vias; (i.e. the fatigue life of the solder balls is enhanced when the ratio of these dimensions is equal to 1.0).

There are two methods of defining land pads on PCB – *solder mask defined* and *non-solder mask defined*. In the *solder mask defined*, the desired land area is defined by the opening of the solder mask. The advantage of this technique is that the land pad size is controlled and the solder mask promotes the adhesion of the copper pad to the PCB. However, the copper pad dimension is larger which makes routing more difficult. In the *non-solder mask defined*, the land area is etched inside the solder mask area. The final land pad dimension is dependent on the accuracy of the copper etching method. The advantage of *non-solder mask defined* over the *solder mask defined* methods is routability (it allows larger trace width/spacing between the solder balls). Figure 5.1 illustrates the land pad dimension for the 96 and 114 ball LFBGA package using the solder mask defined and non-solder mask defined method.

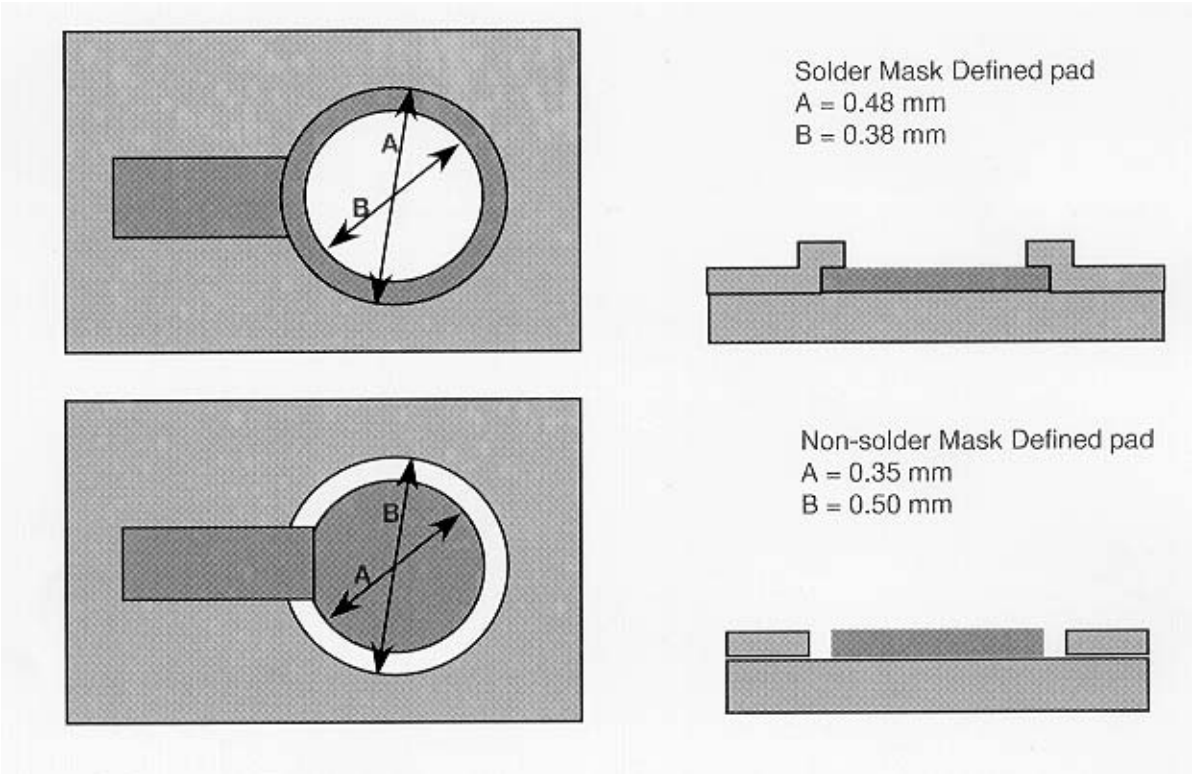


Figure 5.1 – LFBGA Recommended Land Pad Design

5.2 Line and Spaces

This section describes the maximum trace width/spacing dimension allowed for 0.8mm ball pitch LFBGA packages with 0.5 mm ball diameter. It becomes a challenge to the designers to route this package on a single layer board unless the PCB supplier has fine pitch trace width/spacing capabilities. PCB capabilities are currently in the 4 to 5 mil (100 – 125 µm) trace width/spacing range and using a finer pitch trace width/spacing will increase the overall PCB cost to the end-user. The optimum design is to use current PCB capability, which allows one signal to be routed between the land pads. Using the recommended land pad dimension outlined in section 5.1, the PCB supplier needs to have trace width/spacing capabilities of 4.2 mil (107 µm) and 5.9 mil (150 µm) respectively for the solder mask and non-solder mask defined pads.

Figure 5.2 represents a visual layout as described in section 5.2 and 5.3.

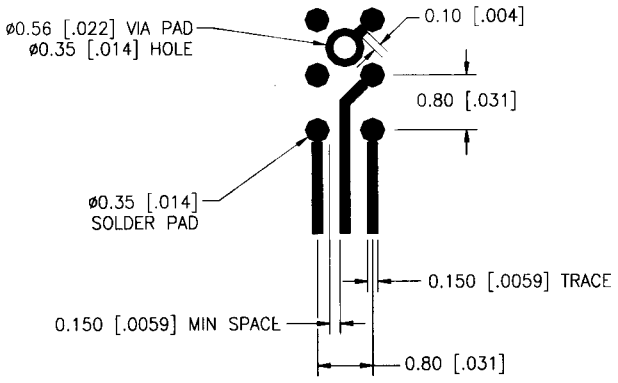


Figure 5.2 – LFBGA Trace Width/Spacing Dimensions (mm)

5.3 Vias

Via density can be just as challenging to the designers when routing a high-density board. Via density is defined as the number of vias in a particular board area. Using smaller vias increases the via density and the routability of the board by requiring less board space. Holes can be mechanically drilled down to 6 mil (152 µm), however, mechanically drilled holes less than 12 mil (305 µm) begin to add cost to the PCB. To avoid higher PCB costs, other via technology exist (such as laser, punched and plasma-etched) and can be used to form smaller holes. The invention of the micro-via has solved many of the problems associated with via density. Micro-vias are often created using a plasma-etched technique, which penetrates layers of dielectric and allows signal routing to the internal layers. Current micro-via technology allows a 2.4 to 4.0 mil (60 – 100 µm) via diameter. Micro-vias can also be designed directly into the land pad thereby obsoleting trace fan-outs.

Table 5.1 summarizes the maximum via diameter that can be used for routing the LFBGA package using recommended land pad dimensions outlined in section 5.1.

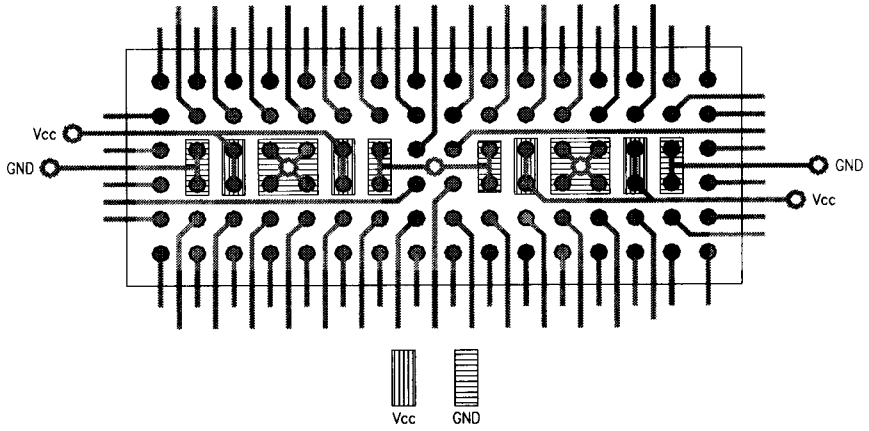
	Solder Mask Defined Land Pad	**Non-solder Mask Defined Land Pad**
Trace width/spacing	0.107 mm (4.2 mil)	0.150 mm (5.9 mil)
Drill bit diameter	0.23 to 0.25 mm (9 to 10 mil)	0.35 to 0.38 mm (14 to 15 mil)
Unplated hole	0.23 to 0.25 mm (9 to 10 mil)	0.35 to 0.38 mm (14 to 15 mil)
Finished via size (plated)	0.178 to 0.2 mm (7 to 8 mil)	0.30 to 0.33 mm (12 to 13 mil)

Note: Unplated via diameter assumes a 0.2 mm (8 mil) via land dimension and a 0.1 mm (4 mil) clearance between the via land to the adjacent land pad.

Table 5.1 – Maximum Via Diameter

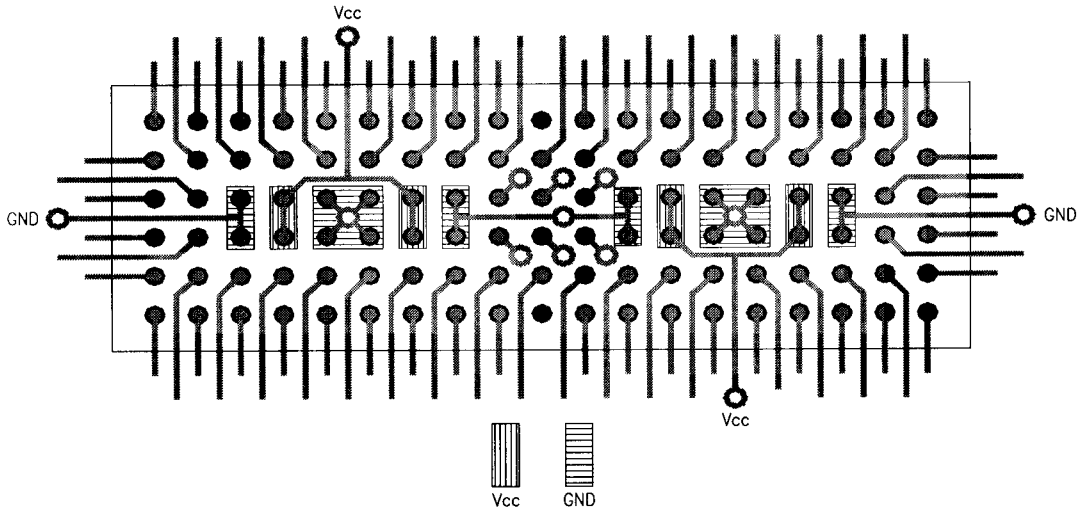
5.4 Routing

The figures below are examples of a PCB routing with two layers of PCB interconnect:



Note 1: Ground balls are connected together within the PCB.

Figure 5.3 – LFBGA-96 Recommended Routing



Note 1: Ground balls are connected together within the PCB.

Figure 5.4 – LFBGA-114 Recommended Routing

6 Conclusion

This joint study by Integrated Device Technology, Philips Semiconductors and Texas Instruments shows the 96 and 114 LBGA packages as the most effective solution for addressing performance issues:
(1) minimal skew due to package layout design; (2) improved thermal power dissipation by taking advantage of the chip overlap over the solder balls; and (3) reduced inductance as functions in these packages take advantage of less capacitance for pin-to-pin inductance, thereby enabling support for high speed applications with close to 2X the bandwidth.
In terms of board integration and miniaturization, these LFBGA packages will reduce board space by up to 65% compared to the corresponding TSSOP package for the same functionality.
Additionally, designers may take advantage of improved reliability and reduced manufacturability costs when the diameter of the PCB land pad is equal to the diameter of package vias as explained in section 5.

With the introduction of the LFBGA by Integrated Device Technology, Philips Semiconductors and Texas Instruments, OEMs are assured of an agreed upon JEDEC standardized package, pin out and availability of the product families and functions to be initially introduced. Integrated Device Technology, Philips Semiconductors and Texas Instruments will continue to work with the market identifying new requirements in terms of product family, and functions.

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Jeff West, Allen Glaus, Hal Hanson, Joe Schultze, Henk Kloen, Alma Anderson from Philips Semiconductors;
and Tam Vu, Ernie Oregano, Ronnie Tanhueco, from
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Package Thermal Characterization Methodologies

SZZA003
March 1999

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Contents

List of Illustrations

Abstract

Improving the performance of semiconductor devices has increased per-device power consumption, but not allowable junction temperatures. Historically, thermal-resistance measurements have been made in a variety of ways that have not been explained thoroughly. The advantages of the JEDEC 51 method (JESD 51) are explained and compared with other methods used to determine thermal resistance of semiconductor devices.

Introduction

Even with lower voltage levels, the steady increase in logic clock speed and gate count has resulted in device parasitic heat loss that would have been almost unbelievable just a few years ago. Some leading-edge processors must dissipate as much as a small incandescent room light. This offers significant challenges to system-level designers, particularly because allowable junction temperatures are not increasing. Conversely, in some technologies, junction temperatures must be maintained lower than could previously be allowed due to reliability concerns with newer metal systems and smaller geometries.

Historically, one tool that system designers have used to compare devices and determine operating junction temperatures are properties published by semiconductor manufacturers that specify the ability of device packages to dissipate junction-generated heat away from the surface of the silicon die. Although relatively simple in concept, these thermal-resistance values are sometimes misunderstood and misused, partly because manufacturers rarely publish how they are measured and what they represent physically.

Without this knowledge, the advantages of the new JEDEC 51 method (JESD 51) of measuring thermal impedance cannot be appreciated. This application report begins with an explanation of how thermal-impedance values have been obtained historically, and then describes the advantages of the newer JESD 51 method.

Background

Thermal resistance in a solid is much like electrical resistance in that the steady-state defining equation is:

$$\Delta T \text{ across solid} = R_T \times \text{heat (watts) conducted through solid}$$

or

$$R_T = \frac{\Delta T}{W} \quad \text{(usually expressed in °C/W)} \tag{1}$$

Where R_T is thermal resistance of a material.

That is, a measured temperature, ΔT, across a solid would mean $\Delta T/R_T$ watts of power passes through it.

Figure 1 shows a simplified two-dimensional diagram of resistance to heat flow from the junctions on a die surface to the surface of the package.

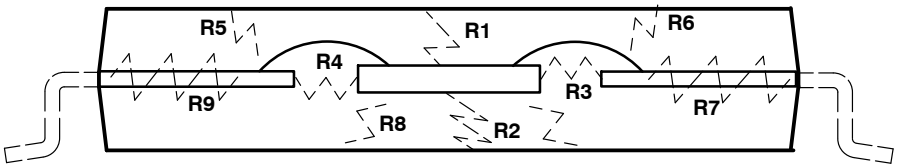


Figure 1. Representation of the Distributed Resistance to Thermal Dissipation in a Device

Rl, R2, etc., are the equivalent thermal resistances from the die surface to a section of the package. Because thermal resistance in a solid depends on material properties, length of path, and cross-sectional area of the path, each section of the package contributes a unique thermal resistance. Thermal power dissipation from die surface to the surface of the package can be calculated by:

$$\text{Overall power dissipated} = (T_J - T_S1)/R1) + (T_J - T_S7)/(R3 + R7) + \ldots (T_J - T_{SN})/(R_N) \quad (2)$$

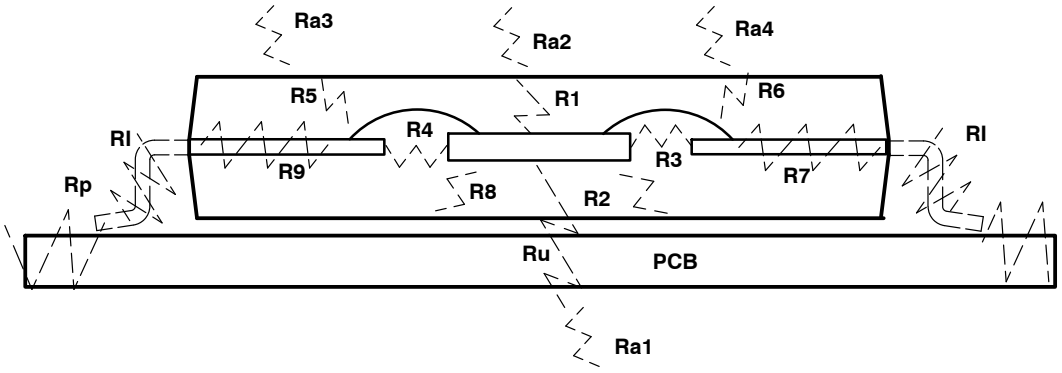
Where:

T_S l...T_S n = package surface temperatures at the exterior locations shown
T_J = average junction temperature at the surface of the die
Rl...Rn = distributed thermal resistances for each section of the package

The smaller the overall package thermal resistance becomes, the better able a package is to conduct heat away from the die surface.

If the ability of a package to conduct heat from the die to the outside surface were all that is required to predict junction temperatures, semiconductor manufacturers could provide accurate thermal resistance using finite-element analysis (FEA) or equivalent discrete models. Unfortunately, external factors, such as airflow and spacing from the printed circuit board (PCB), can affect package thermal resistance much more than the package construction itself.

Figure 2 shows the effects of external factors on thermal resistance of an assembled device.



Ral...Ran = thermal resistance of the air around the device
Ru = thermal resistance of whatever is under the package (e.g., thermal grease and air gap)
Rl = lead thermal resistance
Rp = PCB thermal resistance, etc.

Figure 2. Representation of Distributed Thermal Resistance With External Factors Added

Table 1 shows the effects of environment on junction temperature.

Table 1. Selected Thermal-Resistance Values

MATERIAL	THERMAL RESISTIVITY °C • m/W
Copper (lead frame)	0.003
Silicon (die)	0.007
Ceramic	0.055
Mold compound (plastic case)	1.59 to .7468
Thermal grease	2
FR 4 (PWB)	3.5
Air	38.2

These values most often are published inversely (as conductivity), but are listed here as resistive to be consistent with the way overall package thermal resistance is expressed.

These values are for thermal conduction only. Actual thermal analysis involves conduction, convection, and radiation, all of which are calculated differently and can be estimated accurately only by dedicated FEA using empirical data. For the purpose of explaining package thermal resistance, a simplified resistor model is used here.

Because the external resistances of the surrounding air, PCB, thermal grease, etc. are in series with the package resistance, factors external to the package affect junction temperature significantly. If a package has an overall thermal resistance equivalent to Equation 1 and Figure 1 of about 14°C/W after adding in the external resistive factors, such as the surrounding air (equivalent to Figure 2), a thermal resistance of 40°C/W, or higher, could be expected.

This presents a problem to device manufacturers who want to provide thermal information about their packages because external factors are not known at package thermal characterization. As a solution, semiconductor manufacturers historically have provided two types of resistance values: θ_{JC} (resistance from junction to case) and θ_{JA} and θ_{JMA} in an attempt to account for end-use environments.

Junction-to-Case Thermal Resistance

θ_{JC} is, approximately, the ability of a device to dissipate heat in an ideal environment, that is, mounted with an infinite or temperature-controlled heat sink. However, test methods used to determine θ_{JC} have varied in the past and proper use of this value depends on which method was used to determine the specified value.

Military Standard

Description

Instructions for determining θ_{JC} for military products are specified in MIL-STD-883 Method 1012.1. θ_{JC} determined using this method defines the ability of a device to dissipate heat if it is mounted on a temperature-controlled heat sink.

To establish a temperature reference on the surface of the die, the temperature-dependent forward bias voltage of a bipolar junction is calibrated at constant bias current for several different temperatures in an oven. This can be an unused junction on the device, but usually a special die for thermal characterization is assembled in the package being tested (see Figure 3).

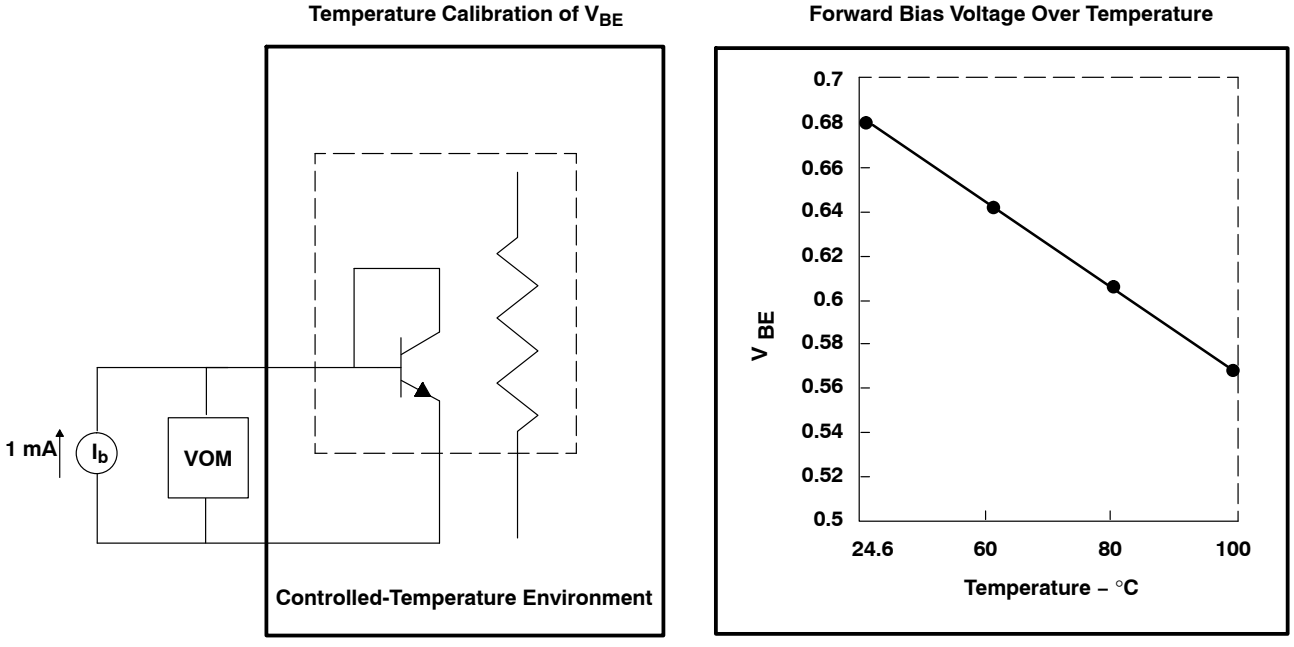


Figure 3. Die Schematic for Thermal Characterization

The device is then placed on a copper heat sink that is maintained at a constant temperature, using thermal grease to ensure the best possible conductivity. A thermocouple is inserted through the heat sink and is pressed against the underside of the package nearest the device to record package surface temperature. MIL-STD-883 Method 1012.1 specifies that the thermocouple be placed on the hottest part of the case (see Figure 4).

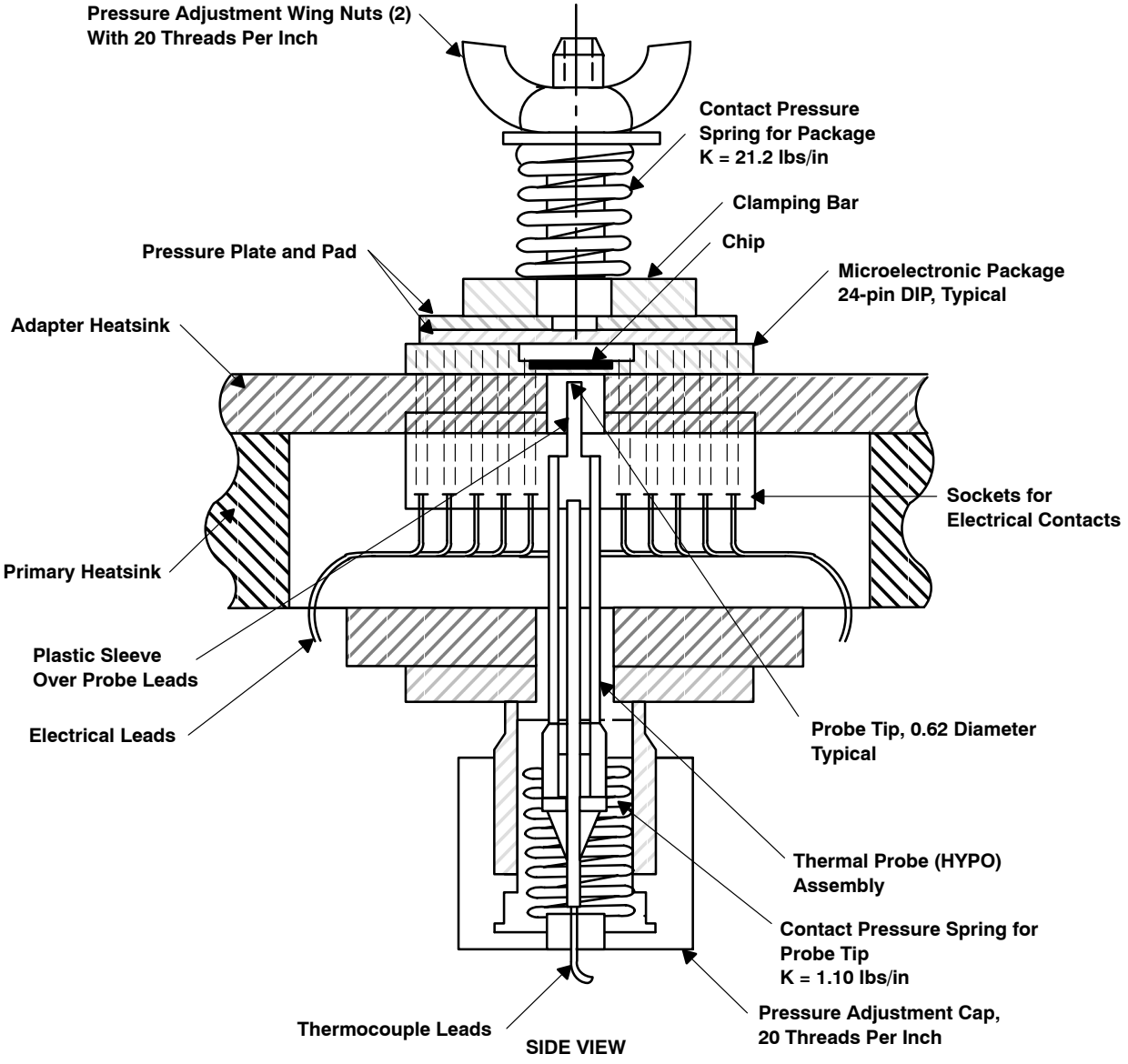


Figure 4. Military θ_{JC} Test Configuration as Illustrated in MIL-STD-883 Method 1012.1

With some amount of power applied to the power-dissipating elements on the die, the forward bias voltage is measured after temperature has stabilized and the surface temperature of the die determined. θ_{JC} is then calculated using the formula:

$$\theta_{JC} = \frac{\text{Die surface temperature} - \text{Package surface temperature}}{\text{Power applied}} \quad (3)$$

Package surface temperature is the temperature recorded by the thermocouple pressed against the underside of the package. Die surface temperature is the temperature derived from the previously calibrated forward bias voltage. Power applied is the product of voltage and current applied to the die resistive network (bias current is small enough to be ignored).

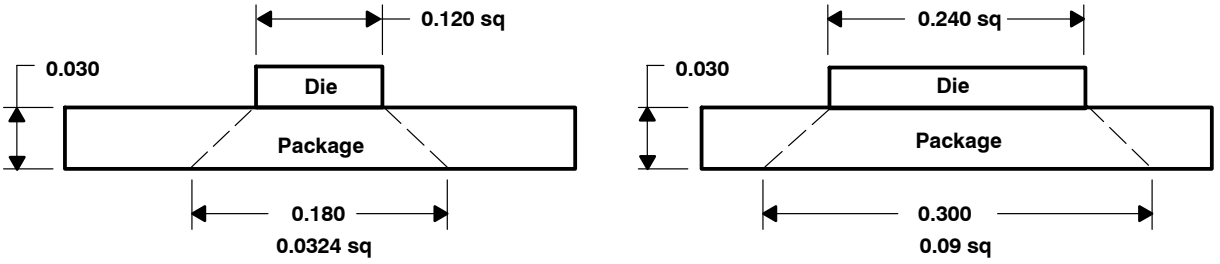
Use

The configuration in Figure 4 represents, as nearly as possible, an ideal heat sink placed directly under the die. It does not comprehend any other heat sink position, nor does it include any additional cooling, such as air flow. With the heat sink maintained at a constant temperature during testing, MIL-STD-883 Method 1012.1 provides a more nearly ideal θ_{JC} than if the device were mounted on a passive heat slug.

Assembly designers often use θ_{JC} measured in this way to approximate junction temperatures at circuit conception. If the unit is to be mounted on a surface with known thermal properties, such as a thermal rail, and all heat is assumed to be taken out along this path, estimation of junction temperature is straightforward.

Because many military applications are enclosed, with heat extraction through a heat sink on the bottom of the device case to a thermal rail (in the same configuration as the test), a thermocouple attached to the *measured* package surface can be used to estimate realistic junction temperatures in the assembled system. A thermocouple applied in this manner gives erroneous results if no heat sink is used or the in-use configuration differs from the test configuration.

By far, the largest variation potential in θ_{JC} values measured in this manner is the size of the die used in the test. With two of the standard thermal die sizes available, unidirectional heat flow from a finite source fans out at approximately a 45-degree angle in an isotropic material (see Figure 5).



All dimensions are in inches.

Figure 5. Small-Die and Large-Die Dissipation Areas

The larger die dissipates power over an area three times that of the smaller die, thus the heat dissipated by the large-die device is about one-third that of the smaller die.

This is not as much of a problem as it may seem at first because test-die sizes are chosen to match the size of the device die. It does explain though, why smaller packages, and, therefore, smaller die, have significantly higher θ_{JC} values when measured using MIL-STD-883 Method 1012.1. In addition, several devices of slightly varying die size may use the same package, causing slight deviations from published thermal-resistance values.

Default values of θ_{JC} that are significantly higher than if the package were measured have been published in miltary standards. Therefore, if a particular package type has not been characterized by a manufacturer, the default values are used and may cause some military thermal-resistance values to seem extraordinarily high.

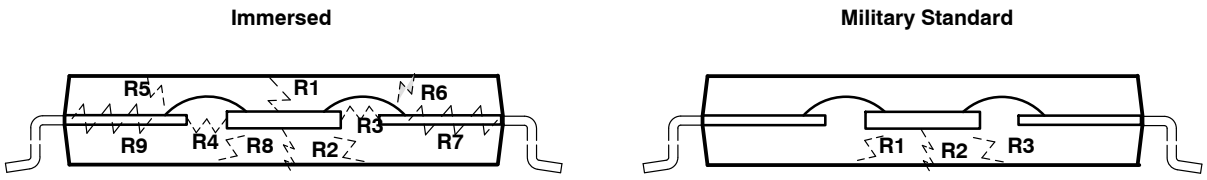
Although ceramic is a much better thermal conductor than most organics, military semiconductor users occasionally are confused by the fact that plastic packages sometimes have lower published θ_{JC} (and θ_{JA}, discussed later in this application report) values than equivalent ceramic-package devices. The root of this paradox is not in the package materials, but in different methods of characterizing θ_{JC}.

Simulated Infinite Heat Sink

Description

One historical method of characterizing θ_{JC} is similar to that used for military devices, but the device is immersed in an agitated, electrically insulating fluorinert fluid rather than sitting on a heat sink. This test method is an attempt to measure directly the overall thermal resistance of a package. Even though the thermal resistance of the fluorinert is poor, this method emulates, to some extent, an infinite heat sink on all parts of the package.

Figure 6 shows the practical difference between a simulated infinite heat sink and the military-standard method.



$$\frac{1}{1/(R1 + FR) + 1/(R2 + FR) + ... + 1/Rn + FR} \qquad \frac{1}{1/R1 + 1/R2 + 1/R3}$$

Where:

FR = fluid thermal resistance exterior to the package

Figure 6. Simulated Infinite Heat Sink vs Military-Standard Method

The parallel resistance net, composed of the entire package as opposed to only the bottom section, explains why a package made of thermally inferior material, such as plastic instead of ceramic, sometimes can have lower published thermal resistance values.

Use

Thermal resistance determined in this way is best used for comparison purposes only (with other similarly measured devices). Thermal resistance cannot be used to approximate junction temperatures prior to component assembly and power up because all of the package surface is used to extract heat during this test and it is impossible to know how the package will be affected by the system environment.

Other θ_{JC} and θ_{JC}-Like Determinations

There is no universal standard for θ_{JC}, so it has been determined in various ways. For instance, some package vendors use FEA models to determine thermal performance of their packages. In this category, θ_{JC} has been calculated from the die surface to the most remote part of the package, as well as calculated from resistance meshes similar to equation 1.

A newer method, differentiated by the designator Ψ_{JT} is defined by EIA/JESD 51-2. This method entails measuring case temperature using a fine-gage thermocouple glued to the top of the package during operation on a PCB. This allows a more accurate calculation of system-level *in situ* junction temperatures because it more closely replicates typical end-use conditions[1].

Semiconductor data sheets typically are published using consistent thermal-resistance-measuring techniques as described here, but, if thermal information is obtained from a third party, such as a package vendor, it is important to understand their definition of θ_{JC}.

θ_{JA} and θ_{JMA} Prior to JEDEC Method 51

Description

θ_{JA} is a measure of the ability of a device to dissipate heat while operating in open air without a heat sink. Recently, JEDEC has refined the terminology for open-air testing so that, if the test is performed in still air, it is properly termed θ_{JA}. If performed in a wind tunnel with calibrated air velocity, it is called θ_{JMA}. Before this refinement, all types of open-air testing usually were labeled θ_{JA}. Due to the lack of standardized methodology, this general description also has led to differing methods and results.

Military Ceramic

There is no specific requirement in military specifications to provide θ_{JA} or θ_{JMA}, but as is typical of military testing, when θ_{JA} is published, usually it is determined by the most conservative interpretation. For example, TI Military Semiconductor Group tests θ_{JA} with a unit suspended in open air under a 1×1×1-foot cover with no air flow. Because air is a very good insulator, the thermal resistance values produced are worst case. At times, this is troublesome because a device that would be usable if provided the added heat-dissipative capabilities of a PCB mount, might be eliminated during preliminary consideration due to deceptively high junction temperatures derived from a highly conservative value of θ_{JA}. Devices suspended in air can have θ_{JA} values two or more times that of mounted units, depending on device configuration.

Plastic

θ_{JA} values for plastic-package devices have been characterized in environmental conditions considered by the manufacturer to be adequate for in-use junction-temperature estimation. This can vary from suspended in air, mounted on boards, sitting on countertops, or inserted in sockets.

Use

Generally, θ_{JA} is used as a comparison tool between package types. For preliminary estimates of on-board junction-temperature, derating curves are derived from θ_{JA} using the formula in Equation 4.

$$\text{Maximum device power} = \frac{\text{Maximum junction temperature allowed} - \text{Estimated ambient temperature}}{\theta_{JA}} \quad \textbf{(4)}$$

θ_{JA} can be considered worst case if measured in open air, in a socket, or, possibly, as nominal if measured mounted on a PCB. PCB trace dimensions, device orientation, air turbulence and method of measuring air velocity, proximity of the ambient temperature thermocouple, and enclosure size, if any, are additional factors that can change the θ_{JA} value.

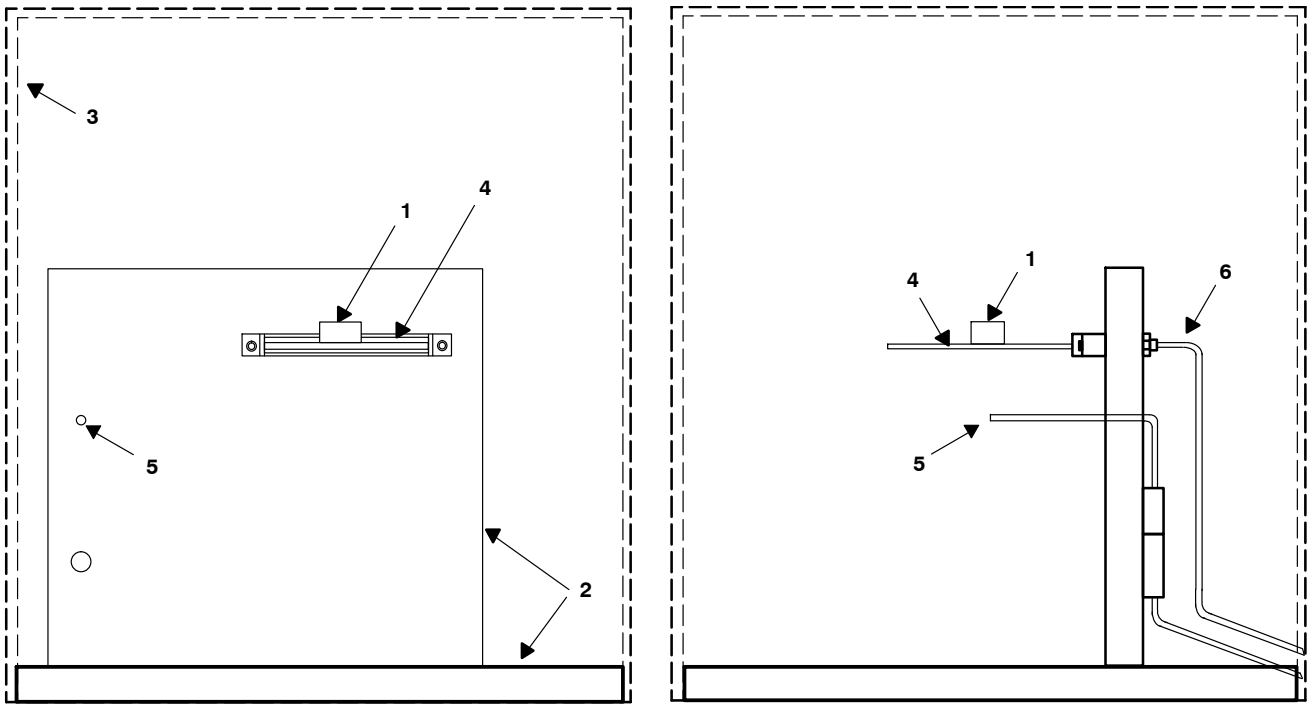
Junction and maximum allowable ambient temperatures often are calculated from θ_{JA} by device product engineers, but this can be a very conservative approach if θ_{JA} is measured in open air with no conduction to a PCB. Experiments have shown that 85% of the heat produced by the die in a typical package is dissipated from the test board[2].

Conversely, this calculation may result only in nominal to optimistic values if θ_{JA} was measured mounted on a PCB, particularly if the PCB has thermal vias or power planes. Unfortunately, semiconductor manufacturers often do not publish how their thermal-resistance values were determined.

Characterizing θ_{JA} Using JEDEC Method 51

JEDEC Method 51 provides the semiconductor industry a method of eliminating the most troublesome aspect of θ_{JA} characterization: inconsistency. In addition, this test method emulates a slightly conservative, but realistic, system-level environment for junction-temperature estimations.

Method 51 enforces rigid environmental requirements, controlling parameters that contributed previously to resistance variability. Figure 7 shows the test fixture for the still-air portion of the test.



1. Unit under test
2. Insulating suport of specific dimensions
3. Insulating 1' x 1' x 1' cover
4. PCB of specific dimensions without planes or thermal vias; trace size and length, connector type and board material and construction defined. (see Note A)
5. Thermocouple used to record ambient temperature; location defined by JEDEC
6. Test leads

NOTE: Although EIA/JEDEC Standard 51-3 (August 1998) lists only the board described here (no planes or thermal vias) there is another board design pending publication that has four layers and two power planes. Because the currently published board is called low effective thermal-conductivity test board, the power-plane design could be considered a high- or higher-conductivity test board. This board is used by many companies.

Figure 7. JEDEC Method 51 Test Setup for Still-Air Portion of the Test

JEDEC has explicitly defined all parameters because studies indicated surprising thermal effects of the environment, in addition to parameters mentioned previously. For example, one study shows that PCB trace length can affect measured θ_{JA} on a plastic package almost as much as the presence or absence of a 500 lf/m airflow[1].

Also, FEA modeling evaluations have shown that this methodology is sufficiently controlled so that only one package configuration need be measured. Other packages of the same material and configuration, but different size, can then be characterized by FEA using parameters determined from the measured unit.

Because a large portion of the heat generated by a die surface is conducted to the PCB, this arrangement provides a much more consistent and realistic value of θ_{JA} between characterization laboratories than any of the previous methods. In addition, junction-temperature calculations based on this method of characterization provide a good conservative nominal first-pass value.

The new JEDEC method of measuring θ_{JA} does not provide junction temperatures from case temperature as θ_{JC} or the newer Ψ_{JT} provide, so these values, or an equivalent, continue to be required data-sheet entries. Presumably, ambiguous characterization methods, such as immersion, will be replaced by defined methods similar to military θ_{JC} or Ψ_{JT}.

Summary

The primary purpose of this application report is to inform users of thermal-resistance values and derating curves of hidden variabilities in historical values and to emphasize the importance of inquiring into test methodology before using the results. In addition, an explanation of the inconsistencies in measurements between manufacturers and package types has been provided. New JEDEC methods have potential for greatly improving the accuracy and reliability of semiconductor-package thermal characterization.

This application report also explains the rationale behind TI's conversion to the new JEDEC standard. TI provides θ_{JC} per MIL-STD-883 method 1012.1 for military parts, and adds the more realistic JEDEC method. TI commercial plastic devices have been characterized using the JEDEC method since 1995.

Acknowledgment

The author of this application report is R. A. Pauley.

References

1. JEDEC Standard 51
2. *K-Factor Test-Board Design Impact on Thermal Impedance Measurements*, literature number SCAA022A

Radiation Exposure Test Results of F Logic Functions

SDFA001
May 1997

TEXAS INSTRUMENTS

Introduction

Military system functionality in a radiation environment is increasingly becoming more of a design criteria. System designers have a need for comparative integrated circuits radiation tolerance data, because exposure to gamma radiation degrades the performance of integrated circuits. The amount of performance degradation for various manufacturers' logic families is variable since process technologies differ. Comparison studies that expose various vendors' logic devices to radiation can be used to determine a logic family's suitability for use in a system. These studies may, in fact, influence the selection of product for design in.

There are numerous guidelines/methods for radiation testing. Also, there is room for interpretation regarding the failure modes of irradiated logic devices. Some IC manufacturers define a radiation-induced failure as the total-dose level at which a logic error occurs. Others define failure at the point at which data sheet parametrics are exceeded. These variable test methodologies and definitions make direct comparisons of existing studies difficult. Therefore, many OEMs have developed their own radiation test criteria to assure program compliance.

It is helpful to have some generic radiation data to use as comparisons for initial selection of logic families for new designs. To that end, the following is offered as a guide for that selection process. The data is presented in two sections:

1. Results of testing done by Texas Instruments, and
2. Results of testing done by a third-party OEM and printed herein with their permission.

The comparisons are necessarily generic and any conclusions that are drawn from the data may warrant further investigation. Results of the tests do indicate the TI F logic product is more radiation tolerant than currently available FAST™ product.

Testing Performed by TI

Failure to meet data sheet parametric specifications is one consequence of exposing devices to radiation. After a device is irradiated, typically the first parametric specification to be violated is the input leakage current (I_{IH}) as it will increase beyond the maximum data book limit. For the radiation tolerance tests done by TI, the parameter monitored was I_{IH}. The data book maximum limit for this parameter is 20 μA for the F logic family. In typical system applications with 10 unit loads, 200 μA is considered a representative value for I_{IH}. Test conditions simulated a total-dose radiation environment.

Both the supply voltage (V_{CC}) and the inputs were kept at 5.5 V during irradiation. The dose rate was 201.9 rad(Si)/second, and the highest readings in each sample of four units of each device type ('54F00, '54F74, '54F244) are tabulated in Table 1. Initial tests were done with total doses of 50, 100, 200, and 100 krad(Si). Since some devices were beyond the 20 μA data book limit at the 50 krad(Si) total dose level, an additional test point of 20 krad(Si) was added. A few tests were stopped at 200 krad(Si) because the devices read over the full-scale test capability of 3031 μA. Full MIL-STD-883C-compliant product from each vendor was used except where indicated.

FAST is a trademark of National Semiconductor Corporation.

The following specific devices and date codes were subjected to the radiation testing:

Texas Instruments	Date Code
'54F00	B8735Z
'54F74	8647
'54F244	8706

Fairchild Semiconductor	Date Code
'54F00	8430, Recertification tested 8604
'54F74	Non-883C compliant P-DIP, 8718
'54F244	8641

Motorola Inc.	Date Code
'54F00	8513B
'54F74	8640A
'54F244	8619B

Signetics Corporation	Date Code
'54F00	8717
'54F74	8648
'54F244	8644

Table 1. Relative Radiation Tolerance

PARAMETER	TEXAS INSTRUMENTS	FAIRCHILD	MOTOROLA	SIGNETICS
'54F00				
I_{IH} at 20 krad(Si)	—	<0.1 μA	380.1 μA	—
I_{IH} at 50 krad(Si)	14.3 μA	2.4 μA	1231.1 μA	2725 μA
I_{IH} at 100 krad(Si)	174.4 μA	283.7 μA	2114.3 μA	>3031 μA
I_{IH} at 200 krad(Si)	526.2 μA	840.1 μA	>3031 μA	>3031 μA
I_{IH} at 500 krad(Si)	834.9 μA	1408.3 μA	>3031 μA	—
I_{IH} at 1000 krad(Si)	739.5 μA	1570.8 μA	>3031 μA	—
'54F74				
I_{IH} at 20 krad(Si)	—	597.8 μA	6.95 μA	192.7 μA
I_{IH} at 50 krad(Si)	7.2 μA	>3031 μA	230.9 μA	1648.9 μA
I_{IH} at 100 krad(Si)	138 μA	>3031 μA	389.3 μA	>3031 μA
I_{IH} at 200 krad(Si)	475.4 μA	>3031 μA	713.1 μA	>3031 μA
I_{IH} at 500 krad(Si)	732.5 μA	—	1417.2 μA	—
I_{IH} at 1000 krad(Si)	648.4 μA	—	1528.3 μA	—
'54F244				
I_{IH} at 20 krad(Si)	—	48.6 μA	350.9 μA	59.4 μA
I_{IH} at 50 krad(Si)	0.7 μA	583.1 μA	1062 μA	280.7 μA
I_{IH} at 100 krad(Si)	64.7 μA	2972.1 μA	1650.1 μA	751.9 μA
I_{IH} at 200 krad(Si)	296.7 μA	>3031 μA	2644 μA	1296.8 μA
I_{IH} at 500 krad(Si)	560.2 μA	—	>3031 μA	1545 μA
I_{IH} at 1000 krad(Si)	525.5 μA	—	—	1395.5 μA

NOTE: Supply voltage V_{CC} and input voltage V_{IH} were both 5.5 V during irradiation.
Dose rate = 201.9 rad(Si)/second
Tester full-scale limit for I_{IH} = 3031 μA max
Table listings were the highest I_{IH} reading obtained in each sample of four units.

Third-Party OEM Test Results†

Eight samples of the '54F04 hex inverters and '54F11 triple 3-input AND gates along with four samples of a '54F20 dual 4-input NAND gate were tested in a total-dose environment. They were exposed to gamma radiation and irradiated at approximately 500 rad(Si)/minute or 8 rad(Si)/second. Test data was taken every 2 krad(Si) up to 30 krad total dose. If the first four samples showed no significant degradation, the remaining parts were irradiated at 1000 rad(Si)/minute or 16.7 rad(Si)/second and data was taken every 5 krad(Si) up to 100 krad(Si). All devices were exercised, both functionally and parametrically, using the Eagle Multiplexer with the NUGPMUX test package on the EAGLE LSI-4 automated test equiment.

In addition to monitoring I_{IH}, the propagation delay (t_{pd}) of four samples of each device type was measured independently at baseline and following exposure to the highest total dose level tested – between 60 and 80 krad(Si). A custom propagation delay fixture was used. In all cases, one input received a 3-V amplitude square wave while the other inputs were tied to 5 V or 0 V so that the output yielded a positive square wave. The propagation delay was then measured using the 50% points of the input and output waveforms as reference. *No significant degradation was observed in any of the devices tested.*

During irradiation, the parts were statically biased with highs and lows as in Table 2 and dc parametric test conditions were selected according to data book specifications.

Table 2. Biasing Schemes for Devices

PART	S/N	PIN NUMBER													
		1	2	3	4	5	6	7	8	9	10	11	12	13	14
'54F00	1–4	H	X	L	X	H	X	GND	X	L	X	H	X	L	V_{CC}
	5–8	H	X	L	X	H	X	GND	X	L	X	H	X	L	V_{CC}
'54F11	1–4	H	L	H	L	H	X	GND	X	L	H	L	X	L	V_{CC}
	5–8	H	L	H	L	H	X	GND	X	L	H	L	X	L	V_{CC}
'54F20	5–8	H	L	NC	H	L	X	GND	X	H	H	NC	H	H	V_{CC}

† Only Texas Instruments Incorporated product was used in the study.

Dosimetry data showed that each device received radiation at a slightly different dose rate due to its positioning on the multiplexer. The actual exposure is shown in Table 3.

Table 3. Actual Dose Rates

DEVICE	S/N	DOSE RATE/ rad(Si)	AVERAGE	Δ% POSITION
'54F04	1	472	496	12.5
	2	498		
	3	484		
	4	531		
	5	939	1011	16
	6	1003		
	7	1016		
	8	1089		
'54F11	1	472	496	12.5
	2	498		
	3	484		
	4	531		
	5	1038	1144	25.5
	6	1090		
	7	1145		
	8	1303		
'54F20	1	1038	1144	25.5
	2	1090		
	3	1145		
	4	1303		

The minimum, mean, and maximum values for all parameters are shown for all device types in Tables 4 through 9. Table 4 and Figure 1 exhibit the input leakage current for the '54F04. Similarly, Tables 5 and 6 and Figures 2 and 3 represent the parametric performance for the I_{IH} and I_{CC} for the '54F20, respectively. And finally, Tables 7 through 9 and Figures 4 through 9 correspond to I_{IH}, I_{CC}, and V_{OH} of the '54F11.

Summary

The tests performed by Texas Instruments can be used as a gauge of relative radiation tolerance of various vendors' 54F-type logic families. Defining the data sheet parametric failure points, as opposed to defining the points where logic error occur, was the basis for both studies. Test results do indicate that the TI 54F logic family is more radiation tolerant within the constraints of the parameters monitored. Significantly lower I_{IH} readings were recorded for TI 54F logic devices at several total-dose levels. An additional point for comparison is the data contained in the third-party OEM study.

The study that was performed by the third-party OEM gives a definition of radiation tolerance of TI 54F devices that is based on additional data sheet parametrics. Although no functional failure was observed in any of the eight samples of the devices tested, the dc parametrics did show some degradation. The various parameters monitored were the input leakage current (I_{IH}), the supply current (I_{CC}), and the output voltage (V_{OH}). Data sheet parametric failures for input leakage current for the '54F04, '54F11, and '54F20 were exhibited at 65, 60, and 70 krad(Si) total dose, respectively. The supply current exceeded data book specifications at 51 and 55 krad(Si) for the '54F20 and '54F11, respectively. No significant degradation was observed in the supply current for the '54F04 to 85 krad(Si). The output voltage for the '54F11 fell below the data book minimum specified value at total-dose levels exceeding 45 krad(Si). No degradation in propagation delays (t_{pd}) was observed in any of the devices irradiated.

PART NUMBER: '54F04 S/N 5–8
DATE CODE: A8709
VENDOR: TI
TEST DATE: 3-OCT-88

HIGH-LEVEL INPUT CURRENT
vs
TOTAL DOSE

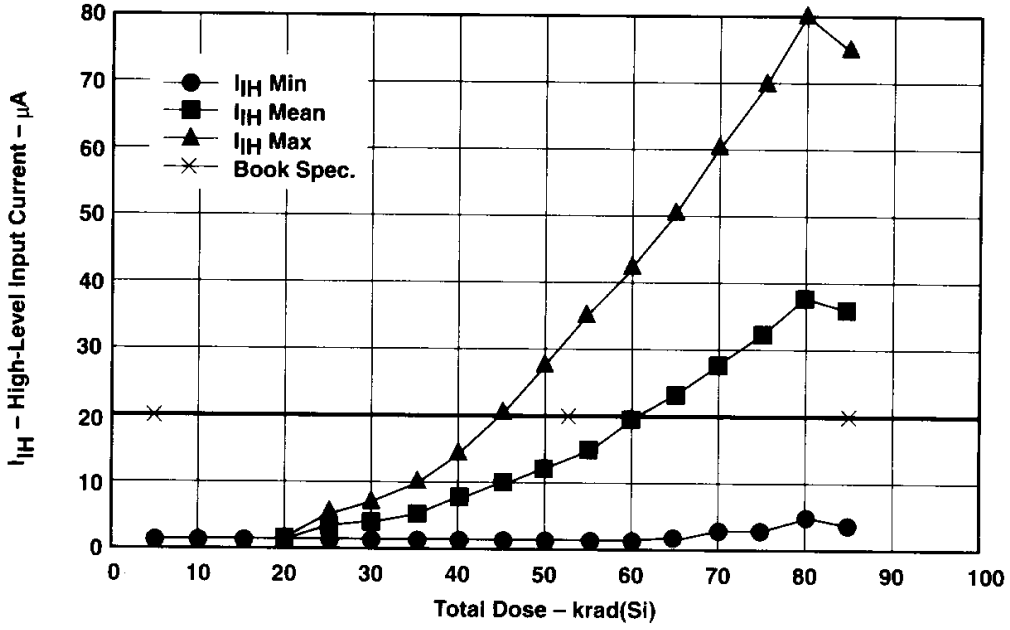


Figure 1

Table 4. High-Level Input Current vs Total Dose – '54F04

TOTAL DOSE/ krad(Si)	I_{IH} (μA) @ V_I = 2.7 V		
	MIN	MEAN	MAX
00	0.2	0.2	0.2
05	0.2	0.2	0.2
10	0.2	0.2	0.2
15	0.2	0.2	0.2
20	0.2	0.3	0.6
25	0.2	1.1	2.6
30	0.2	2.5	5.8
35	0.2	4.5	10.3
40	0.2	6.8	15.3
45	0.2	9.5	21.1
50	0.2	12.4	27.5
55	0.5	15.7	34.5
60	0.8	19.3	42.2
65	1.2	23.3	50.4
70	1.8	27.7	59.3
75	2.6	32.3	68.6
80	3.6	37.2	77.8
85	3.2	35.9	75.5
Book Spec	—	—	20

PART NUMBER: '54F20 S/N 1–4
DATE CODE: 8726
VENDOR: TI
TEST DATE: 4-OCT-88

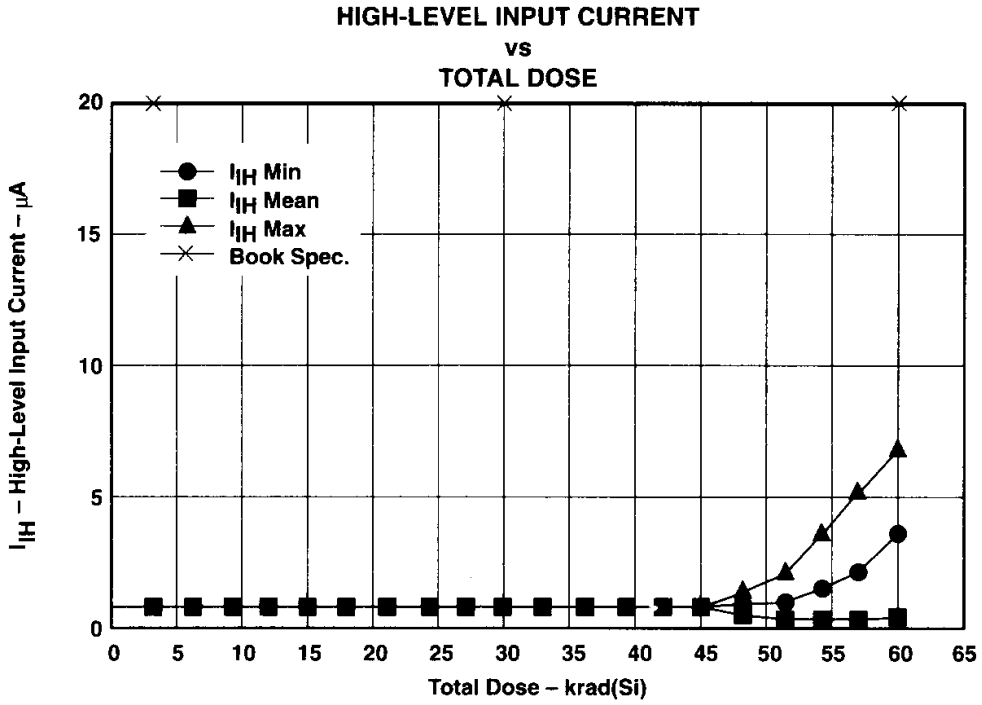


Figure 2

Table 5. High-Level Input Current vs Total Dose – '54F20

TOTAL DOSE/ krad(Si)	I_{IH} (µA) @ V_I = 2.7 V		
	MIN	MEAN	MAX
00	0.5	0.5	0.5
03	0.5	0.5	0.5
06	0.5	0.5	0.5
09	0.5	0.5	0.5
12	0.5	0.5	0.5
15	0.5	0.5	0.5
18	0.5	0.5	0.5
21	0.5	0.5	0.5
24	0.5	0.5	0.5
27	0.5	0.5	0.5
30	0.5	0.5	0.5
33	0.5	0.5	0.5
36	0.5	0.5	0.5
39	0.4	0.5	0.5
42	0.4	0.5	0.5
45	0.4	0.4	0.4
48	0.3	0.5	0.9
51	0.3	0.8	1.8
54	0.3	1.4	3.2
57	0.3	2.2	4.9
60	0.5	3.3	7.2
Book Spec	—	—	20

PART NUMBER: '54F20 S/N 1–4
DATE CODE: 8726
VENDOR: TI
TEST DATE: 4-OCT-88

SUPPLY CURRENT
vs
TOTAL DOSE

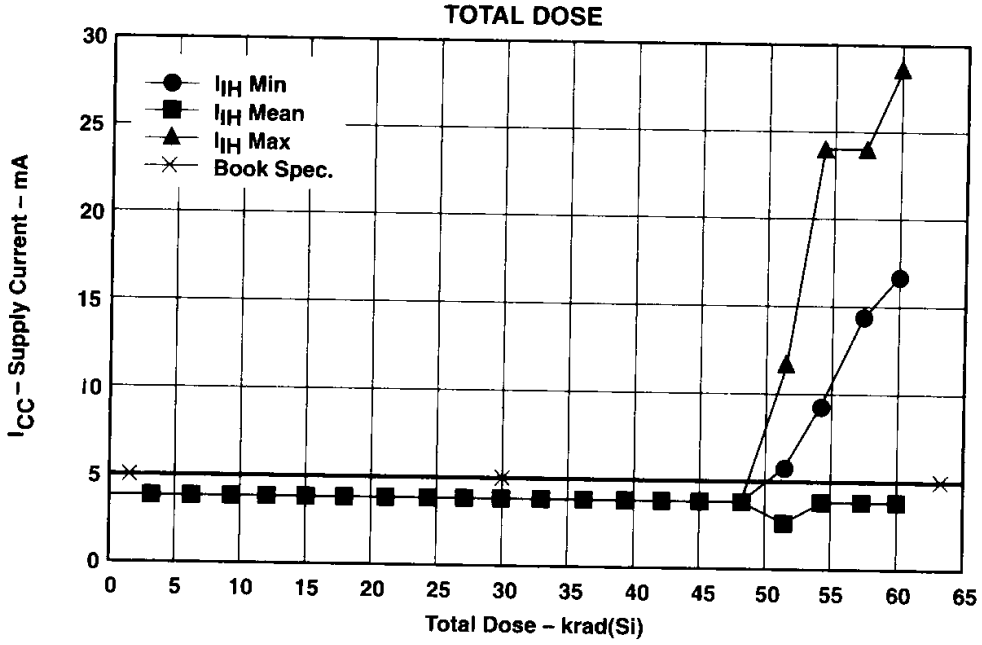


Figure 3

Table 6. Supply Current vs Total Dose – '54F20

TOTAL DOSE/ krad(Si)	I_{CCH} (mA) @ V_{CC} = 5.5 V		
	MIN	MEAN	MAX
00	3.962	4.007	4.042
03	3.958	4.003	4.04
06	3.954	4	4.037
09	3.946	3.996	4.043
12	3.948	3.994	4.032
15	3.945	3.992	4.029
18	3.941	3.99	4.028
21	3.94	3.988	4.026
24	3.941	3.987	4.024
27	3.937	3.985	4.023
30	3.936	3.983	4.021
33	3.936	3.983	4.02
36	3.933	3.981	4.019
39	3.932	3.979	4.017
42	3.932	3.979	4.017
45	3.931	3.979	4.017
48	3.93	3.978	4.015
51	3.078	5.667	11.629
54	3.974	8.782	23.159
57	4.015	14.447	23.243
60	4.015	16.91	28.721
Book Spec	—	—	5.1

PART NUMBER: '54F11 S/N 5–8
DATE CODE: 8822
VENDOR: TI
TEST DATE: 4-OCT-88

HIGH-LEVEL INPUT CURRENT
vs
TOTAL DOSE

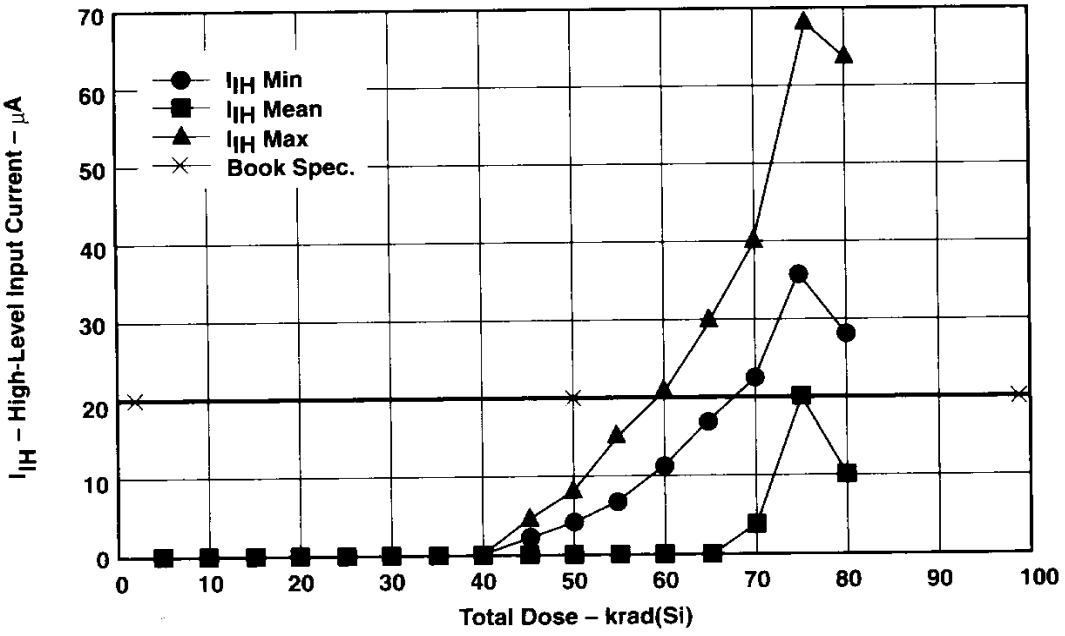


Figure 4

Table 7. High-Level Input Current vs Total Dose – '54F11

TOTAL DOSE/ krad(Si)	I_{IH} (μA) @ V_I = 2.7 V		
	MIN	MEAN	MAX
00	0.5	0.5	0.5
05	0.5	0.5	0.5
10	0.5	0.5	0.5
15	0.5	0.5	0.5
20	0.5	0.5	0.5
25	0.5	0.5	0.5
30	0.4	0.4	0.5
35	0.4	0.4	0.4
40	0.4	0.7	1.1
45	0.4	1.7	3.6
50	0.4	3.6	7.5
55	0.5	6.8	13.4
60	0.9	11	20.9
65	0.7	16	29.8
70	4.2	22.7	40
75	20.6	45.1	66.8
80	10.4	38.4	64.2
Book Spec	—	—	20

PART NUMBER: '54F11 S/N 5–8
DATE CODE: 8822
VENDOR: TI
TEST DATE: 4-OCT-88

SUPPLY CURRENT
vs
TOTAL DOSE

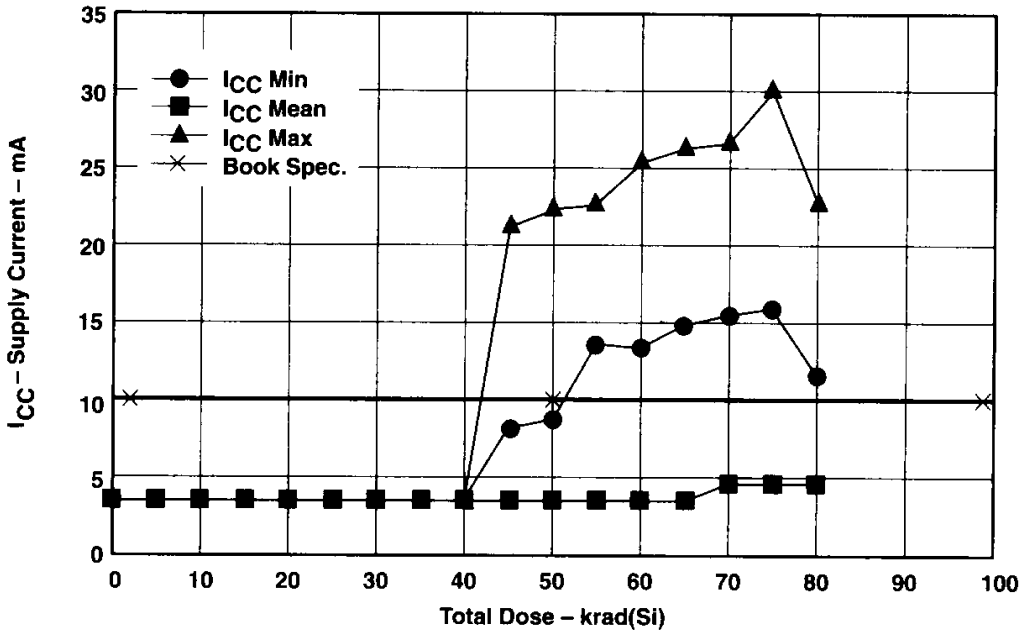


Figure 5

Table 8. Supply Current vs Total Dose – '54F11

TOTAL DOSE/ krad(Si)	I_{CCH} (mA) @ V_{CC} = 5.5 V		
	MIN	MEAN	MAX
00	3.41	3.48	3.55
05	3.41	3.48	3.55
10	3.41	3.47	3.54
15	3.4	3.5	3.53
20	3.39	3.46	3.53
25	3.4	3.47	3.54
30	3.4	3.47	3.54
35	3.39	3.47	3.54
40	3.41	3.46	3.5
45	3.41	7.94	21.43
50	3.37	8.2	22.57
55	3.34	12.94	22.92
60	3.35	12.82	25.49
65	3.36	14.91	26.54
70	4.61	15.16	26.96
75	4.62	15.52	30.53
80	4.63	11.1	22.7
Book Spec	—	—	9.7

PART NUMBER: '54F11 S/N 5–8
DATE CODE: 8822
VENDOR: TI
TEST DATE: 4-OCT-88

HIGH-LEVEL OUTPUT VOLTAGE
vs
TOTAL DOSE

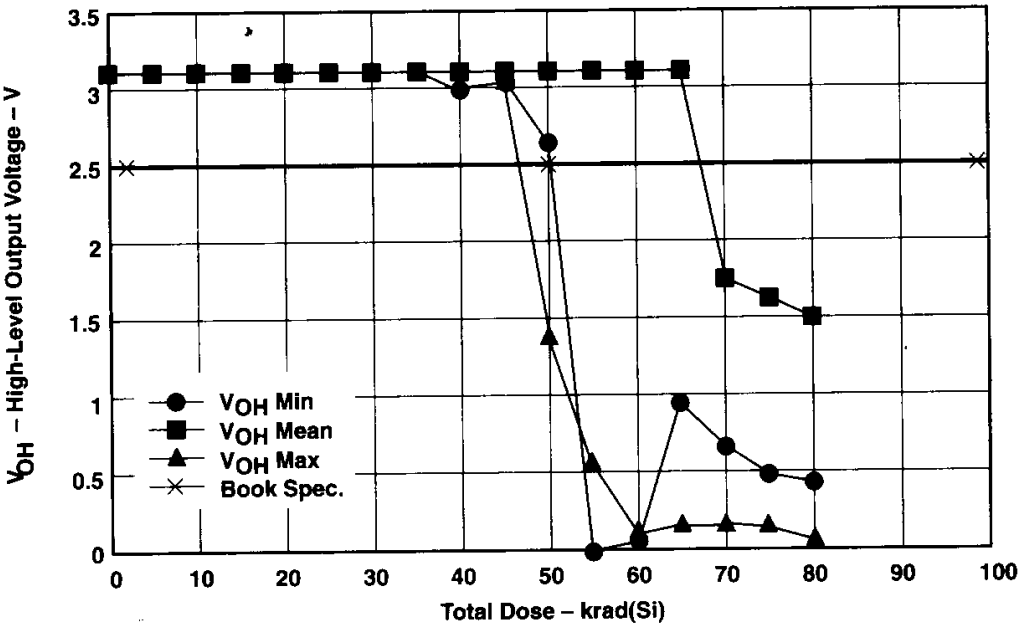


Figure 6

Table 9. High-Level Output Voltage vs Total Dose – '54F11

TOTAL DOSE/ krad(Si)	V_{OH} @ I_{OH} = –1 mA		
	MIN	MEAN	MAX
00	3.063	3.066	3.069
05	3.064	3.067	3.072
10	3.064	3.068	3.073
15	3.065	3.069	3.074
20	3.065	3.069	3.074
25	3.065	3.069	3.074
30	3.065	3.069	3.074
35	3.065	3.07	3.077
40	3.011	3.056	3.077
45	3.069	3.073	3.082
50	1.411	2.657	3.075
55	0.551	0.035	3.076
60	0.076	0.032	3.073
65	0.15	0.994	3.073
70	0.15	0.654	1.719
75	0.15	0.512	1.597
80	0.051	0.469	1.523
Book Spec	2.5	—	—

PART NUMBER: '54F11 S/N 5–8
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vs
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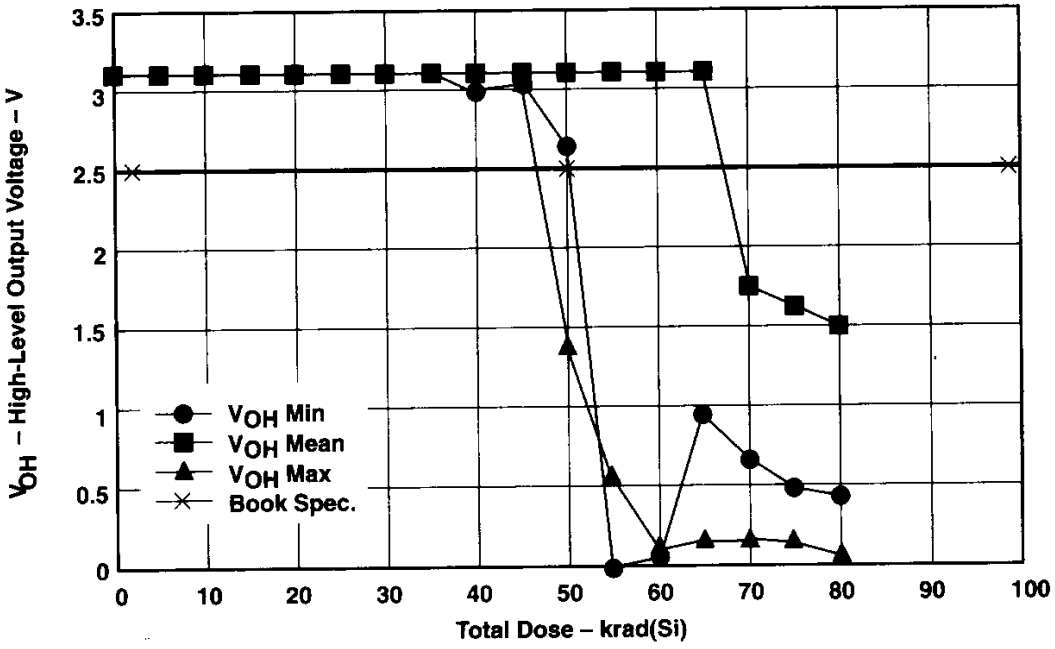

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35	3.065	3.07	3.077
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Shelf-Life Evaluation of Nickel/Palladium Lead Finish for Integrated Circuits

SZZA002
April 1998

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Abstract

The integrated-circuit (IC) industry is converting to nickel/palladium (Ni/Pd)-finished leadframes for assembly of ICs. To date, Texas Instruments (TI™) has over 20 billion Ni/Pd ICs in the field. Users of IC components need to know the maximum length of time that components can be stored before being soldered. The goal of this study was to predict shelf life of Ni/Pd-finished components by exposing a sample set to a controlled environment with known age-acceleration factors. Ni/Pd-finished components were exposed to a Battelle Class 2 environment both in and without their normal packing materials. Results show that Ni/Pd-finished ICs stored in tubes, trays, or tape-and-reel packing material pass solderability testing after 96 hours of exposure to the Class 2 environment. This length of exposure correlates to eight years in an uncontrolled indoor environment.

Introduction

This study was undertaken to determine the shelf life of electronic components that have Ni/Pd-finished leads instead of the more conventional tin/lead (Sn/Pb). TI introduced the Ni/Pd plating finish for leadframes used in plastic-package ICs in 1989. There are more than 20 billion ICs with Ni/Pd-finished leads now in the field.

Uncontrolled assessments of shelf life measured by dip-and-look or surface-mount solderability testing have been performed by various groups within TI. The results have shown no degradation in solderability after two years of shelf storage of the components. This study looks at shelf-life solderability in a controlled fashion, using standardized environmental test conditions for accelerating aging.

The need for an Ni/Pd lead finish is due in part to the desire to remove lead (Pb) from electronics components and end products. Use of Ni/Pd preplated leadframes allows the entire Sn/Pb solder-plating operation and associated chemicals to be removed from the IC assembly process. Additional benefits of using Ni/Pd-finished leadframes include elimination of solder flakes/burrs, improved lead-tip planarity versus Sn/Pb, and a reduction in IC manufacturing cycle time.[1,2,3]

Background

One method used to examine shelf life, as measured by solderability, is to expose the subject devices to a known, controlled atmosphere that accelerates the effects from normal environmental exposure. This is a useful tool if reasonable care is taken to select a test method and conditions so that the time-acceleration factor is valid and the failure mechanism is consistent with actual conditions.

Steam aging of the IC units prior to solderability testing is a common method used to accelerate IC aging, and is used by many manufacturing operations. Previous work has shown that when Pd-finished components are exposed to a steam age environment, mold resins may be deposited onto the surface of the palladium. These deposits inhibit dissolution of the palladium during solderability testing.[4] In contrast, for Sn/Pb-finished leads, the soldering mechanism used is a reflowing of the solder on the lead. If there are contaminants on the surface from the steam aging procedure, then they simply are floated off the surface of the solder. This artifact of the steam aging process does not correlate with actual shelf storage conditions for Ni/Pd-plated leads. In the soldering process, the palladium dissolves and the solder wets to the underlying nickel. Steam age exposure prior to solderability testing has proven to be a nonreproducible method of predicting solderability performance of Ni/Pd-finished components. For this shelf-life study, it was decided to use an acceleration method with known acceleration factors, and with a mechanism more like that seen in actual practice.

Procedure

To study the shelf life and post-storage solderability of surface-mount ICs with an Ni/Pd finish, a Battelle Class 2 mixed flowing-gas environment was selected. This test has been well characterized by previous work and represents a slightly corrosive indoor atmosphere, where the gas concentrations and humidity levels result in pore corrosion of plated-copper (Cu) materials, but do not promote copper creep corrosion.[5,6] Class 2 environments generally are described as indoor environments having no humidity control.

This test is conducted in a mixed flowing-gas chamber designed to the schematic shown in Figure 1; the conditions are shown in Table 1 and described in ASTM B827-92.[7]

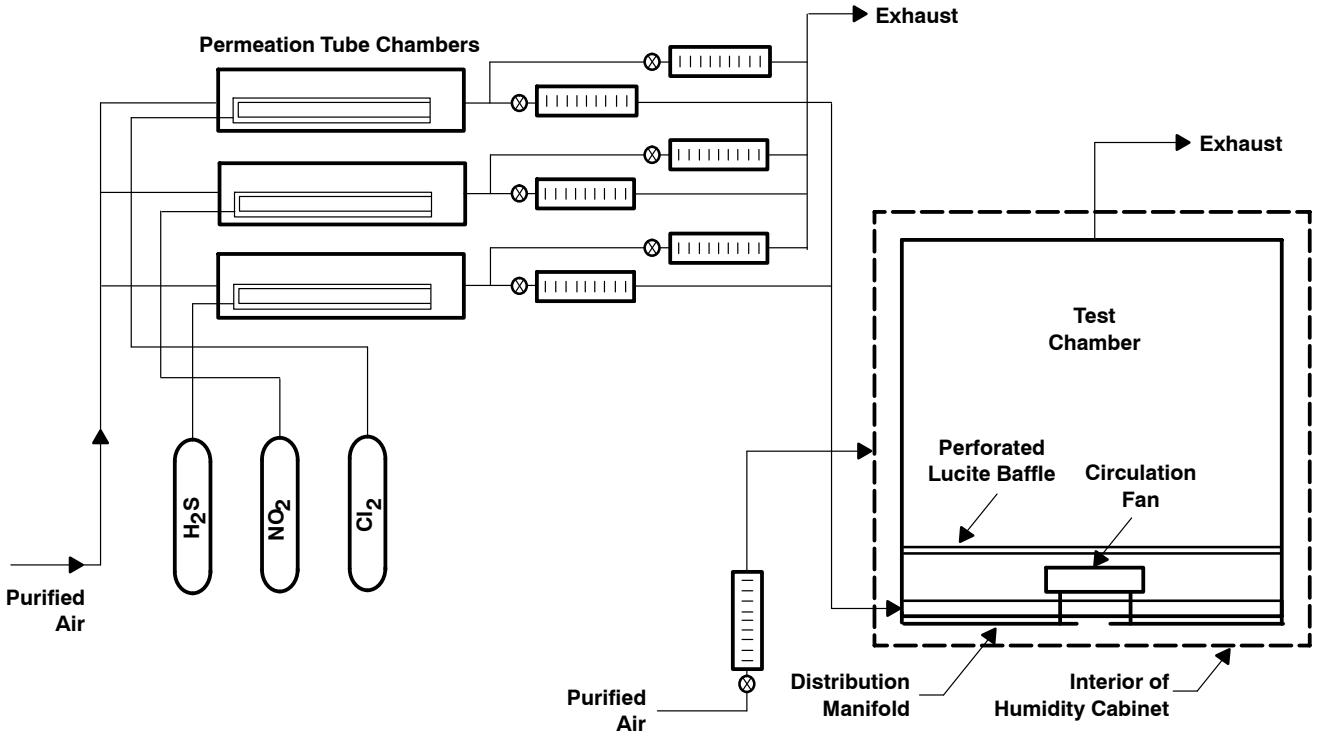

Figure 1. Schematic of Mixed Flowing-Gas Chamber

Concentrations of gases in the chamber are precisely controlled. It is important to include standard reactivity coupons, along with the test specimens. This allows measurements of mass gain, film thickness, and percent oxides on the coupons, so that proper test conditions are maintained, and to facilitate verification of acceleration factors.[8,9,10]

Subject surface-mount IC devices, assembled with Ni/Pd-plated Cu base-metal leadframes, were placed in the chamber, both unprotected and partially protected from the gas flow. Unprotected samples were totally exposed to the mixed flowing-gas environment. Additional samples from the same lots were left in the typical (opened) packing used in product shipment. Small-outline ICs (SOICs) were left in shipping tubes and in tape and reel. Quad flatpack (QFP) devices were in a stack of plastic shipping trays. None of these parts was in an antistatic bag or cardboard shipping/packing box.

The attenuation effects of the packing materials (tubes, trays, tape and reel) were found to be significant. Abbott (Battelle) has stated that the attenuation by packing materials perhaps is the major reason that electronic components can perform reliably in field environments.[11] Virtually any type of packing provides some degree of environmental attenuation compared to free surface exposure. Although it is beyond the scope of this application report, one could speculate that the kinetics are controlled by Fick's third law, since the reactive species are in the gas phase, and gas concentration at the metal surface controls the corrosion rate. This can be intuitively contrasted with the mechanism of the steam age test, which seems not to mimic actual storage conditions.

Device samples and reactivity coupons were removed from the chamber at intervals (12, 24, 36, 48, 72, and 96 hours). Visual microscopic examination was used to ‘‘grade” the visual effects of the gas exposure, followed by solderability testing. Measurement of the reactivity coupons was done to confirm reaction rates and to determine the appropriate acceleration factor.

Table 1. ASTM B827-92 Standard Practice for Conducting Mixed Flowing-Gas Environmental Test

CLASS 2 MIXED-GAS CONDITIONS	
Cl_2 concentration	10 ± 3 ppb
NO_2 concentration	200 ± 50 ppb
H_2S concentration	10 ± 5 ppb
Relative humidity	70 + 3%/–0%
Temperature	30 ± 2°C
Chamber volume change	3 to 6 times per hour
Acceleration factor	400–1000

Assessment Procedures

Visual Examination – Parts from each of the cells of the matrix were examined under a microscope at up to 40× magnification. The parts were graded subjectively as to the amount of corrosion products seen on the surface of the leads. An arbitrary scale of 0 to 5 was used to grade the amount of corrosion, with 0 being no corrosion and 5 being severe corrosion.

Analysis of Corrosion Products – The composition of corrosion products on the surface of representative parts was analyzed by SEM/EDAX. This was done for heavily corroded parts and corrosion-free parts.

Surface-Mount Solderability Test – Solderability of the components exposed to the Class 2 environment was judged with the Surface-Mount Solderability Test per ANSI/EIA-638.[12] This test method simulates the actual reflow environment that surface-mount devices encounter in a board-mount application. Testing has shown that this method is more appropriate for surface-mount devices than the traditional ‘‘dip-and-look” method.

This test procedure begins with screening solder paste onto a ceramic plate (0.035 inch thick) using a solder stencil (see Figure 2). The paste print must match the pattern of the leads to be tested. The devices to be tested are then placed onto the solder paste print (see Figure 3).

Figure 2. Solder Is Screened Onto the Ceramic Substrate

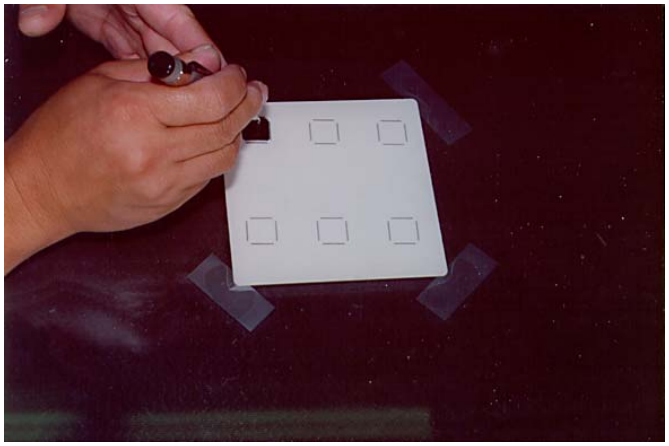

Figure 3. Devices Are Placed Onto the Solder Paste Print

The ceramic substrate is processed through a reflow cycle and allowed to cool. After reflow, the units are removed from the ceramic and inspected. The advantage of this test method is that the IC devices are subjected to the same reflow environment experienced in actual processing and use of a ceramic substrate allows for inspection of the surface to be soldered.

The accept/reject criteria given in ANSI/EIA-638 indicates that ‘‘all terminations shall exhibit a continuous solder coating, free from defects for a minimum of 95% of the critical surface area of any individual termination.” For the surface-mount packages tested, the critical area is defined as the underside of the leads, plus both sides of the leads, up to 1× the lead thickness.

Results

Results of the visual inspection (Table 2) indicate that all of the devices left in the normal shipping materials showed no visible corrosion products. The parts that were completely exposed to the mixed flowing gas showed a time dependency in which the amount of corrosion tracked well with exposure to the atmosphere.

Table 2. Visual Classification of ICs After Exposure to the Class 2 Environment

CLASS 2 EXPOSURE HOURS	GROUP 1 20-PIN SOIC OUTSIDE OF PACKING	GROUP 2 20-PIN SOIC TUBES	GROUP 3 20-PIN SOIC TAPE AND REEL	GROUP 4 80-PIN TQFP OUTSIDE OF PACKING	GROUP 5 80-PIN TQFP TRAY
12	1	0	0	2	0
24	1.5	0	0	2	0
36	3	0	0	2	0
48	4	0	0	3 – bottom 1 – top	0
72	5	0	0	4 – bottom 1.5 – top	0
96	5	0	0	5	0

There was little difference between the SOICs and the QFPs in the unprotected state. Likewise, whether the packing method was tube, tape and reel, or stacked tray, the attenuating effects of the packing were similar.

Micrographs are shown in Figures 4 through 7. The level of corrosion on QFPs not in their shipping trays is quite evident. EDAX analysis of the corrosion deposits confirms that the predominant species are oxides, sulfides, and chlorides of Cu. This is consistent with the nature of the corrosive gases in the Battelle Class 2 environment.

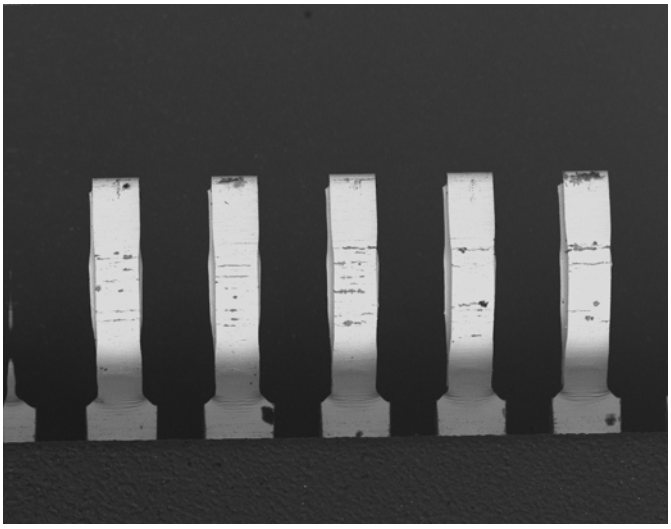

Figure 4. QFP in Tray After 48-Hour Exposure to Class 2 Environment

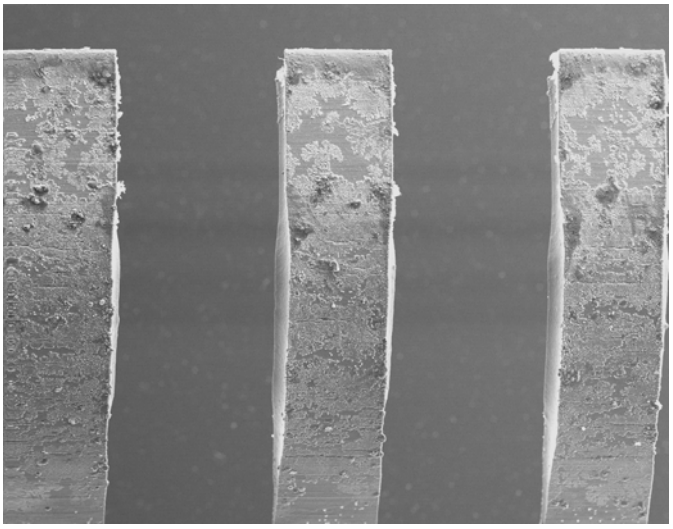

Figure 5. QFP Outside of Tray After 48-Hour Exposure to Class 2 Environment

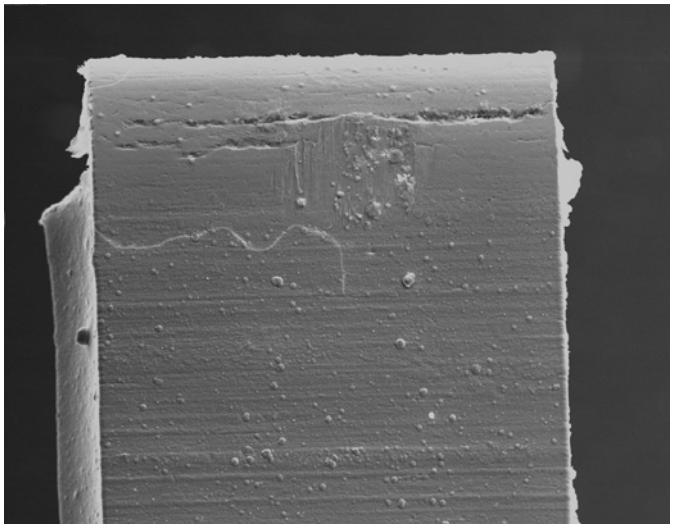

Figure 6. QFP Lead, Stored in Tray After 48-Hour Exposure to Class 2 Environment

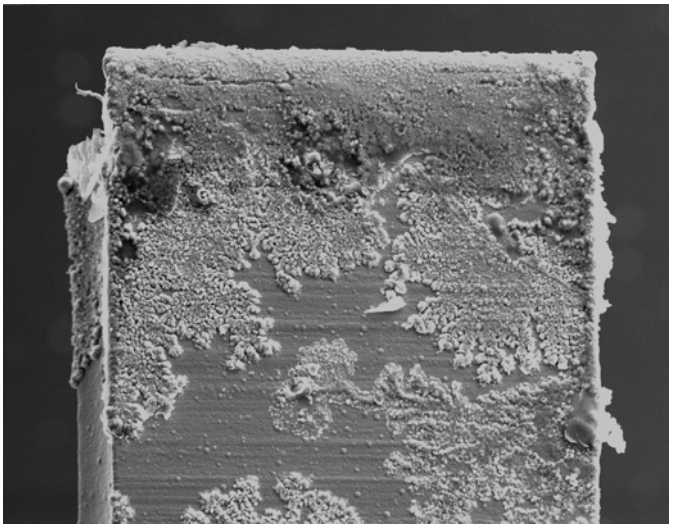

Figure 7. QFP Lead, Stored Outside of Tray After 48-Hour Exposure to Class 2 Environment

The results for the surface-mount solderability test method are shown in Table 3. Results are shown as sample size/number of fails for each group.

Table 3. Solderability Test Results

CLASS 2 EXPOSURE HOURS	GROUP 1 20-PIN SOIC OUTSIDE OF PACKING	GROUP 2 20-PIN SOIC TUBES	GROUP 3 20-PIN SOIC TAPE AND REEL	GROUP 4 80-PIN TQFP OUTSIDE OF PACKING	GROUP 5 80-PIN TQFP TRAY
12	4/0	4/0	4/0	4/0	4/0
24	3/3	4/0	4/0	4/2	4/0
36	4/4	4/0	4/0	4/4	4/0
48	4/4	4/0	4/0	3/3	3/0
72	4/4	4/0	4/0	3/3	4/0
96	5/5	4/0	4/0	4/4	6/0

Confirmation that the test conditions were as expected is shown in Table 4 and Figure 8. Two methods were used to assess test conditions. Simple mass gain measurements were taken and then converted to film thickness, using the area of the coupon and the average density of the film based on previously published experimental observations. The second method was an electrochemical reduction of the corrosion film. This method allows one to distinguish between CuO and Cu_2S, and is the reason for the *Percent Oxide* column in Table 4. The measurements on test coupons show good agreement between the film thickness calculated by mass gain and by electrochemical reduction. Based on field observations for films of these thicknesses, the acceleration factor for this test is roughly 730:1 or 48 hours = 4 years, as expected. At short exposure time, there is a discrepancy between the electrochemical reduction method and the mass gain. This, in part, may be caused by the error in weighing very small masses of material.

Table 4. Corrosion Effects on Copper Control Specimens

SPECIMEN NUMBER	EXPOSURE TIME (HOURS)	MASS GAIN (mg)	FILM THICKNESS BY MASS GAIN (ANGSTROM)	EQUIVALENT YEARS	FILM THICKNESS BY E-CHEM REDUCTION (ANGSTROM)	PERCENT OXIDE	EQUIVALENT YEARS	AVERAGE YEARS
1	24	0.18	730	1.3	1317	19%	2.4	
2	24	0.17	689	1.3	1277	16%	2.3	2.4
3	48	0.56	2269	4.1	2234	22%	4.1	
4	48	0.51	2066	3.8	2162	24%	3.9	4
5	72	0.84	3403	6.2	3624	25%	6.6	
6	72	0.91	3687	6.7	3644	24%	6.6	6.6
7	96	1.12	4538	8.3	4437	29%	8.1	
8	96	1.29	5277	9.5	4880	30%	8.9	
9	96	1.29	5277	9.5	4448	36%	8.1	8.4

Figure 8 graphically shows the data from Table 4. On the left Y-axis of the table, exposure time is expressed in hours. On the right Y-axis, units are the corresponding equivalent shelf times expressed in years (48 hours = 4 years) based on field observations. For each copper control specimen taken from the chamber at the various read points, the exposure time in hours is plotted against the Y-axis on the left side of the table. Equivalent years by mass gain and electrochemical reduction of the corrosion film are plotted against the Y-axis on the right side of the table for each specimen. Figure 8 graphically displays good correlation between measurements on test coupons and between the film thickness calculated by mass gain and by electrochemical reduction.

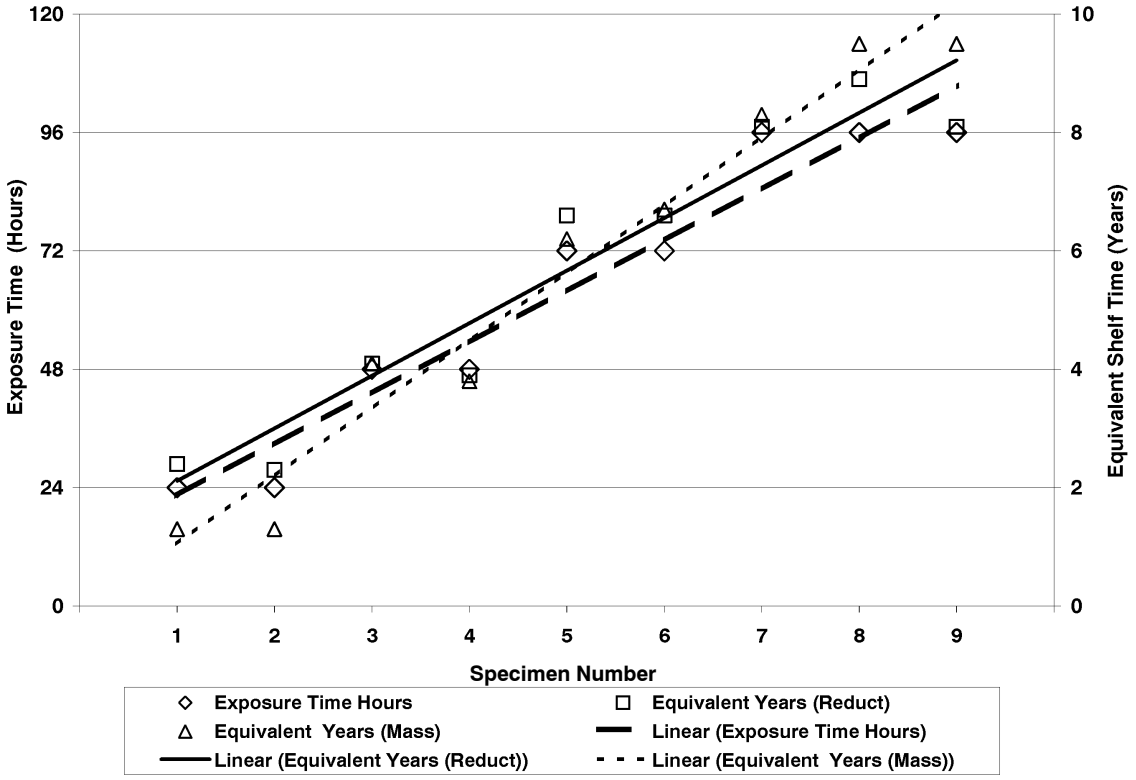

Figure 8. Time Acceleration Data for Battelle Class 2 Mixed Flowing-Gas Test

Conclusion

The results of this study indicate that NiPd-finished components can achieve good solderability after eight years of shelf storage in normal packing materials (tubes, trays, tape and reel). Finished ICs typically are stored in the tubes, trays, or tape-and-reel packing materials until immediately before being soldered by the end user. When storage is completely open to the atmosphere, with no packing materials, the Ni/Pd-finished components achieve good solderability after being stored for over one year.

Acknowledgment

The authors of this application report are Donald C. Abbott, Raymond A. Frechette, Gardner Haynes, and Douglas W. Romm.

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Steam-Age Evaluation of Nickel/Palladium Lead Finish for Integrated Circuits

SZZA004
September 1998

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Abstract

Removal of lead (Pb) from finished integrated-circuit (IC) packages, as well as IC package assembly and printed circuit board (PCB) assembly operations, is an ongoing effort by many electronics manufacturers. Toward this end, the semiconductor industry is converting to nickel/palladium (Ni/Pd)-finished leadframes in the assembly of integrated circuits. This technology eliminates Pb from the IC package. The best estimates are that more than 30 billion ICs are in the field with Ni/Pd-finished leads.

Historically, users of IC components have employed steam aging prior to solderability testing to simulate accelerated aging of devices, to stress devices to accentuate or magnify lead-finish defects, and to provide a "guard band" of performance for incoming product inspection. Preconditioning of IC leads by steam aging is well known and established for solderability testing of tin/lead (Sn/Pb)-finished leads. This study compares solderability performance of Ni/Pd-finished components, both after steam aging and shelf storage, to determine the relevance of steam aging for preconditioning Ni/Pd-finished IC packages.

Several groups of Ni/Pd-finished ICs were chosen for testing. Units that had been stored on a shelf in a warehouse environment for up to 51 months were used as a baseline for comparison. Recently built units (9 months old) were also tested with no steam aging, 1-hour steam aging, and 8-hour steam aging. Tests performed were wetting balance, measurement of the palladium thickness, cross-section after board mount, solderability test per ANSI/EIA-638, lead pull, and surface analysis using Auger electron spectroscopy.

Mechanical and solderability tests showed good results for all groups. However, the wetting-balance test showed delayed wetting for the steam-aged groups. Surface analysis of all groups showed that silicon (Si) and elevated carbon (C) were found on the surface of the steam-aged units. No Si was seen on shelf-aged units. These artifacts of the steam-aging test method do not correlate with normal aging or normal stressing of the package leads and can contribute to erroneous solderability test results. Previous studies have shown that constituents of the mold compound are picked up in the steam during steam aging and deposited onto the surface of the leads. Silicon and carbon are major components of the mold compound and hinder dissolution of the palladium when deposited onto the leads during steam-aging exposure.

Background

Ni/Pd finished leads offer several advantages to the IC maker and the end user [1,2,3,4]. This finish eliminates Pb from the IC manufacturing process and, when used with a Pb-free solder paste, allows elimination of Pb from the final electronic product [5,6,7,8]. Other advantages that accrue to the leadframe maker are elimination of cyanide from the process flow, elimination of selective plating, and use of simplified, high-speed manufacturing flow. For the IC assembly operation this finish removes the need for solder-plating equipment and associated personnel, waste treatment, process water supply, and floor space required for these operations. Use of Ni/Pd plated leadframes also reduces cycle time, eliminates solder flakes and burrs in the trim/form operation, and improves lead tip planarity. At the board level, this finish was designed to be a drop-in replacement for Sn/Pb-finished leads.

The process of steam aging consists of placing IC units above boiling water inside a test chamber for a specified period of time. Typically, the test specimens are located 1.5 to 3 inches above the boiling water. There are two types of steam-aging systems in use. One type is a glass beaker that sits on a hot plate and is filled with deionized water to a specified level. The ICs rest on a perforated plastic or ceramic plate suspended above the water. The second type of steam-aging system is a rectangular box made of Teflon™-coated stainless steel. With this system, the units are placed in drawers that are inserted into the chamber. Each drawer has a perforated bottom panel that allows the steam to pass through. After steam aging by either system, the IC units are tested for solderability using various standard test methods.

Currently, in ANSI/J-STD-002 [9] Ni/Pd-finished components are considered "Category 2: ...non Sn/Pb finishes," requiring 1 hour of steam aging prior to testing for solderability. The default steam aging time for Sn and Sn/Pb finished components is 8 hours.

Teflon is a trademark of E. I. du Pont de Nemours and Company.

A major issue encountered during the implementation of Ni/Pd finish at a new user (IC assembly site or PCB assembly house) is solderability test performance after steam aging. When performed with well-controlled equipment and procedures, steam aging presents no problems for Ni/Pd-finished components. However, when control is lacking, either in the performance of the test or maintenance of the equipment, solderability test performance after steam aging can be impacted negatively.

Historically, dip-and-look solderability testing of steam-aged Ni/Pd-finished components can result in small solder voids on the surface of the leads. When analyzed using Auger electron spectroscopy, these voids show a layer of C covering Pd at the bottom of the nonwet area. The reason is that a C-rich coating is deposited during the steam-aging process. The C layer masks the Pd surface from contact with the molten solder and prevents dissolution of the Pd and contact with the Ni by the solder.

This study was undertaken to evaluate board-mount and solderability test performance of Ni/Pd-finished components of various ages and after steam aging.

Procedure and Test Results

Seven groups of 20-pin small-outline integrated-circuit (SOIC) packages were tested in this evaluation (see Table 1). The units tested included four groups of Ni/Pd finished components that had been stored on a shelf in a warehouse environment for various times. Recently built units also were tested with no steam aging, 1-hour steam aging, and 8-hour steam aging.

Table 1. Aging Time of 20-Pin SOIC Packages Used in the Evaluation

GROUP	AGE
1	51 months
2	38 months
3	25 months
4	23 months
5	9 months
6	9 months + 1 hour of steam aging
7	9 months + 8 hours of steam aging

Cross-Section After Board Mount

Units from each of the seven groups were mounted on PCBs using an industry-standard water-soluble solder paste [10]. The reflow oven used was a BTU model VIP98A convection reflow with no nitrogen purge. After board mounting, individual units from each group were sectioned to document the contact angle to the backside of the lead. The contact angle is the angle formed by the tangent to the backside of the lead and the tangent to the solder fillet at the point of contact of the lead with the fillet. In general, lower contact angles indicate a soldering condition that has produced good results; higher contact angles indicate either a situation where the wetting rate has been decreased or where the equilibrium wetting point has changed [11]. Typical cross-section results for groups 1, 5, 6, and 7 are shown in Figures 1, 2, 3, and 4. Visual results show good solder wetting on all seven groups independent of shelf storage time or steam exposure.

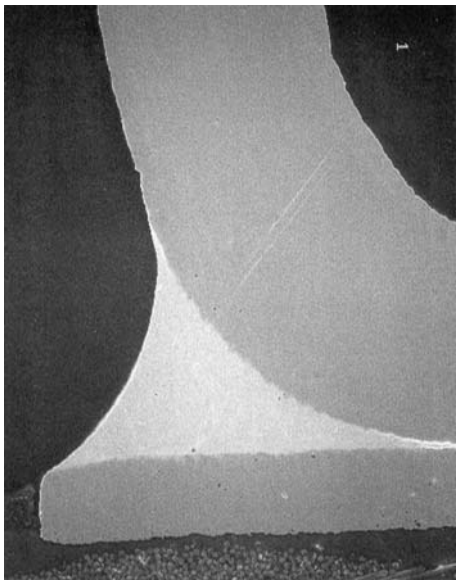

Figure 1. 51 Months of Shelf Storage

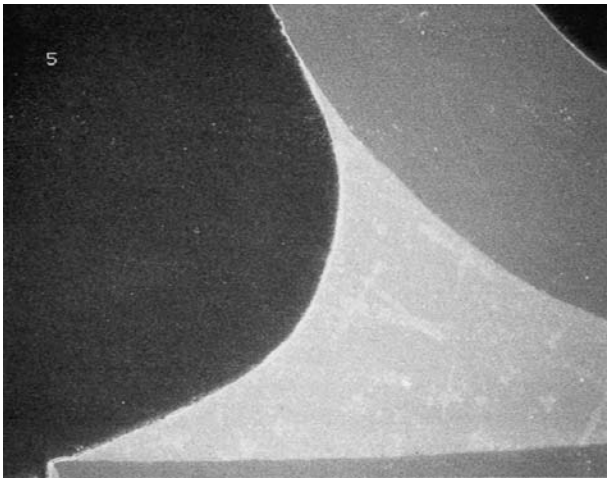

Figure 2. 9 Months of Shelf Storage

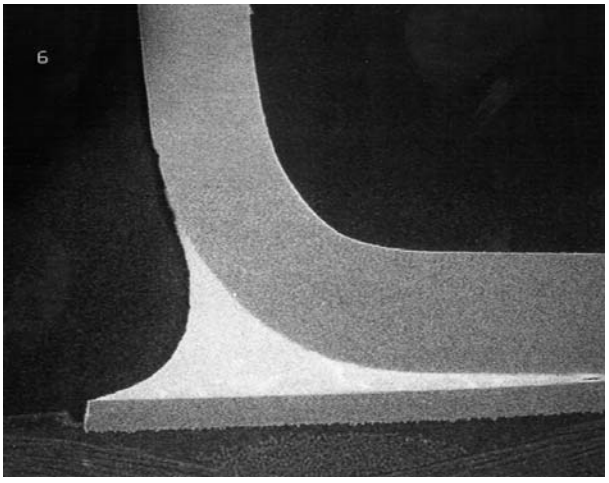

Figure 3. 9 Months of Shelf Storage + 1 Hour of Steam Aging

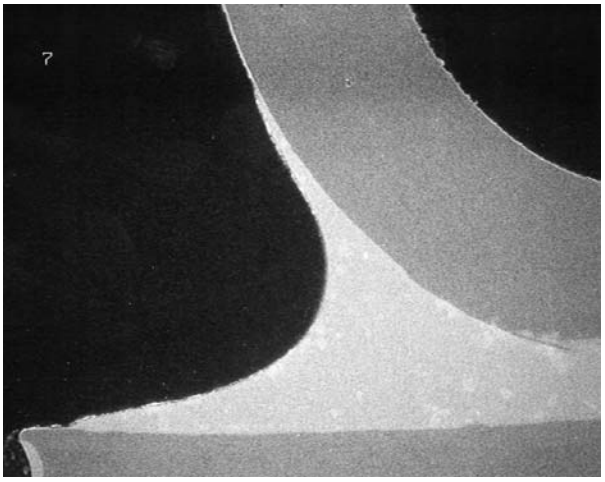

Figure 4. 9 Months of Shelf Storage + 8 Hours of Steam Aging

Contact-angle measurements were taken for each of the seven groups and the average for each group is shown in Figure 5. Steam aging or shelf aging appeared to have no effect on contact angle.

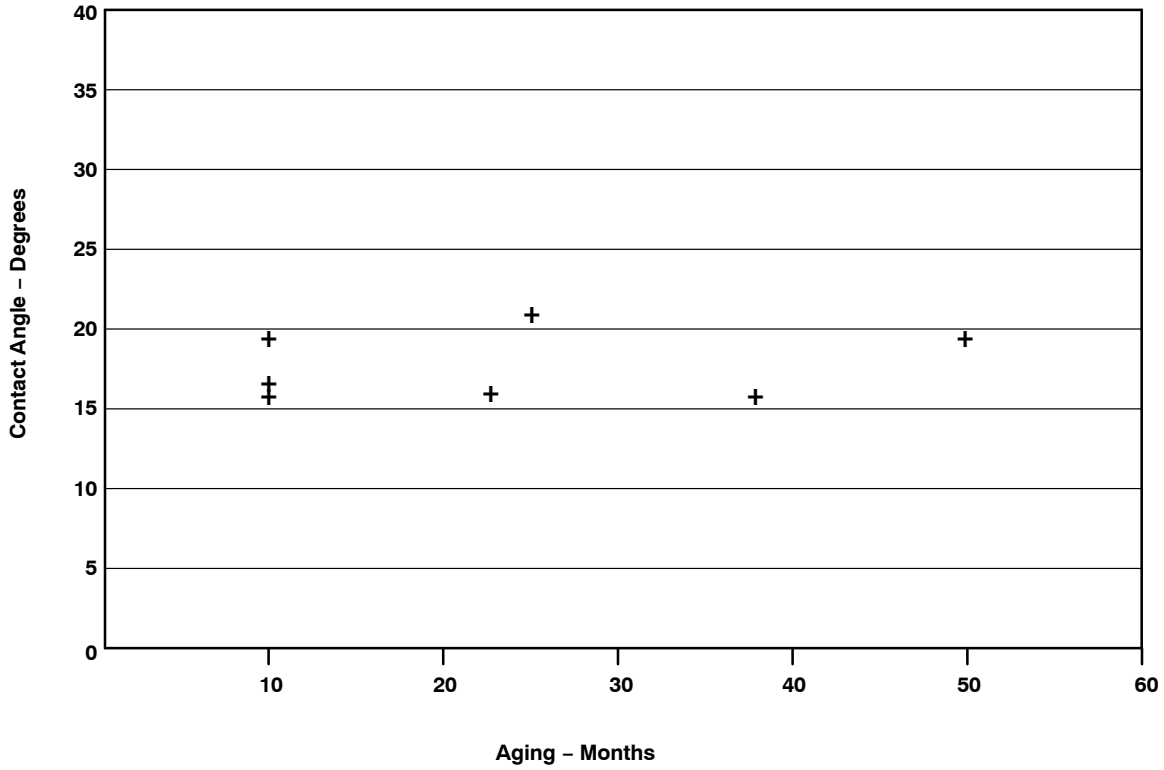

Figure 5. Contact-Angle Measurements vs Age

Wetting-Balance Test

The wetting-balance test can be used to test wettability of IC leads. The wetting-balance test is classified in ANSI/J-STD-002 as a "Test Without Established Accept/Reject Criterion." This test method is recommended for engineering evaluations only, not as a production pass/fail monitor.

The wetting-balance test measures the forces imposed by the molten solder on the test specimen (IC lead) as the specimen is dipped into and held in the solder bath. This wetting force is measured as a function of time and plotted. A typical wetting-balance curve is shown in Figure 6.

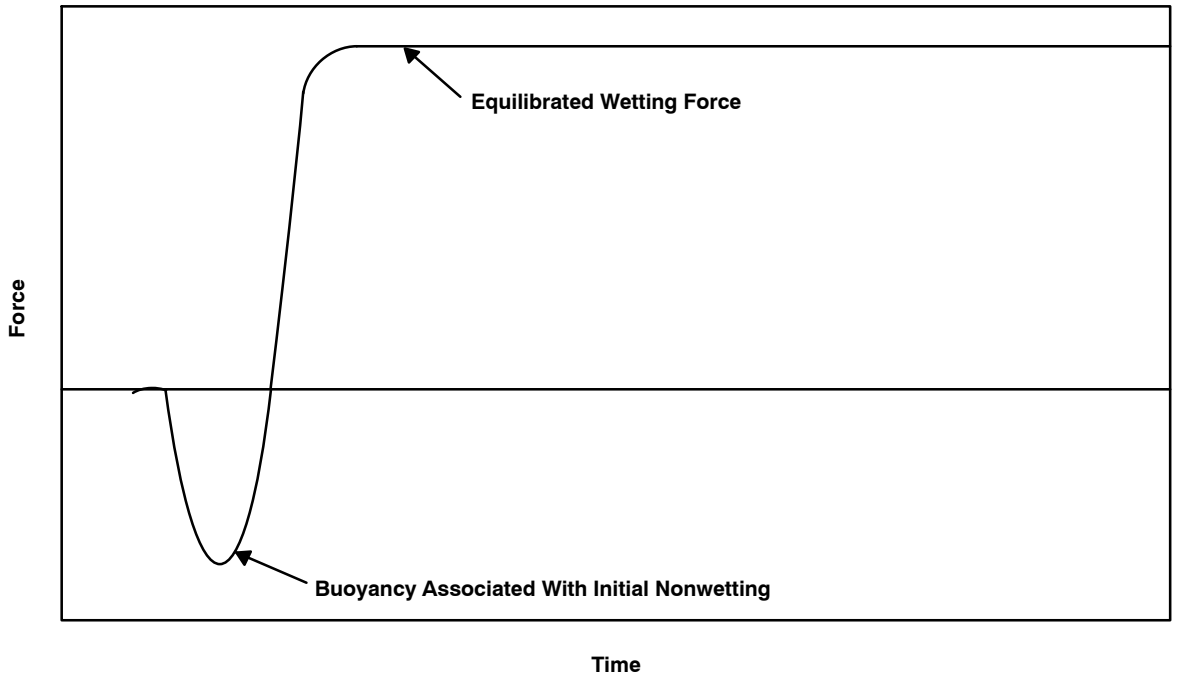

Figure 6. Typical Wetting-Balance Curve

Initially, the force is negative, indicating that the solder has not begun to wet the specimen and, in fact, shows a bouyancy effect. The force exerted by the solder approaches zero as the solder begins to wet to the specimen. One commonly used performance measure is the time to cross the zero axis of wetting force. This point indicates the transition from nonwetting (F<0) to wetting (F0).

Wetting-balance measurements were taken for each group. Ten readings were taken per group and the average time to zero for each group was recorded. Palladium-thickness readings also were taken on each group to see if the thickness of the palladium had any impact on wetting time. Palladium-thickness measurements and wetting-balance readings are shown in Table 2.

Table 2. Palladium-Thickness Measurements and Wetting-Balance Readings

GROUP	AGING (months)	Pd THICKNESS (microinches)	TIME TO CROSS ZERO (seconds)
1	51	4.7	1.09
2	38	4.9	1.41
3	25	3.6	1.35
4	23	4.2	1.02
5	9	3.5	0.75
6	9 months + 1 hour of steam aging	3.5	1.38
7	9 months + 8 hours of steam aging	3.5	3.37

Time-to-zero is plotted against aging time and palladium thickness in Figures 7 and 8.

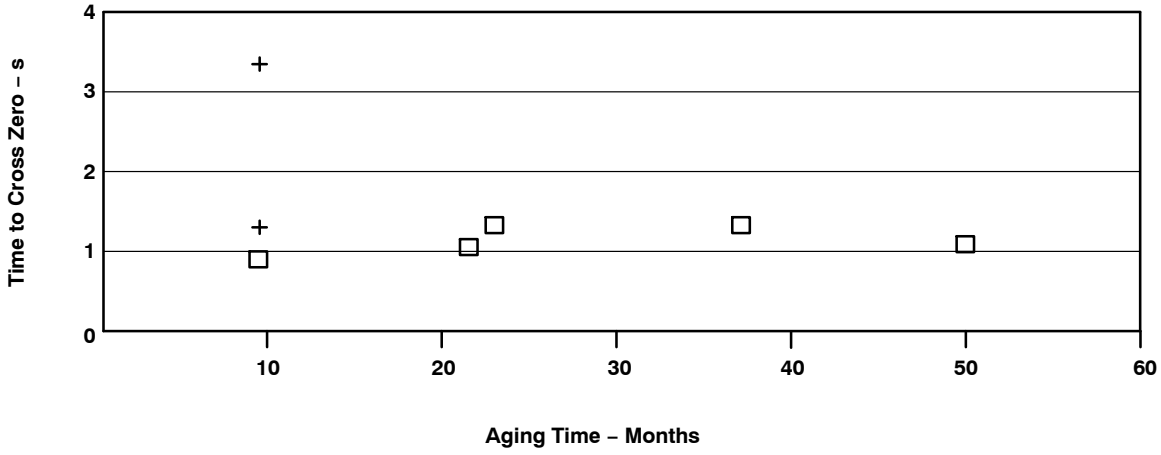

Figure 7. Average Time to Zero vs Aging Time

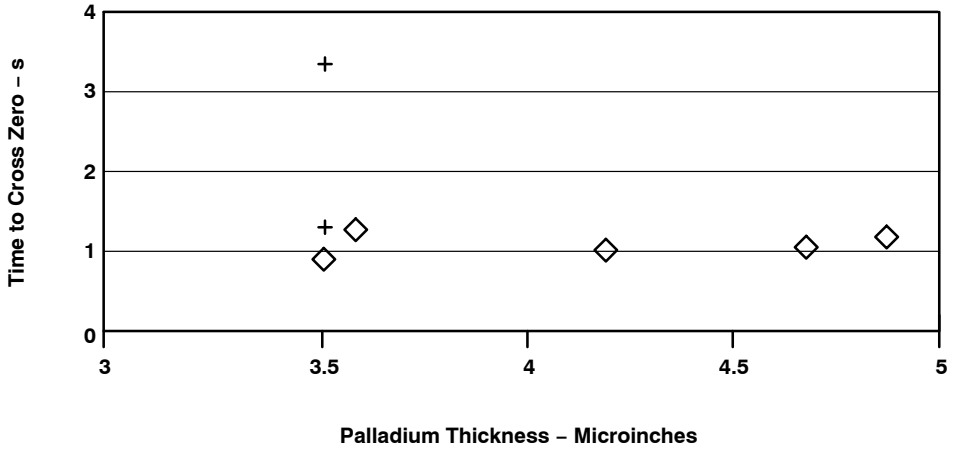

Figure 8. Average Time to Zero vs Pd Thickness

The time-to-zero values for the steam-aged groups are shown with a "+". Results indicate that wetting time is not affected by normal shelf storage. However, steam aging did have a dramatic impact on wetting time for both 1-hour and 8-hour steam aging. Palladium thickness for these samples had no impact on wetting time.

Lead Pull

Lead-pull testing was performed to determine the mechanical force needed to pull the individual IC leads from the PCB land pattern after soldering. First, to allow for access to an individual lead on the PCB, the leads are cut near the package body. Next, with the leads separated from the package body, the PCB is fastened in a test fixture. Then the lead is pulled until it separates from the PCB. The force needed to pull the lead from the PCB is measured and recorded.

Lead pull was performed on ten units from each of the seven groups. The average lead-pull value for each group is plotted against shelf-aging time of the components in Figure 9.

Lead-pull values for groups 5, 6, and 7 overlap, indicating that steam age had no impact on lead-pull strength, contrary to the impact on wetting-balance performance. In fact, there is no significant difference between any of the seven groups in lead-pull results, indicating good adhesion to the PCB, independent of shelf age.

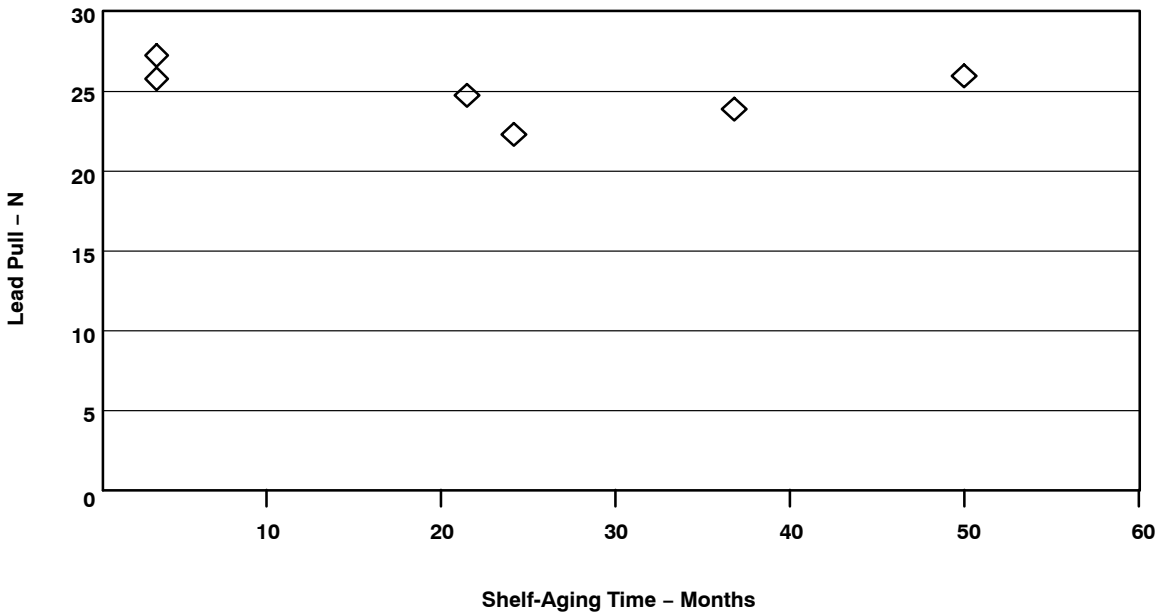

Figure 9. Lead-Pull Force vs Shelf-Aging Time

Surface-Mount Solderability Test

Solderabilility testing was performed per the ANSI/EIA-638 Surface Mount Solderability Test method [12]. This test procedure begins with screening solder paste onto a 0.035-inch-thick ceramic plate using a solder stencil. The paste print mirrors the pattern of the leads to be tested. The devices to be tested are then placed onto the solder paste print. The ceramic substrate is processed through a reflow cycle, then allowed to cool. After reflow, the units are removed from the ceramic and inspected. The benefit of this test method is that the IC devices are subjected to the same reflow environment as used in actual processing, and use of a ceramic substrate allows for inspection of the surface to be soldered.

Pass/fail criteria indicated in ANSI/EIA-638 says “all terminations shall exhibit a continuous solder coating free from defects for a minimum of 95% of the critical surface area of any individual termination. Anomalies other than dewetting, nonwetting, and pinholes are not cause for rejection.” The critical surface area for gull-wing components is defined as the underside of the lead up to 1× the thickness of the lead and the edges (sides) also up to 1× the lead thickness. Units from all seven groups were tested and inspected per ANSI/EIA-638. Typical solderability test results for groups 1, 5, 6, and 7 are shown in Figures 10, 11, 12, and 13. No failures were seen on any of the groups when this solderability test method was used.

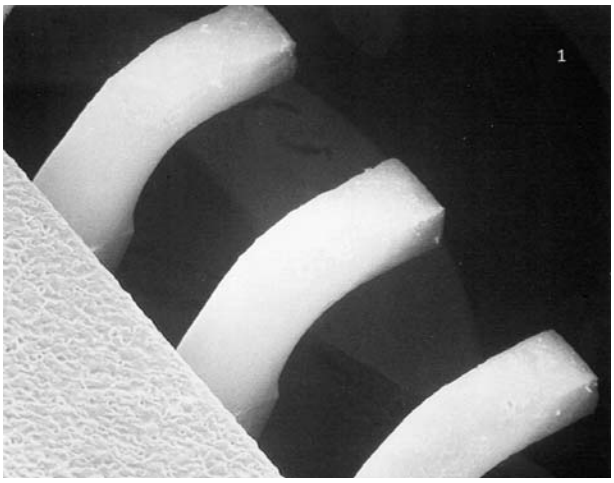

Figure 10. 51 Months of Shelf Storage

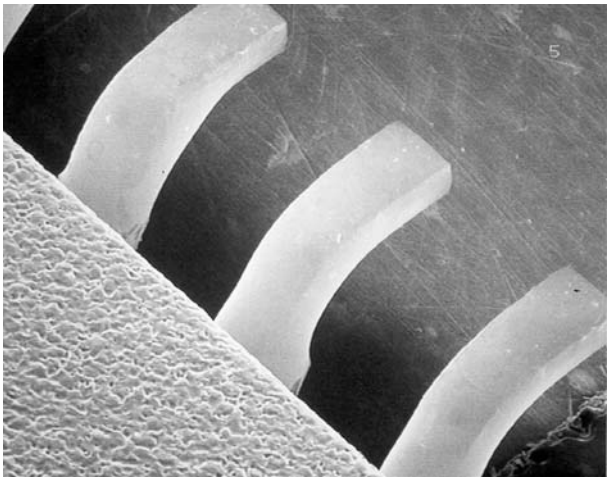

Figure 11. 9 Months of Shelf Storage

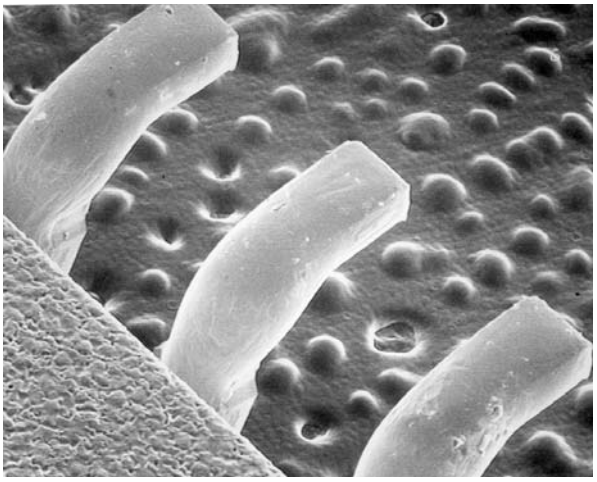

Figure 12. 9 Months of Shelf Storage + 1 Hour of Steam Aging

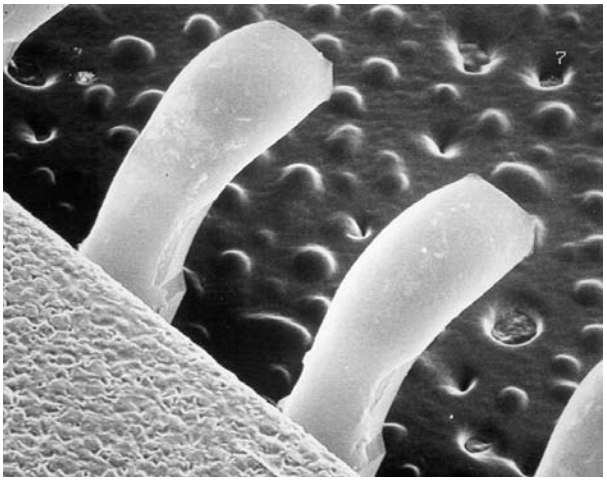

Figure 13. 9 Months of Shelf Storage + 8 Hours of Steam Aging

Surface Analysis

Surface analysis of the leads was performed on units from each group. Auger electron spectroscopy was used to scan the surface of the leads and identify the chemicals present. This surface analytical technique is widely applied to determine chemical composition of solid-state surfaces and interfaces in various fields of materials research. Results are presented in Table 3.

Table 3. Auger Electron Spectroscopy Surface-Analysis Results

		ELEMENTAL CONTENT ON SURFACE (ATOMIC %)							
GROUP	AGE	S	C	Pd	N	O	Ni	Cu	Si
1	51 months	6.9	46.7	26.4	7.4	12.6	0	0	0
2	38 months	10.9	27.8	47.6	6.0	7.7	0	0	0
3	25 months	11.2	46.4	35.4	3.0	4.1	0	0	0
4	23 months	5.0	44.7	34.5	5.7	10.1	0	0	0
5	9 months	4.3	63.1	25.1	2.8	4.7	0	0	0
6	9 months + 1 hour of steam aging	0.5	80.7	1.0	2.9	4.8	0	0	10.1
7	9 months + 8 hours of steam aging	2.3	55.4	14.1	3.2	8.7	0.2	0.8	15.2

The Auger spectra were taken on the foot of the leads from each group. All of the data on the groups that were not subjected to steam aging is fairly consistent, with Pd in the range of 25–50%, carbon (C) being 25–65%, and the balance was small amounts of sulfur (S) and nitrogen (N). For the steam-aged samples, the Pd levels are less than 15%, C in the range of 50–80%, and significant silicon (Si) in the range of 10–15%. No Si was seen on any of the shelf-aged units, only on the steam-aged units. Silicon is a major component of the mold compound used to encapsulate the package and, along with carbon, hinders dissolution of the palladium when deposited onto the leads during steam-aging.

Occasionally, failures are seen during dip-and-look solderability testing of Pd-finished components. Previous work has shown that the majority of steam-aged palladium solderability nonwets result from the palladium adsorbing an organic compound by during the steam-aging process. The organic has been identified as mold compound or some constituent of the mold compound using Fourier Transform Infrared Spectroscopy (FTIR). The same organic also has been found in the steam-aging water. The silicon seen on steam-aged units during this study correlates with this previous work that identified mold compound constituents on the leads and in the steam-aging water. The fact that the steam-aging process can cause the leads to be coated with mold compound residue, thus inhibiting dissolution of the palladium, indicates that steam aging is not a valid preconditioning method for Pd-finish IC packages.

Conclusion

All of the tests performed, except wetting balance and Auger electron spectroscopy analysis, showed good correlation between the steam-aged samples and the natural shelf-aged samples. The wetting-balance test showed a marked degradation in wetting time for the steam-aged samples. The Auger results show the presence of atypical Si contamination and elevated C on the surface of the steam-aged samples when compared to shelf-aged samples.

From the results shown in this application report and the experience noted with steam-age testing of both solder finished and Ni/Pd finished parts in commercial use, it can be concluded that steam-age exposure inordinately affects solderability test performance of Ni/Pd-finished units. This statement particularly applies if pass/fail is based on either wetting-balance or dip-and-look testing. Steam aging is not a proper preconditioning treatment for Ni/Pd-finished components because constituents of the mold compound can be deposited on the surface of the leads, a phenomenon which does not occur naturally. This view is supported by the wholly different mechanisms of soldering for the two finishes — dissolution of Pd versus reflow of Sn/Pb — that render leads more susceptible to solderability test failures caused by contamination of the lead surface during steam aging.

Acknowledgment

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Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices

SCZA005B
March 1998

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Contents

Thermal Considerations for Standard Linear and Logic (SLL) Packages and Devices

Users of Texas Instruments (TI™) SLL products must consider device power dissipation, package power capability, and maximum ambient temperatures when designing with these products. The product users also need to be aware of the long-term reliability impact of maximum device-junction temperatures.

This application report is intended to help users understand and evaluate these factors. Three concepts — package thermal performance, device power dissipation, and reliability — are discussed in separate sections.

The first section, *Package Thermal Performance*, includes data about the recently developed EIA/JEDEC Standard JESD 51 for package thermal-impedance measurement. It discusses most SLL package types and lists θ_{JA} (thermal impedance) values for those packages.

The second section, *Power Calculation*, discusses the power consumption by CMOS and BiCMOS/bipolar semiconductors. Standard formulas are given that allow the user to calculate the maximum power dissipated by a device in a typical application using data-book specifications, operating frequency, and voltage. The only characteristic not readily known is the output loading of the devices under consideration.

The third section, *Benefits of Minimizing Power Consumption*, discusses ways to reduce power consumption and the benefits thereof.

The final section, *Reliability Implications*, discusses the effects of chip temperature on reliability and electromigration. Information presented in this section allows the user to make an informed judgment as to the maximum chip temperature versus device wearout acceptable in the particular application.

The recommended analysis procedure is to assume a maximum chip temperature (see *Reliability Implications*) then, using θ_{JA} values for the chosen package (see *Package Thermal Performance*) and the known environmental requirements, calculate the maximum permissible power for that package. The formula presented in the *Power Calculation* section can then be used to ensure the operating conditions do not exceed the power capability of the chosen package type. Of course, the user can choose to calculate the maximum power from the application, then select a package that can meet the power dissipation requirement.

Package Thermal Performance

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the chip junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_j - T_a}{P} \quad (1)$$

Where:

T_j = chip junction temperature
T_a = ambient temperature
P = device power dissipation

θ_{JA} values are also the most subject to interpretation. Factors that can greatly influence the measurement and calculation of θ_{JA} are:

- Whether or not the device is board mounted
- Trace size, composition, thickness, and geometry
- Orientation of the device (horizontal or vertical)
- Volume of the ambient air surrounding the device under test and airflow
- Whether other surfaces are in close proximity to the device being tested

JEDEC established the JC 15.1 committee, comprising industry representatives, to develop industry-standard specifications for thermal testing. The specifications include development of electrical test procedures, careful descriptions of appropriate test environments, guidelines for the design of thermal test chips, guidelines for thermal modeling, and specifications for component mounting. The specifications for component mounting are divided into a series for different package types. The specifications include test-board descriptions for low effective thermal-conductivity test boards with a single metal layer and high effective thermal-conductivity test boards with embedded solid copper planes simulating system power and ground planes.

In August 1996, the Electronics Industries Association released JESD 51-3 titled *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*. The standard describes guidelines with parameters for thermal-test-board design for low effective thermal conductivity (one signal layer in the trace fanout area) as differentiated from a multilayer printed-circuit board (PCB), which might include power and ground planes. The specified parameters include the area of the test board, the amount of copper traces on the test board, and the resulting trace fanout area, each important to the heat-sinking characteristics of the PCB. Prior to release of the standard, thermal-impedance data for similar packages varied widely within the industry due to the use of different test-board designs. As the industry adopts this standard methodology, thermal-impedance variations from test-board design should be minimized.

Key features of the standard test-board design are:

- Board thickness: 0.062 in.
- Board dimensions: 4.0 × 4.5 in. for packages > than 27 mm in length, 3.0 × 4.5 in. for packages ≤ 27 mm in length
- Trace thickness: 0.0028 in.
- Trace length: 25.0 mm (0.984 in.)

The SLL product group uses test boards designed to JESD 51-3 for thermal-impedance measurements. The parameters outlined in the standard also are used to set up thermal models. The thermal-model program used by SLL is ThermCAL, a finite-difference thermal-modeling tool.

Eleven SLL packages were tested using a JEDEC test-board design and compared to ThermCAL model results to validate the correlation between model results and data (see Table 1). This comparison shows that the models are accurate to within 10% of measured data. In many cases the model data varies from measured data by less than 5%.

Table 1. Package Comparison

PACKAGE TYPE (PINS, DESIGNATION)	DIE SIZE (mils)	θ_{JA} MEASURED (°C/W)	θ_{JA} MODELED (°C/W)	CHANGE (%)
56 DL	120 × 120	73.5	78.3	6.5
20 DW	62 × 62	96.6	90.9	–5.9
160 PCM	240 × 240	34.9	34.9	0
52 PAH†	120 × 120	87.2	92.2	5.7
52 PAH‡	120 × 120	72.7	75.2	3.4
100 PZ	360 × 360	45	42.8	–4.9
208 PDV	240 × 240	50.1	52.8	5.4
48 DGG	120 × 120	89.1	93.5	4.9
14 DGV	62 × 62	181.5	191.7	5.6
48 DGV	62 × 186	92.9	89.9	–3.2
100 PCA	240 × 240	33.3	34.9	4.8

† S-pad leadframe
‡ Conventional leadframe

After the accuracy of the model results was established, all other SLL packages could be modeled. θ_{JA} data based on JESD 51-3 is available for all SLL leaded surface-mount packages (see Table 2). The data is grouped by package type with values of θ_{JA} shown at different airflow levels. Leadframe pad size and die size are shown.

Junction-to-case thermal-impedance (θ_{JC}) data is shown with the junction-to-ambient data. Measured θ_{JC} data was generated for the packages tested using the JEDEC PCB. Previously published values of θ_{JC} are used for packages not yet tested using the PCB designed to JESD 51-3.

Table 2. SLL Package Thermal-Impedance Data

PIN COUNT	TI PACKAGE	JEDEC SPECIFICATION	PAD SIZE (mils)	CHIP SIZE (mils)	θ_{JA} (°C/W) AT AIRFLOW (LFM)				MEASURED/ MODELED	θ_{JC} (°C/W)
					0	150	250	500		
SOIC										
14	D	MS-012	70 × 70	32 × 37	126.6	104	96.4	87.4	Modeled	46
16	D	MS-012	90 × 90	44 × 65	112.6	91.2	83.9	74.8	Modeled	42
20	DW	MS-013	90 × 110	62 × 62	96.6	82.2	77.7	71.5	Measured	38.3
24	DW	MS-013	140 × 160	84 × 122	80.7	53.7	47.5	40.7	Modeled	25
28	DW	MS-013	120 × 140	90 × 128	78.2	54.3	48.4	41.9	Modeled	
SSOP										
14	DB	MO-150	71 × 71	43 × 52	158	128.6	118.9	106.5	Modeled	47
16	DB	MO-150	83 × 91	51 × 61	130.8	105.9	97.3	86.5	Modeled	47
20	DB	MO-150	87 × 106	61 × 65	114.6	92	84	74.7	Modeled	45
24	DB	MO-150	87 × 106	74 × 91	104.2	83.5	76.3	67.5	Modeled	42
20	DBQ	MS-137	96 × 140	61 × 75	118.1	95.3	86.9	76.7	Modeled	46
24	DBQ	MS-137	96 × 140	61 × 75	113	92	84.1	74.6	Modeled	42
28	DL	MO-118	150 × 180	97 × 142	97	77.2	70.9	63.1	Modeled	
48	DL	MO-118	120 × 180	73 × 128	93.5	69.9	63.8	57.1	Modeled	26
56	DL	MO-118	150 × 220	120 × 120	73.5	62.3	59	54.6	Measured	27.3
PLCC										
28	FN	MS-018	300 × 348	214 × 319	70.9	58.8	52.7	46	Modeled	26.7
44	FN	MS-018	270 × 270	235 × 235	46.2	38.6	35.4	31.6	Modeled	22
68	FN	MS-018	325 × 325	280 × 280	39.3	33	30.5	27.6	Modeled	14.5
84	FN	MS-018	275 × 275	188 × 185	39.7	33.9	31.8	29.4	Modeled	11.9
QFP										
52	RC	MS-022	210 × 210	120 × 120	78.9	48.4	43.6	38.1	Modeled	20
80	PH		265 × 265	232 × 240	76.1	67.9	61.4	53.6	Modeled	15.1
132	PQ	MO-069	315 × 315	272 × 272	46.3	34.5	31.6	28.3	Modeled	9.8
144	PCM	MS-022	433 × 433	338 × 338	38.8	27.3	25.1	22.4	Modeled	14.5
160	PCM	MS-022	511 × 511	433 × 433	34.9	29.9	28.3	24.7	Measured	11.4
208	PPM	MO-143	413 × 413	268 × 268	36.7	30.4	28.1	26.7	Modeled	
TQFP										
52	PAH	MO-136	S-Pad	120 × 120	87.2	76.1	71.5	67	Measured	28.3
52	PAH	MO-136	3.5 × 3.5 mm	120 × 120	72.7	62.6	59.2	53.8	Measured	24.0
64	PM	MO-136	6.75 × 6.75 mm	235 × 235	66.9	53.6	47.6	40.6	Modeled	10.4
64	PAG	MO-136	S-Pad	240 × 240	58.2	48.8	45.2	40.3	Measured	22.6
80	PN	MO-136	S-Pad	240 × 240	61.5	52.8	49.3	44.6	Measured	26.4
100	PZ	MO-136	S-Pad	360 × 360	45	38.3	35.3	27.9	Measured	7.6
100	PZ	MO-136	S-Pad	240 × 240	50.1	42.7	40.4	36.8	Measured	21.1
100	PCA	MO-136	6.5 × 6.5 mm	240 × 240	33.3	24.7	21.8	19.2	Measured	4.3
120	PCB	MO-136	6.5 × 6.5 mm	240 × 240	28.1	22.3	21	18	Modeled	3.3
144	PGE	MO-136	342 × 350	378 × 378	48.3	39.1	35.5	31	Modeled	9.9
208	PDV	MO-136	S-Pad	240 × 240	50.1	43.63	40.9	37.3	Measured	9.9

Table 2. SLL Package Thermal-Impedance Data (Continued)

PIN COUNT	TI PACKAGE	JEDEC SPECIFICATION	PAD SIZE (mils)	CHIP SIZE (mils)	θ_{JA} (°C/W) AT AIRFLOW (LFM)				MEASURED/ MODELED	θ_{JC} (°C/W)
					0	150	250	500		
SOP										
14	NS	EIAJ-TYPE-II	79 × 87	55 × 57	127.1	103.7	95.5	85.2	Modeled	95
16	NS	EIAJ-TYPE-II	87 × 142	76 × 86	111.3	89.3	81.4	71.5	Modeled	95
20	NS	EIAJ-TYPE-II	87 × 118	60 × 77	100.3	82.8	76.2	68	Modeled	90
TSSOP										
14	PW	MO-153	71 × 71	48 × 53	169.8	146.7	136	121.7	Modeled	35
16	PW	MO-153	104 × 104	56 × 76	148.9	127.9	117.6	103.9	Modeled	35
20	PW	MO-153	102 × 106	53 × 69	128	110.6	101.9	90.8	Modeled	34
24	PW	MO-153	94 × 140	74 × 91	119.9	98.8	90.6	80	Modeled	33
48	DGG	MO-153	4.6 × 3.2 mm	120 × 120	89.1	78.5	75.1	69.4	Measured	25.2
56	DGG	MO-153	3.94 × 5.08 mm	132 × 176	81.2	72.8	65.8	57.9	Modeled	13
64	DGG	MO-153	5.7 × 3.6 mm	120 × 120	72.9	63.3	61.8	57.1	Measured	21.3
TVSOP										
14	DGV	MO-194	75 × 75	62 × 62	181.5	165.8	159.5	150.4	Measured	66.7
16	DGV	MO-194	75 × 75	65 × 65	179.6	153.2	141.7	126.3	Modeled	
20	DGV	MO-194	104 × 104	94 × 94	146.1	122.3	111.6	97.4	Modeled	
24	DGV	MO-194	104 × 104	94 × 94	138.6	116.2	106.2	93.2	Modeled	
48	DGV	MO-194	100 × 240	62 × 186	92.9	80.9	77.1	71	Measured	27.2
56	DGV	MO-194	100 × 274	90 × 262	85.9	64.6	57.1	48.4	Modeled	
80	DBB	MO-194	100 × 224	93 × 203	105.6	78.4	71.8	63.7	Modeled	
PDIP (assumes zero trace length)										
8	P	MS-001			104					41
14/16	N	MS-001			78					32
20	N	MS-001			67					33
24	NT	MS-001			67					25
		BGA								
256	GFN	MO-151			42				ANAM data	6.2
388	GFW	MO-151			18.9				Model data	

Power Calculation

Reduction of power consumption makes a device more robust and reliable. When calculating the total power consumption of a circuit, both the static and the dynamic currents must be taken into account. Both bipolar and BiCMOS devices have varying static-current levels, depending on the state of the output (I_{CCL}, I_{CCH}, or I_{CCZ}), while a CMOS device has a single value for I_{CC}. These values can be found in the individual data sheets. TTL-compatible CMOS and BiCMOS inputs, when driven at TTL levels, also consume additional current because they may not be driven all the way to V_{CC} or GND; therefore, the input transistors are not switched completely off. This value, known as ΔI_{CC}, also is provided in the data sheet.

Due to the high operating frequencies, there is a strict limit on power consumption in computer systems. Therefore, allowable power consumption for each device on a board must be minimized. Power calculations are made to determine power-supply sizing, current requirements, cooling/heatsink requirements, and criteria for device selection. Power calculation also can determine the maximum reliable operating frequency.

There are two components that establish the amount of power consumption in a CMOS circuit:

- Static power consumption
- Dynamic power consumption

Dynamic power consumption results from charging and discharging external load and internal parasitic capacitances. The parameter for CMOS device parasitic capacitance is C_{pd}, which is listed in the data sheet and is obtained using equations 2 and 3:

$$C_{pd} = \frac{I_{CC}}{V_{CC} \times f_I} - C_{L(eff)} \quad (2)$$

$$C_{L(eff)} = C_L \times N_{SW} \times \frac{f_O}{f_I} \quad (3)$$

To explain the C_{pd} and the method of calculating dynamic power, see Table 3, which indicates the C_{pd} test conditions for AHC devices. The symbols used in Table 3 are:

V = V_{CC} (5 V)
G = ground (0 V)
1 = high logic level = V_{CC} (5 V)
0 = low logic level = ground (0 V)
X = don't care: 1 or 0, but not switching
C = 50% duty cycle input pulse (1 MHz) (see Figure 1)
D = 50% duty cycle input (1/2 frequency) out-of-phase input pulse (see Figure 1)
S = standard ac output load (50 pF to GND)

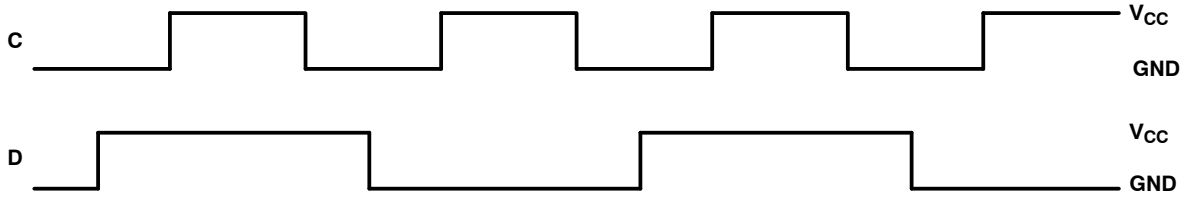

Figure 1. Input Waveform

Table 3 shows the switching of each pin for AHC devices. Once the C_{pd} is determined from the table, the P_D is easy to calculate using equations explained in the following sections.

Although a C_{pd} value is not provided for ABT and LVT, the I_{CC} versus frequency curves display essentially the same information (see Figures 2 and 3). The slope of the curve provides a value in the form of mA/(MHz × bit), which when multiplied by the number of outputs switching and the desired frequency, provides the dynamic power dissipated by the device without the load current. Equations 4 through 14 can be used to calculate total power for CMOS or BiCMOS devices.

Table 3. C_{pd} Test Conditions With One- or Multiple-Bit Switching

TYPE	PIN NO.																			
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
AHC00	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC02	S	C	0	S	X	X	G	X	X	S	X	X	S	V						
AHC04	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC08	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC10	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC11	C	1	X	X	X	S	G	S	X	X	X	S	1	V						
AHC14	C	S	X	S	X	S	G	S	X	S	X	S	X	V						
AHC32	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC74	1	D	C	1	S	S	G	S	S	X	X	X	1	V						
AHC86	C	1	S	X	X	S	G	S	X	X	S	X	X	V						
AHC138	C	0	0	0	0	1	S	G	S	S	S	S	S	S	S	V				
AHC139	0	C	0	S	S	S	S	G	S	S	S	S	X	X	X	V				
AHC240	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC244	0	C	S	X	S	X	S	X	S	G	X	S	X	S	X	S	X	S	X	V
AHC245	1	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC373†	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC374‡	0	S	D	D	S	S	D	D	S	G	C	S	D	D	S	S	D	D	S	V
AHC540	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC541	0	C	X	X	X	X	X	X	X	G	S	S	S	S	S	S	S	S	0	V
AHC573†	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V
AHC574‡	0	D	D	D	D	D	D	D	D	G	C	S	S	S	S	S	S	S	S	V

† All bits switching, but with no active clock signal

‡ All bits switching

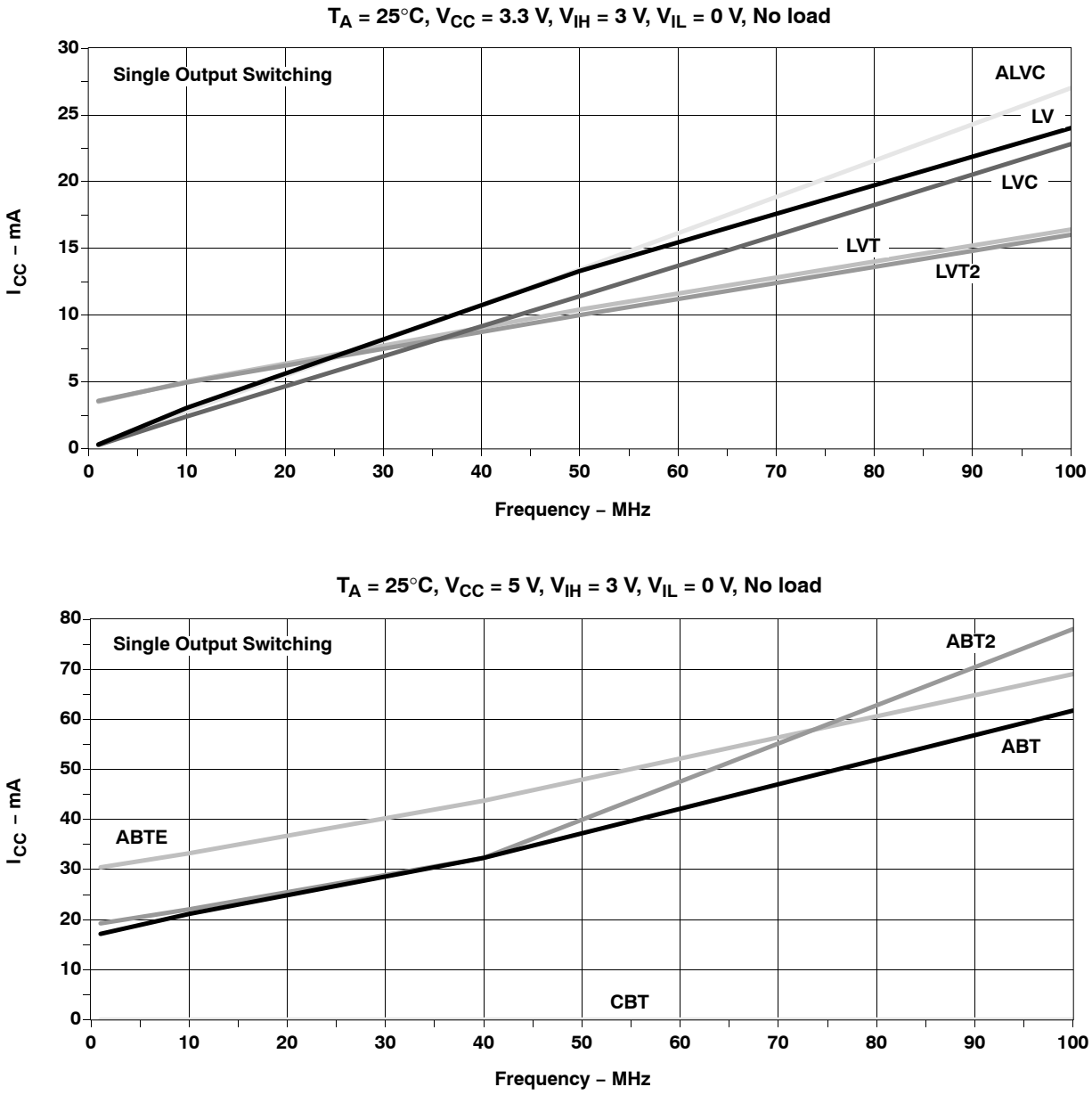

Figure 2. Power Consumption With a Single Output Switching

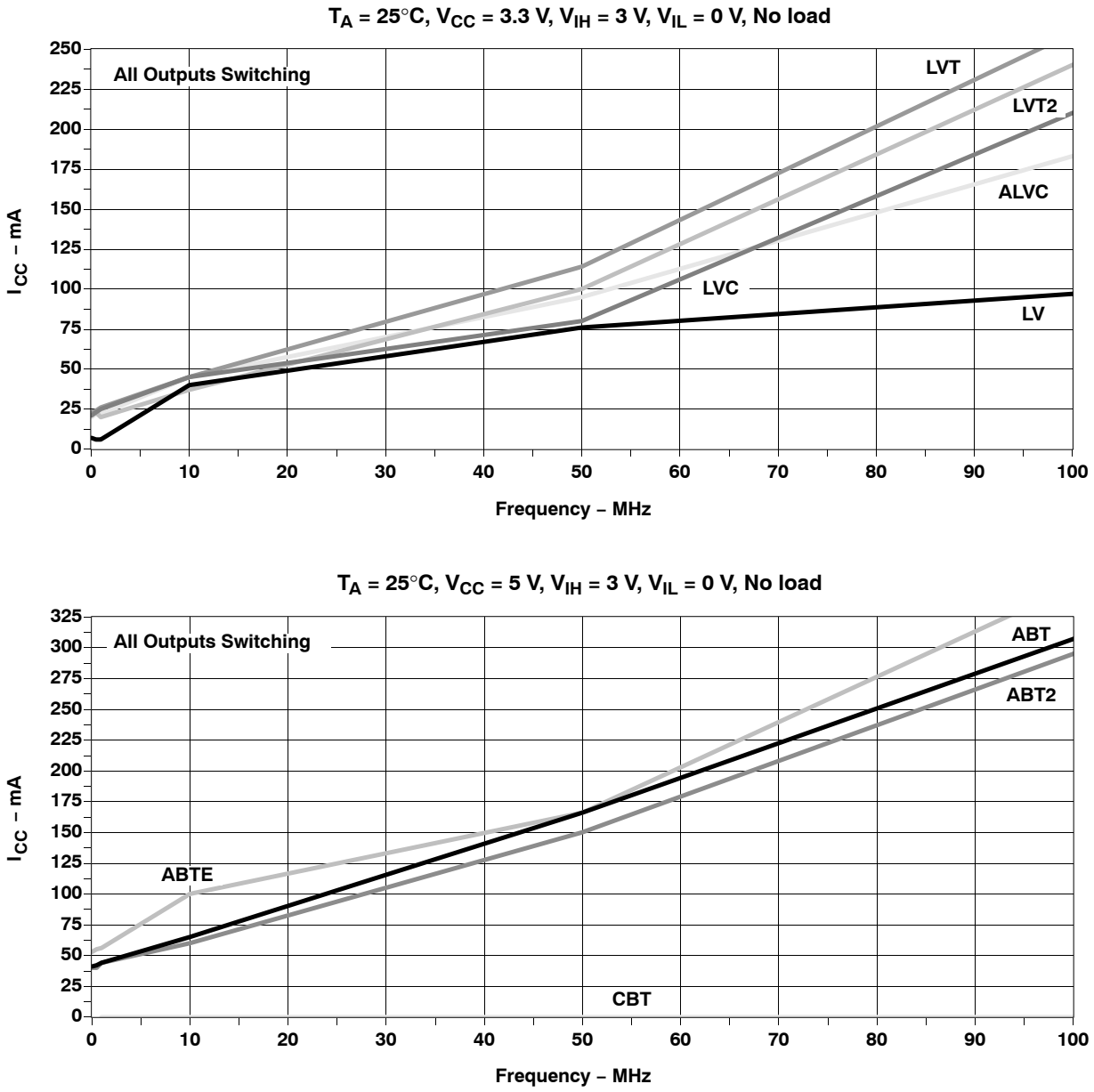

Figure 3. Power Consumption With All Outputs Switching

CMOS

CMOS-Level Inputs

Static power consumption can be calculated using equation 4.

$$P_S = V_{CC} \times I_{CC} \quad (4)$$

The dynamic power consumption of a CMOS device is calculated by adding the transient power consumption and capacitive-load power consumption.

Transient Power Consumption

The transient power is due to the current that flows only when the transistors of the devices are switching from one logic state to another. This power is a result of the current required to charge the internal nodes (*switching current*) plus the current that flows from V_{CC} to GND when the p-channel and n-channel transistors turn on briefly at the same time during the logic transition (*through current*). The frequency at which the device is switching, plus the rise and fall time of the input signal, as well as the internal nodes of the device, have a direct effect on the duration of the current spike. For fast input transition rates, the through current of the gate is negligible in comparison with the switching current. For this reason, the dynamic supply current is governed by the internal capacitance of the device and the charge and discharge current of the load capacitance.The transient power consumption can be calculated using equation 5.

$$P_T = C_{pd} \times {V_{CC}}^2 \times f_I \times N_{SW} \quad \textbf{(5)}$$

In case of single-bit switching, N_{SW} in equation 5 becomes 1.

Capacitive-Load Power Consumption

Additional power is consumed in charging of external load capacitance and is dependent on switching frequency. Equation 6 can be used to calculate this power while all outputs have the same load and are switching at the same output frequency.

$$P_L = C_L \times {V_{CC}}^2 \times f_O \times N_{SW} \text{ (C_L is the load per output)} \quad \textbf{(6)}$$

In case of different loads and different output frequencies at all outputs, equation 7 is used to calculate capacitive-load power consumption.

$$P_L = \Sigma(C_{Ln} \times f_{On}) \times {V_{CC}}^2 \quad \textbf{(7)}$$

Therefore, dynamic power consumption (P_D) is the sum of these two power consumptions, and is expressed in equation 8 (single-bit-switching case) and 9 (multiple-bit switching with variable load and variable output frequencies):

$$P_D = \left(C_{pd} \times f_I \times {V_{CC}}^2\right) + \left(C_L \times f_O \times {V_{CC}}^2\right) \quad \textbf{(8)}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma\left(C_{Ln} \times f_{On}\right)\right]{V_{CC}}^2 \quad \textbf{(9)}$$

Total power consumption with a CMOS-level input is the sum of static and dynamic power consumption.

TTL-Level Inputs

Similarly, with TTL-level inputs, both static and dynamic power consumption can be calculated using equations 10, 11, and 12.

$$P_S = V_{CC}[I_{CC} + (N_{TTL} \times \Delta I_{CC} \times DC_d)] \quad \textbf{(10)}$$

$$P_D = \left(C_{pd} \times f_I \times {V_{CC}}^2\right) + \left(C_L \times f_O \times {V_{CC}}^2\right) \text{ (single-bit switching)} \quad \textbf{(11)}$$

$$P_D = \left[\left(C_{pd} \times f_I \times N_{SW}\right) + \Sigma(C_{Ln} \times f_{On})\right]{V_{CC}}^2 \quad \textbf{(12)}$$

(multiple-bit switching with variable load and frequency)

BiCMOS

Static Power

$$P_S = V_{CC}\left\{DC_{en}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] + (1 - DC_{en})I_{CCZ} + (N_{TTL} \times \Delta I_{CC} \times DC_d)\right\} \quad \textbf{(13)}$$

Where:

ΔI_{CC} = 0 for bipolar devices

NOTE:
For a continuous waveform at 50% duty cycle, DC_{en} = 1.

Equation 13 becomes:

$$P_S = V_{CC}\left[\left(N_H \times \frac{I_{CCH}}{N_T}\right) + \left(N_L \times \frac{I_{CCL}}{N_T}\right)\right] \quad \textbf{(14)}$$

NOTE:
If half of the time the waveform is high and half of the time the waveform is low and the waveform is switching continuously, $\Rightarrow (N_H = N_L = 1/2\ N_T)$, P_S becomes:

$$P_S = \left(\frac{V_{CC}}{2}\right)(I_{CCH} + I_{CCL}) \quad \textbf{(15)}$$

Dynamic Power

$$P_D = (DC_{em} \times N_{SW} \times V_{CC} \times f \times I_{CCD}) \text{ Condition is } 50\ pF \parallel 500\ \Omega \quad \textbf{(16)}$$

I_{CCD} is calculated with 50 pF ‖ 500 Ω, and given number of outputs switching.

NOTE:
For a continuous waveform at 50% duty cycle, $DC_{en} = 1$.

Dynamic power with external capacitance:

$$P_D = DC_{en} \times N_{SW} \times V_{CC} \times f \times (V_{OH} - V_{OL}) \times (C_L - 50\ pF) + DC_{en} \times N_{SW} \times V_{CC} \times f \times I_{CCD} \quad \textbf{(17)}$$

I_{CCD} is calculated with 50 pF ‖ 500 Ω, and given number of output switching.

Power is also consumed by the upper output driver due to the output resistor (500 Ω in most load circuits for outputs in the data sheet). This power is very small but must be included in the dynamic power consumption calculation. Equation 18 is used to calculate this power consumption.

$$P_{\_Res} = (V_{CC} - V_{OH}) \times \frac{V_{OH}}{R} \quad \textbf{(18)}$$

NOTE:
Assume that the output waveform is always at logic high and is not frequency dependent.

Therefore, total dynamic power consumption is:

$$P_{D\_TOT} = P_D + P_{\_Res} \quad \textbf{(19)}$$

Finally, total power consumption can be calculated as:

$$P_{\_Total} = P_{D\_TOT} + P_S \quad \textbf{(20)}$$

Where:

V_{CC} = supply voltage (V)
I_{CC} = power-supply current (A) (from the data sheet)
I_{CCL} = power-supply current when outputs are in low state (A) (from the data sheet)
I_{CCH} = power-supply current when outputs are in high state (A) (from the data sheet)
I_{CCZ} = power-supply current when outputs are in high-impedance state (A) (from the data sheet)
ΔI_{CC} = power-supply current when one input is at a TTL level (A) (from the data sheet)
DC_{en} = % duty cycle enabled (50% = 0.5)

DC_d = % duty cycle of the data (50% = 0.5)
N_H = number of outputs in high state
N_L = number of outputs in low state
N_{sw} = total number of outputs switching
N_T = total number of outputs

N_{TTL} = number of inputs driven at TTL levels

f_I = input frequency (Hz)
f_O = output frequency (Hz)
f = operating frequency (Hz)
V_{OH} = output voltage in high state (V)
V_{OL} = output voltage in low state (V)
C_L = external-load capacitance (F)
I_{CCD} = slope of the I_{CC} versus frequency curve (A/Hz × bit)

$C_{L(eff)}$ = effective-load capacitance (F)
f_O/f_I = ratio of output and input frequency (Hz)
P_T = transient power consumption
P_D = dynamic power consumption
P_S = static power consumption
$P_{\_Res}$ = power consumption due to output resistance
P_{D_TOT} = total dynamic power consumption
$P_{\_Total}$ = total power consumption

C_{PD} = dynamic power dissipation capacitance (F)
P_L = capacitive-load power consumption
Σ = sum of n different frequencies and loads at n different outputs
f_{On} = all different output frequencies at each output numbered 1 through n (Hz)
C_{Ln} = all different load capacitances at each output numbered 1 through n

For GTL and BTL/FB devices, the power consumption/calculation is similar to a BiCMOS device with the addition of the output power consumption through the pullup resistor, since GTL is open drain and BTL/FB is open collector.

The total power calculated using these equations should be less than the package power dissipation mentioned in the data sheets. Otherwise, the device might not function properly.

Benefits of Minimizing Power Consumption

Power consumption can be minimized in a number of ways. DC power consumption can be reduced to leakage by using only CMOS logic, as opposed to bipolar and BiCMOS logic. The leakage, in turn, is proportional to the area of diffusion, so the use of minimum-size devices is an advantage. Dynamic power consumption can be limited by reducing supply voltage, switched capacitance, and the frequency at which the logic is clocked. Supply voltage tends to be a system design consideration, and low-power systems use 1.5-V to 3.3-V supplies.

Power consumption is a function of the load capacitance, the frequency of operation, and the supply voltage. A reduction of any one of these is beneficial. A reduction in power consumption provides several other benefits. Less heat is generated, which reduces problems associated with high temperature, such as the need for heatsinks. This provides the consumer with a product that costs less. Furthermore, the reliability of the system is increased due to lower-temperature stress gradients on the device, and the integrity of the signal is improved due to the reduction of ground bounce and signal noise. An additional benefit of the reduced power consumption is the extended life of the battery in battery-powered systems.

Reliability Implications

The integrated-circuit component power dissipation during operation elevates the device junction temperature. The thermal impedance (θ_{JA} or k-factor) of a device package is defined as the increase in the junction temperature, above ambient temperature, due to the device power dissipation. Thermal impedance is measured in degrees Celsius per watt. Thermal characteristics of a device package are commonly described using two indices, Q_{JA} (junction to ambient) and Q_{JC} (junction to case). Controlling the junction temperature within a desired range is critical for proper device functionality and long-term reliability.

Table 4, based on long-term sustained temperatures, shows the relationship between junction temperature and predicted failure rate.

Table 4. Junction Temperature Versus 100,000-Hour Predicted Failure Rate

JUNCTION TEMPERATURE (°C)	FAILURE RATE (%)
100	0.02
110	1
120	11
130	46
140	80
150	96

Higher component temperatures increase the possibility of component wearout due to such failure mechanisms as electromigration and ball-bond intermetallic failures.

Thermal Definitions

Heat — A form of energy associated with the motion of atoms or molecules in solids, and capable of being transmitted through solid and fluid media by conduction, through fluid media by convection, and through empty space by radiation

Conduction Heating — The most commonly recognized form of heat transfer. Metal materials are good conductors of heat and can be quantified by a proportionality constant (k), also known as thermal conductivity. The higher the thermal-conductivity number, the more quickly heat transfer, by means of conduction, occurs. Leadframes are the primary media for conduction heating in plastic-encapsulated devices; however, mold compound materials play a major role in this type of heat transference.

Convection Heating — The heat transfer by fluid motion between regions of unequal density that result from nonuniform heating. This type of heat transfer is most commonly seen when air is forced across a heated surface, resulting in the cooling of the heat source. Heat is transferred to the air by means of convection heating. The rate of heat transfer depends on the surface area of the heat source and the velocity and physical properties of the airflow. When a device package is generating heat through normal operation, the device can be cooled by applying a constant airflow across the surface of the package.

Radiation — Radiant heat transfer occurs between two objects separated within a vacuum.

Ambient Temperature — The temperature of the surrounding air, usually used as a reference point to calculate the junction or case temperature. This temperature is measured at some specific distance from the device.

Case Temperature — The temperature on the package surface measured at the center of the top of the package

Junction Temperature — The temperature of the die inside the device package

Acknowledgment

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Thermal Derating Curves for Logic-Products Packages

SZZA013A
March 1999

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Abstract

Thermal metrics, such as θ_{JA} and θ_{JC}, are used to compare thermal performance of plastic integrated circuit (IC) packages. The thermal conductivity of all materials of the IC packaging and of the test board affect the thermal resistance values reported by semiconductor manufacturers. Recent advancements in reporting thermal data include standard test-board designs. Texas Instruments (TI™) has published values for all logic-products IC packages. Also, derating curves that allow calculation of the maximum power dissipation of a plastic IC package have been developed. The derating curves, which are available on a TI web page, can be modified interactively to determine maximum power dissipation with different ambient-temperature ranges and junction temperatures.

Introduction

The maximum allowable power consumption of an IC package can be calculated, given the thermal resistance of the package, the junction temperature, and the ambient temperature. This calculation of maximum power using thermal resistance values with different airflows makes possible the generation of derating curves. These derating curves allow the system designer to see the effect of ambient-temperature changes on the maximum power that the package can dissipate. The system designer can also use this type of thermal data to compare performance of packages from different suppliers, assuming the same test-board conditions.

Thermal data and derating curves for TI logic-products IC packages have been published on a TI web page discussed in *Application to Semiconductor Packaging*. The user can vary the junction temperature and ambient-temperature range used to calculate the derating curves for each package as described in *Derating Curves.*

Background

Semiconductor users need to know the thermal performance of IC packages to be used in their end equipment. Knowing the thermal performance of the IC package for a given device allows the system designer to determine the maximum power that the package can handle. However, it is critical that the user of any thermal data know the test conditions under which the thermal data was generated.

Many thermal metrics exist for IC packages. These include thermal resistance of the package measured from junction to ambient (θ_{JA}) and measured from junction to case (θ_{JC}). A simple analogy can be used to define these terms before applying them to semiconductor packages.

The Concept

Consider a closed cup of heated coffee at a certain temperature (see Figure 1). The temperature of the coffee is analogous to the junction temperature (T_J) of a semicondutor device. The outer surface of the coffee cup is at some temperature analogous to the temperature of the outside of the semiconductor package, or case temperature, (T_C). Finally, the room is at ambient, or free-air, temperature (T_A). Clearly, $T_J > T_C > T_A$.

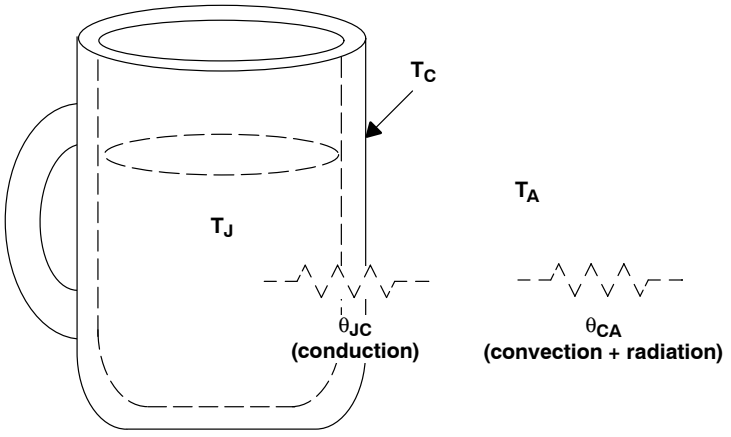

Figure 1. Coffee-Cup Example for Thermal Metrics

Heat transfers from the coffee through the cup by conduction. Thus, there is a temperature differential between the coffee and the outer surface. The rate of heat transfer through the cup is determined by the thermal resistance of the walls of the cup. The thermal resistance is a function of the material used to make the cup (e.g., paper, Styrofoam™, or porcelain), the thickness of the walls of the cup, and the overall geometry of the cup. The higher the thermal resistance, the slower the heat travels through the cup. The thermal resistance between the junction (the coffee) and the case (cup) can be designated θ_{JC}.

Moving away from the junction, heat then transfers from the surface of the cup by radiation and convection. There is a thermal resistance associated with this transfer that is expected to be a function of the geometry, smoothness, and color of the surface. This thermal-resistance value is termed θ_{CA}.

The overall rate of heat transfer is then a combination of θ_{JC} and θ_{CA}. There is a temperature drop (much like a voltage drop) from the inner side to the outer side of the cup and another drop from the surface of the cup to the ambient environment. Of course, the objective is to keep coffee warm. But, with semiconductors, the objective is to move heat away from the IC chip as quickly as possible.[1]

Application to Semiconductor Packaging

Figure 2 shows a typical IC plastic package with the silicon chip and the thermal metrics identified.

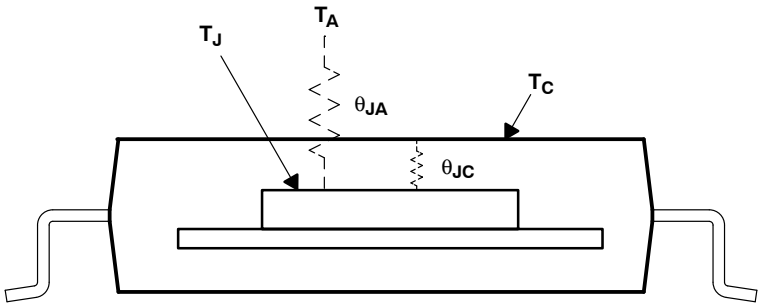

Figure 2. IC Package Thermal Metrics

For semiconductor devices, the junction-to-ambient thermal resistance (θ_{JA}) is the most commonly used thermal metric and is defined mathematically in Equation 1.

Styrofoam is a trademark of Dow Chemical Company.

$$\theta_{JA} = \left(T_J - T_A\right) / P \quad (21)$$

Where:

T_J
= junction temperature of the chip

T_A
= ambient temperature

P
= power to the chip

Thermal resistance is the resistance of the package to heat dissipation and is related inversely to the thermal conductivity of the package. Of course, the source of heat in an IC package is the chip. All electrical circuits dissipate some amount of power in the form of heat, which is conducted through the package to the ambient environment. Because the process is not 100% efficient, the temperature of the die (T_J) rises above ambient. The thermal conductivity of the silicon chip, die-attach epoxy, copper leadframe, and mold compound all affect the rate at which the heat is dissipated. The geometries of the package and of the printed circuit board (PCB) greatly influence how quickly the heat sinks into the PCB and away from the chip.

To eliminate the test-board design as a variable in data reported between IC manufacturers, thermal-test-board design standards have been developed and released.[2,3] The primary factors in these test-board designs are shown in Table 1.

Table 1. Critical PCB Design Factors for JEDEC 1s and 2s2p Test Boards

DESIGN FACTORS	THERMAL TEST-BOARD DESIGNS	
	JEDEC 1s (Low-K) (inches)	JEDEC 2s2p (High-K) (inches)
Trace thickness	0.0028	0.0028
Trace length	0.98	0.98
PCB thickness	0.062	0.062
PCB width	4	4
PCB length	4.5	4.5
Power/ground-plane thickness	No internal copper planes	0.0014 (2 planes)

When reviewing thermal data supplied by the IC manufacturer, it is critical that users know the details of the PCB design in Table 1 to accurately compare data from different suppliers.

In 1996, TI's Logic Products group published θ_{JA} values for its IC packages. The data published in 1996 was generated using a JEDEC 1s PCB design. Thermal data is either generated in a laboratory environment or arrived at from thermal models of the PCB and IC package. The thermal model program used by TI is ThermCAL, a proprietary finite-difference thermal-modeling tool. The thermal data for SLL packages is available on the TI external web page:

http://www.ti.com/sc/docs/asl/package/thermal.htm

The Thermal Comprehensive Data Table on this web page lists the θ_{JA} data for each package at airflows of 0, 150, 250, and 500 linear feet per minute (lfm). Pertinent information about leadframe pad size and die size is listed for each package. Also, the source of the data (laboratory measurements or model) is indicated. Model data has been verified to be accurate within ±10% of laboratory measurements.

Derating Curves

When a device reaches a state of thermal equilibrium, the electrical power delivered is equal to the thermal heat dissipated. This thermal energy is in the form of heat and is given off to the surroundings. The maximum allowable power consumption (P) at a given ambient temperature (T_A) is computed using the maximum junction temperature for the chip (T_J) and the thermal resistance of the package (θ_{JA}) (see Equation 2).

$$P = \left(T_J - T_A\right) / \theta_{JA} \quad \textbf{(22)}$$

Over time, heat destroys semiconductors. Thus, manufacturers usually specifiy a maximum junction temperature [$T_{J(max)}$]. If the junction temperature goes above this value, irreversible damage occurs. Because the IC user typically knows the ambient temperature of the operating environment (T_A), the thermal resistance of the IC package (θ_{JA}) provided by the supplier, and a specified maximum junction temperature, Equation 2 can be used to determine the maximum power that can be applied to the particular package under the specified test conditions.

In Equation 2, by varying the ambient temperature at a given airflow, a derating curve can be developed for each package. By using the thermal resistance value of the package at different airflows, a derating curve can be developed for each airflow. A typical set of derating curves for the 16-pin SOIC (DW) package is shown in Figure 3. The data for the 16-pin SOIC (DW) package (θ_{JA}) used to calculate the curves was generated using a JEDEC 1s PCB design.

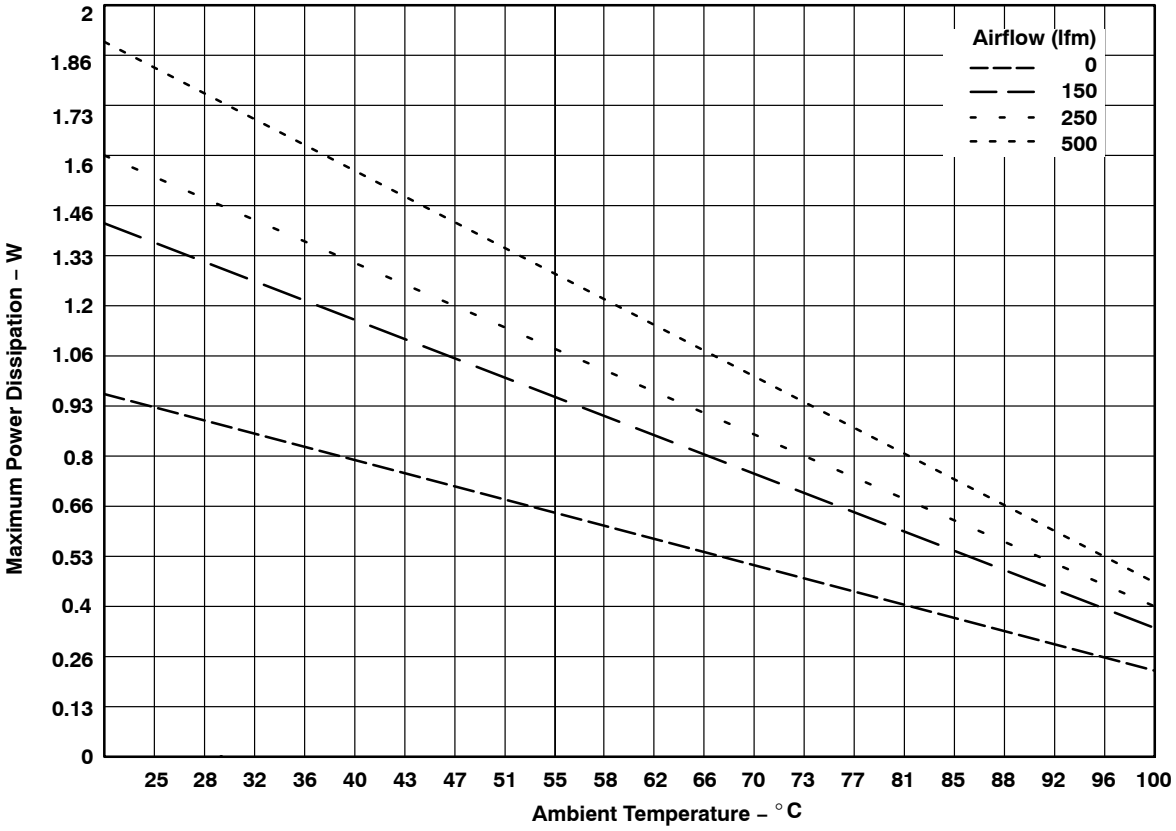

Figure 3. Derating Curves for 16-Pin SOIC (DW) Package

As an example, the 16-pin SOIC (DW) package has a θ_{JA} value of 104.6°C/W at 0-lfm airflow. The maximum power that the package can withstand at T_A = 25°C and T_J = 125°C, remembering that the θ_{JA} value was derived using a JEDEC 1s PCB, is:

$$P = (125°C - 25°C)/104.6\ °C/W = 0.956\ W \quad \textbf{(23)}$$

For a given package, these derating curves allow the designer to see the effect of rising ambient temperature on the maximum power allowed. The derating curves for each package can be viewed on the TI web page mentioned previously. The program uses the θ_{JA} data shown to display the maximum power dissipation (y-axis) of the package over a range of ambient temperatures

(x-axis). This maximum power dissipation of the package is equivalent to the maximum allowable consumption of the IC device. The user can vary the junction temperature and the ambient-temperature range used in the interactive calculation of maximum power dissipation.

Conclusion

Integrated-circuit designers and end users need to compare the thermal performance of plastic IC packages. The most commonly used thermal metrics are package thermal resistance measured either from junction to ambient (θ_{JA}) or junction to case (θ_{JC}). Once the thermal resistance of the package is determined, it is possible to calculate the maximum power that a package can take at an assumed junction temperature and ambient temperature. By calculating the maximum power dissipation a package can withstand at a number of different ambient temperatures, derating curves can be developed for each package. These curves allow the user to see graphically the maximum power dissipation for a given package over a range of conditions. The web-based derating curves allow the user to vary the junction temperature and the ambient-temperature range used to calculate the curves.

Acknowledgment

The authors of this application report are Douglas W. Romm and Jeffrey D. Pfeifle.

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3 EIA/JESD 51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages,* February 1999.

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