TEXAS INSTRUMENTS

# TVP5020 NTSC/PAL Digital Video Decoder

## Initialization

Application Report

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# *TVP5020 NTSC/PAL Digital Video Decoder Initialization*

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**ABSTRACT**

This application report describes the general requirements for initialization of the TVP5020 NTSC/PAL video decoder. The covered topics include hardware reset, microcode download, microcode file format conversion, register initialization, and register write/read latency issues.

## 1 Introduction

The internal microprocessor and program RAM of the TVP5020 NTSC/PAL video decoder provides the flexibility of rapid algorithm upgrades. This architecture requires that the microcode program be downloaded into program RAM as part of the power-up initialization sequence. This application report covers initialization of the TVP5020, which consists of the following steps:

1. Hardware reset
2. Microcode download
3. Register initialization

Also covered are microcode file format conversions and a discussion of register write/read latency issues.

# 2 Hardware Reset

## 2.1 At Power-Up

The hardware reset pin (RSTINB) must be asserted low for at least 10 ms at power up to ensure proper initialization of the TVP5020. Since the system power supply ramp-up time may vary, the instant when the digital power supply reaches 2.7 V can be taken as time zero. The system design must ensure that the TVP5020 input clock (at pin XTAL1) is oscillating before the end of the RSTINB pulse. For a crystal-generated clock, this startup time can be in the order of milliseconds. A running clock is required during hardware reset to correctly sample the power-up configuration pins.

Tables 1 and 2 show the PCLK and SCLK frequencies produced by the TVP5020 before and after device initialization. Before initialization, the pixel clock (PCLK) frequency is the XTAL1 clock frequency divided by 6, and the system clock (SCLK) frequency is 2× the PCLK frequency. After initialization, PCLK runs at the pixel rate (which depends on the video standard and sampling mode initialized), and SCLK again runs at 2× the PCLK frequency.

Thus, a good way to determine the success of initialization of the TVP5020 device is to measure the PCLK (or SCLK) frequency.

## 2.2 After Device Initialization

A hardware reset occurring after the device has been successfully initialized is, for the most part, undistinguishable from a power-up reset. Their differences are:

- The input clock (at pin XTAL1) is already oscillating.
- The program memory is already initialized.
- The PCLK/SCLK frequencies are already as shown in Table 2.

**Table 1. Clock Frequencies Before Device Initialization**

| VIDEO STANDARD SAMPLING MODE | NTSC | | PAL | |
|---|---|---|---|---|
| | CCIR601 | SQUARE PIXEL | CCIR601 | SQUARE PIXEL |
| XTAL clock frequency (MHz) | 24.576 | 26.800 | 24.576 | 26.800 |
| PCLK frequency (MHz) | 4.096 | 4.466 | 4.096 | 4.466 |
| SCLK frequency (MHz) | 8.192 | 8.933 | 8.192 | 8.933 |
| 4 × PCLK period (ns) | 977 | 896 | 977 | 896 |

**Table 2. Clock Frequencies After Device Initialization**

| VIDEO STANDARD SAMPLING MODE | NTSC | | PAL | |
|---|---|---|---|---|
| | CCIR601 | SQUARE PIXEL | CCIR601 | SQUARE PIXEL |
| XTAL clock frequency (MHz) | 24.576 | 26.800 | 24.576 | 26.800 |
| PCLK frequency (MHz) | 13.5 | 12.2727 | 13.5 | 14.75 |
| SCLK frequency (MHz) | 27.0 | 24.5454 | 27.0 | 29.5 |
| 4 × PCLK period (ns) | 296 | 326 | 296 | 271 |

## 2.3 Configuration Pins

At the trailing edge of the hardware reset pulse (the low-to-high transition of RSTINB), a number of configuration pins are read to set up the initial operating mode of the TVP5020. These configuration pins determine the host port configuration ($I^2C$, VMI, or VIP). These pins must be connected with 10 kΩ pull-up/pull-down resistors to $V_{CC}$ or GND, respectively. Furthermore, these configuration pins must not be driven by external logic while RSTINB is asserted low. Tables 3 and 4 show the configuration pins and their functions.

**Table 3. Power-Up Strapping for Host Port Selection**

| GLCO PIN 31 | PALI PIN 32 | FID PIN 33 | FUNCTION SELECTED |
|---|---|---|---|
| 0 | 0 | 1 | $I^2C$ host port |
| 0 | 1 | 0 | VIP host port |
| 1 | 0 | 1 | VMI host port mode A |
| 1 | 1 | 0 | VMI host port mode B |
| 1 | 1 | 1 | VMI host port mode C |

**Table 4. VIP Power-Up Strapping for Setting Vendor ID**

| PINS 51–53,55,56, 58–60 | FUNCTION SELECTED |
|---|---|
| UV[7:0] | VIP vendor ID |

## 2.4 Behavior of I/O Pins

Table 5 describes the behavior of the I/O pins during and immediately after reset.

**Table 5. Behavior of I/O Pins**

| SIGNAL NAMES | DURING RESET | AFTER RESET |
|---|---|---|
| RSTINB, OEB, EXT_DATA_8 | In | In |
| GLCO, PALI, FID, GPCL | In | Out |
| UV[7:0] | In | Hi-Z |
| PCLK , SCLK , PREF | Hi-Z | Out† |
| Y[7:0], HSYN, VSYN, AVID | Hi-Z | Hi-Z |
| Host interface pins: A[1:0], D[7:0], VC0, VC1,VC2, VC3, INTREQ | Hi-Z | Active |

† These clocks are active at the end of reset. However, when the microprocessor resumes operation after the microcode download, the SCLK, PCLK, and PREF outputs are placed in the high-impedance state. Register programming is then required to enable these outputs.

## 2.5 Pre-Download Register Initialization

### *2.5.1 $I^2C$ Host Interface*

None required.

### *2.5.2 VIP Host Interface*

None required.

### *2.5.3 VMI Host Interface*

For the VMI host interface, some registers may require initialization before the microcode download begins. See Section 6—*Host Interface Latency Issues* for a discussion on register write/read latency matters and use of the operation-complete interrupt.

In order for the operation-complete interrupt to function, that particular interrupt source must be enabled. Optionally, the polarity of the INTREQ pin may be configured (this is irrelevant if interrupt status register polling is used). Table 6 shows a typical set of pre-download register initializations.

**Table 6. For VMI Host Interface Only: Pre-Microcode Download Register Initialization**

| REGISTER | ADDRESS | MODIFIED VALUE | DESCRIPTION |
|---|---|---|---|
| Interrupt enable | C1h | 20h | Enable operation-complete interrupt source |
| Interrupt configuration | C2h | 05h | Make INTREQ output active high (optional), enable YUV outputs† |
| Interrupt status | C0h (or VMI status register) | FFh | Clear all interrupt status bits |

† In all cases, address 03h bit 4 must be set to 1 to enable the YUV outputs. For the VMI host interface, address C2h bit 2 must also be set to 1 to enable the YUV outputs.

# 3 Microcode Download

The TVP5020 has an internal processor and an associated 5K×20 instruction RAM. The microprocessor controls many of the device functions including PLL operation, AGC, and sync and register configuration. This programmable architecture allows the TVP5020 performance to be enhanced with upgraded algorithms. The microcode for the internal processor is downloaded to the TVP5020 during each power up as described later.

The details of downloading the microcode depend on the host interface being used ($I^2C$, VIP, or VMI). For information on programming the TVP5020 host interfaces, see application reports SLAA051, SLAA052, and SLAA054.

## 3.1 Timing Requirement for Start of Download

Following the negation of the reset signal (RSTINB asserted high), the microcode instructions may be downloaded after at least 4 pixel clock (PCLK) cycles have elapsed. Note that this time period is longer if the TVP5020 has not already been initialized. See the 4×PCLK period data shown in Tables 1 and 2.

## 3.2 General Microcode Download Procedure

In general, the procedure is initiated by addressing the program RAM write register (address 7Eh) for a write operation. After this the internal microprocessor is disabled and the internal microcode RAM is ready for microcode download. The first instruction byte and subsequent instruction bytes written to the program RAM write register are loaded to sequential locations of the microcode RAM. Each 20-bit instruction is transmitted using three bytes, with the most significant byte first. Since the microcode RAM is 20-bits wide, the upper four bits of the most significant byte are discarded before the data is written to the microcode RAM.

It is possible to complete the microcode download in a single burst of consecutive write cycles. If needed, the data may be transmitted in separate blocks, so long as no other TVP5020 register (other than address 7Eh) is accessed in between blocks. If another TVP5020 register is accessed, the microprocessor internal instruction RAM address pointer will be reset to zero and will resume operation.

## 3.3 Microprocessor Restart Operation

As noted before, the internal microprocessor unit is disabled during microcode download. Therefore, after completion of the microcode download (that is, all microcode instructions have been written to the program RAM), a write cycle to a register *other than* 7Eh is required to wake up the microprocessor and resume normal operation of the TVP5020. Register 7Fh is recommended for this purpose.

### *3.3.1 Timing Requirement for Microprocessor Restart*

After the microprocessor-restart operation has been initiated, the microprocessor will take up to 5 ms for its initialization code to complete. Only then can register initialization via the host port begin. The following sections describe how this latency is handled for the different host interfaces.

#### 3.3.1.1 Implementation for I2C Bus

After the restart operation has been performed, the TVP5020 drives the I2C clock (SCL) low to signal the I2C master to wait.

I2C implementations vary in the way this is handled. A problem arises when the I2C master tries to generate a STOP condition without checking if the I2C bus is free (that is, SCL high). This attempted-STOP condition is not recognized by the I2C slave. The master then stops for a software-generated delay to meet the timing requirement mentioned in Section 3.3.1. Finally, the I2C master resumes operation by generating a START condition. Since no STOP condition was recognized by the slave, this is seen as a RE-START condition, which the TVP5020 does not support.

To prevent this from happening, it is necessary for the master to wait until the I2C bus is free (that is, SCL high) before generating a STOP condition, thus insuring that a valid STOP condition is generated. This provides the optimal amount of delay and eliminates the need for a software-generated delay.

The I2C master must also wait until the I2C bus is free (that is, SCL high) before generating a START condition.

#### 3.3.1.2 Implementation for VMI Bus

For VMI host interface-based applications, the interrupt request (INTREQ) pin (or interrupt status register polling) may be used to determine when the TVP5020 is ready to proceed with host interface activity. This eliminates the need for a software-generated delay.

#### 3.3.1.3 Implementation for VIP Bus

For VIP host interface-based applications, the slave-terminate and master-retry mechanisms are used to handle the latency after microprocessor restart. TVP5020 will slave terminate all VIP access until the microprocessor initialization has completed. Meanwhile, the VIP master repeatedly retries the current VIP access until it is accepted by the TVP5020. This eliminates the need for a software-generated delay.

# 4 Post-Download Register Initialization

After the microcode download, initiation of the microprocessor restart, and completion of the microprocessor initialization code (see section 3.3.1—*Timing Requirement for Microprocessor Restart*) the TVP5020 internal registers initialize to the default values specified in the TVP5020 data manual. Depending on system design, some register values may have to be changed from the data manual defaults. A typical set of register modifications is shown in Table 7.

**Table 7. Typical Post-Download Register Modifications**

| SUBADDRESS | MODIFIED VALUE | DESCRIPTION |
|---|---|---|
| 03h | 19h | YUV, HSYN, VSYN, AVID, SCLK and PCLK outputs enabled |
| 07h | 10h | Luma bypass during vertical blank |
| 0Dh | 0Fh | 8-bit ITU-R BT.656 interface (system dependent) |
| C2h | 05h | YUV outputs enabled†, INTREQ output active high (optional) |

† In all cases, address 03h bit 4 must be set to 1 to enable the YUV outputs. For the VMI host interface only, address C2h bit 2 must also be set to 1 to enable the YUV outputs.

# 5 Microcode Data File

## 5.1 File Naming Convention

The microcode file naming convention is shown in Figure 1. For example, a file named 2001N601.hex would contain TVP5020 microcode version 01 for the NTSC video standard with CCIR601 sampling.

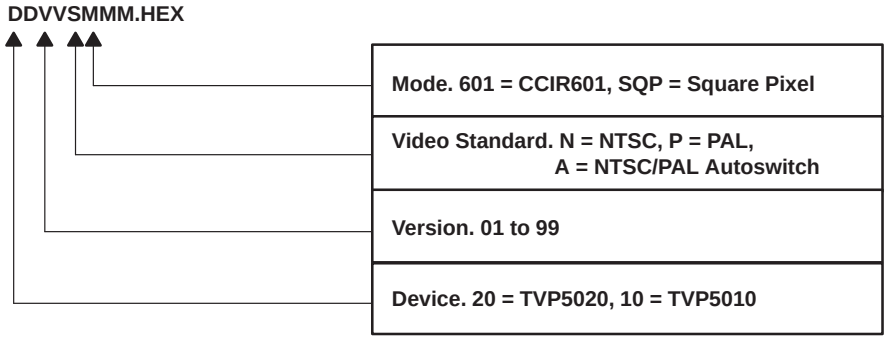


**Figure 1. Video Decoder Microcode File Naming Convention**

## 5.2 File Format Conversion

TI provides the TVP5020 microcode as binary code in a Hex-ASCII file format. Figure 2 is an example of this file format. This file may be converted to other formats using a TI-provided file conversion utility called HEXCONV as illustrated in Figure 3. Figure 4 shows the dialog box that appears when running HEXCONV. The standard-C header (.H) file generated from the example input file is shown in Figure 5. The C-language style comments in Figure 5 are not part of the output of HEXCONV, but were added here for illustration purposes. This format can be used when the TVP5020 microcode must be embedded into a larger program. The Intellec 8/MDS (.PRM) file generated from the same example input file is shown in Figure 6. This file format is compatible with most PROM programmers. This format can be used when the TVP5020 microcode must be programmed directly into a memory device.

```
80000
00000
303FC
.
.
.
C3F80
```

**Figure 2. TVP5020 Microcode in Hex-ASCII Format**

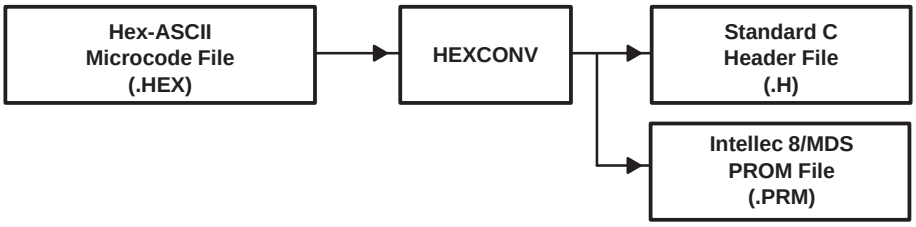


**Figure 3. Microcode File Format Conversion**

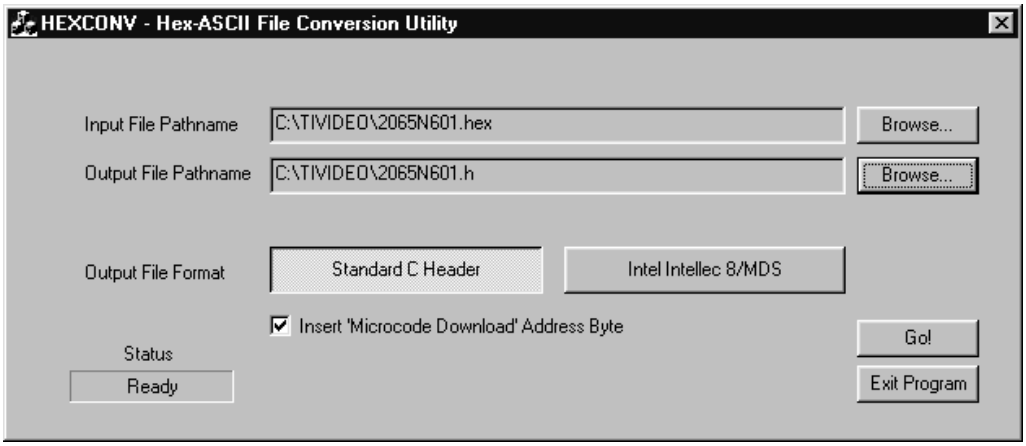


**Figure 4. HEXCONV Program Dialog Box**

```
#define TVP5020_CODE_SIZE 0x27B8

unsigned char TVP5020_CODE[] =
{
0x7E,  /*Register Address = 7Eh */
0x08,  /* MSB */
0x00,
0x00,  /* LSB */
0x00,
0x00,
0x00,
0x03,
0x03,
0xFC,
.
.
.
0x0C,
0x3F,
0x80
} ;
```

**Figure 5. TVP5020 Microcode After Conversion to Standard C Header File**

```
:03000000080000F5
:03000300000000FA
:030006000303FCF5
.
.
.
:03276C000C3F809F
:00000001FF
```

**Figure 6. TVP5020 Microcode After Conversion to Intellec 8/MDS PROM File**

# 6 Host Interface Latency Issues

Some TVP5020 registers (referred to as non-VDP registers below) have a latency associated with register access. This latency is at most one horizontal sync period (on the order of 64 μs). When writing to a non-VDP register, there is a latency before the TVP5020 is ready to accept another data byte. When loading the address of a *readable* non-VDP register, there is a latency before the data byte can be read from the TVP5020.

## 6.1 I2C Host Interface

The I2C slave (TVP5020) will only process one transaction per horizontal line. After a read/write operation to/from a non-VDP register (see Section 6.3.2) the TVP5020 drives the I2C clock (SCL) low. This signals the I2C master to wait before making another register access.

At this point, it is necessary for the master to wait until the I2C bus is free (that is, SCL high) BEFORE generating a STOP condition. This insures that a valid STOP condition is generated. This provides the optimal amount of delay and eliminates the need for a software-generated delay.

The I2C master must also test for the I2C bus to be free (i.e., SCL high) before generating a START condition.

## 6.2 VIP Host Interface

For VIP host interface-based applications, the slave-terminate and master-retry mechanisms are used to handle the register write/read latency issue. TVP5020 will slave-terminate all VIP access until the next horizontal line begins. Meanwhile, the VIP master repeatedly retries the current VIP access until it is accepted by the TVP5020. This eliminates the need for a software-generated delay.

## 6.3 VMI Host Interface

Use of the operation-complete interrupt is recommended for handling the register write/read latency issue. Three schemes can be used to detect the operation-complete interrupt:

- The TVP5020 interrupt-request signal (INTREQ) generates a hardware interrupt to the host.
- The host polls the INTREQ signal.
- The host polls the TVP5020 interrupt status register (Address C0h or directly through the VMI status register).

In order for the operation-complete interrupt to function, that particular interrupt source must be enabled. Optionally, the polarity of the INTREQ pin may be configured. See Table 6 for typical register initializations to set up the operation-complete interrupt.

### *6.3.1 Vertical Blanking Interval Data Processor (VDP) Registers*

VDP registers are defined as all registers in the address range 90h–C2h. These registers can be accessed before or after device initialization. There is no latency associated with read or write cycles to these registers.

### 6.3.2 Non-VDP Registers

Non-VDP registers are defined as all registers that are not in the address range 90h–C2h. These registers, with the exception of the program RAM write and read registers, can only be accessed after device initialization. There is latency associated with the read and write cycles to all non-VDP registers, except for the program RAM read and write registers.

#### 6.3.2.1 Write Latency

When writing to a non-VDP register, a latency will occur before the TVP5020 is ready for another data byte to be written. This latency is at most one horizontal sync period (on the order of 64 μs). After this latency period, the operation-complete interrupt is generated.

##### 6.3.2.1.1 Read Latency

When loading the address of a *readable* non-VDP register, a latency will occur before the data byte is ready for the TVP5020 to read. This latency is at most one horizontal sync period. The operation-complete interrupt is generated after this latency period.

# 7 Reference Materials

The TVP5020 microcode download procedure is described in more depth in the application reports SLAA051, SLAA052, and SLAA054. Each of these reports provides a complete source-code example for initializing the TVP5020 using a specific host interface.

Table 8 shows sections of the TVP5020 Data Manual (TI literature #SLAS186) that provide additional details about the host interfaces.

**Table 8. Reference Material for Host Interfaces**

| HOST INTERFACE | SECTION OF TVP5020 DATA MANUAL |
|---|---|
| $I^2C$ microcode write operation | Section 2.4.4 |
| VIP microcode write operation | Section 2.5.4 |
| VMI microcode write operation | Section 2.9.2 |

## 7.1 Related Documents from Texas Instruments

1. *TVP5020 NTSC/PAL Video Decoder Data Manual*, literature number SLAS186.
2. *TVP5020 NTSC/PAL Video Decoder: Programming for the VMI Host Interface Application Report,* literature number SLAA051.
3. *TVP5020 NTSC/PAL Video Decoder: Programming for the $I^2C$ Host Interface Application Report,* literature number SLAA052.
4. *TVP5020 NTSC/PAL Video Decoder: Programming for the VIP Host Interface Application Report,* literature number SLAA054.