A Low-Cost Single-Phase Electricity Meter Using the MSP430C11x

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ABSTRACT

This application report describes a low-cost single-phase electricity meter design using the MSP430C11x to achieve analog-to-digital conversion (ADC), self-calibration, and anti-tampering protection.

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1 Introduction

Mechanical electricity meters (e-meters) have been used for household electricity measurement for decades. New, fully electronic e-meters are replacing mechanical e-meters, but, up to now, electronic e-meters have been limited by higher costs associated with the analog-to-digital converter (ADC) and the processor.

The MSP430C11x is a low cost member of the MSP430 family of devices from Texas Instruments. It does not have built-in hardware blocks such as ADCs and hardware multipliers that are normally associated with electronic e-meters. However, with three channels of powerful capture registers, it is possible to construct three channels of low-cost but high-resolution ADCs. With its high performance 16-bit RISC processor, the ’C11x can be used to build a high-precision low-cost fully electronic e-meter. Some of the main features are:

- Three channels of slope ADC using the built-in capture timer
- Two ranges of current input with automatic control to cover current up to 400%
- High accuracy with less than 1% error required in class 1 meter
- Anti-tampering to prevent electricity theft
- Simple and easy self-calibration
- Single chip with no external MCU required
- DC offset removal for both voltage and current channel
- Low pass filter for instantaneous power
- Energy to pulse frequency conversion

2 Analog-to-Digital Conversion

For e-meter applications, special consideration must be given to the ADC stage. Real time power calculation requires instantaneous samples of both voltage and current signals. The most straightforward way to do this is to simultaneously sample both the current and voltage signals, which is the approach described in this report. In this application, three channels of parallel ADC are available; use of the third channel will be explained later. By using a single-slope ADC technique, three ADC channels can be constructed cost effectively that give good resolution (11 bits) and adequate sampling rates (1 K samples/sec/channel).

2.1 Single Slope ADC

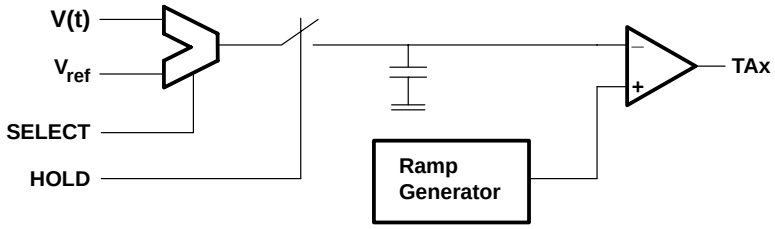


Figure 1. Single Slope A to D

The analog-to-digital conversion uses a traditional single slope approach. An analog multiplexer selects the signal input and the reference voltage on alternate cycles. After the sample and hold, the output is compared with a ramp input. The comparator then triggers the capture timer when the ramp has reached the input voltage. The time corresponding to the signal input and the reference voltage are both taken, and the actual input value can be calculated with the following equation.

$$V[n] = V_{ref} \times \left(\frac{t_v}{t_{ref}} \right)$$

Where V[n] is a sequence given by $V(n \times t_C)$

2.2 Ramp Generation

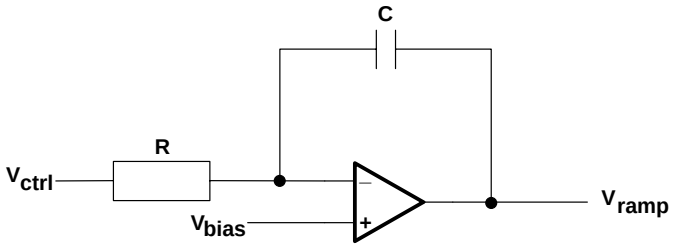


Figure 2. A Ramp Generator

The ramp generator consists of an operational amplifier (op amp) integrator. With a constant voltage input, a constant current equal to $(V_{bias}\text{-}V_{ctrl})/R$ flows through capacitor C. This develops a linear voltage ramp output on the op amp.

2.2.1 Ramp Generation Cycle Time

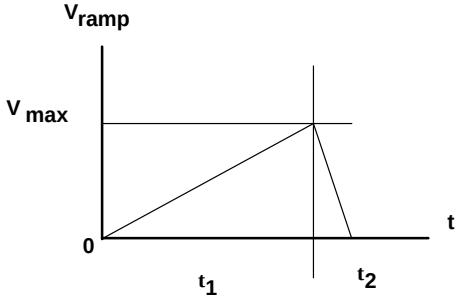


Figure 3. Ramp Generation Cycle

In Figure 3, if V_{ctrl} is set to 0 at t = 0, the output V_{ramp} starts to ramp up from 0. After time t_1, if V_{ctrl} is brought to V_{cc} while the V_{ramp} reaches V_{max}, the V_{ramp} now ramps down. And after another time t_2, V_{ramp} drops to 0. Setting V_{ctrl} to 0 again starts a new cycle.

Given $C = Q / V_c$

then $C = I_c/(dV_c/dt)$

or $C = ((V_{bias} - V_{ctrl}) / R) / (d(V_{ramp}-V_{bias})/dt)$

or $\Delta t = RC \times \Delta V_{ramp} / (V_{bias}-V_{ctrl})$

so $t_1 = RC \times V_{max} / V_{bias}$

and $t_2 = RC \times V_{max} / (V_{cc} - V_{bias})$

The cycle time will be

$$t_c = t_1 + t_2 = RC \times V_{max} \times \left(\frac{1}{V_{bias}} + \frac{1}{(V_{cc}-V_{bias})} \right)$$

The above equation tells how to select the RC value with a given sampling frequency. However, the following points should be taken into account:.

- V_{max} should be set to a value as big as possible to maximize the input signal dynamic range. It can be either the saturation output of the op amp or the maximum input value of the comparator, whichever is smaller.
- In Figure 2, V_{bias} should be as small as possible. For a single slope ADC, we are only interested in the rising part of the generator, and, therefore, the falling time should be minimized--that is $t_1 >> t_2$. A small V_{bias} can give a big t_1 and small t_2.
- A little desirable over charging or discharging can be achieved by selecting an RC value smaller than the calculated value. This ensures that the initial voltage in charging or discharging is 0 or V_{max}. Unknown initial conditions can shift the ramp up and down.
- The software control delay causes the actual t_1+t_2 to be smaller than t_c. This is another reason for using a smaller RC value.

2.2.2 A Practical Example

V_{cc} = 5 V

V_{max} = 3.5 V

V_{bias} = 0.6 V

Sampling frequency = 995 Hz => $t_c = 1 / (2 \times 975)$

If C = 1000 pF, R = 75.8 K. To have a smaller RC value, select R′ = 68 K (or even 62 K).

2.2.3 Time Measurement of the Ramp

The MSP430′s capture timer can be easily configured to capture the end results of a comparator. But, there is no external hardware control to start the timer at the beginning of the ramp signal. At present, the start of the ramp is detected by comparing the ramp with a preset threshold slightly higher than zero. The amount of time it takes to get from zero to the threshold is determined as a portion of the capture time using the reference signal as input.

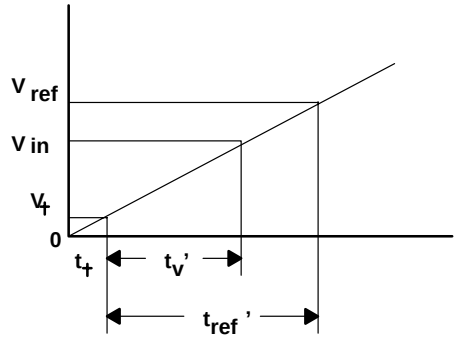


Figure 4. Ramp Time Measurement

From Figure 4, the slope is given by:

$V_{ref}/(t_{ref}' + t_t) = V_t/t_t$

Solve for $t_t = t_{ref}' \times (V_t / (V_{ref} - V_t))$

Or $t_t = t_{ref}' \times K_t$

Where $K_t = V_t/(V_{ref} - V_t)$

Since a multiplication is required, K_t should be a simple number so that simple shift and/or add/sub operations can be used to replace the high MIPS multiplication routine.

2.3 Dual Range ADC for Current Channels

The rms value of the voltage input to an electricity meter should show only a small variation. However, the rms value for the current input varies according to the amount and type of loading, and this exhibits a much larger variation. Due to this large variation, either a relatively high resolution ADC or a low resolution ADC with selectable ranges should be used. To cover a range from 5% to 400% with a ±1% error, the minimum range of $400/5 \times 100/(1+1) = 4000$ is needed. A minimum of 12 bits is required. In a single slope ADC, there is a tradeoff between resolution, sampling speed, and noise. A resolution of 10 bits is more practical. A 12-bit resolution is effectively achieved by adding an extra gain of 4 for small inputs. Even though the target single range resolution is 10 bits, the actual resolution achieved in this design is about 11 bits.

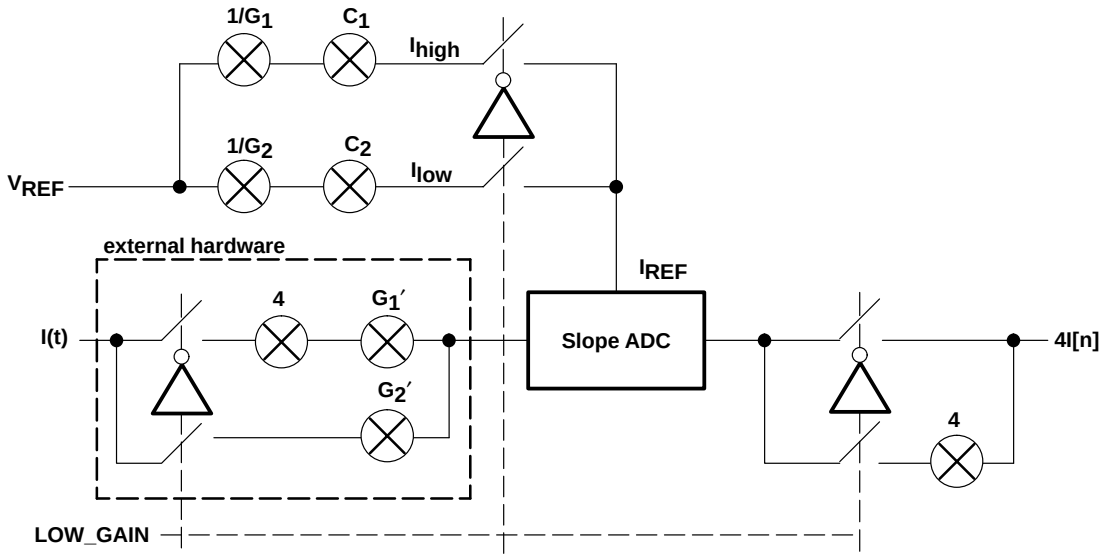


Figure 5. Dual Range ADC BLOCK DIAGRAM

Figure 5 shows the block diagram of a dual range ADC. It consists of a single range ADC and external hardware to provide an extra gain of 4 for small input signals. Theoretically, all gains, G_1, G_2, $1/G_1$ and $1/G_2$ should be unity, but the external hardware may not be able to provide a multiplication of 1 or 4 due to the limited choice of component values. To take this deviation into the account, extra gains, G_1 and G_2 are added. Usually, the deviation is small.

C_1 and C_2 compensate gains G_1' and G_2' that deviate from the original G_1 and G_2 due to component error. Therefore, $C_1 = G_1/G_1'$ and $C_2 = G_2/G_2'$. Since G_1' and G_2' are unknown and differ from unit to unit, a calibration must be carried out to obtain values for C_1 and C_2: these values may be store in EEPROM for later use.

In normal or low gain mode, the lower switches are closed and the higher switches are open. Still using the V_{ref} as reference, gives:

$$I'[n] = V_{ref} \times (t_i / t_{ref})$$

Where:

$$I'[n] = I[n] \times G_2'$$

and $I_{ref} = I_{low} = V_{ref} / G_2 \times C_2 = V_{ref} / G_2'$

so $I[n] \times G_2' = (I_{ref} \times G_2') \times (t_i / t_{ref})$

i.e. $I[n] = I_{ref} \times (t_i / t_{ref})$

The right hand side of the equation is the standard equation for calculating a single slope ADC value with I_{ref} as the reference. This means the ADC output will be $I_{ad}[n] = I[n]$. And the final output is $I_{out[}[n] = 4 \times I_{ad}[n] = 4I[n]$.

In high gain mode, the switches are switched over, i.e. higher switches closed and lower switches open. Using the same equation:

$$I'[n] = V_{ref} \times (t_i / t_{ref})$$

But now $I'[n] = 4I[n] \times G_1$

and $I_{ref} = I_{high} = V_{ref} / G_1$

so $4I[n] \times G_1 = (I_{ref} \times G_1) \times (t_i / t_{ref})$

that is $4I[n] = I_{ref} \times (t_i / t_{ref})$

or $4I[n] = I_{ad}[n]$

The final output is $I_{out}[n] = I_{ad}[n] = 4I[n]$.

Both cases give the same final output and maintain the accuracy. The extra gain of 4 in low gain mode balances the external hardware gain in high gain mode. Another alternative is to just scale down the high gain value with no change on low gain input. But this is undesirable since it reduces the number of significant digits and increases the computation error. In actual computation, all input values are further scaled up to provide more working digits.

2.4 Automatic Gain Switching

Gain switching between high and low gain of the dual range ADC should be done automatically and transparently. At the beginning of Section 2.3, note that the maximum ADC value is 4000 which corresponds to 400% of current input. In high gain mode with small input signals, the 10-bit ADC covers the lower range up to 1024, or roughly 100%. In low gain mode with big input signals, a 10-bit ADC with a gain of 4 can cover 4 to 4096, or 4% to 400%. This means that any selection from 4% to 100% can be used as a decision for gain switching.

In this application, the covered ranges of the high and low gain overlap each other. This introduces some amount of hysteresis that prevents the system from frequent switching between the two ranges. The two ranges used are 5% to 80% for high gain, and 60% to 400% for low gain. This selection is rather arbitrary but reasonable as it provides a 20% overlap and 20% (100%-80% in high gain) saturation margin.

3 Anti-Tampering to Prevent Electricity Theft

In some countries, electricity theft by illegal tampering with the electricity meter is a serious problem. The examples below show some possible tampering methods.

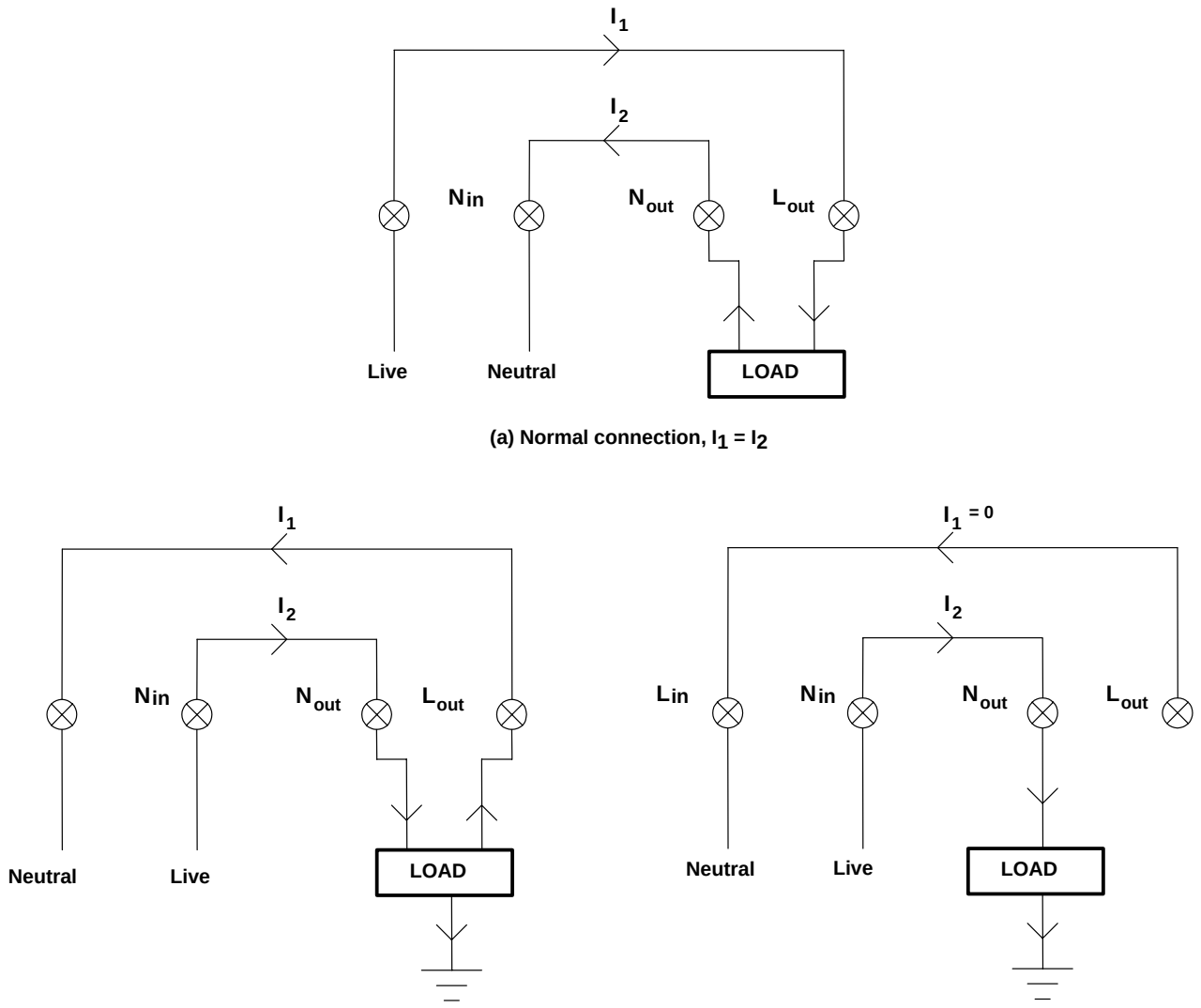


Figure 6. Examples of Different Meter Tampering

The main method for tampering is to reduce or prevent current flow from either the live or neutral sensor. If current is only taken from one of the lines, little or no electricity can be measured. A simple and straightforward way to prevent this, is to measure both lines and use the bigger one to calculate the amount of electricity used. This requires one additional ADC channel. Adding one ADC channel normally requires substantial additional hardware cost. Fortunately, the capture timer of the MSP430C11x provides three channels of ADC at almost the same cost as two channels.

4 System Data Flow

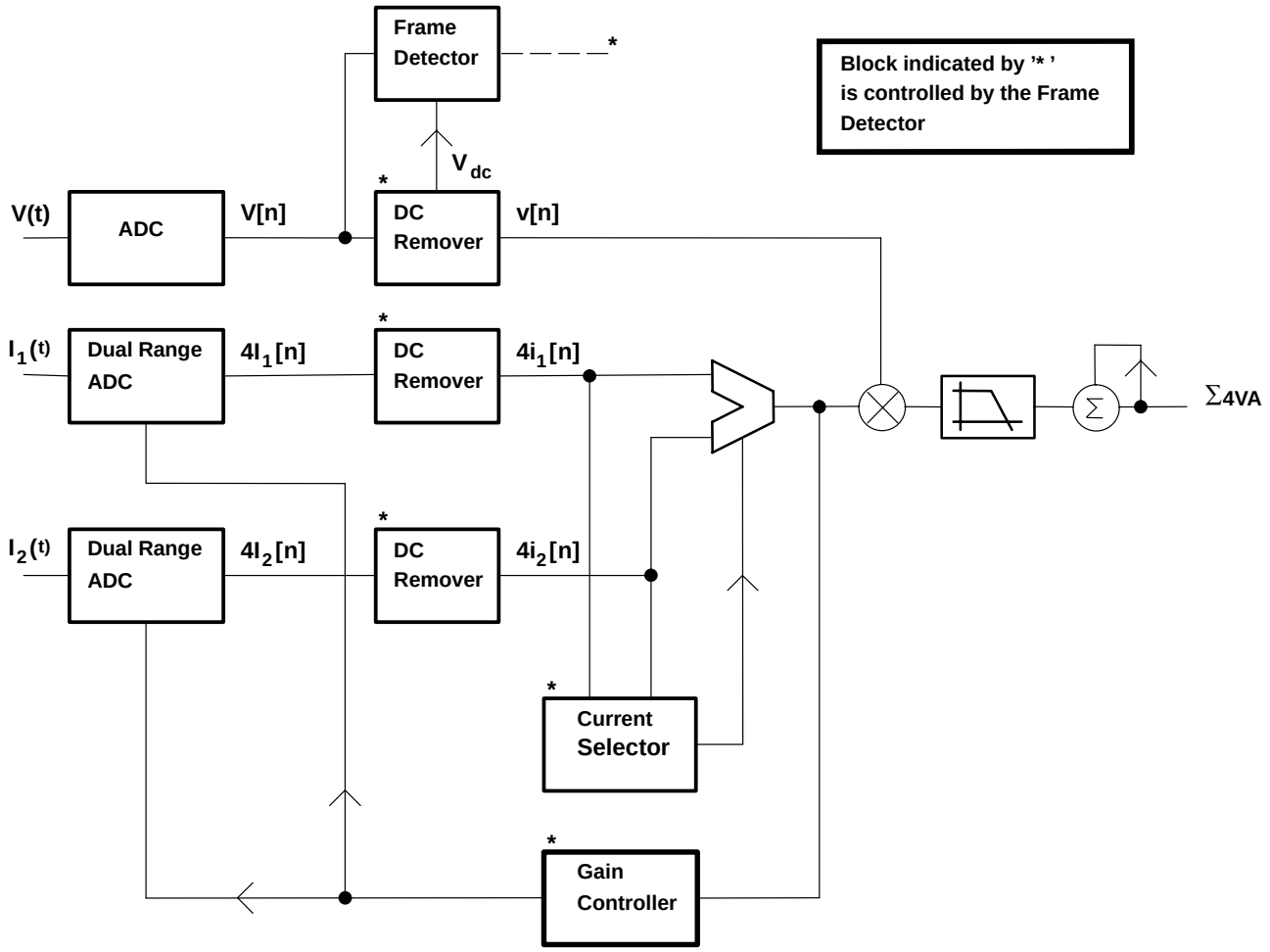


Figure 7. Internal Data Flow Block Diagram

Understanding data flow is the key to understanding a system. Figure 7 shows all the internal data flow except the high voltage front end and the energy-to-pulse converter. The input voltage and the two input currents, after scaling down (or up) from the high voltage front end, are first sampled by three ADCs simultaneously. The voltage channel uses a simple single-slope ADC. The ADCs of the two current channels are similar, but with dual gain amplifiers on top. The gain controller provides an automatic gain control for these two ADCs. The dc remover provides the ac component (v[n], $4i_1[n]$ and $4i_2[n]$) for each channel. The bigger current selected by the current selector is multiplied with the voltage output to give the instantaneous power. With the low pass filter, the average power can be extracted and is continuously accumulated to give the normalized energy, $\sum 4VA$. This value is finally fed to the energy-to-pulse converter to drive an electro-mechanical dial or other pulse-counting display for visual output.

4.1 Frame Detector

A frame is defined as a number of complete ac cycles of the voltage input. It provides a periodic time to update the data in the unit. At the end of each frame, the dc level of the voltage and current input, the current selection and the gain selection are updated. An ac cycle boundary is

detected by checking the zero crossing of the voltage input signal. The selection of the number of cycles per frame is arbitrary but should be sufficiently large. The current design uses 90 cycles as a frame. This averages out the possible error in the voltage dc level and cycle detection. There is a possibility that the assumed dc level lays outside the voltage swing. In this case, a time out is used to end a frame.

4.2 DC Remover

The dc content of an input signal is removed by subtracting the input from its dc level. For a number of multiple cycles (or a frame), the dc level is given by the mean of the total input samples.

i.e. $V_{dc} = \sum V[n] / N$
and $I_{dc} = \sum I[n] / N$

Where N is samples per frame

If the number of cycles is big enough, this will be very accurate.

The dc removers for the two current channels do a little more than the dc remover for the voltage channel. There could be a reversed current flowing if the connection of the mains input and the load output are reversed. This results in a negative power (or negative energy). To prevent this, the sign of the energy output ($\sum$4VA) is checked in each frame boundary. If it is negative, the sign of the ac current output ($4i_1[n]$ or $4i_2[n]$) is reversed so that positive energy will be obtained on the next frame.

It is not strictly necessary to include the dc remover for the current channels if the voltage offset can be found, i.e. the current dc offset can be left unremoved throughout the calculation.

Since $v(t) = V_{dc} + V_o \times \sin(\omega t)$
and $i(t) = I_{dc} + I_o \times \sin(\omega t+\theta)$
then $\sum vi=\sum V_{dc} \times I_{dc}+(V_{dc} \times I_o+I_{dc} \times V_O) \times \sum \sin(\omega t)+V_o \times I_o \times \sum \sin(\omega t)\sin(\omega t+\theta)$

For a complete cycle,

$\sum \sin(\omega t) = 0$

So $\sum vi = \sum V_{dc} \times I_{dc}+V_o \times I_o \times \sum \sin(\omega t)\sin(\omega t+\theta)$

If V_{dc} is found, the computation becomes

$\sum((v-V_{dc}) \times i) = V_o \times I_o \times \sin(\omega t)\sin(\omega t+\theta)$

Which does not include the I_{dc} term.

Certainly, there is always a small error on the V_{dc}, but the only effect is a slightly bigger error in the energy output. So if this can be accepted, the dc remover for the current channels can be ignored.

One further point regarding the dc shift for the current signal needs to be considered. Because of the hardware design, a small dc level variation on the current inputs could severely affect the accuracy. The dc level is amplified by 4 in a high gain mode. This shifts the whole signal up or down and limits the possible input swing. The measurement will be incorrect for large input due

to saturation. If, for example, the range of the ADC is 0 to 3.5 V with a bias of 1.75 V, a 0.2-V dc offset will give 0.8 V in the high gain mode. This shifts the output bias to 2.55 V, and the margin is reduced from 1.75 V to 0.95 V.

4.3 Current Selector

The current selector is included solely for anti-tampering purposes. Tampering with the meter can only consist of reducing or removing one of the current inputs, but not both. The bigger current still reflects the actual amount of electricity used. The simplest way to find the bigger current is to compare the sum of the absolute values of the two current channels. On each frame boundary, the current selector updates a pointer according to the compared result. The pointer then selects a current input on the next frame.

4.4 Gain Controller

As described in section 2.4, the automatic gain control requires the detection of the input current passing a certain threshold. Figure 8 shows how this can be done.

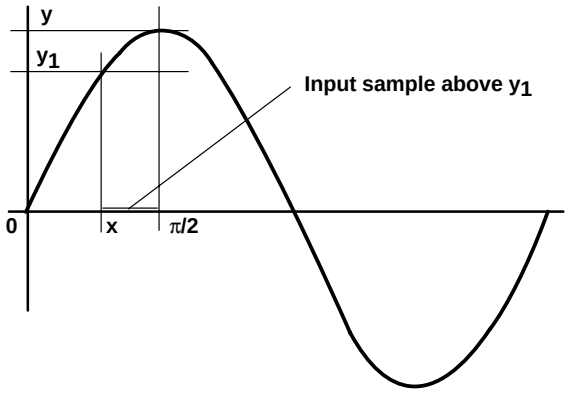


Figure 8. Threshold Detection

Suppose a signal is required to detect whether it is passing a certain threshold *y*. A simple way to do this is to capture the peak, or the maximum sampled value, of the signal. The problem with this method is the serious possibility of false detection in a noisy environment. To improve this, additional points around the peak are taken. Considering a threshold $y_1 = \sin(x)$ which is slightly below *y*, there are ($\pi/2$-*x*) input samples above y_1 in the first quarter cycle. In other words, if the number of samples greater than y_1 is greater than ($\pi/2$-*x*), the signal peak should be greater than *y*. Although this approach does not find the actual peak value, it determines whether the signal passes the threshold. At each frame boundary, the gain controller compares the number of samples above y_1 with the total input samples. If it exceeds or falls below a certain percentage, the gain is switched.

4.5 Low-Pass Filter

The last component on Figure 7 is the low pass filter.

Consider $v(t) = V_o \times \sin(\omega t)$
and $i(t) = I_o \times \sin(\omega t)$
so $p(t) = V_o \times I_o \times \sin^2(\omega t) = (1/2 \times V_o \times I_o) \times (1-\cos(2\omega t))$

From the above equation, the instantaneous power is actually the average power with a ripple on top. The ripple size is so big that it has a peak-to-peak value twice the value of the average power. But, for long term accumulation, it does not matter how big the ripple is as it will be cancelled out after a number of complete cycle integrations. The low pass filter simply improves the stability of the instantaneous display; it has no effect on the overall accuracy.

5 Energy to Pulse Converter

The gain factor of the high voltage front end to the low voltage ADC and the internal scale factors (and/or other constants) required to compute the real energy output are all taken together in the energy display.

If the high voltage front end is governed by

$$V_h(t) = K_v \times v(t)$$
$$I_{1h}(t) = K_i \times i_1(t)$$
$$I_{2h}(t) = K_i \times i_2(t)$$

and the scale factor for internal computation is K_s which gives

$$V(t) = K_s \times v(t)$$
$$I_1(t) = K_s \times i_1(t)$$
$$I_2(t) = K_s \times i_2(t)$$

i.e. $V_h(t) = K_v / K_s \times V(t)$

$$I_{1h}(t) = K_i / K_s \times I_1(t)$$
$$I_{2h}(t) = K_i / K_s \times I_2(t)$$

then the accumulated energy is

$E = \sum V_h A_h \times t_c$	Where t_c is the sampling period and A_h is I_{1h} or I_{2h} which ever is higher
$= \sum VA \times K_v \times K_i / K_s^2 \times t_c$	where A is I_1 or I_2 which ever is higher
$= \sum E_s / 4 \times K_v \times K_i / (K_s^2 \times f_s)$	where $E_s = 4VA$ and $f_s = 1/t_c$ is the sampling freq

Assuming the energy is displayed in 0.1-KWh (Kilowatt-hour) resolution, the displayed value is

$$E_d = E / (0.1 \times 1000 \times 3600)$$
$$= \sum E_s / \delta \quad \text{where } \delta = 0.1 \times 1000 \times 3600 \times 4 \times K_s^2 \times f_s/(K_v \times K_i)$$

Obviously, δ is the unity display energy in the domain of the internal scaled energy $E_s = 4VA$. If each δ is represented by a single pulse, the total energy can be shown on a pulse-count type of display. Using δ as a threshold, a simple approach for pulse generation is developed. Figure 9 is the flow diagram.

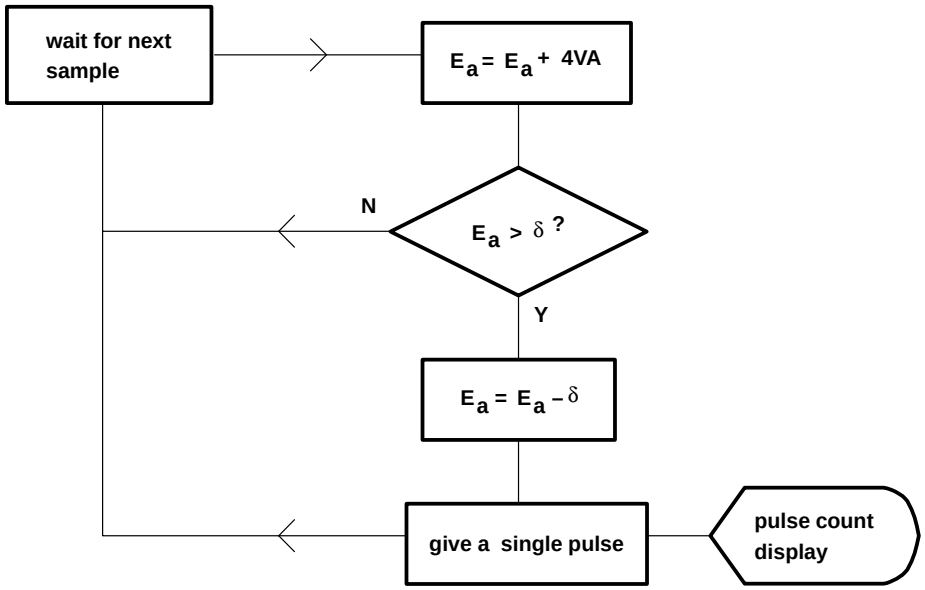


Figure 9. Flow Chart for the Incremental Energy Display

For each sample input, the sampled and scaled energy E_S = 4VA is first added to the accumulated energy E_a. If E_a is greater than the unity energy δ, subtracts δ from E_a and gives a pulse output. The display is incremented by 1.

A typical pulse-count display device is an electro-mechanical dial. This kind of display can be emulated using a decimal counter in the software. The counter value is displayed on an LCD or on 7-segment LEDs.

In case a high frequency pulse is required for accuracy measurement, δ can be reduced accordingly to give more frequent pulses. Each energy display pulse is taken as a number of these small pulses.

6 Calibration

Although most of the critical resistors for different gain control are (or should be) high accuracy, calibration is required to further improve the accuracy to meet tight requirements. Although the current and voltage channels are separated, calibration is done together on the volt-ampere product. As there are two gain stages for each current, this gives four calibration points. This is troublesome and time consuming in real production, so an automatic or self-calibration method is needed to make production easier.

The idea is to read a number of energy pulses from an accurate reference meter connected in parallel. The time taken is compared with the time of the same number of pulses generated internally. The compared errors or calibration factors are stored on an EEPROM that can be used to adjust the reading in normal operation.

7 Summary

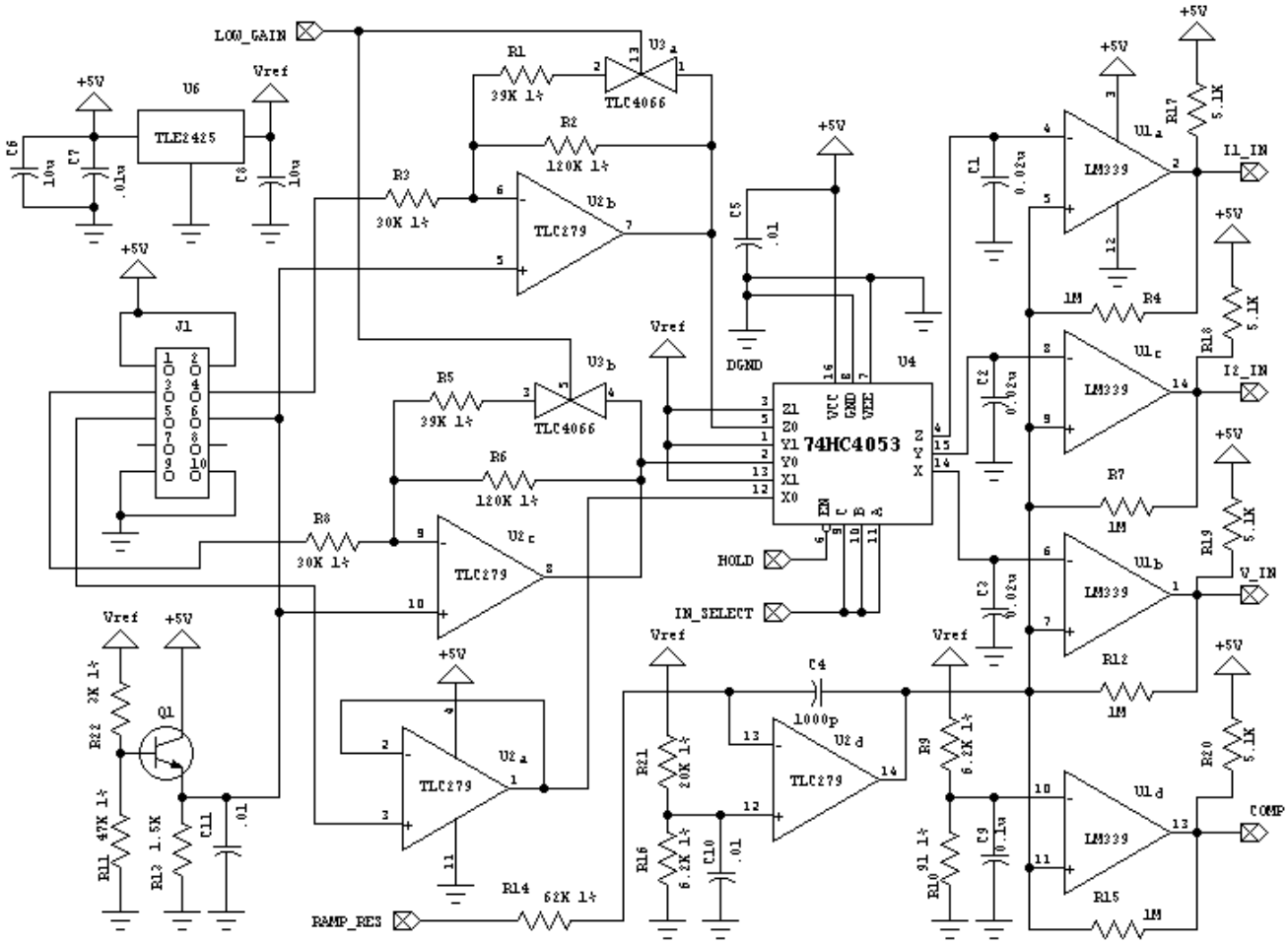
This application report illustrates how a low-cost fully electronic electricity meter can be constructed using the MSP430C11x. Other more sophisticated solutions exist but they invariably

are more expensive since they do not have the advantage of the low cost ADC stages and the low cost processing power. In this application, the low cost ADC is tightly coupled with the internal timer of the 'C11x and the high performance 16-bit core fulfills the requirements of the demanding measurement algorithms. This makes the MSP430C11X based e-meter circuit very cost competitive.

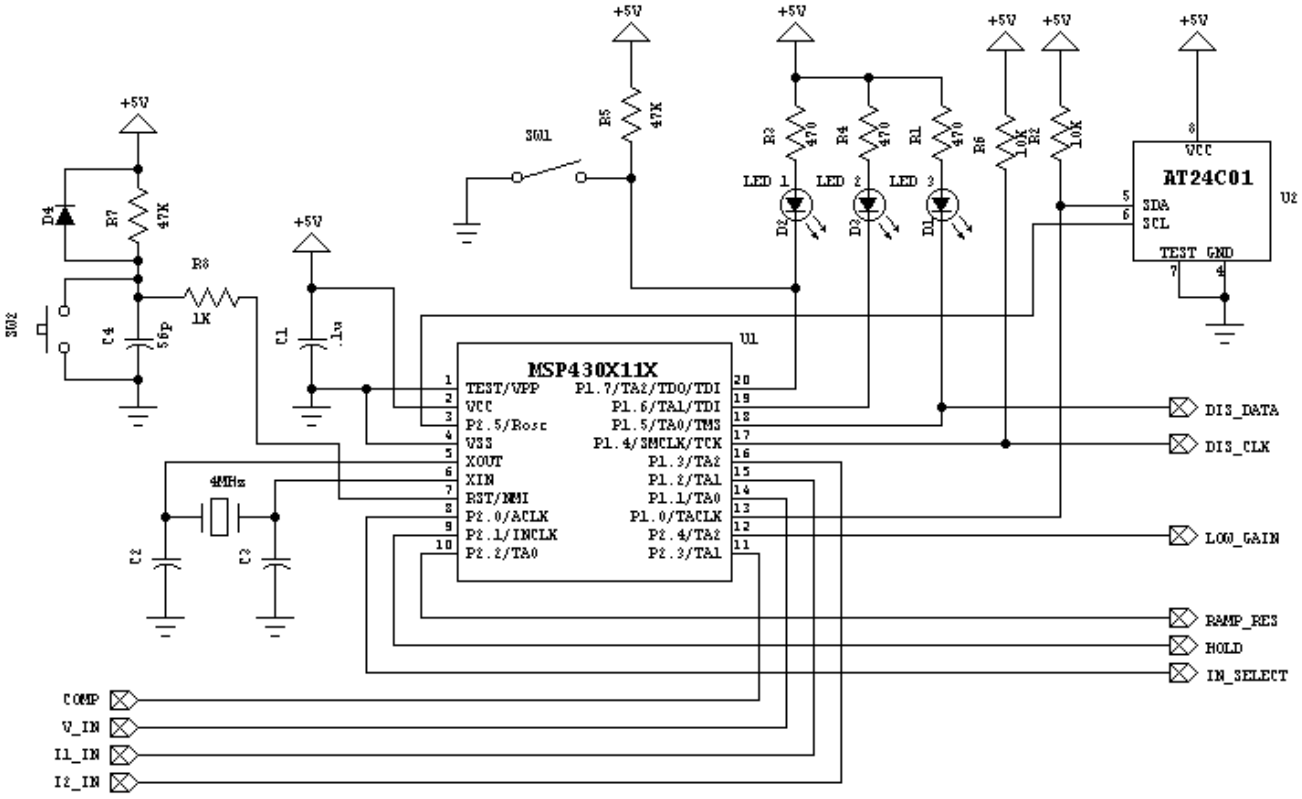
8 References

1. Bureau of Indian Standards, *AC Static Watthour Meters*, Class 1 and 2 Specification, Reference number ET13 (1379)
2. MSP430 Family, *Architecture Guide and Module Library User's Guide*, Literature Number SLAUE10B
3. MSP430 Family, *Metering Application Report*, Literature Number SLAAE10C
4. MSP430 Family, *Software User's Guide*, Literature Number SLAUE11
5. MSP430 Family, *Assembly Language Tools User's Guide*, Literature Number SLAUE12

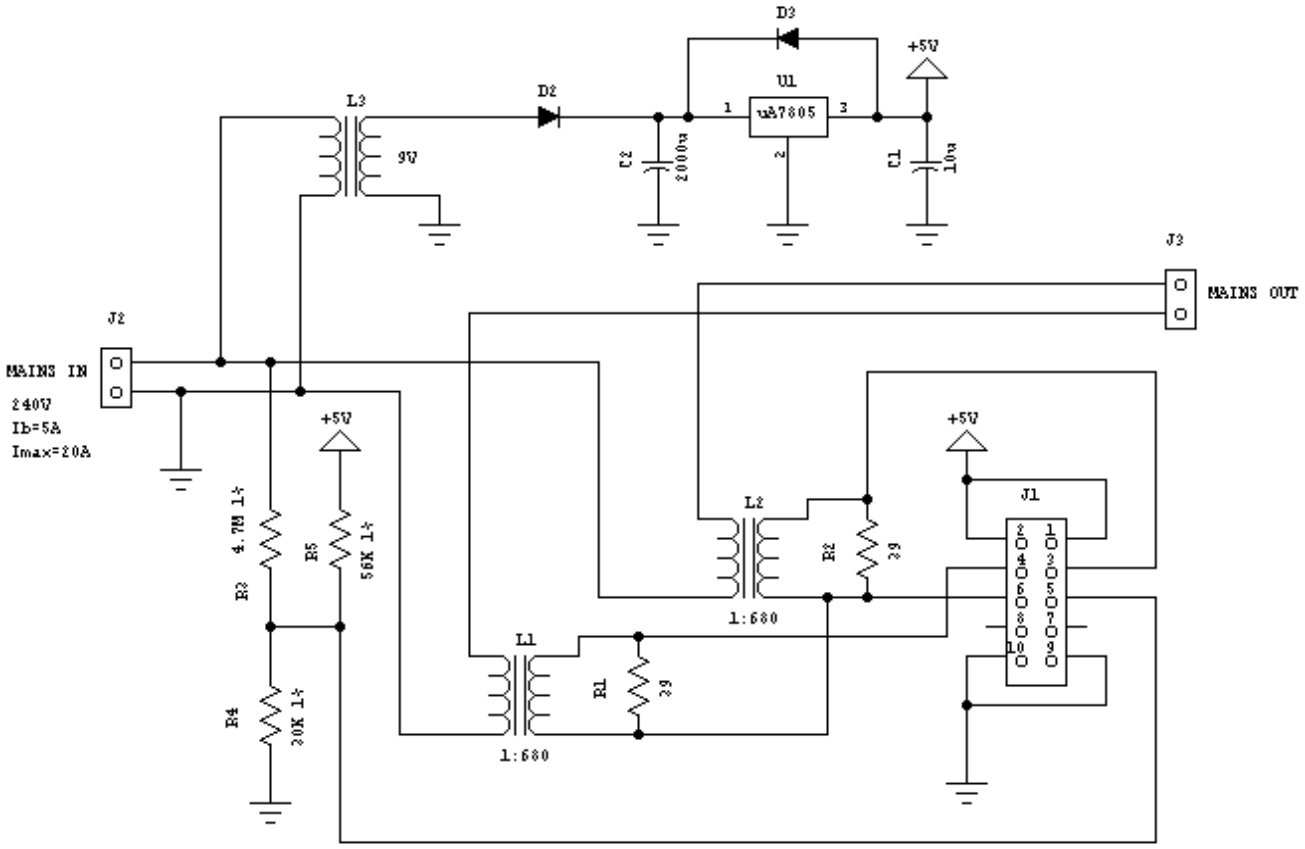
Appendix A Schematics



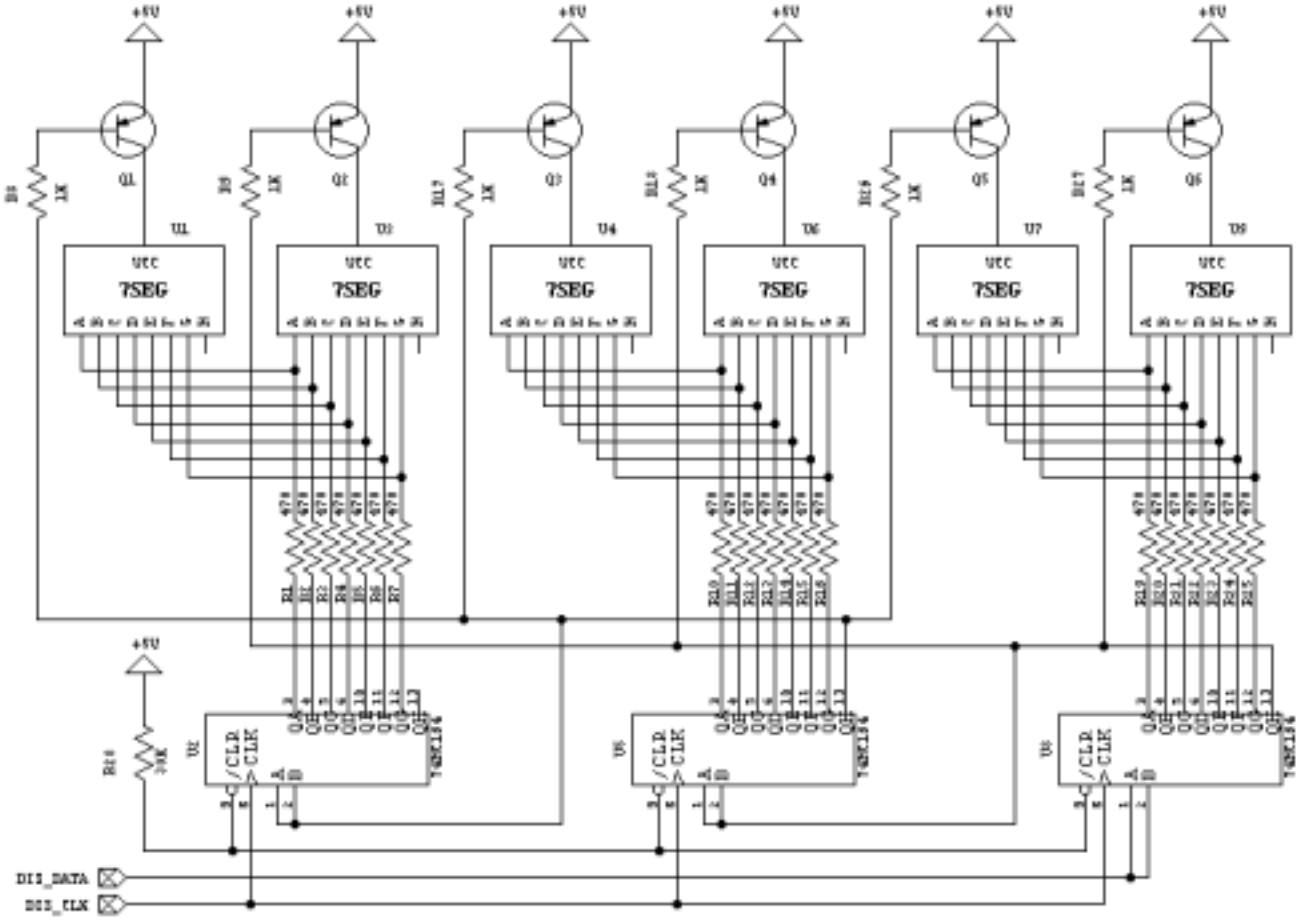
Schematic 1


+5V
D4
R7
47K
R8
1K
S002
C4
56p
C1
S001
R5
47K
LED 1
LED 2
LED 3
D2
D3
D1
R3
470
R4
470
R1
470
R6
10k
R2
10k
U2
AT24C01
SDA
SCL
TEST
GND
VCC
U1
MSP430X11X
TEST/VPP
VCC
P2.5/Rosc
VSS
XOUT
XIN
RST/NMI
P2.0/ACLK
P2.1/INCLK
P2.2/TA0
P1.7/TA2/TDO/TDI
P1.6/TA1/TDI
P1.5/TA0/TMS
P1.4/SMCLK/TCK
P1.3/TA2
P1.2/TA1
P1.1/TA0
P1.0/TACLK
P2.4/TA2
P2.3/TA1
4MHz
C2
C3
DIS_DATA
DIS_CLK
LOW_GAIN
RAMP_RES
HOLD
IN_SELECT
COMP
V_IN
I1_IN
I2_IN

Schematic 2


D3
+5V
U1
uA7805
L3
D2
9V
C2
2000u
C1
10u
J3
MAINS OUT
J2
MAINS IN
240V
Ib=5A
Imax=20A
+5V
+5V
4.7M 1%
R3
R5
56K 1%
L2
R2
39
1:680
J1
L1
R1
39
R4
20K 1%
1:680

Schematic 3


+5V
Q1
Q2
Q3
Q4
Q5
Q6
1K
U1
U2
U3
U4
U5
U6
U7
U8
Vcc
7SEG
/CLR
CLK
74HC164
DIS_DATA
DIS_CLK

Schematic 4

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