

Design Guidelines for the TLC320AD50

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ABSTRACT

This document provides board-level guidelines and techniques for designing with the TLC320AD50. This includes topics such as printed-circuit board construction, power-supply decoupling, noise reduction, and general design guidelines. The intent is to provide strategies to help users attain first-pass design success with the TLC320AD50.

A flow diagram explaining the initialization of the AD50 after power-up reset is included.

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1 Introduction

The TLC320AD50 (AD50) is an analog-interface circuit that provides high-resolution conversion from analog to digital (A/D), and from digital to analog (D/A) using oversampling sigma-delta technology. The AD50 is a mixed-signal device, and the user should follow good mixed-signal printed-circuit board design practices when designing with this device.

This document presents design techniques to help achieve first-pass success with the AD50. Appendix A presents a sample flow diagram depicting the initialization scheme for the AD50.

2 PC Board Construction

The printed-circuit board containing a TLC320AD50 can be fabricated with as few as four layers. Standard FR4-type material can be used. For best performance, the layers should be configured as follows:

- Top (layer 1): signal
- Internal Layer 2: ground
- Internal Layer 3: power
- Bottom (layer 4): signal

The ground and power planes are sandwiched between the top and bottom signal-carrying layers. This minimizes the coupling of RF noise into the system by providing a very low impedance between power and ground, and by shielding signal traces.

2.1 Ground Plane Details

The AD50 is designed with separate analog and digital ground pins (AVss, DVss) to avoid coupling of digital signals into the analog circuits.

To obtain the best signal-to-noise ratio, it is recommended that the ground plane on the printed-circuit board be split into separate analog and digital sections, with the AD50 ground pins connected to their respective planes. The analog and digital ground planes should be joined together in only one place, preferably back at the power supply.

The analog and digital ground planes should be designed with the split occurring under the AD50 package, between the analog and digital ground pins of the device. The splitting of the ground plane prevents digital noise from corrupting the analog circuits within the device.

2.2 Power Plane Details

The AD50 is designed with separate analog and digital power pins (AVdd, DVdd). Table 1 shows the power configurations possible.

Table 1. Power Configurations

OPTION	ANALOG POWER (AV _{DD} and AV _{DD} (PLL))	DIGITAL POWER (DV _{DD})
Option #1	5 V	5 V
Option #2	5 V	3.3 V

For an ideal design, it is recommended that separate analog and digital power be supplied to the AD50. This can be accomplished because the AD50 can operate from a 5-V supply for the analog circuitry, and a 3.3-V supply for the digital circuitry.

However, if 5 V is used to power both the analog and digital power pins on the AD50, the use of two separate 5-V supplies rarely occurs. When a single 5-V supply is used to power both the digital and analog circuits, it is suggested to isolate the power going to the analog supply of the AD50 from the digital supply, as shown in Figure 1.

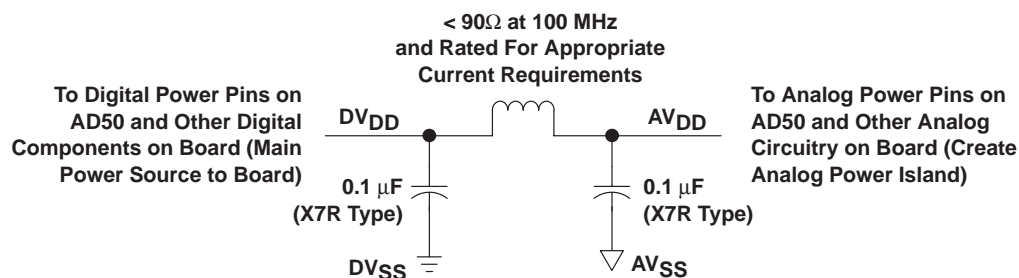


Figure 1. Isolating Analog and Digital Powers to the AD50

A ferrite bead isolates and filters the power supplied to the analog supply pin. Two high-frequency bypass capacitors are also used, one on either side of the ferrite bead. Basically, a separate analog power island is created for the AD50.

The connection from the ferrite bead to the HF decoupling cap and analog power pins on the AD50 should be done as an *island* or small plane. If this is not possible, very wide traces should be used, as wide or wider than the pad on the surface-mount discrete components.

3 Special Connections

Several pins on the AD50 should be either decoupled to a specific power or ground, or attached directly to those planes. The following section details these special connections.

3.1 Analog Power and/or Ground Planes

The connections described in Table 2 must go directly to the analog power and/or ground planes.

Table 2. Connections to the Analog Power and/or Analog Ground Planes

PIN OR COMPONENT NAME	DESCRIPTION	CONNECTION
AVss	Analog ground reference pin on the AD50	Connected directly to the analog ground plane
AVss (PLL)	Analog ground pin for the internal PLL on the AD50	Connected directly to the analog ground plane
AVdd	Analog power supply pin for the AD50	Connected directly to the analog power plane or island
AVdd (PLL)	Analog power supply for the internal PLL on the AD50	Connected directly to the analog power plane or island
HF-bypass capacitor #1 (0.1 μ F)	HF decoupling of the analog power supply on the AD50	Connected between the analog power and analog ground planes, located at the AVdd pin on the AD50.
HF-bypass capacitor #2 (0.1 μ F, X7R type ceramic)	HF decoupling of the Analog PLL power supply on the AD50	Connected between the analog power and analog ground planes, located at the AVdd (PLL) pin on the AD50.
HF-bypass capacitor #3 (0.1 μ F, X7R type ceramic)	HF decoupling of the bandgap reference on the AD50	Connected between the FILT pin and analog ground planes, located at the FILT pin on the AD50.
LF-bypass capacitor #1 (optional 22-47 μ F, electrolytic)	Optional low-frequency decoupling of the analog power supply on the AD50.	Connected between the analog power and analog ground planes, located at the AVdd pin on the AD50.

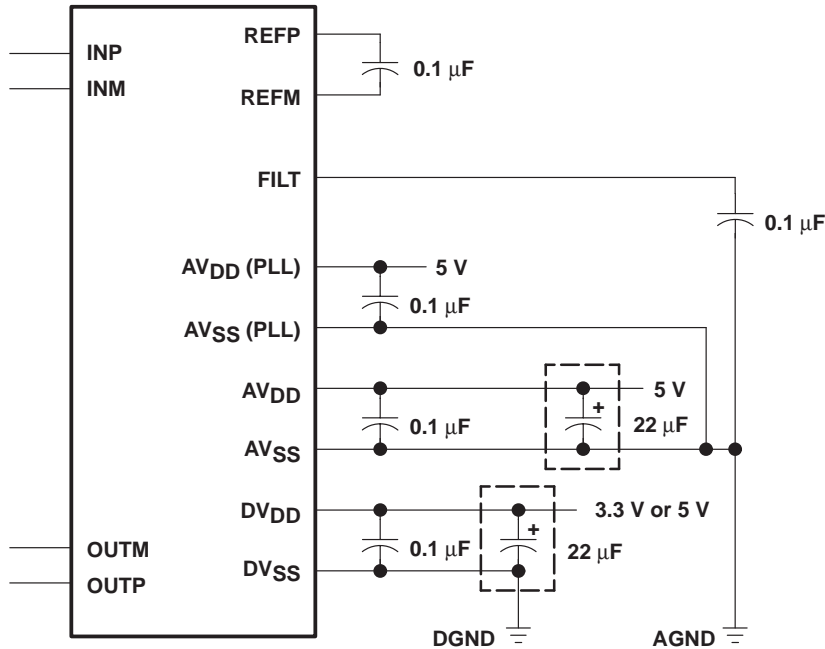
3.2 Digital Power and/or Ground Planes

The connections described in Table 3 must go directly to digital power and/or ground planes.

Table 3. Connections to the Digital Power and/or Digital Ground Planes

PIN OR COMPONENT NAME	DESCRIPTION	CONNECTION
DVss	Digital ground reference pin on the AD50	Connected directly to the digital ground plane
DVdd	Digital power supply pin for the AD50	Connected directly to the digital power plane
HF-bypass capacitor #4 (0.1 μ F, X7R type ceramic)	HF decoupling of the digital power supply on the AD50	Connected between the digital power and digital ground planes, located at the DVdd pin on the AD50.
LF-bypass capacitor #2 (optional 22-47 μ F, electrolytic)	Optional low-frequency decoupling of the digital power supply on the AD50	Connected between the digital power and digital ground planes, located at the DVdd pin on the AD50.

Refer to Figure 2 for a schematic showing the decoupling capacitors required.



NOTE: Components in Dashed Boxes are Optional

Figure 2. Decoupling Requirements for the AD50

3.3 Bandgap Voltage Reference Pin Decoupling

The internal bandgap reference voltage (REFP and REFM) for the converters is brought out to pins on the AD50. External filtering of this bandgap reference voltage is required. A 0.1- μF ceramic capacitor must be located at the REFP pin and connected across pins REFP and REFM. A surface-mount component should be used.

3.4 Bandgap Filter Reference Decoupling

External decoupling of the power supply to the bandgap reference is required. The FILT pin is provided as this point in the circuit. A 0.1- μF ceramic capacitor must be located at the FILT pin and connected between the FILT pin and analog ground (AVSS).

4 Clocks

Termination of high-frequency digital signals, such as clock signals, depends on the frequency of the clocks being used, the length of the signal traces, and the rise and fall times of these clock signals.

In many cases it is useful to place series-termination resistors at the clock-source pin. It is easier to place a shunt or zero-ohm resistor across the pads if the termination is not required, than to spin a board just to add a series resistor. In a board design using the AD50, it is useful to place a series-termination resistor at the following clock source points:

- At the oscillator or clock source for MCLK

- At the SCLK pin of the AD50, when the AD50 is configured as a master (M/S=high)

See Figure 3 for the optimum location of the series resistor.

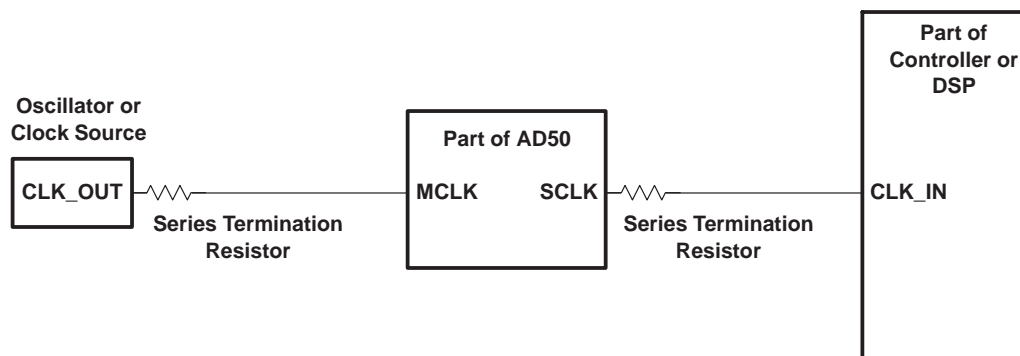


Figure 3. Termination of Clocks

5 Resetting the AD50

Properly controlling the AD50 during and after reset is very important.

- The AD50 requires at least six full MCLK cycles to occur while the reset is active (low).
- A finite amount of time is required *after* reset is inactive (high) before the control registers in the AD50 are written. It is suggested that the controller wait a minimum of 150 μ s after reset is inactive before writing control words or configuration data to the AD50.
- The internal phase locked loop circuitry requires at least 18 frame syncs to occur before valid conversion data is available. The internal PLL circuitry needs at least 18 frame syncs to occur before it is stabilized.

These timing requirements apply to both hardware and software resets.

6 General

It is important to design and lay out a printed-circuit board properly to attain a low noise, high-quality design. In addition to the techniques and tips previously suggested, a few other points can contribute to producing a low noise system:

- Keep analog and digital-signal traces physically separated from each other.
- Do not run analog and digital signals side by side.
- Run high-speed clock lines entirely on the top or bottom signal layers, and avoid using vias on these lines.
- Route clock signals carefully so they are kept away from analog signals and circuitry, as well as from any voltage references.
- Always try to use solid ground planes—do not use routed ground traces.
- Use surface-mount discrete components to minimize parasitic capacitance and inductance.

- Locate power-supply decoupling capacitors at power supply pins on devices. Place ceramic capacitors (HF capacitors) closer to IC pins when using both HF and LF bulk capacitors.
- Locate switching power supplies away from analog circuits.
- Adequately filter power-supply inputs to the PC board at the power-supply input to the board. Both high and low-frequency decoupling should be used.
- Keep clock-trace paths as short as possible.
- Route analog signals and the analog power plane over the analog ground plane (not the digital ground)
- Route digital signals and the digital power plane over the digital ground plane (not the analog ground)

7 Preventing Latch-Up

Latch-up is possible in all CMOS devices. It is caused by the firing of a parasitic transistor that is present due to the inherent nature of CMOS devices. When a latch-up condition occurs, the device draws excessive amounts of current and continues to draw heavy current until power is removed. Latch-up can result in permanent damage to the device if supply current is not limited.

Even though the AD50 is heavily protected against latch-up, it is still possible to cause a latch-up condition under certain conditions in which excess current is forced into or out of one or more terminals. Latch-up can occur when the supply voltage drops momentarily below ground, or possibly when a signal is applied to a terminal after power has been applied, but before the ground is connected.

To ensure that latch-up does not occur, it is considered good design practice to connect a reverse-biased Schottky diode with a forward-voltage drop that is less than or equal to 0.4 V (1N5711 or equivalent) between the power supply and its ground.

7.1 Device Power-Up Sequence

Latch-up can also occur if a signal source is connected without the device being properly grounded. A signal applied to one terminal could then find a ground through another signal terminal on the device. To ensure proper operation of the device, and as a safeguard against this sort of latch-up, it is recommended that the following power-up sequence be observed:

- Ensure that no signals are applied to the device before the power-up sequence is complete.
- Connect the ground.
- Apply power (AVdd, then DVdd).
- Force a power-down condition in the device using the hardware power-down feature.
- Connect the master clock.
- Release the power-down condition.
- Apply the analog signals.

When powering down the device, this procedure should be followed in reverse order.

8 Using AD50s as Slaves With No Masters

In some designs, it can be useful to configure one or more AD50's as slave devices, without configuring an AD50 as a master. This configuration is acceptable, but may require additional components to generate the frame syncs and clocks required.

Table 4 lists the configuration of the I/O pins required to achieve the slave configuration, including their direction and description. Figure 4 shows a sample interconnection between a TMS320Cxxx DSP and multiple AD50s configured as slaves.

Table 4. AD50 I/O Configuration for Slave Mode

PIN NAME	CONFIGURATION	DESCRIPTION
$\overline{\text{FS}}$	Input	Frame sync input generated by controller or other logic
M/S	Input tied low	Configures device as slave
SCLK	Input	Shift clock generated by controller or other logic

Note that the controller or other logic must generate the frame sync for all slave AD50s as well as for the DSP, and must also generate the shift clock for all the slave devices.

The DSP must receive a frame sync for every AD50 slave data communication. Therefore, multiple frame syncs (slave1, slave2, DSP, and so on) are required from the external logic or controller:

- One frame sync is provided to the DSP for continual frame-sync pulses for every time slot.
- One frame sync is provided for every slave, where each slave frame sync is active only in its designated time slot.

A timing diagram for the frame syncs generated by the PLD is shown in Figure 5.

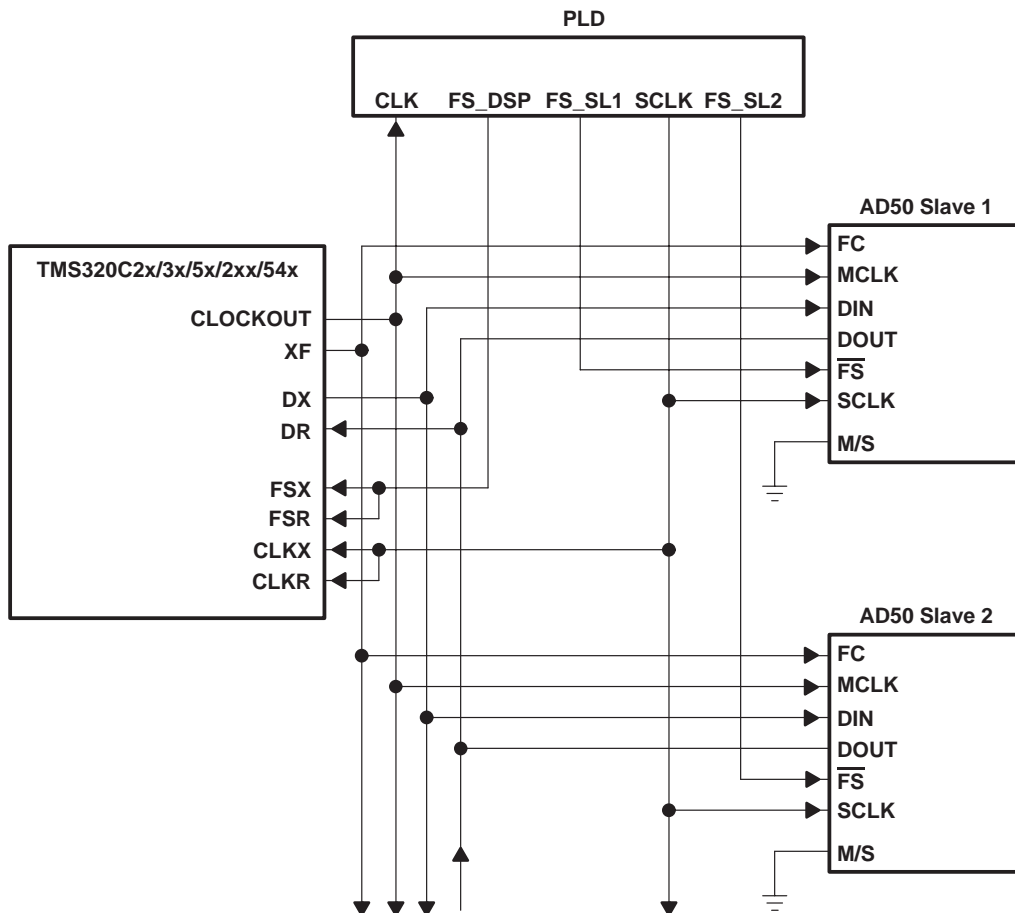


Figure 4. DSP Interfaced to AD50 Slaves

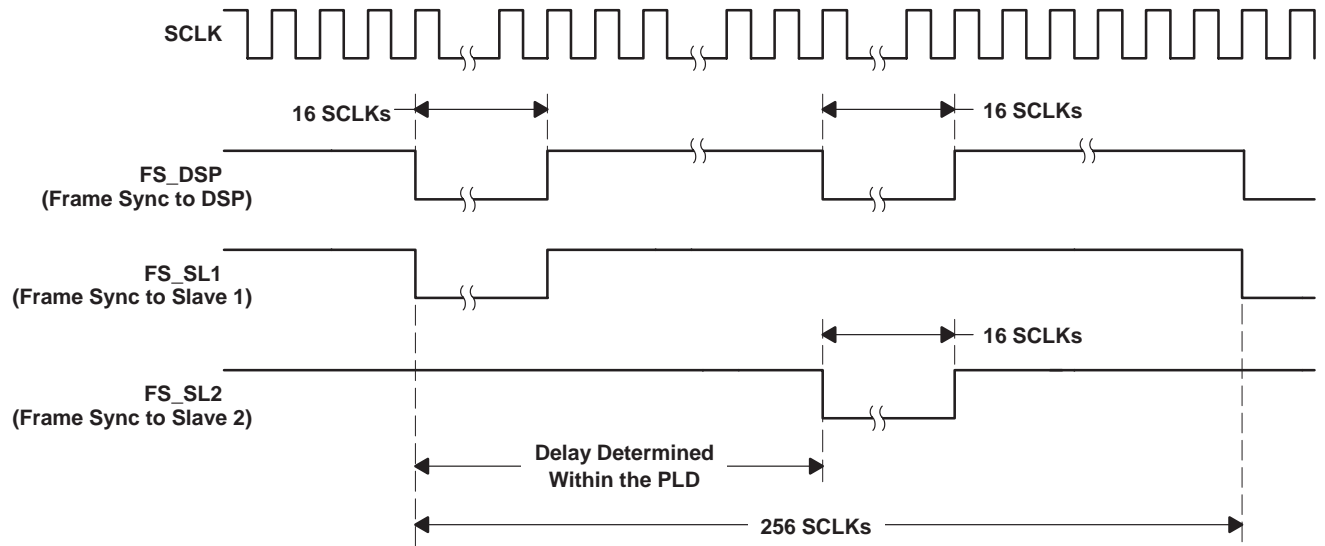


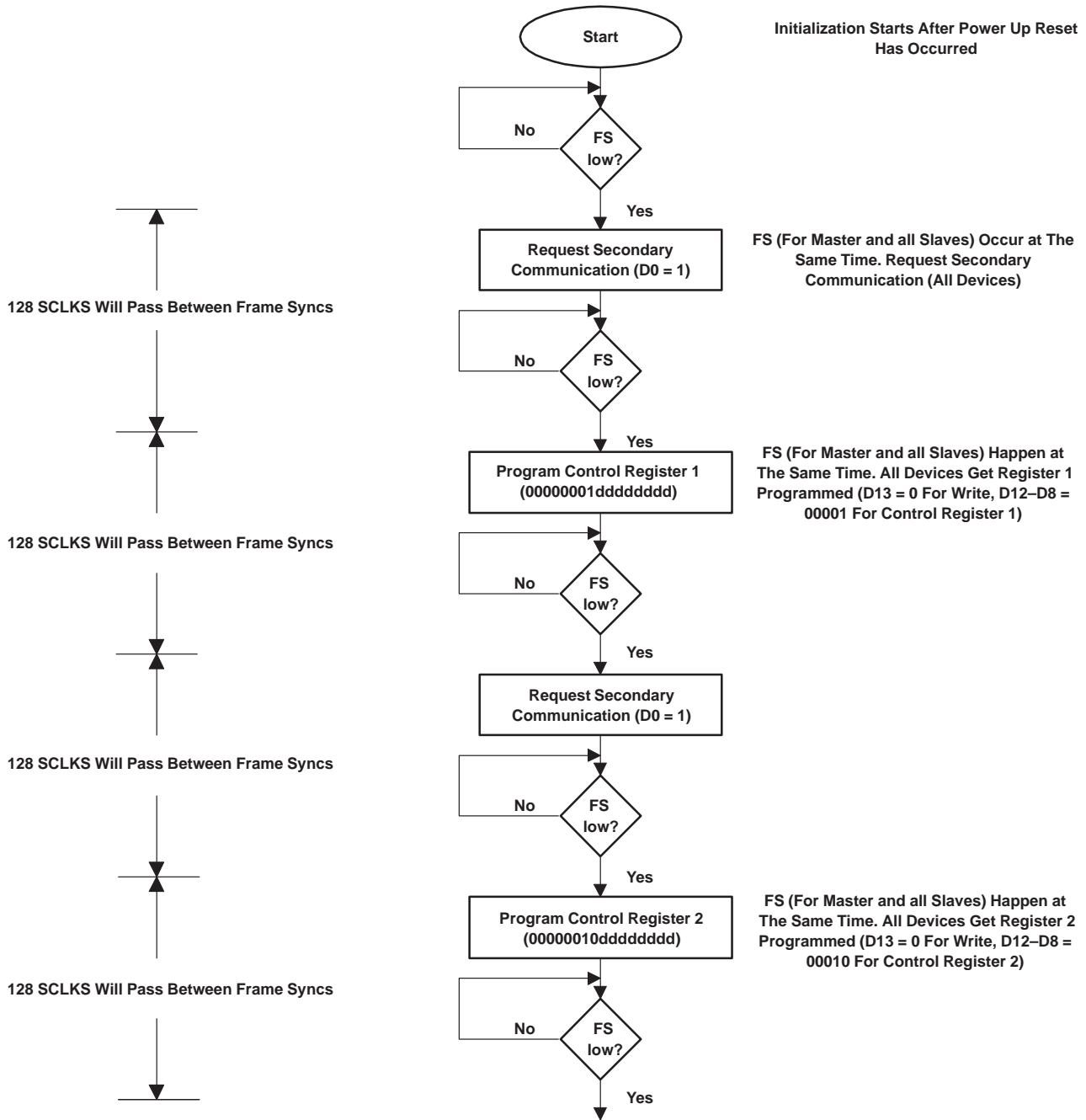
Figure 5. Timing Diagram for Frame Syncs Generated by PLD for All-Slave Configuration

9 References

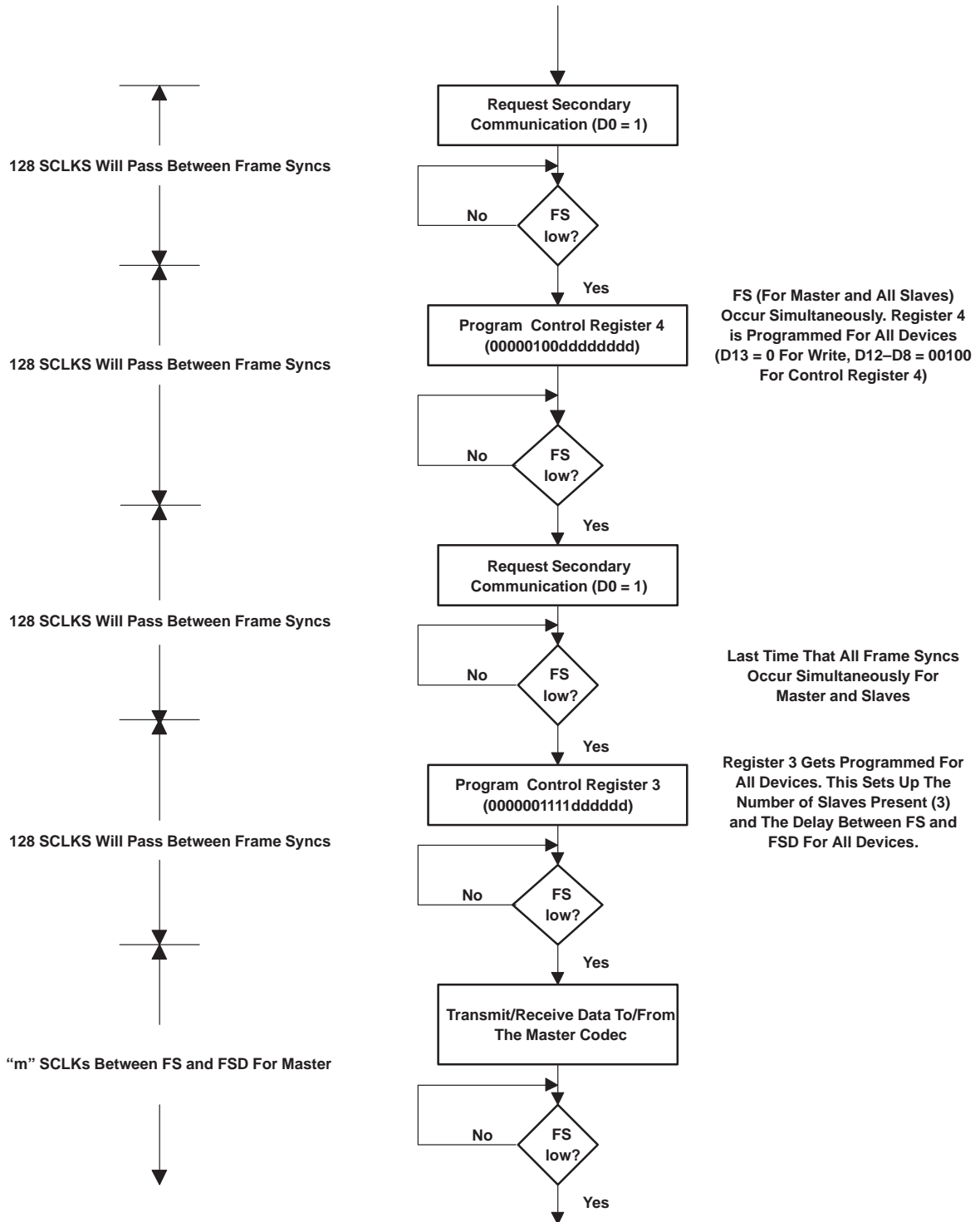
1. *TLC320AD50C/I, TLC320AD52C Data Manual*, literature number SLAS131
2. *Evaluation Board for the TCL320AD50C DSP Analog Interface Circuit*, literature number SLAAE15

Appendix A AD50 Initialization

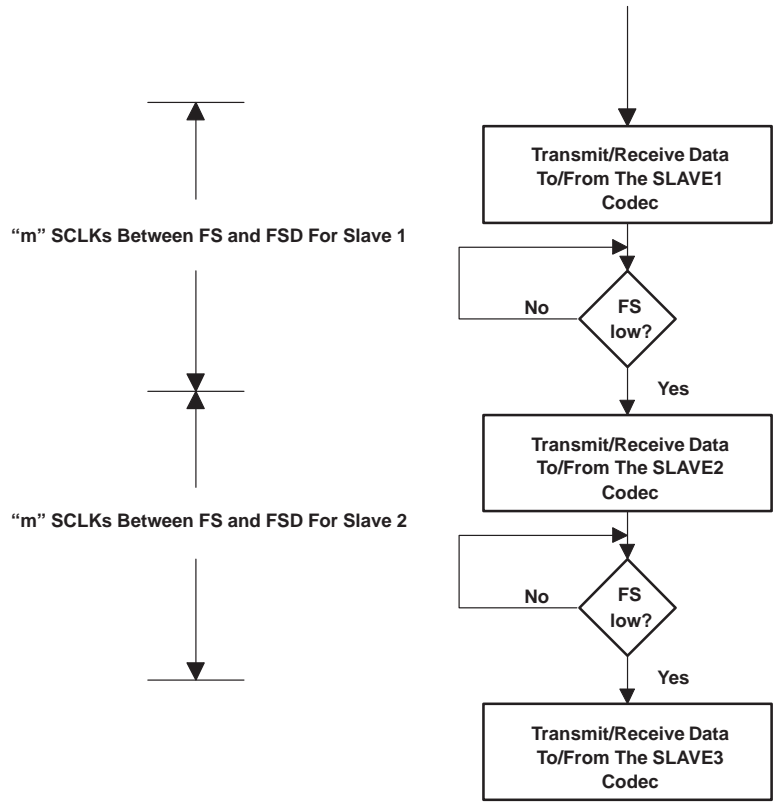
A.1 Flow Chart for Initializing a TLC320AD50 With One Master and Slaves



A.1 Flow Chart for Initializing a TLC320AD50 With One Master and Slaves (Continued)



A.1 Flow Chart for Initializing a TLC320AD50 With One Master and Slaves (Continued)



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