Interfacing the ADS8364 to the TMS320F2812 DSP

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ABSTRACT

The ADS8364 16-bit parallel output analog-to-digital converter has a number of features that allow for an easy interface to the TMS320F2812 digital signal processor. This application note focuses on configuring, sampling, and converting analog data presented to the ADS8364 ADC. Portions of ports A, E, and F are used for general-purpose control, while the parallel data bus accepts data from the ADC via RE, WE and IS. The software code developed for this application note shows how the ADC's end of conversion (EOC) pin can be used as an interrupt source to the host processor. The sample code discussed in this application note can be downloaded from http://www.ti.com/lit/zip/SLAA163.

Contents

1 Introduction 2
2 The ADS8364 EVM Interface 3
3 Setting Up The eZdsp F2812 4
3.1 Setup of The Conversion Clock 4
3.2 Set Up Port A, E, and F GPIO / Pin Functions 4
3.3 Chip Select (CS), Read (RD) and Write (WR) 4
4 ADC Initialization and Operation 5
4.1 RESET 5
4.2 HOLDx 5
4.3 End of Conversion (EOC) 5

Figures

Figure 1. System Block Diagram. 2
Figure 2. ADS8364 Waveforms 6

Tables

Table 1. ADS8364EVM to The eZdsp F2812 3
Table 2. ADS8364EVM Address Definitions 4

1 Introduction

The ADS8364 is a six channel, simultaneous sampling, 16-bit parallel ADC. The device features a chip select (CS), input clock (CLK), parallel data input (D [0:15]), and flexible control signals that can interface directly to the TMS320C2000™ DSP platform of digital signal processors.

The ADS8364 operates from 5-volt analog (AVdd) and digital (DVdd) supplies. The device also incorporates an internal buffer that can be powered from the same 3.3-V supply as the DSP. The buffer voltage (BVdd) allows direct interfacing to 3- or 5-volt systems, eliminating the need to level shift the data and control lines.

The sample code for this report was developed using *Code Composer Studio*™ V2.12 on the TMS320F2812. This simple code example demonstrates how to configure the DSP, initialize the data converter, and process an interrupt (via the EOC pin) from the data converter.

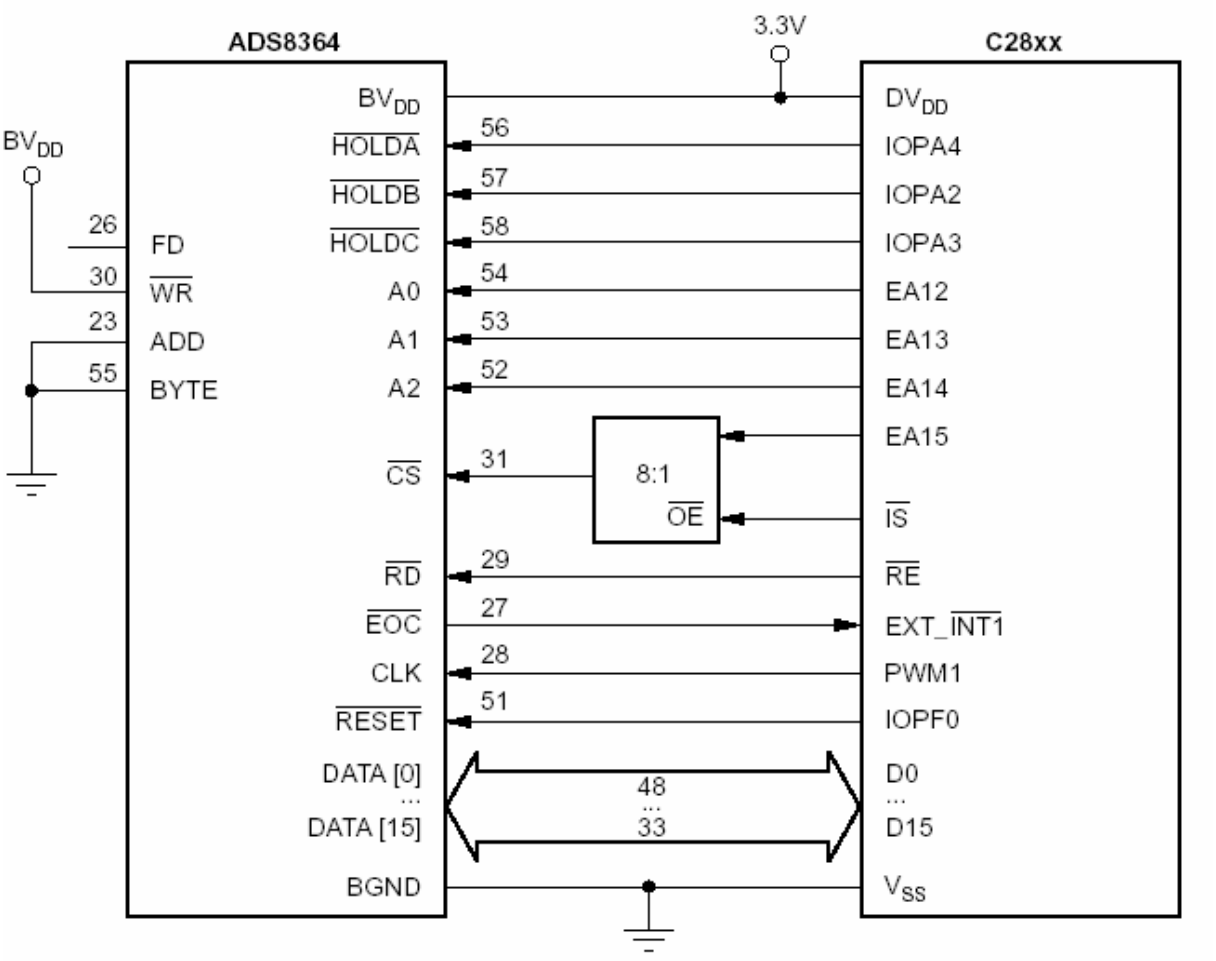

Figure 1. System Block Diagram

2 The ADS8364 EVM Interface

The ADS8364 operates from a maximum clock frequency of 5 MHz. The sample / conversion process is completed within 20 conversion clock cycles. All six channels of the ADS8364 can be sampled and converted simultaneously, providing a maximum 250 ksps throughput rate. In this application note, the ADS8364 is operated from a 4.4 MHz clock, providing a throughput of approximately 140 ksps per channel.

The EVM uses four address lines to access the data converter. The user has the option of selecting A2 through A5, or A12 through A15. The lower address lines control the A0, A1 and A2 pins of the ADC, while the upper most address line is sent through a single gate inverter to act as chip select (CS).

The DSP's read enable (RE), write enable (WE) and I/O chip select (IS) are all used in the parallel interface to read data from; as well as write commands to; the ADC. The lower 16 data lines from the DSK are connected directly to the ADC—aligned LSB to LSB.

This application note uses the eZdsp F2812 from Spectrum Digital, Incorporated, (www.spectrumdigital.com). Table 1 shows the connections incorporated on the evaluation module for the ADS8364 and the eZdsp F2812.

Table 1. ADS8364EVM to The eZdsp F2812

EVM Connector / Pin No.	eZdsp Connector / Pin No.	ADC Pin No.	Signal Description
J11.7-10	P2.31-34	31,56, 57, 58	Upper address selection via U10 and U11
J11.23-26	P2.21-24	31,56, 57, 58	Lower address selection via U10 and U11
J11.53-60	P2.11-18	33-40	Upper data byte [D15..D8]
J11.63-70	P2.3-10	41-48	Lower data byte [D7..D0]
J11.73	P2.44	29	ADC input - RD
J11.74	P2.43	30	ADC input - WR
J12.35	P8.11	57	ADC input - HOLD_B#
J12.36	P8.24	51	ADC input - RESET#
J12.39	P8.13	56	ADC input - HOLD_A#
J12.41	P8.12	58	ADC input - HOLD_C#
J12.45	P8.9	28	ADC input – CLOCK (optional)
J12.53	P8.5	27	ADC output - EOC

3 Setting Up The eZdsp F2812

The following section provides details on assigning the parallel data and communication pins to the ADS8364 device.

3.1 Setup of The Conversion Clock

The PWM1 output of the F2812 is an excellent conversion clock source for the ADS8364. For the purpose of this application note, the PWM1 output is set for 50/50 duty cycle to provide an approximate 4.4 MHz conversion clock to the converter. An external conversion clock can also be applied through BNC connector (J9) and jumper W15. The maximum clock conversion clock rate for the ADS8364 is 5 MHz.

3.2 Set Up Port A, E, and F GPIO / Pin Functions

In order to show the flexible interface of the ADS8364, ports A, E, and F port on the F2812 are used as a general purpose I/O, Ext interrupt via EOC, and PWM output for the conversion clock.

Setting up the F2812 ports as GPIO is a fairly straightforward task—simply clear the associated MUX Control register then set the port data register (GpioDataRegs) for the desired functions. The EVM uses GPIOA.2, 3, 4 and GPIOF.1 as general-purpose outputs for the HOLDx and RESET functions.

3.3 Chip Select (CS), Read (RD) and Write (WR)

Chip select to the ADS8364 is an active-low input signal. When CS is high, the parallel data pins are in a high-impedance state. When CS is low, the parallel data lines reflect the current state of the output buffers. In order to properly read data from the parallel data bus of the ADS8364, CS to the device must be asserted. The ADS8364EVM uses the DSP's IS signal as a master chip select for the board. Since the ability to select two different address spaces is implemented in the EVM's design, the MSB of the address space is inverted and used as the chip select when writing to, or reading from the ADCs' base address. The additional three address lines control the A0 – A2 hardware pins as shown in table 2.

Table 2. ADS8364EVM Address Definitions

Lower Address	Function	Upper Address
0x080020	ADC base address—enable CS, select CH_A0	0x088000
0x080024	Select CH_A1	0x089000
0x080028	Select CH_B0	0x08A000
0x08002C	Select CH_B1	0x08B000
0x080030	Select CH_C0	0x08C000
0x080034	Select CH_C1	0x08D000
0x080038	Select CYCLE mode	0x08E000
0x08003C	Select FIFO mode	0x08F000

Read (RD) and write (WR) are also active low signals. When CS is low, the output buffers of the ADS8364 are updated on the falling edge of the RD signal. Data is read into the F2812 on the following rising edge of RD.

The ADS8364 can also be controlled through software commands. This is accomplished by writing to the lower BYTE of the ADC. When using software control, it is only necessary to write to the base address of the ADS8364 to enable the chip select. Channels A0 through C1 can be read individually, or the CYCLE and FIFO modes can be set. For more information on controlling the ADS8364 through software commands, please refer to document number SLAA155. Enter SLAA155 in the search window from the Texas Instruments home page (www.ti.com)

4 ADC Initialization and Operation

4.1 RESET

Toggling the active low reset pin (RST) of the ADS8364 ensures that the read pointer is pointing to the first data position. As part of the initialization sequence for the ADC, the RST pin of the ADS8364 toggled via GPIOF.1. GPIOF.1 is initially asserted high, then toggled low after the system clocks are stabilized. This ensures the data output of the ADC is aligned with the first set of data corresponding to channel A0, then A1, B0, B1, C0 and finally C1.

4.2 HOLDx

The HOLDx pins on the ADS8364 are active low sampling triggers. When the three HOLD lines are brought low together, all six analog inputs are simultaneously sampled—the conversion process begins on the next rising clock edge. The conversion is completed after 20 clock cycles, at which time the end of conversion pin goes low for 1/2 clock cycle. The HOLDa, HOLDb and HOLDc lines are controlled by GPIOA.4, GPIOA.2 and GPIOA.3 respectively.

4.3 End of Conversion (EOC)

The EOC signal is active low once for each channel *pair* converted. The ADS8364, as depicted in the application note, provides three EOC pulses to the eZdsp F2812. Each pulse represents the completion of a conversion from the active channel. When all three hold pins of the ADC are brought low at the same time, all three channels (A, B and C) are considered active, and are converted simultaneously. The EOC signal is routed to EXT_INT1 on the eZdsp F2812, located at pin 5 on the I/O connector P8. The following figure shows the signal flow for a complete conversion / read cycle.

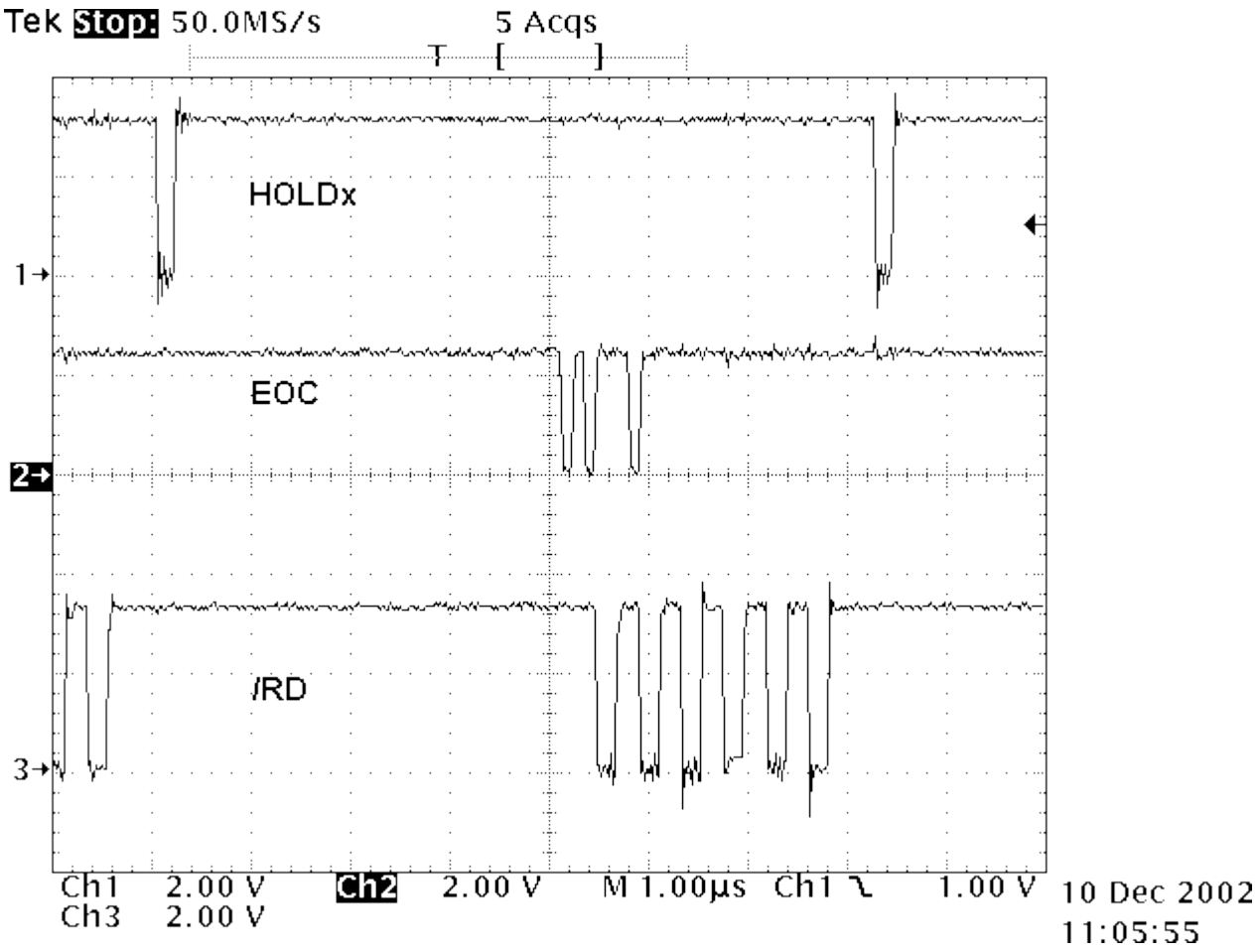

Figure 2. ADS8364 Waveforms

References

1. ADS8364, 6 Channel, Simultaneous Sampling Parallel ADC, data sheet, (SBAS219)
2. TMS320F2812 data sheet (SPRS088)
3. TMS320C28x™ DSP CPU and Instruction Set, reference guide (SPRU430)
4. TMS320F28x™ DSP Peripherals, reference guide (SPRU566)

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