Application Report
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Building a Stable DAC External Reference Circuit

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ABSTRACT

This application report is written to help design engineers implement a stable DAC external reference circuit for TI's digital-to-analog converters (DACs) that do not have an internal reference. This report points out the critical aspects and the importance of a reference buffer driver.

Introduction

The performance of a digital-to-analog converter depends on various design practices, most of which are construed to be second nature to electronic designers. But, in reality, there are more subtle areas in DAC design to be considered to get good performance from a DAC, depending on the application requirement. This report focuses on one key specific area, which is the external reference circuit design. Providing a stable reference source is one of the biggest contributing factors in the successful performance of a DAC. Because of its simple concept, the DAC reference circuit can be misunderstood, overlooked, or assumed to work just fine. Normally this is not a big problem for TI DACs with a built-in reference source, because its complexities are already taken into consideration and the solutions are already implemented internal to the DAC. This is assuming that the internal reference fits the requirement of the system application. Unfortunately, not all digital-to-analog converters include a built-in reference circuit, mainly due to restrictions in layout design and, in some cases, because the internal reference is just not practical for the intended DAC application, where an external source of reference is better suited for the application.

For DACs that require an external source of voltage reference, careful considerations should be taken in selecting the external source of voltage. The source should at least be clean and stable because it serves as the DAC's reference point. TI's general purpose DACs are meticulously planned and any impending problems attributable by internal factors are carefully taken into design consideration. The force and sense concept is implemented to take care of these foreseeable errors pertaining to the reference circuit of the DAC.

The Force and Sense Circuit

The basic concept of the force and sense circuit is to provide a reference driver that assures the DAC a stable voltage by sensing the IR drop caused by the fixed internal resistance (due primarily to copper, metal and pin) and the code dependent current. Since the reference current is code dependent, it varies through the span of the code, therefore, the IR drop becomes hard to track since the voltage is now varying constantly as the code is changed.

Simply said, the digital input code of the DAC dictates the amount of current that has to be supplied into the $V_{REF}H$ input pin and out of $V_{REF}L$ pin. This can vary from a few microamps to approximately 2 mA, which makes the reference input appear as a varying load to the reference.

The Solution

Because the IR drop is not a fixed voltage, it cannot be easily compensated by building a simple passive circuit. As a solution, the reference sense pin is used to provide a feedback path to the outside such that the IR drop can be tracked and compensated accurately by using a buffer. The op-amp is provided primarily to maintain a stable voltage for the reference and minimize errors caused by the varying currents. The op-amp basically detects the voltage drop across the internal wiring resistance of the DAC reference input through the feedback sense pin. In essence, the op-amp adjusts for the IR drop in V_{REF} force input line of the DAC. This process maintains a firmly established voltage seen by the DACs reference circuit at all times. This configuration now yields the best linearity performance of the DAC.

An example reference driving circuit is shown in Figure 1 below for a dual ±10-V reference circuit used with the TI DAC7744. The DAC7744 pinout provides reference force and sense pins so that the externally applied reference voltage is applied correctly internal to the DAC7744. To better understand, consider the internal wiring metal resistance of the DAC reference inputs as shown by R_{W1}, R_{W2}, R_{W3}, and R_{W4}. Since the DAC reference input currents can vary from a few microamps to approximately 2 mA depending on the DAC code (see Fig. 7 and 8), internal IR drops are generated across R_{W2} and R_{W3}. These internal DAC IR drops, if left uncompensated, can cause undesirable linearity errors (see Fig. 3 and 4). By using the reference buffer configuration shown, the output voltage of each op-amp buffer is self-adjusted for each DAC code to ensure that the internal DAC reference sense point maintains the external buffered reference voltage.

The addition of the 100-Ω resistor and 1000-pF capacitor to each op-amp buffer configuration acts as both a decoupling circuit and also provides noise reduction for the external reference. The 2200-pF capacitor provides a low impedance path at high frequencies to close the op-amp loop providing stable compensation.

This configuration can also be applied for ±5-V reference application.

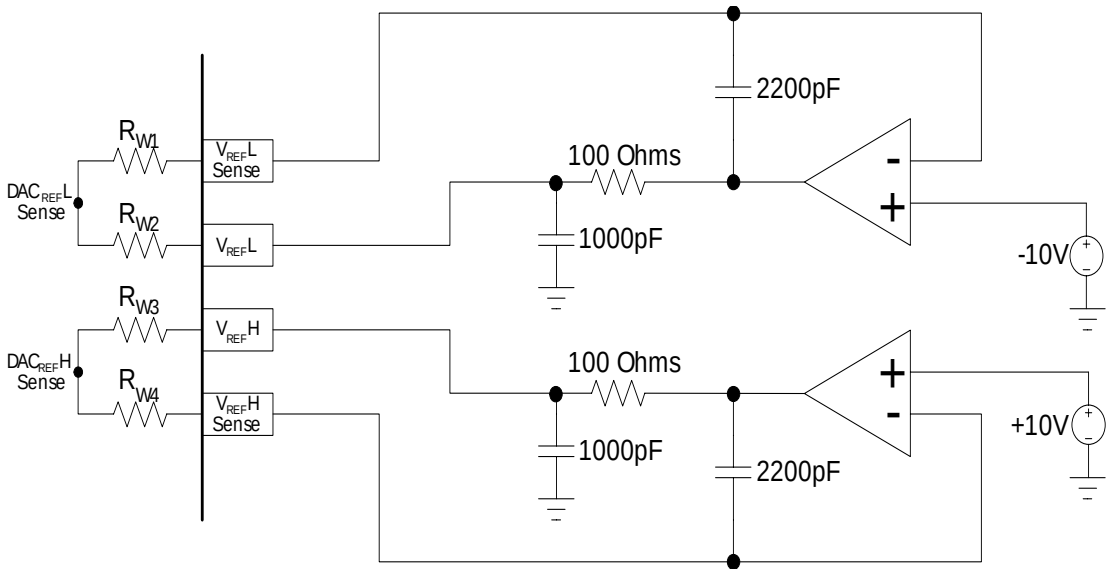

Figure 1. Dual Supply ±10-V Buffered Configuration

Another example circuit is shown in Figure 2 below for a single supply reference circuit. This configuration can also be applied for +5-V reference applications with the exception that the 99.5-KΩ resistor must be replaced with a 99-KΩ resistor and the 500-Ω resistor with a 1-KΩ resistor.

Both the OPA350 and OPA227 operate in single supply operation. The 50-Ω resistor connected from the $V_{REF}L$ pin to GND acts as a *helper resistor* providing a constant 1-mA sink current on the $V_{REF}L$ pin. This assists the OPA350 to sink the varying $V_{REF}L$ currents out of the DAC.

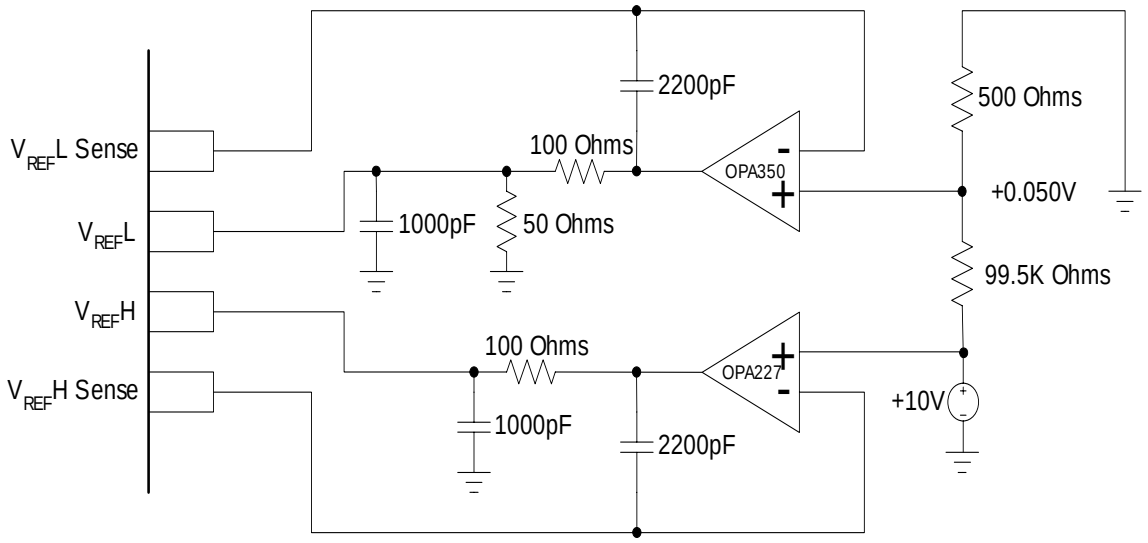

Figure 2. Single Supply 10-V Buffered Configuration

Performance Result (No-Buffer-Configuration)

The graphs showed in Figures 3 and 4 displays the linearity error as the result of a laboratory test of the no-buffer-configuration for the DAC7734. As shown, the linearity performance for DNL and INL are greatly degraded due to the improper use of the force and sense reference input of the DAC.

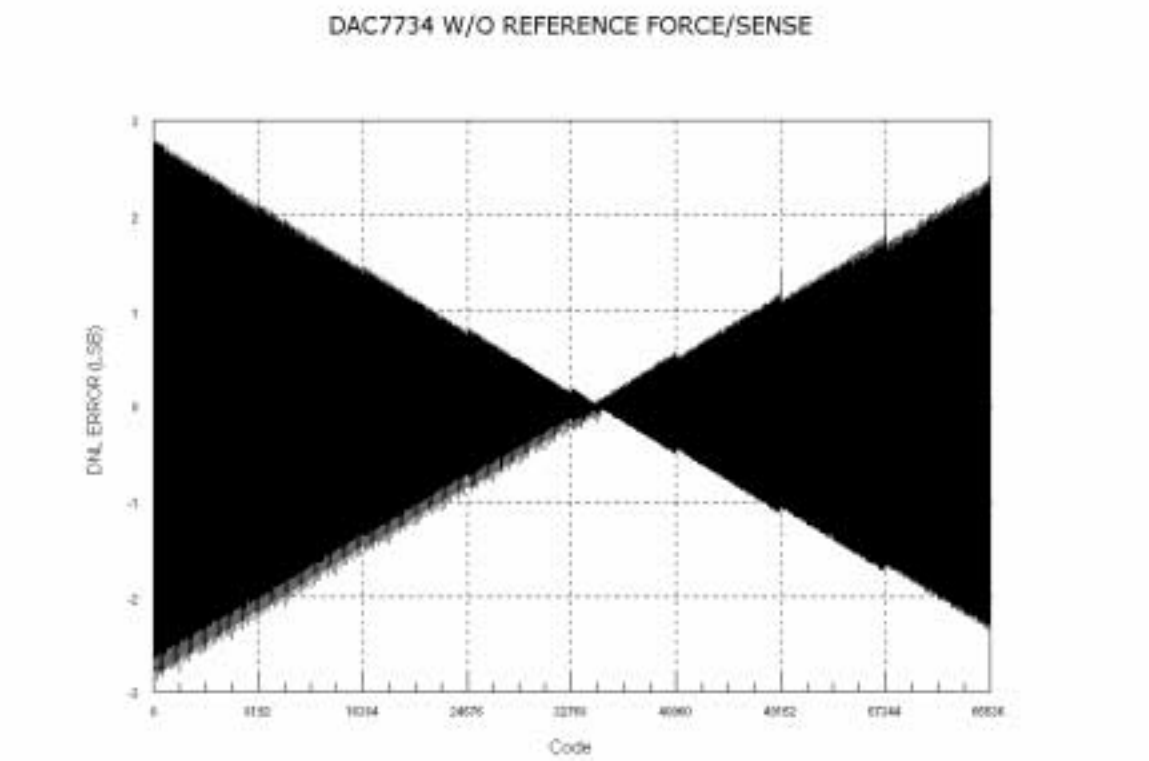

Figure 3. DAC7734 DNL Error

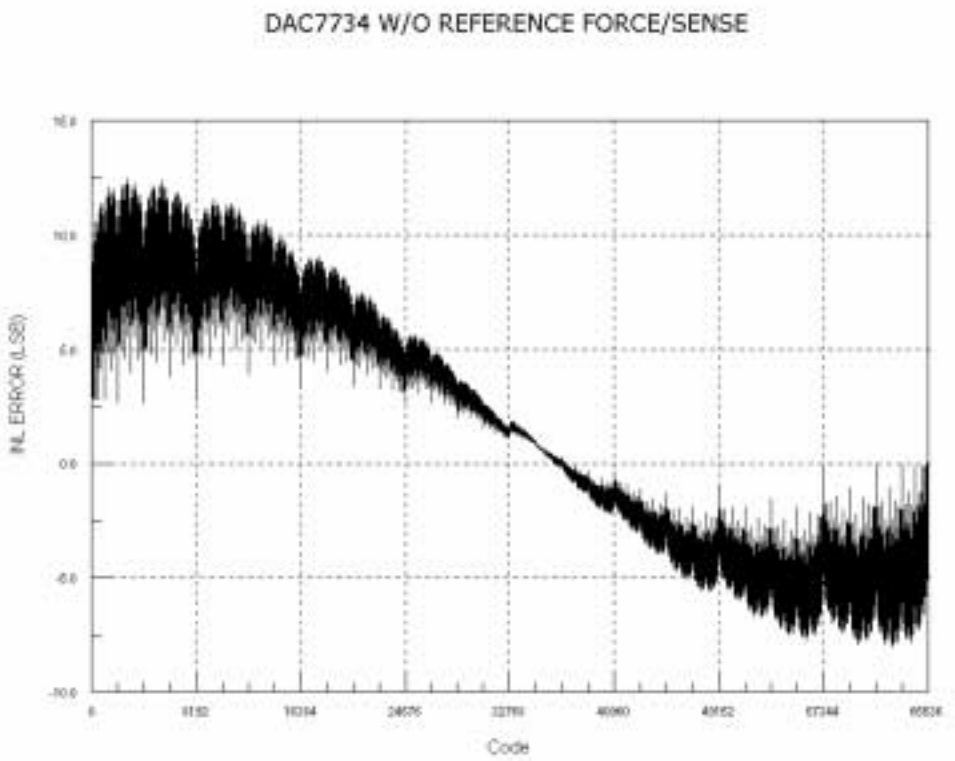

Figure 4. DAC7734 INL Error

The Reference Buffer Configuration

The most important detail to note is that the reference force/sense buffers should be used in a noninverting configuration such that no current flows in the reference sense input internal wiring resistances R_{W1} and R_{W4} as shown in the diagram of Figure 1.

The force and sense buffer configuration should be just a simple voltage follower and should not be intended for any other combination op-amp function, such as combining a gain amplifier circuit with it, as shown in Figure 5 below. Adding the feedback resistor, Rf, into the circuit introduces the current into the reference sense pin, which is undesirable. The current can cause the part to act differently in ways that affect the overall performance of the DAC.

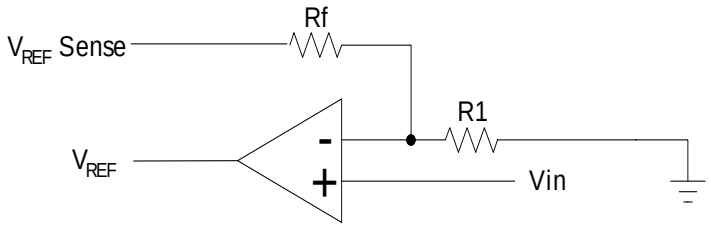

Figure 5. Rf Introduces Undesirable Current into the Reference Sense Pin

The ideal way to implement such function is to separate the gain amplifier from the voltage follower circuit, as shown in Figure 6 below, so that the DAC performance is not affected.

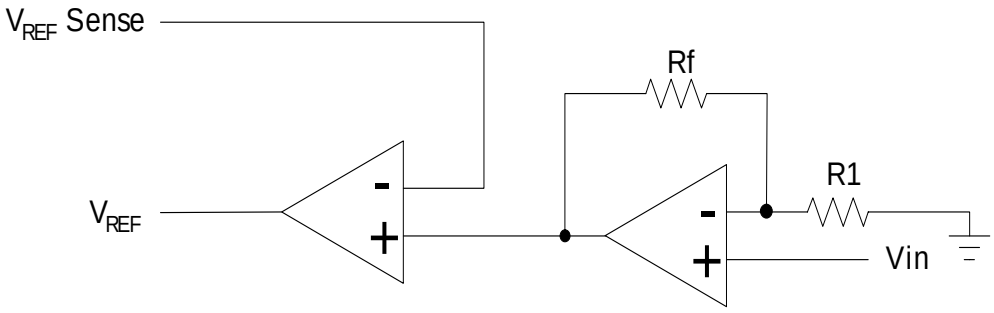

Figure 6. Correct Configuration

The Reference Current

The graphs in Figures 7 and 8 below are provided to show the relationship between the reference input current and the digital code for dual supply application.

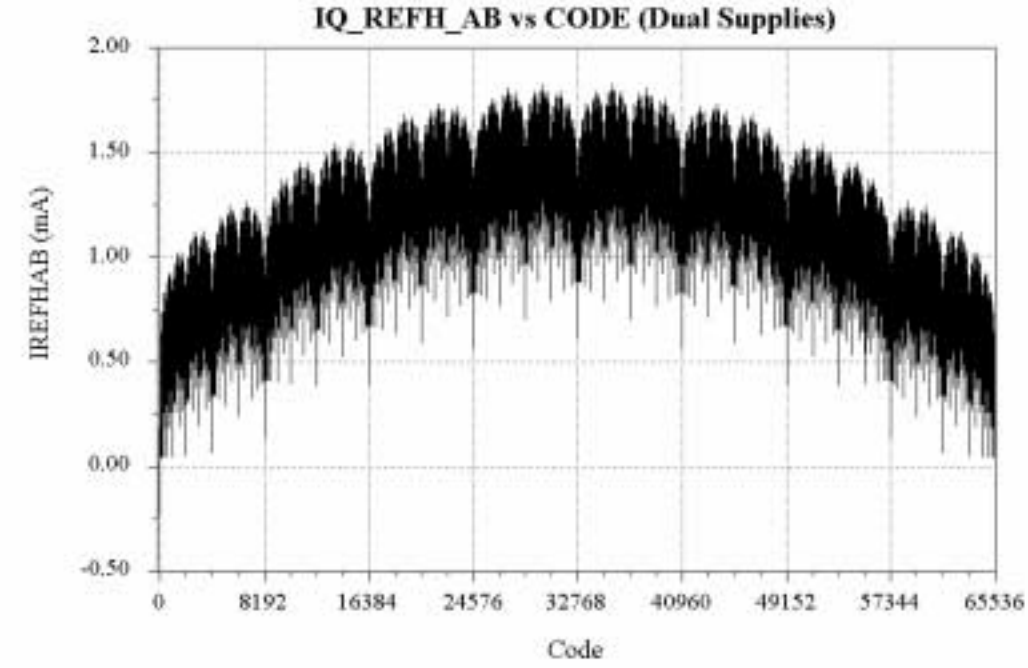

Figure 7. $I_{REF}H$ versus Code

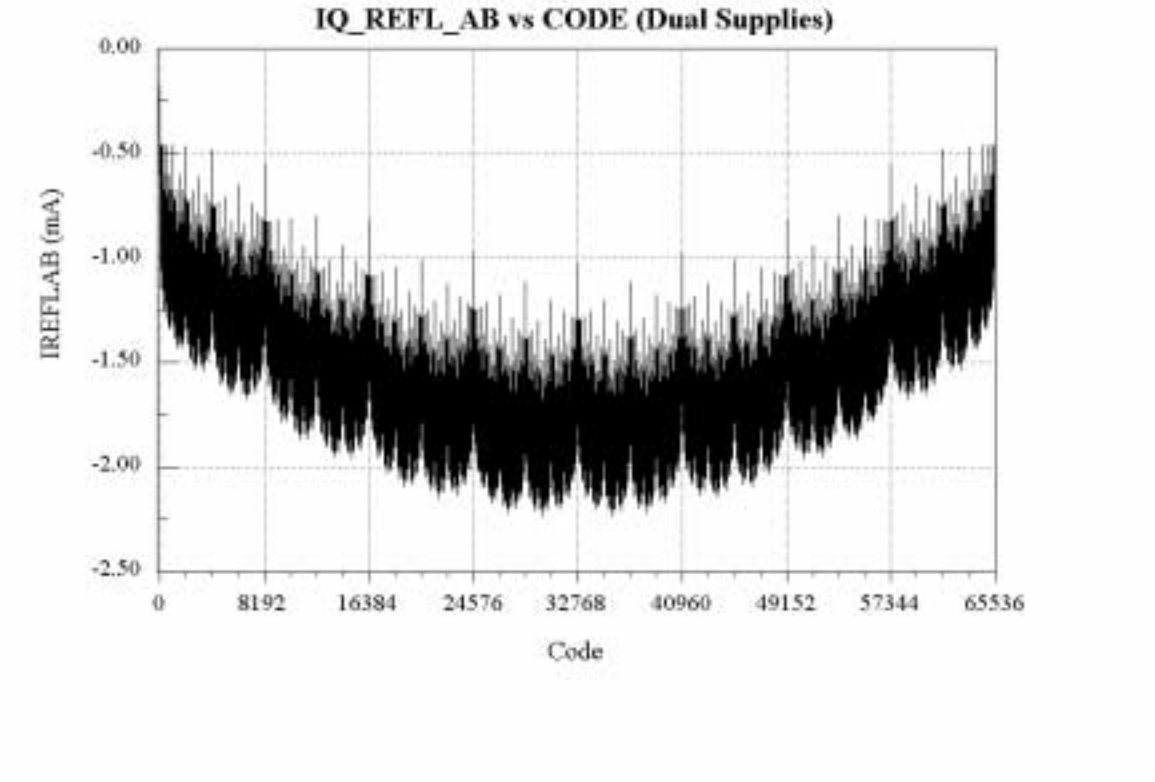

Figure 8. $I_{REF}L$ versus Code

Conclusion

In summary, the reference buffer is an essential component in establishing a stable voltage for reference if the linearity performance of the DAC is considered to be a fundamental part of the design. Without the reference buffer, the DACs performance is greatly degraded as shown in Figures 3 and 4. The degradation in performance of the DAC is mainly due to the effect of the changing reference current (shown in Figures 7and 8) as it acts with the DACs internal impedance and is left uncompensated.

References

1. *DAC7744 Datasheet, 16-Bit Quad Voltage Output DAC* (SBAS120)
2. *DAC7734 Datasheet, 16-Bit Quad Voltage Output, Serial Input DAC* (SBAS138)
3. *OPA350 Datasheet, High-Speed, Single Supply, Rail-to-Rail Op-Amp* (SBOS099A)
4. *OPA227 Datasheet, High Precision, Low Noise Op-Amp* (SBOS110)

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