

Programming Audio Power Up/Down on TSC210x and TLV320AIC26/28

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ABSTRACT

This application report presents some general and practical programming sequences for the audio power up/down of Texas Instruments TSC2100/TSC2102/TLV320AIC26 and TSC2101/TLV320AIC28 devices, so as to avoid a possible malfunction or errors during and after power up or down.

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1 Introduction

TI's touch screen controller (TSC) devices, such as TSC2100, TSC2101, or TSC2102, have a stereo audio CODEC built in. The stereo CODEC device TLV320AIC26 (or simply called AIC26) shares the same core with the TSC2100 CODEC function; the TLV320AIC28 (AIC28) shares the same core with TSC2101 also. This application report focuses on the powering up/down for the audio CODEC only. The details of these TSC/CODEC integrated or CODEC-only devices can be found, respectively, in [1] and [5] of the Reference Section.

In many mobile and handheld applications, the on-chip audio drivers, the internal ADC/DAC converters, the internal PLL, and even the external clocks (such as MCLK) may be required to power up and down frequently in order to reduce power consumption as much as possible. The aforementioned TI CODEC devices have high configurability and power-control flexibility. On the CODEC circuitry, the input amplifiers, output amplifiers and drivers, the virtual ground, the audio ADC and DAC converters, the PLL, and so on, can be powered up and down individually by software. Additionally, a hardware power-down pin exists for further power consumption reduction. Moreover, the external clock to the CODEC (such as the MCLK) and/or one or more power supplies to the CODEC also can be turned off when not being used.

In the TSC2100, TSC2101, TSC2102, AIC26, or AIC28 device, the power up/down sequences and orders are often important or critical for the internal state machines of the device to understand and work properly. The power DOWN sequences of the audio ADC, audio DAC, or the main clock MCLK are especially important, as an improper sequence of the ADC, DAC, or MCLK power down can cause device malfunctions and operation errors.

2 Outline of Power-Up/Down Sequences

These TI CODEC devices are mainly powered up or down in two ways: by hardware or software-controlled hardware and by software only. Usually, hardware power down may save more power; however, powering down by software has more flexibility and makes powering back up easier and faster. Also, before any hardware power down, the proper software power down is usually needed and should be implemented first.

The power-up and -down sequences for TSC2100, TSC2101, TSC2102, AIC26, or AIC28 are outlined in the following sections. Not all steps are required if the corresponding circuits were not used and never powered up.

2.1 Power-Up Sequence

1. **Power up all power supply pins of the CODEC device.** These CODEC devices generally have four types of power supply pins: the digital core power supply pin, the digital I/O power supply pin, the analog power supply pin(s), and the analog output driving power supply pin(s). It is OK to power up all pins simultaneously. If controllable, the suggested hardware power-up sequence can be:
 - a. Digital core
 - b. Digital I/O
 - c. Analog
 - d. Analog drivers
2. **Release hardware power down** to power up the CODEC, and implement a hardware reset ($\overline{\text{RESET}}$).
3. **Set up, generate, and enable MCLK.** The MCLK is the master clock to the CODEC, which must be present while the CODEC is operating. The MCLK is always an input to the CODEC device from the processor or any other synchronized clock resource.
4. **CODEC's power-up initialization and the PLL setup.** Enable the processor-CODEC control interface and initialize the CODEC's on-chip registers by software. During the initialization, the PLL can be set up and enabled, if needed. Also note : DO NOT power up or unmute any CODEC ADC, DAC, PGAs (programmable gain amplifier) , or drivers during the initialization.
5. **Set up audio input circuitry, if needed;** the normal sequence within this step is:
 - a. Power up the used audio input PGA.
 - b. Power up ADC.
 - c. Unmute audio input PGA.
6. **Set up audio output circuitry, if used;** the normal sequence within this step is:
 - a. Power up DAC (and DAC PGAs).
 - b. Power up the used output driver.
 - c. Unmute audio DAC left and right PGAs.

The preceding Steps 1 to 3 are usually the *hardware or software-controlled hardware* power-up steps; Steps 4 to 6 are the *software only* power-up implementations.

2.2 Power-Down Sequence

1. **Power down audio output.** Specifically:
 - a. Mute audio DAC left and right PGAs.
 - b. Power down output driver/amplifiers, if powered up.
 - c. Check DAC left and right PGA soft-stepping flags.
 - d. If both soft-stepping flags have completed and the flags have been set, power down both DACs; if not, return to Step 1c.
2. **Power down audio input;** the sequence is:
 - a. Mute audio input PGA.
 - b. Power down input PGAs, if powered up.
 - c. Check the soft-stepping flag of the PGA connected to the audio ADC.
 - d. If the soft stepping has completed and the corresponding flag has been set, power down the ADC; if not, return to Step 2c.
3. **Disable PLL.** If PLL is used and/or the PLL settings need to be changed, disable the PLL at this step.

4. **Disable MCLK.** If MCLK needs to be powered or turned down:
 - a. Check the CODEC's ADC and DAC power-down flags.
 - b. If both ADC and DAC have actually powered down and the power-down flags had been set, then power down or disable the MCLK; if not, return to Step 4a.
5. **Activate or enable the hardware power down.**
6. **And/or turn off all power supplies to the CODEC.**

Steps 1 to 3 comprise a *software* power-down sequence, and Steps 4 to 6 comprise a *hardware* or *software-controlled hardware* power-down sequence.

Note that the proper sequence or order is requested and is important especially at power down. Experience has shown that with an improper power-down sequence, not only may there be louder noise or clicks, but also certain malfunctions of the CODEC may show up, such as some of the CODEC registers may be reset and/or cannot be written to. Therefore, closely following the preceding power-down sequence is recommended .

3 TSC2100/TSC2102/AIC26 CODEC Power Up/Down

This section provides an example showing more details on the power up and down of the TSC2100, TSC2102, and AIC26. Because these three devices share the same core and have almost the same internal registers on memory page 2, their power up/down program or sequence can be the same, as the following procedural steps show.

3.1 To Power Up

1. **Power up all power-supply pins of the CODEC device.** If applicable, the suggested hardware power up order is:
 - a. Digital core: DVDD
 - b. Digital I/O: IOVDD
 - c. Analog: AVDD
 - d. Analog drivers: DRVDD
2. **Release or disable hardware power down;** that is, put the $\overline{\text{PWD}}$ pin to logic HIGH (and also issue a hardware-reset signal to the RESET pin).
3. **Set up, generate, and enable MCLK** to the CODEC.
4. **CODEC power-up software initialization and set up/enable the PLL, if used.**
 - a. Set up all audio registers (but power down and mute all audio) as desired, including the PLL registers (Reg1BH/Page2 and Reg1CH/Page2).
 - b. If the PLL is to be used, enable the PLL as:

$$\text{D15/Reg1BH/Page2} = 1$$
5. **Set up CODEC and input circuitry, if needed.**
 - a. Power up CODEC and sidetone:

$$\text{D15/Reg05H/Page2} = 0$$

$$\text{D13/Reg05H/Page2} = 0$$
 - b. Power up ADC:

$$\text{D9/Reg05H/Page2} = 0$$
 - c. Unmute ADC:

$$\text{D15/Reg01H/Page2} = 0$$
6. **Set up audio-out circuitry, if needed.**
 - a. Power up VGND, if at capacitorless (capless) mode; otherwise, power down VGND:

$$\text{D8/Reg05H/Page2} = 0 \text{ if at capless mode or}$$

$$\text{D8/Reg05H/Page2} = 1 \text{ if at capacitor (cap)-coupled mode}$$
 - b. Power up DAC:

$$\text{D10/Reg05H/Page2} = 0$$
 - c. Power up audio output driver:

$$\text{D12/Reg05H/Page2} = 1, \text{ if at high-power mode}$$
 - d. Unmute left and right audio DAC:

D15/Reg02H/Page2 = 0

D7/Reg02H/Page2 = 0

3.2 To Power Down

1. **Software power down DAC channels;** the sequence is:
 - a. Mute both audio DAC channels:
 - D15/Reg02H/Page2 = 1
 - D7/Reg02H/Page2 = 1
 - b. Power down output amplifiers (PGA), if powered up:
 - D12/Reg05H/Page2 = 0
 - c. Check DAC soft-stepping flag, and see if:
 - D3/Reg05H/Page2 = 1 and
 - D2/Reg05H/Page2 = 1
 - d. If true, power down DAC, i.e., set
 - D10/Reg05H/Page2 = 1
Otherwise, return to Step 1c.
2. **Software power down ADC channels;** the sequence is:
 - a. Mute audio ADC:
 - D15/Reg01H/Page2 = 1
 - b. Power down CODEC and sidetone, if powered up:
 - D15/Reg05H/Page2 = 1
 - D13/Reg05H/Page2 = 1
 - c. Check ADC soft-stepping flag to see if:
 - D0/Reg05H/Page2 = 1
 - d. If true, power down ADC, and set
 - D9/Reg05H/Page2 = 1
Otherwise, return to Step 2c.
3. **Disable PLL,** if needed, that is, set
 - a. D15/Reg1BH/Page2 = 0
4. **Disable MCLK,** if needed:
 - a. Check if :
 - D7/Reg05H/Page2 = 1 and
 - D6/Reg05H/Page2 = 1
 - b. If yes, then power down or disable the MCLK.
 - Otherwise, return to Step 4a.
5. **Enable the hardware power down;** put $\overline{\text{PWD}}$ pin to LOW.
6. **And/or turn off all power supplies to the CODEC.**

4 TSC2101/AIC28 CODEC Power Up/Down

This section provides another example showing the power up/down details of the TSC2101 and AIC28; these two devices share the same core and have the same internal audio registers.

4.1 To Power Up

1. **Power up all power-supply pins of the CODEC device.** If applicable, the suggested hardware power up sequence is:
 - Digital core: DVDD
 - Digital I/O: IOVDD
 - Analog: AVDD1, AVDD2
 - Analog drivers: DRVDD, BVDD
2. **Release hardware power down**, that is, put the `PWD_DN` pin to logic HIGH (and issue a hardware-reset signal to the `RESET` pin).
3. **Set up, generate, and enable MCLK.**
4. **CODEC power up software initialization, and set up/enable the PLL, if used.** (The same as Step 4 in the previous section for TSC2100/TSC2102/AIC26.)
5. **Set up CODEC and input circuitry, if needed**
 - a. Power up the used audio input PGA:
 - D15/Reg05H/Page2 = 0 — if using headset MIC_IN
 - D14/Reg05H/Page2 = 0 — if using headset MIC_IN
 - D13/Reg05H/Page2 = 0 — if using sidetone
 - D15/Reg1FH/Page2 = 0 — if using CELL_IN or
 - D6/Reg1FH/Page2 = 0 — if using BUZZ_IN
 (Note that headset, handset, and cell_in cannot be fed to the ADC simultaneously because there is only one audio ADC. See relevant data sheets for details.)
 - b. Power up ADC:
 - D9/Reg05H/Page2 = 0
 - c. Unmute the used ADC PGA(s)
 - D15/Reg01H/Page2 = 0 — if using headset MIC_IN or
 - D15/Reg1EH/Page2 = 0 — if using headset MIC_IN
 - D15/Reg03H/Page2 = 0 — if using sidetone
6. **Set up audio-out circuitry, if needed:**
 - a. Power up VGND, if at capless mode; otherwise, power down VGND:
 - D8/Reg05H/Page2 = 0 — if at capless mode, or
 - D8/Reg05H/Page2 = 1 — if at cap-coupled mode
 - b. Power up DACs:
 - D10/Reg05H/Page2 = 0
 - c. Power up audio output driver:
 - D12/Reg05H/Page2 = 1 — if using SPK1
 - D11/Reg05H/Page2 = 1 — if using SPK2
 - D6/Reg05H/Page2 = 1 — if using OUT32N (receiver driver) or
 - D7/Reg05H/Page2 = 1 — if using CP_OUT
 (Note that the headset drivers, SPK1 and SPK2, and the receiver driver, OUT32P/OUT32N, CANNOT be turned ON simultaneously. See relevant data sheet for details.)
 - d. Unmute output driver(s):
 - D2/Reg20H/Page2 = 0 — if using SPK1
 - D1/Reg20H/Page2 = 0 — if using SPK2
 - D7/Reg21H/Page2 = 0 — if using LoudSPK or
 - D6/Reg21H/Page2 = 0 — if using CP_OUT
 - e. Unmute left and right audio DAC:
 - D15/Reg02H/Page2 = 0
 - D7/Reg02H/Page2 = 0

4.2 To Power Down

1. **Power down audio-out circuitry, if powered up;** the sequence is:
 - a. Mute both left and right audio DAC channels:
 - D15/Reg02H/Page2 = 1
 - D7/Reg02H/Page2 = 1
 - b. Mute output driver(s):
 - D2/Reg20H/Page2 = 1 — to mute SPK1
 - D1/Reg20H/Page2 = 1 — to mute SPK2
 - D7/Reg21H/Page2 = 1 — to mute LoudSPK or
 - D6/Reg21H/Page2 = 1 — to mute CP_OUT
 - c. Power down output driver(s), if powered up:
 - D12/Reg05H/Page2 = 1 — to power down SPK1
 - D11/Reg05H/Page2 = 1 — to power down SPK2
 - D6/Reg05H/Page2 = 1 — to power down OUT32N (receiver driver) or
 - D7/Reg05H/Page2 = 1 — to power down CP_OUT
 - d. Check DAC PGAs soft-stepping flags and make sure:
 - D3/Reg04H/Page2 = 1 and
 - D2/Reg04H/Page2 = 1
 - e. Wait for Step 1d to become true; then, power down DACs:
 - D10/Reg05H/Page2 = 1
2. **Software power down ADC, if powered up;** the sequence is:
 - a. Mute the used audio ADC PGA:
 - D15/Reg01H/Page2 = 1 — to power down headset MIC input
 - D15/Reg1EH/Page2 = 1 — to power down handset MIC input
 - D15/Reg03H/Page2 = 1 — to power down sidetone input
 - b. Check the soft-stepping flag and make sure that:
 - D0/Reg04H/Page2 = 1 — if headset/handset to ADC; or
 - D7/Reg1FH/Page2 = 1 — if Cell_IN to ADC
 - c. Wait until Step 2b becomes true, and then power down ADC, that is:
 - D9/Reg05H/Page2 = 1
 - d. Power down whichever input PGA is powered up:
 - D15/Reg05H/Page2 = 1 — to power down headset MIC In
 - D14/Reg05H/Page2 = 1 — to power down MIC In
 - D13/Reg05H/Page2 = 1 — to power down sidetone
 - D15/Reg1FH/Page2 = 1 — to power down Cell_IN or
 - D6/Reg1FH/Page2 = 1 — to power down BUZZ_IN
3. **Disable PLL,** if needed by setting:
 - D15/Reg1BH/Page2=0
4. **Disable MCLK,** if needed; the sequence must be:
 - a. Check if:
 - D5/Reg05H/Page2 = 1
 - D4/Reg05H/Page2 = 1 and
 - D3/Reg05H/Page2 = 1
 - b. If yes: then power down or disable the MCLK;
 - Otherwise, return to Step 4a
5. **Active the hardware power down:** put $\overline{\text{PWD_DN}}$ pin to LOW.
6. **Turn off all power supplies to the CODEC.**

5 Conclusion

The programming examples for power up/down of TSC2100, TSC2101, TSC2102, AIC26, and AIC28, discussed in this application report offer practical and important tips for using these devices. The most critical steps are to check the soft-stepping flags before powering off the audio ADC/DAC and to check the power-down flags before disabling MCLK.

6 References

1. *TSC2100, Programmable Touch Screen Controller with Integrated Stereo Audio CODEC and Headphone/Speaker Amplifier* data sheet ([SLAS378](#))
2. *TSC2101, Audio CODEC with Integrated Headphone, Speaker Amplifier and Touch Screen Controller* data sheet ([SLAS392](#))
3. *TSC2102, Programmable Touch Screen Controller with Integrated Stereo Audio DAC and Headphone Amplifier* data sheet ([SLAS379](#))
4. *TLV320AIC26, Low Power Stereo Audio CODEC with Headphone/Speaker Amplifier and 12-Bit Battery/Temperature/Auxiliary ADC* data sheet ([SLAS412](#))
5. *TLV320AIC28, Stereo Audio CODEC with Integrated Headphone and Speaker Amplifiers* data sheet ([SLAS418](#))

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