Application Report
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Synchronizing WiMAX Synthesizer TRF1x21/TRF1x12 to Arbitrary Reference

Russell Hoppenstein *High Speed - Wireless Infrastructure*

ABSTRACT

Texas Instruments has a WiMAX RF chipset for base station and CPE applications that include integrated synthesizers to realize the superheterodyne architecture. For optimum channel resolution, these devices must be tied to an 18-MHz reference frequency. In some systems, the synthesizer reference frequency needs to be synchronized to a system reference frequency that may not be an integral multiple of 18 MHz. This application report presents the circuitry required to synchronize the 18-MHz reference to an arbitrary system reference clock and illustrates that negligible degradation occurs in the RF performance of the radio.

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1 Introduction

Texas Instruments offers the TRF1xxx RF chipsets as part of the WiMAX solution for CPE (customer premise equipment) and base station (BTS) equipment. The block diagram for the complete base station application is shown in Figure 1. The circuitry requires clocking for the digital components related to the digital up/down converters, data converters, and SerDes (SERializers and DESerializers) device. In addition, the integrated synthesizers in the TRF1x21 and TRF1x12 device require a reference frequency.

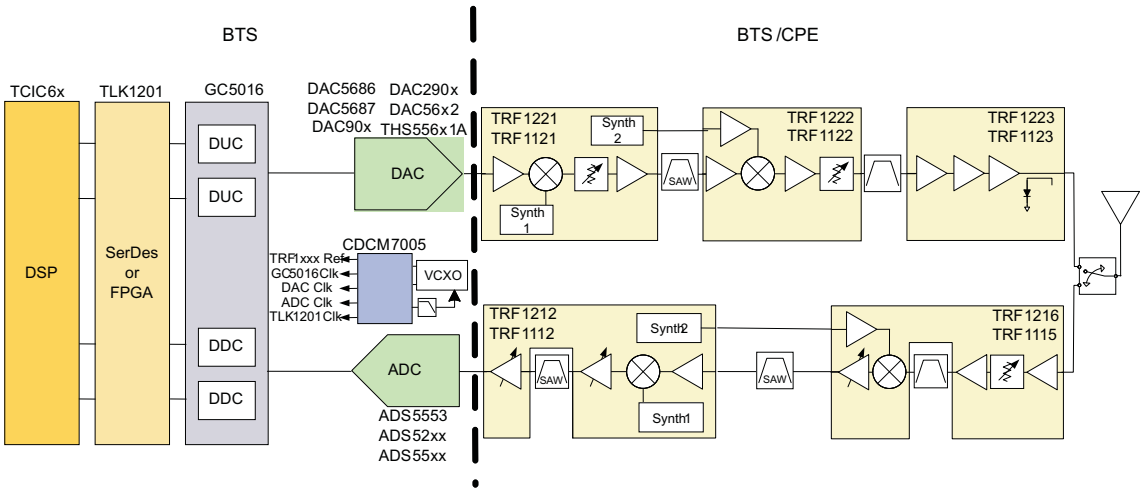

Figure 1. Block Diagram of WiMAX CPE and BTS Using TRF1xxx Chipset

The reference frequency of the TRF1xxx device sets the resolution of the frequency synthesizers. Although the devices can accept a reference frequency from about 10 MHz to 50 MHz, it is desirable to keep the reference frequency at 18 MHz. An 18-MHz reference corresponds to frequency resolution of the S-band VCO (voltage controlled oscillator) of 1 MHz and 62.5 kHz for the UHF VCO (50 kHz for the TRF1121). Altering the reference frequency adjusts the resolution steps of the S-band synthesizer according to:

$$\Delta f = \frac{f_{Ref}}{18} \times \Delta f_i \quad (1)$$

Where:

f_{Ref} = Frequency reference in MHz
Δf_I = 1 MHz (S-band VCO)
Δf_I = 62.5 kHz (UHF-band VCO of TRF12xx)
Δf_I = 50 kHz (UHF-band VCO of TRF11xx)

Deviating from the standard 18 MHz results in fractional step changes in the synthesizer. This does not allow the system to tune the output signal to the desired and pre-defined channel. As such, keeping an 18-MHz reference is required.

The entire system is synchronized to a system reference frequency. This reference frequency is likely generated from a highly stable crystal oscillator and feeds multiple boards in the system The system reference frequency choice is considered fixed and cannot be changed by the designers. It is unlikely that the available reference frequency will be a multiple of 18 MHz suitable for the TRF1xxx devices. Additional components are required to provide the appropriate 18-MHz reference and care must be taken to complete this task with minimal additional components and cost.

2 System Clock Using the CDCM7005

The CDCM7005 is a high-performance, low-jitter differential clock driver and clock distribution chip. The device synchronizes the system reference frequency with a high-performance voltage controlled crystal oscillator (VCXO). Whereas the reference frequency is usually low, around 10-to-20 MHz, the VCXO is generally much higher, around 500 MHz, in order to suitably sample the high-speed data converters. The CDCM7005 has five differential PECL outputs or 10 single-ended CMOS outputs. Each of the five output pairs can be independently divided down by 1, 2, 3, 4, 6, 8, and 16.

One of the outputs of the CDCM7005 can be used to provide the reference frequency to the TRF1xxx devices. In order to keep that reference frequency at 18 MHz, the VCXO used with the CDCM7005 needs to be an integral multiple (i.e., 1, 2, 3, 4, 6, or 8) of 18 MHz so that the dividers could be used appropriately.

The clock distribution chip is a requirement on BTS systems because the clocking devices all need to be synchronized together, yet need to be clocked at different multiples of each other. For example, the DAC may need to be clocked at 448 MHz whereas the ADC is clocked at 112 MHz. These frequencies are multiples of each other and could be realized with a CDCM7005 device paired with a 448-MHz VCXO. With the CDCM7005 and such a VCXO, a variety of output clocks can be derived for the system requirements.

3 Single PLL Loop Reference

One of the divided outputs of the CDCM7005 is suitable for the reference frequency of the TRF1xxx devices' synthesizers; however, it is likely that the VCXO choice for the other system components will not be an integral multiple of the 18-MHz frequency required. In the foregoing example , the 448-MHz VCXO frequency cannot be divided down to exactly 18 MHz, given the divider values available. Additional circuitry is required to provide the 18-MHz reference that is synchronized to the system clock.

It is possible to introduce a second CDCM7005 coupled with an 18-MHz VCXO to solve this problem; however, the CDCM7005 device would be a significant overkill for this application and would not be a cost-effective solution. Instead, the solution is to introduce a single PLL loop with an additional VCXO at 18 MHz.

A block diagram of the solution using the TRF3750 PLL device coupled with an 18-MHz VCXO is shown in Figure 2. The reference for the TRF3750 can come directly from the system reference if it is clean enough. Better yet, the reference can come from one of the divided-down outputs from the CDCM7005 because it is ensured to be clean. For the minimal extra cost of the TRF3750 and the 18-MHz VCXO, the exact reference frequency can be provided.

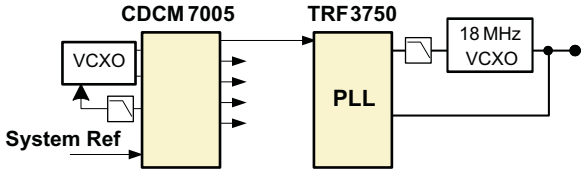

Figure 2. Block Diagram of the TRF3750 Solution

4 PLL Loop Filter

The PLL operates at a low frequency and presumably with a low-frequency reference. The PFD (phase frequency detector) frequency needs to be set to a relatively low value to keep the divider registers within range. For an 18-MHz oscillator and a 10-MHz reference, the PFD frequency is set to 100 kHz. Other parameters related to the oscillator gain (Kv) and charge pump current (Ip) may be different for a crystal oscillator compared to a traditional VCO.

The lower PFD frequency and different oscillator parameters require a change in the loop filter. The loop filter should be designed to provide sufficient attenuation of the PFD spurs and sufficient phase margin in the loop to ensure stability. The CDC7005 PLL Calculator program located at http://www.ti.com/litv/zip/scac059a offers a user-friendly interface to view the open-loop and closed-loop frequency response of the synthesizer for given loop filter values. The recommended loop filter for this application is shown in Figure 3.

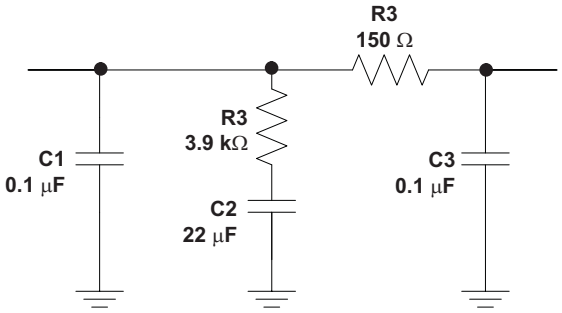

Figure 3. Recommended Loop Filter

5 Phase Noise Performance

The phase noise performance of the S-band synthesizer of the TRF1221 device is measured using a TCXO (temperature-controlled crystal oscillator) as the reference frequency. This is considered the baseline case. Next, the phase noise of the same synthesizer is measured using the TRF3750 coupled with an 18-MHz VCXO as the reference. The system reference frequency for the TRF3750 is arbitrarily chosen to be 10 MHz. The oscillator products used in these experiments follow:

10 MHz TCXO	Vectron	T1115-OSC3B0-10MHz
18 MHz TCXO	Vectron	VVC1-A1D-18M000
18 MHz VCXO	Vectron	VTC1-A0CE-18M00

The phase noise plot comparison is shown in Figure 4.

Figure 4. Phase Noise Comparison With TCXO vs TRF3750 and VCXO as Reference

6 Conclusion

The phase noise plots show that there is negligible difference between the performance using a standard TCXO as the reference versus using the TRF3750 coupled with an 18-MHz VCXO as the reference. The available system reference frequency can be used directly with the TRF3750. If available, it is more desirable to use one of the divided-down outputs from the CDC7005 clock distribution chip as it is certain

to have low jitter. Note that the reference signal for the TRF1xxx devices is TTL, thus requiring a common mode of 2.5 V in order to work properly. To ensure proper centering of the signal, it is recommended to ac-couple the reference signal and supply 10-kΩ pullup and pulldown resistors to the 5-V supply to maintain the proper common mode. With these techniques, the 18-MHz reference can be supplied while synchronizing to any available system clock for minimal extra circuitry and expense.

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