Application Report
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Leveraging Low-Frequency Power Modes on SimpleLink™ MSP432P4xx Microcontrollers

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ABSTRACT

Low power consumption is very important in all battery powered embedded applications. But the operating frequency of these embedded applications can be diverse based the needs of the application. Some applications might require operating at higher frequencies, in the order of several megahertz, while some other applications might require operating at lower frequencies, on the order of a few tens or a few hundreds of kilohertz. There are several microcontrollers in the market that offer good active mode power consumption when the operating frequency is in the order of several megahertz. But it is a challenge to get the power consumption low when the operating frequency is in the order of kilohertz. The low-frequency power modes available on the SimpleLink™ MSP432P4xx microcontrollers offer very low power consumption when low frequency of operation is used by the target application. These and more can be leveraged during development by using the SimpleLink MSP432™ software development kit (SDK) and tools provided for programming.

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Trademarks

1 SimpleLink SDK and Low-Frequency Power Modes

The SimpleLink MCU portfolio offers a single development environment that delivers flexible hardware, software, and tool options for customers developing wired and wireless applications. With an ultimate goal of 100 percent code reuse across host MCUs, Wi-Fi®, *Bluetooth*® low energy, Sub-1 GHz devices, and more, choose the MCU or connectivity standard that fits your design. A one-time investment with the SimpleLink software development kit (SDK) lets you reuse often, opening the door to create unlimited applications. For more information, visit www.ti.com/simplelink.

Inside of the SimpleLink MSP432 SDK, there are a variety of software tools and libraries that can be leveraged to automatically integrate the power optimization vectors such as automatically handling transition from and to the low-frequency power modes through the use of an RTOS such as TI-RTOS or FreeRTOS and the Power Manager API included in the SimpleLink SDK. The SimpleLink MCU SDK includes a Power Manager framework that supports the CC13xx/CC26xx, CC32xx, and MSP432 devices. The same top-level APIs, concepts, and conventions are used for all three MCU families.

SimpleLink MSP432 SDK takes an integrated approach at to power management using TI-RTOS and Free-RTOS. Enabling the Power Manager and using TI Drivers results in automatic power savings when the processor is idle. Application developers do not need to write power management code; it is available by default.

Applications that include the Power Manager framework reduce their power usage because a target specific power policy is invoked during application idle time to make informed decisions about when to activate and maximize power savings. These target-specific power policies understand the reduced power states available on the target. The TI Drivers communicate with the Power Manager to enable and disable peripheral resources and transitions.

From an application development perspective, minimal or no application code is necessary to manage power usage. However, APIs are available for the application to customize its power usage as desired. For more information on the Power Manager API, see *SDK Power Management: MSP432, CC13xx/CC26xx , and CC32xx SimpleLink MCUs*.

The low-frequency power modes on SimpleLink MSP432P4xx microcontrollers are implemented to offer very low power consumption by constraining the maximum operating frequency to 128 kHz. The Power Supply System (PSS), the memory subsystem, and the clock system on the microcontroller are optimally designed to consume very low power in these operating modes and can be leveraged through the Power Manager API.

All peripherals are fully functional in the low-frequency power modes. The maximum operating frequency of the CPU, DMA, and all peripherals is limited to 128 kHz. External reset, all external interrupts, and wake-up sources are available in the low-frequency power modes. Peripheral interrupts can be raised and serviced as in the regular active modes. There are two types of low-frequency power modes. They are low-frequency active modes (AM_LF) and low-frequency LPM0 modes (LPM0_LF). The low-frequency LPM0 modes are identical to low-frequency active modes except that the CPU is disabled and program execution is not possible.

The typical current consumption is 90 µA when the Dhrystone 2.1 program is executed from flash memory at 128 kHz in the low-frequency active mode. See Section 7 for typical current consumption characteristics in low-frequency active modes when the Dhrystone 2.1 program is executed from flash and SRAM memories at different low-frequency conditions. The typical current consumption is 70 µA during low-frequency LPM0 mode with all peripherals disabled.

2 Application View of Low-Frequency Power Modes

The low-frequency active mode can be particularly useful when the application needs to execute an active task under a low-current budget and where the timing requirement is less stringent. The active task can be a CPU-intensive workload, such as calculating a math-intensive equation or performing some type of algorithm. The task could also be leveraging a hardware engine performing digital filters, floating point operations with the built-in DSP or FPU engine, or encrypting or decrypting an AES-encrypted block of data using the integrated AES hardware engine.

Many embedded applications have limited current or power budget, whether operating from a coin cell or from an energy-harvesting source with limited output or energy storage capabilities. This type of application with a maximum allowable current during the majority of the run-time can highly benefit from these low-frequency modes unique to MSP432P4xx.

Because the CPU and all peripheral clocks operate at maximum frequency of 128 kHz in these low-frequency power modes, execution time is significantly longer than in full-performance modes (several MHz). While the modes not suitable for applications with high-speed processing or response time requirements, the modes can be leveraged by applications where ample processing time or delayed response is allowed.

In the low-frequency LPM0 mode, all peripherals except for the CPU are still active. This mode could be particularly useful and power-optimized for applications where multiple peripherals need to operate at relatively slow speed (for example, low-baud-rate serial communication, low-speed timer capture, compare, or PWM activities).

3 Core Voltage Regulators

Two core voltage regulators are available on MSP432P4xx microcontrollers. They are low-dropout regulator (LDO) and DC-DC regulator. Regular active modes can be based on either LDO or DC-DC regulator selected by frequency performance requirements of the application. But the low-frequency power modes are always based on LDO regulator. The DC-DC regulator cannot be used in the low-frequency power modes due to low core voltage regulation efficiency when delivering low load currents.

The LDO regulator can generate two core voltage levels: 1.2 V and 1.4 V (typical). The 1.2-V core voltage level is denoted as VCORE0, and the 1.4-V core voltage level is denoted as VCORE1. This implies that the low-frequency power modes can also be based on either VCORE0 or VCORE1, but the maximum operating frequency restriction of 128 kHz holds true in both cases.

The low-frequency active mode that is based on VCORE0 is represented as AM_LF_VCORE0, and the low-frequency active mode that is based on VCORE1 is represented as AM_LF_VCORE1. Similarly, the low-frequency LPM0 mode that is based on VCORE0 is represented as LPM0_LF_VCORE0, and the low-frequency LPM0 mode that is based on VCORE1 is represented as LPM0_LF_VCORE1. Figure 1 shows the different possible active mode transitions.

Because low-frequency power modes do not require VCORE1, which consumes more power than VCORE0, it is generally advantageous to operate the device in low-frequency modes using VCORE0, especially for long periods of time. However, if the application needs to constantly switch between low-frequency mode and an active mode that requires VCORE1 (for example, MCLK > 24 MHz), it might be more beneficial to keep the device in VCORE1, because frequent VCORE0 to VCORE1 switching can be energy- and time-consuming and therefore outweigh the lower low-frequency power mode current consumption benefit.

4 Clocking Considerations

Several clock sources are available on MSP432P4xx microcontrollers. They are DCO, HFXT, MODOSC, SYSOSC, LFXT, REFO, and VLO. DCO, HFXT, MODOSC, and SYSOSC are high-frequency clock sources, while LFXT, REFO, and VLO are low-frequency clock sources. LFXT is a low-frequency crystal oscillator that delivers a 32.768-kHz clock. REFO is an internal factory-calibrated low-frequency clock source that can be programmed to generate either 32.768-kHz or 128-kHz output clock. VLO is a very low-power low-frequency oscillator that delivers a 9.4-kHz clock (typical).

In low-frequency power modes, all high-frequency clock sources must be turned off by the application. The operating clock must always be generated out of any of the low-frequency clock sources only. It is not recommended to generate the operating clock in low-frequency power modes from any of the high-frequency clock sources using internal clock dividers even though the generated clock frequency is below 128 kHz. The available low-frequency clock sources LFXT, REFO, and VLO offer a good tradeoff between operating frequency, clock accuracy, and current consumption in the low-frequency power modes.

The application needs to consider the proper clock frequency configuration for peripherals operation, as the maximum allowed clock frequency in low-frequency power modes is limited to 128 kHz. This implies that UART baud rate or I^2C communication frequency or timer operating frequency or ADC sampling rate, for example, needs to be carefully considered for the application while using the low-frequency power modes on MSP432P4xx microcontrollers.

5 Entering Low-Frequency Active Modes

After the MSP432P4xx microcontroller is powered up or after every hard reset, the microcontroller enters the AM_LDO_VCORE0 operating mode. This is the LDO-based regular active mode at core voltage level 0. The low-frequency active modes can be entered from AM_LDO_VCORE0 or AM_LDO_VCORE1 operating modes. See Figure 1 for all valid active mode transitions. The transition latencies between AM_LDO_VCOREx and AM_LF_VCOREx are specified in the device-specific datasheet.

The Active Mode Request (AMR) field in the PCMCTL0 register of Power Control Manager (PCM) module must be programmed to enter the desired low-frequency active mode. See the *Power Control Manager (PCM)* chapter in the *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual* for more details. The Driver Library API functions including PCM_setPowerMode() and PCM_setPowerState() can be leveraged to facilitate quick code development and robust and fully compliant transitions between different power modes.

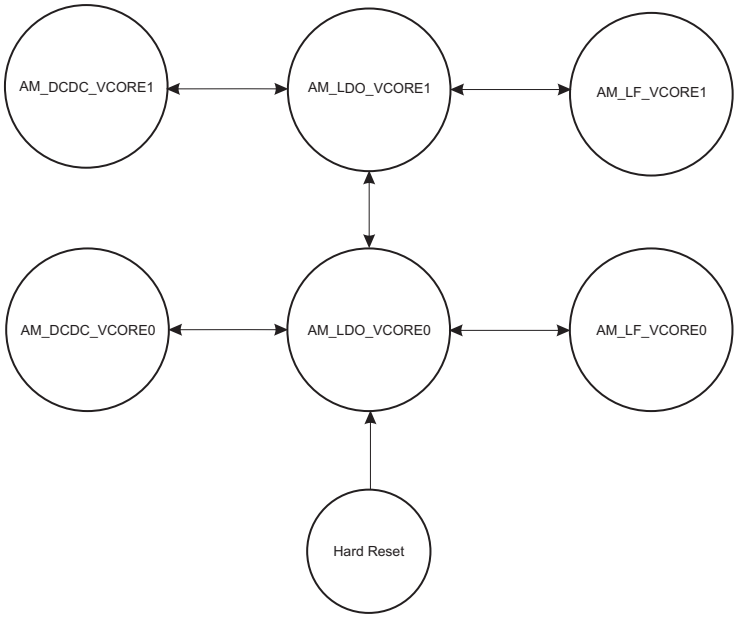

Figure 1. Valid Active Mode Transitions

6 Entering and Exiting Low-Frequency LPM0 Modes

The low-frequency LPM0 modes can be entered from the low-frequency active modes when the CPU executes WFI or WFE instructions. When changing from low-frequency active modes to low-frequency LPM0 modes and vice versa, the core voltage level remains unchanged. For example, LPM0_LF_VCORE0 entry from AM_LF_VCORE0, which has a core voltage level 0, will also be to core voltage level 0.

Changing the core voltage levels during low-frequency LPM0 modes is not possible. If a core voltage level change in LPM0 is required (uncommon scenario), the application must first return to active mode before changing the core voltage level. As with the low-frequency active modes, the maximum peripherals operating frequency in the low-frequency LPM0 modes is limited to 128 kHz.

See Figure 2 for all valid LPM0 mode transitions. The transition latencies between AM_LF_VCOREx and LPM0_LF_VCOREx are specified in the device-specific datasheet. The Driver Library API functions including PCM_setPowerMode() and PCM_setPowerState() can be leveraged to facilitate quick code development and robust and fully compliant transitions between different power modes.

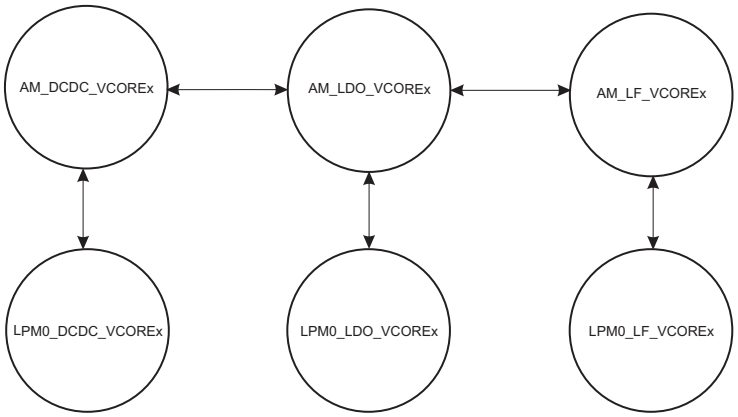

Figure 2. Valid LPM0 Transitions

7 Typical Current Characteristics

The following application use cases compare the typical current characteristics of MSP432P4xx microcontrollers when operating in low-frequency active mode with the characteristics when operating in regular active mode at core voltage level 0 to demonstrate the reduction in current consumption.

7.1 Application Use Case 1: Flash Execution at 128 kHz

Supply Voltage: 3 V

Program Memory: Flash

Clock Configuration: 128 kHz generated out of REFO

Device State: CPU executing Dhrystone 2.1 program at 128 kHz from flash.

All peripherals are inactive. Device I/O pins are set to output and driven with value 0.

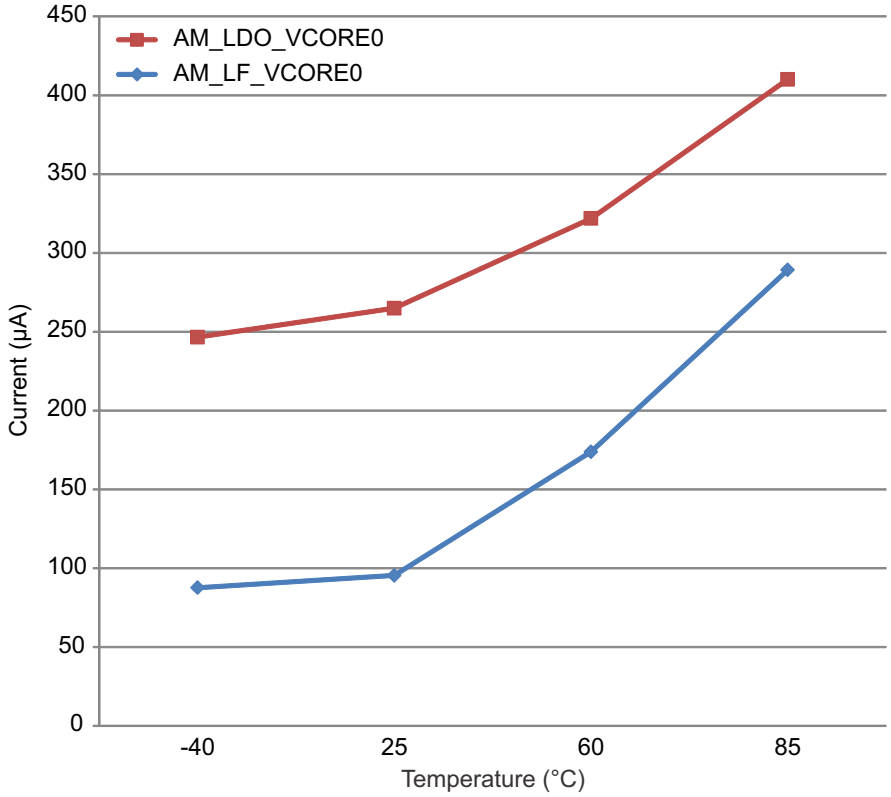

Figure 3. AM_LF_VCORE0 vs AM_LDO_VCORE0 Current – Flash Execution at 128 kHz

7.2 Application Use Case 2: SRAM Execution at 128 kHz

Supply Voltage: 3 V

Program Memory: SRAM

Clock Configuration: 128 kHz generated out of REFO

Device State: CPU executing Dhrystone 2.1 program at 128 kHz from SRAM

All peripherals are inactive. Device I/O pins are set to output and driven with value 0.

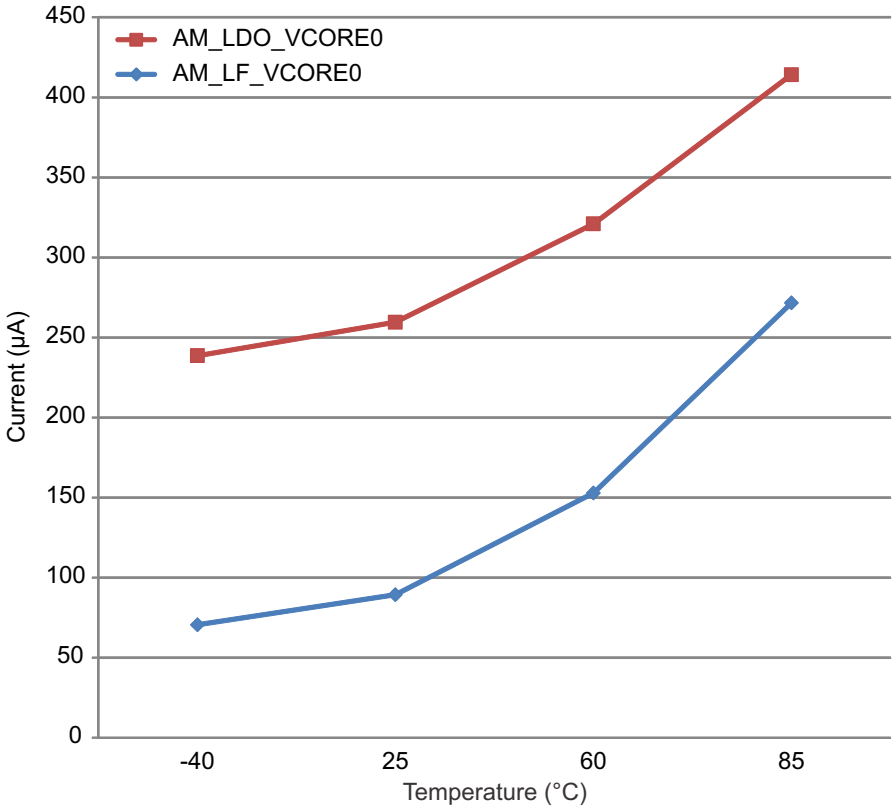

Figure 4. AM_LF_VCORE0 vs AM_LDO_VCORE0 Current – SRAM Execution at 128 kHz

7.3 Application Use Case 3: Flash Execution at 32.768 kHz

Supply Voltage: 3 V

Program Memory: Flash

Clock Configuration: 32.768 kHz generated out of REFO

Device State: CPU executing Dhrystone 2.1 program at 32.768 kHz from flash.

All peripherals are inactive. Device I/O pins are set to output and driven with value 0.

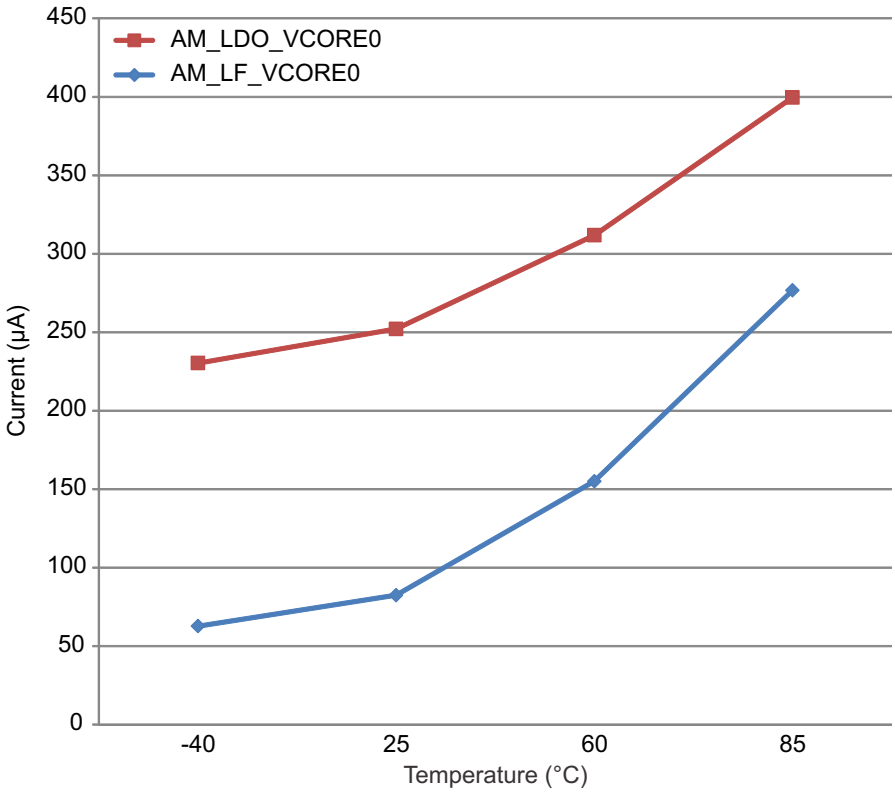

Figure 5. AM_LF_VCORE0 vs AM_LDO_VCORE0 Current – Flash Execution at 32.768 kHz

7.4 Application Use Case 4: SRAM Execution at 32.768 kHz

Supply Voltage: 3 V

Program Memory: SRAM

Clock Configuration: 32.768 kHz generated out of REFO

Device State: CPU executing Dhrystone 2.1 program at 32.768 kHz from SRAM.

All peripherals are inactive. Device I/O pins are set to output and driven with value 0.

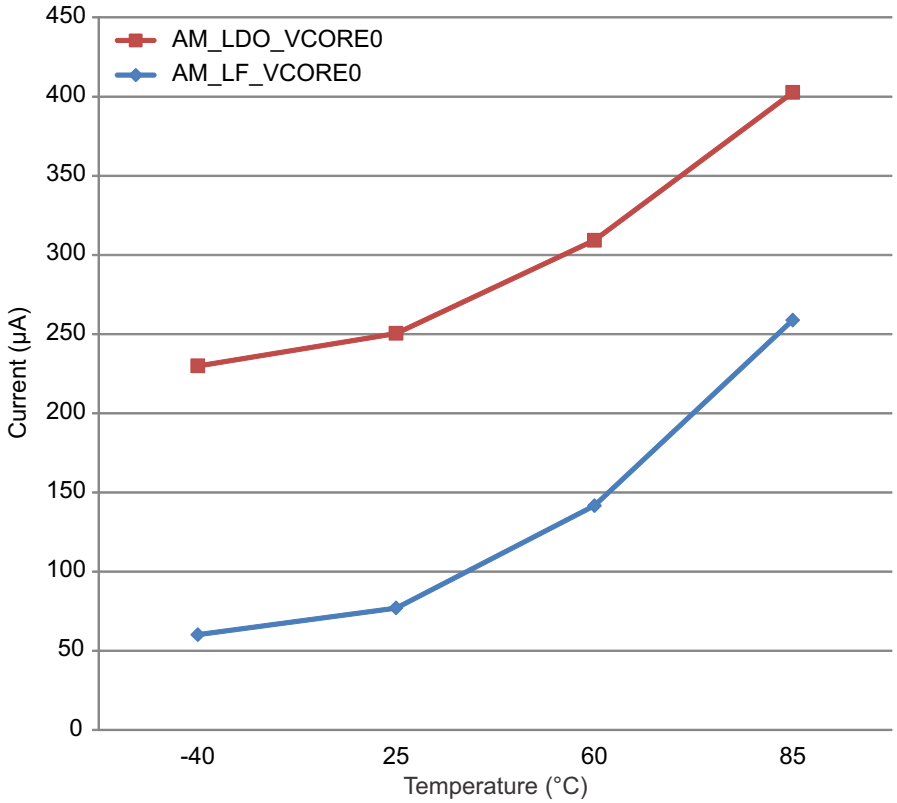

Figure 6. AM_LF_VCORE0 vs AM_LDO_VCORE0 Current – SRAM Execution at 32.768 kHz

8 Other Application Considerations

There are a few other application considerations while operating in the low-frequency power modes. The application cannot program or erase the flash memory while in the low-frequency power modes. Also the SRAM bank enable configuration in SYS_SRAM_BANKEN register or the SRAM bank retention configuration in SYS_SRAM_BANKRET register of System Controller Module (SYS) must not be changed while operating in the low-frequency power modes. These constraints ensure that the limit on current delivery by the Power Supply System (PSS) in the low-frequency power modes is not violated. It is recommended to configure SRAM bank enable or SRAM bank retention control registers as needed by the application while in the regular active modes before entering the low-frequency power modes.

9 Summary

The low-frequency power modes that are available on MSP432P4xx microcontrollers offer very low power consumption for operating frequencies not exceeding 128 kHz. The microcontroller power supply system, memory, and clock systems have been optimally designed to consume very low power in these operating modes. The application considerations on clocking and memory operations are described in this application note. Battery-powered embedded applications that require operating at low frequencies at all times or during parts of execution can benefit from the low-frequency power modes on MSP432P4xx microcontrollers to reduce the overall system power consumption.

10 References

1. *SDK Power Management: MSP432, CC13xx/CC26xx , and CC32xx SimpleLink MCUs*
2. *MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual*
3. *MSP432P401xx SimpleLink™ Mixed-Signal Microcontrollers*
4. SimpleLink MSP432 Software Development Kit (SDK)

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 8, 2016 to March 6, 2017	Page
• Added to list of authors	1
• Added "SimpleLink" branding and updated titles of referenced document as necessary throughout document	1
• Updated abstract contents	1
• Updated all contents in Section 1, *SimpleLink SDK and Low-Frequency Power Modes*	2

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