Application Report
SLAA741A–June 2017–Revised October 2017

Low-Power Analog Measurements With SimpleLink™ MSP432™ Microcontrollers

Connected MCU/MSP432

ABSTRACT

Ultra-low power analog measurements are a common requirement in applications such as non-contact power measurement and wireless condition monitoring. Many of these systems are battery based and must achieve extended life while still providing continuous coverage. This application note describes how to utilize the low-power features of the analog-to-digital converter (ADC) with up to 16-bit precision peripheral found in the SimpleLink™ MSP432™ microcontrollers (MCUs) as well as best practices to achieve ultra-low-power performance.

The software described in this document can be downloaded from http://www.ti.com/lit/zip/slaa741.

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1 Introduction

The precision ADC found in the MSP432P4xx devices is an extremely flexible 14-bit 1-Msps SAR ADC, supporting both high-performance and ultra-low-power modes. This application report focuses on the low-power feature of the precision ADC (see Figure 1) and some of the key low-power features of the MSP432 MCUs in a straight forward data acquisition and processing application.

Applications like wireless voltage monitoring for a year off a coin cell require the MSP432 MCU to periodically wake up from a deep sleep (700 nA, LPM3) and determine the RMS voltage of the differential waveform. The target goal for this application is an average current of 25 µA.

Table 5-27. Precision ADC, Power Supply and Input Range Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	NOM	MAX	UNIT
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V, ADC14PWRMD = 2		1.62		3.7	V
AV_{CC}	Analog supply voltage	AVCC and DVCC are connected together, AVSS and DVSS are connected together, V(AVSS) = V(DVSS) = 0 V, ADC14PWRMD = 0		1.8		3.7	V
V(Ax)	Analog input voltage range(1)	All ADC analog input pins Ax		0		AVCC	V
V_{CM}	Input common-mode range	All ADC analog input pins Ax (ADC14DIF = 1)		0	VREF / 2	VREF	V
$I_{(Precision ADC) single-ended mode}$	Operating supply current into AVCC and DVCC terminals(2)	$f_{ADC14CLK}$ = 25 MHz, 1 Msps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		490	640	µA
			2.2 V		450	580	
		$f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 0, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		215	270	
			2.2 V		210	260	
$I_{(Precision ADC) differential mode}$	Operating supply current into AVCC and DVCC terminals(2)	$f_{ADC14CLK}$ = 25 MHz, 1 Msps (ADC14PWRMD = 0), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		690	875	µA
			2.2 V		620	785	
		$f_{ADC14CLK}$ = 5 MHz, 200 ksps (ADC14PWRMD = 2), ADC14ON = 1, ADC14DIF = 1, ADC14VRSEL = 0xE, REFON = 0, ADC14SHT0x = 0x0, ADC14SHT1x = 0x0	3.0 V		275	335	
			2.2 V		260	320	

Figure 1. Precision ADC Low-Power Features

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2 System-On-Chip (SOC) Peripherals

In addition to the precision ADC, several other peripherals make the MSP432P4xx SOC solution very versatile and especially good at providing low-power solutions. These peripheral include the memory, power management, clock system, and GPIO.

2.1 Memory

The flash and SRAM memories are configurable to support different levels of performance and, in the case of the SRAM specifically, banks can be turned off to conserve power.

2.1.1 Flash

The flash on the MSP432P4xx device has programmable wait states to support different CPU operating speeds. In this application, the maximum core frequency is 24 MHz and, therefore, the flash wait state is kept at level 0 for the entirety of the application. It is important to note that if the speed is going to exceed 24 MHz, the V_{core} needs to be incremented to level 1, and the flash wait state needs to be incremented to level 1 [(1)]. To execute instructions at frequencies above 24 MHz with 0 wait states, the SRAM code can be used for code execution.

2.1.2 SRAM

Executing code from SRAM provides both a performance and power advantage. In this application, the emphasis is on the power benefit.

Figure 2 is taken from the MSP432P401R data sheet and shows the reduction in power consumption when executing out of SRAM. Again, this application is using a frequency of 24 MHz from the digitally controlled oscillator (DCO), and from Figure 2, the power savings is over 600 µA.

over recommended operating free-air temperature (unless otherwise noted)(1) (2) (3) (4) (5)

PARAMETER	EXECUTION MEMORY	V_{CC}	MCLK = 1 MHz		MCLK = 8 MHz		MCLK = 16 MHz		MCLK = 24 MHz		MCLK = 32 MHz		MCLK = 40 MHz		MCLK = 48 MHz		UNIT
			TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM\_DCDC\_VCORE0,Flash}$ (6) (7) (8)	Flash	3.0 V	400	475	925	1050	1530	1720	2060	2300							µA
$I_{AM\_DCDC\_VCORE1,Flash}$ (6) (7) (8)	Flash	3.0 V	430	550	1100	1280	1880	2140	2650	3000	3290	3700	4020	4500	4720	5300	µA
$I_{AM\_DCDC\_VCORE0,SRAM}$ (9)	SRAM	3.0 V	370	450	680	780	1040	1180	1410	1600							µA
$I_{AM\_DCDC\_VCORE1,SRAM}$ (9)	SRAM	3.0 V	390	510	790	940	1250	1440	1720	1960	2200	2480	2670	3000	3050	3420	µA

(1) MCLK sourced by DCO.
(2) Current measured into V_{CC}.
(3) All other input pins tied to 0 V or V_{CC}. Outputs do not source or sync any current.
(4) All SRAM banks are active.
(5) All peripherals are inactive.
(6) Device executing the Dhrystone 2.1 program. Code execution from flash. Stack and data in SRAM.
(7) Flash configured to minimum wait states required to support operation at given frequency and core voltage level.
(8) Flash instruction and data buffers are enabled (BUFI = BUFD = 1).
(9) Device executing the Dhrystone 2.1 program. Code execution from SRAM. Stack and data in SRAM.

Figure 2. Current Consumption in DC-DC Based Active Modes – Dhrystone 2.1 Program

In addition to using the SRAM to execute code, unused banks of SRAM can be turned off when not in use. This is particularly helpful during the LPM3 mode and all controllable banks (bank 1 to bank 7) are turned off. Bank 0 is always enabled, and this is where global variables and the stack are preserved even during LPM3. The configuration of the SRAM is managed in the CCS linker command file, msp432p401r_LPMRAM.cmd. This is graphically depicted in Figure 3.

(1) See the device-specific data sheet (Reference [1]) as read modes other than the normal read mode require different wait states.

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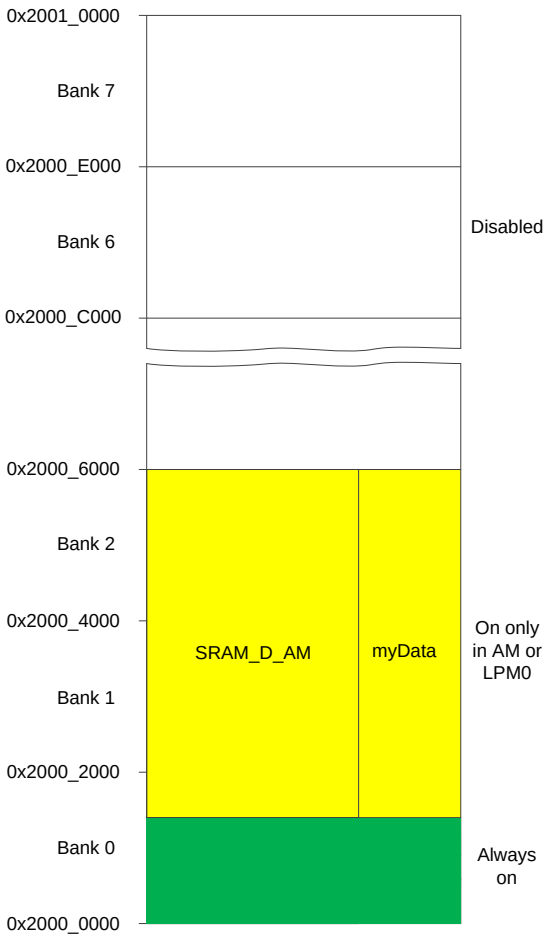

Figure 3. SRAM Organization

Figure 3 also shows when the SRAM banks are active relative to the active, LPM0, and LPM3 modes of the microcontroller. This is done to preserve only the necessary data and provide the maximum power savings.

2.2 Power Management

Power management for this application involves keeping the voltage core at level 0 throughout the application, utilizing the DC-DC converter, disabling the Power Supply Supervisor (PSS) high-side supervisor, and enabling the forced LPM entry mode to ensure that the device enters the LPM3 mode.

By keeping the main clock (MCLK) frequency to a maximum of 24 MHz, the voltage core level does not need to be adjusted during the application, because the MCLK frequency is reduced to 3 MHz before entering LPM3. In order to take advantage of the power savings of the DC-DC during active mode, it is necessary to transition from DC-DC to LDO and back as the application transitions from active mode to LPM3 to LPM0 and back to active mode [(2)].

The PSS is simply disabled, because the functionality is not required for this application. The PSS consumes only 7 µA of current in full speed mode and can be configured into a low-power mode (200 nA) during the LPM3 modes, if needed.

The forced LPM entry mode is provided to override any clock requests and ensure that the device enters LPM3 state. The clock system is discussed in Section 2.3.

(2) Also see Reference 2 for a detailed description in the *Power Mode Transitions* section.

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2.3 Clock System

This application utilizes two internal clocks, the DCO and the system oscillator (SYSOSC), as well as the external low-frequency crystal (LFXT).

The DCO toggles between 3 MHz and 24 MHz during the application. 24 MHz is the operating speed for the data capture and processing, while the 3-MHz operation is used to bridge between active mode, which uses the DC-DC converter, and LPM3 mode, which uses the LDO.

The LFXT sources the real-time clock (RTC) peripheral to provide the periodic (1 second) wake up from LPM3.

2.4 GPIO

In order to provide the sub-µA LPM3 current described in the data sheet, it is very important to properly configure the GPIO. As described in Reference 1, the GPIO structure includes a Schmidt-trigger input which can switch or even oscillate if left in a high-impedance state. Good practice for configuration of unused port pins is provided in Reference 2. In general, all of the unused I/Os are placed in an active low state.

3 Analog Configuration

The internal reference (REF_A), timer (Timer_A), and DMA are used to support the precision ADC peripheral in this application. The precision ADC is placed in a differential configuration and provides a 12-bit result in unipolar representation.

3.1 Timer_A

The Timer_A peripheral is used to generate a PWM waveform to trigger the ADC conversion time as well as define the setup and hold time before the conversion. The sample frequency is variable while the sample and hold time is statically set to 19 timer clock cycles. The Timer_A is sourced from SMCLK, which runs at 12 MHz (DCO/2), resulting in a sample-hold time in the range of approximately 1.58 to 1.38 µs (see Figure 4). The conversion time is a function of the precision ADC configuration and is discussed in Section 3.3.

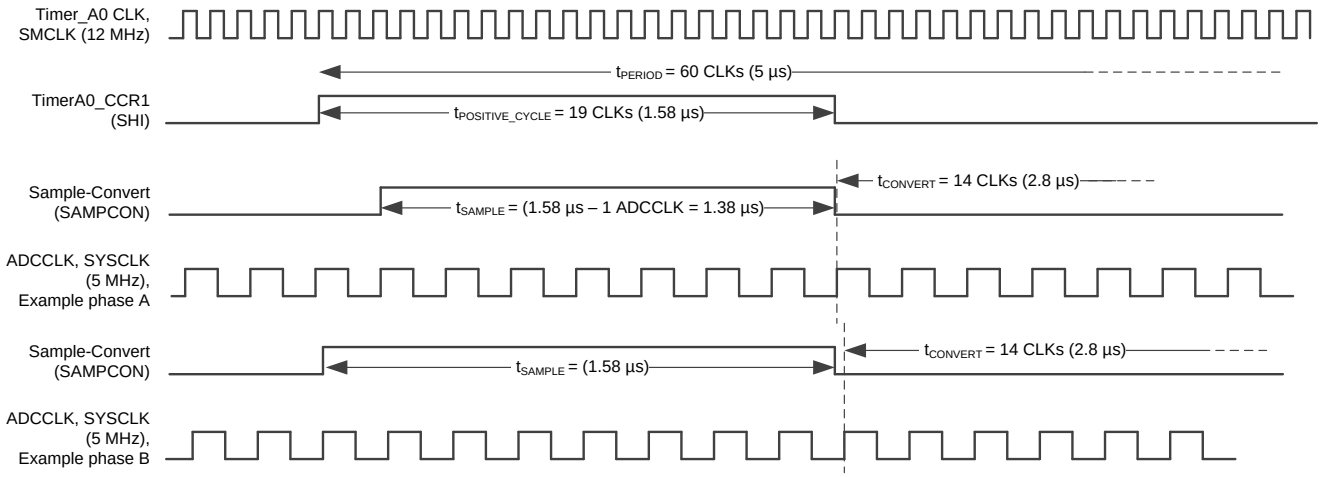

Figure 4. Timer_A Sample-Hold Definition and Sampling Frequency

3.2 REF_A

The internal reference can be configured to supply one of three voltages to the ADC. This application uses the 1.2-V reference. It is important to note that the reference is turned off during LPM3 mode to reduce power consumption, and a delay is inserted in the application to provide sufficient time for the reference and ADC wakeup.

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3.3 Precision ADC

The precision ADC provides both a high-performance mode and a low-power mode. The low-power mode, which is used here, limits the resolution to 12 bits and a maximum sampling rate of 200 ksps. The 12-bit resolution therefore dictates a conversion time of 14 ADC clocks in addition to the additional clock cycles required for the memory transfer (to the conversion memory space) and the synchronization with the timer.

The precision ADC is configured to measure a single differential channel; however, the sequence mode is defined as a sequence of channels where the single channel is written to each memory location, ADC14MEM0 to ADC14MEM31. Using this technique enables the DMA to have a more efficient interaction with the ADC memory space.

3.4 DMA

The DMA uses the scatter-gather configuration to establish tasks for moving the data content between the ADC and SRAM as well as wake up the CPU to perform intermediate processing for an RMS calculation on the dataset currently being collected. This process involves utilizing one of the GPIOs as an interrupt source, and the DMA writes to that source as a signal to wake up the CPU and process the current set of data. Figure 5 shows the DMA task flow.

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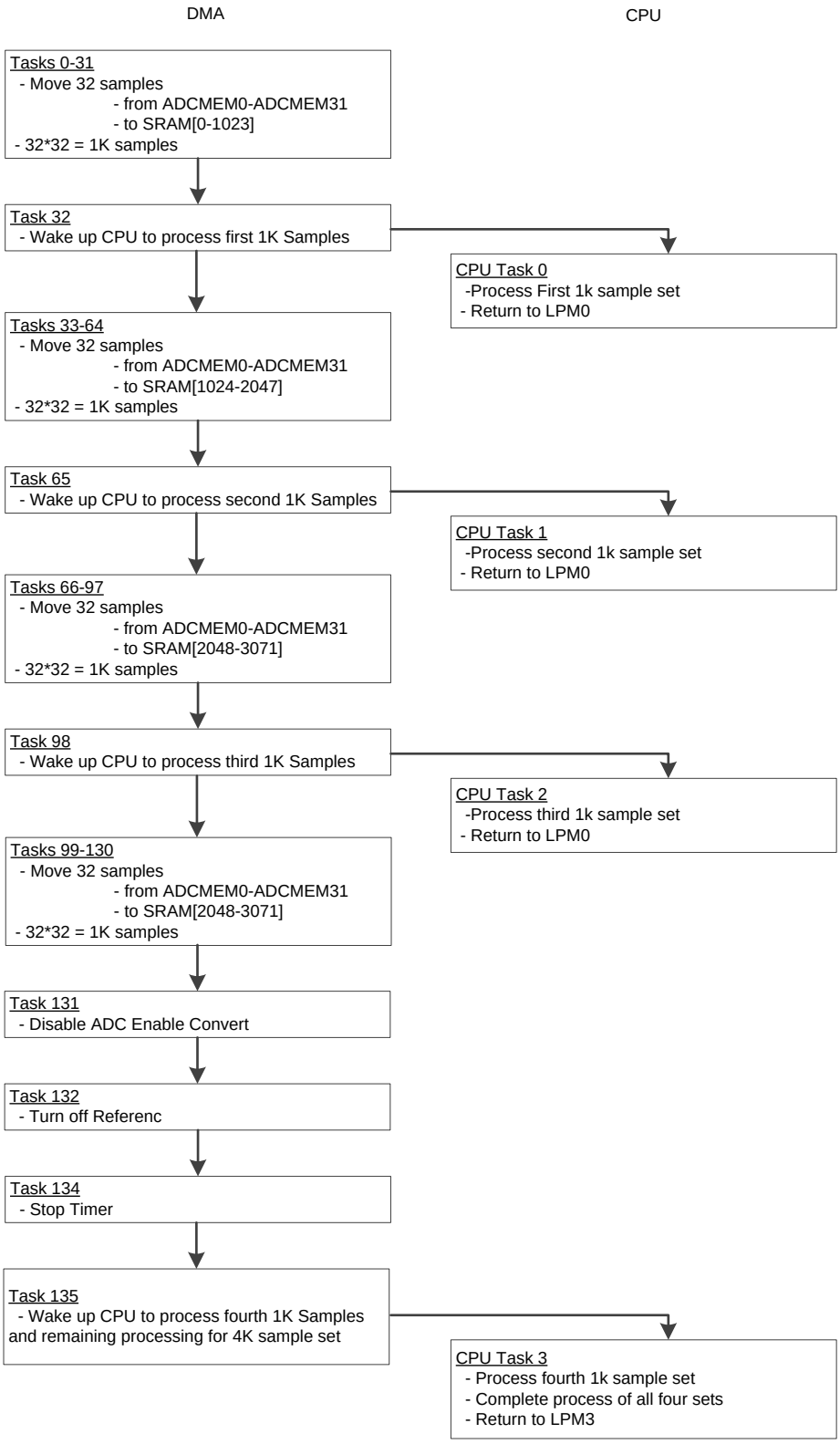

Figure 5. DMA Task Flow

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4 Test Setup

The example code provided with this application report contains all the system variables for it to compile with the SimpleLink MSP432 SDK. The only update that may be required is for the CMSIS installation path. Figure 6 shows how to update the path for CMSIS. Make sure that the check box for *Show system variables* is selected.

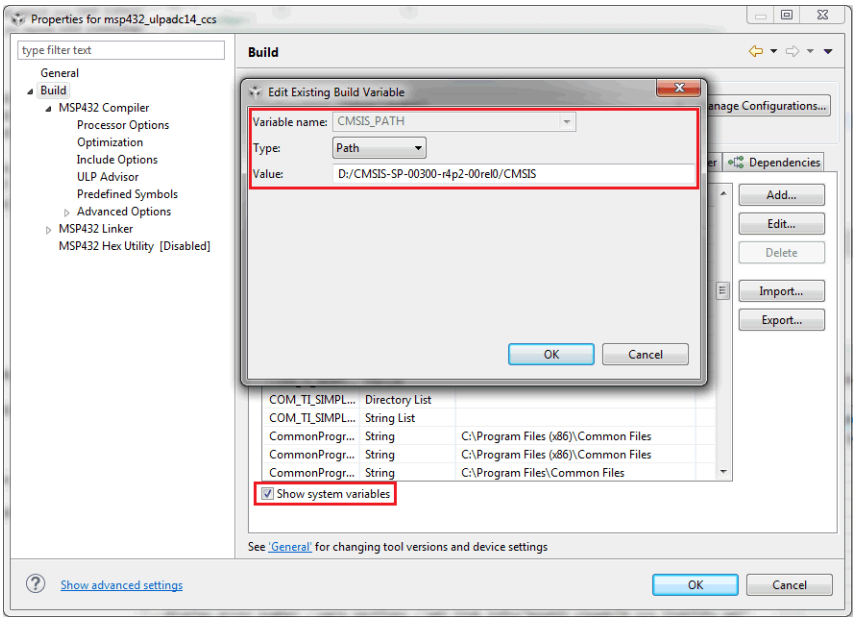

Figure 6. Updating CMSIS_PATH System Variable

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5 Test Results

Using a DC Power analyzer, the flow of the program can be seen in the current profile. Figure 7 and Figure 8 show the overall periodic waveform and a focus on the time when the measurements are made and processed. Table 1 lists the calculations for the average current.

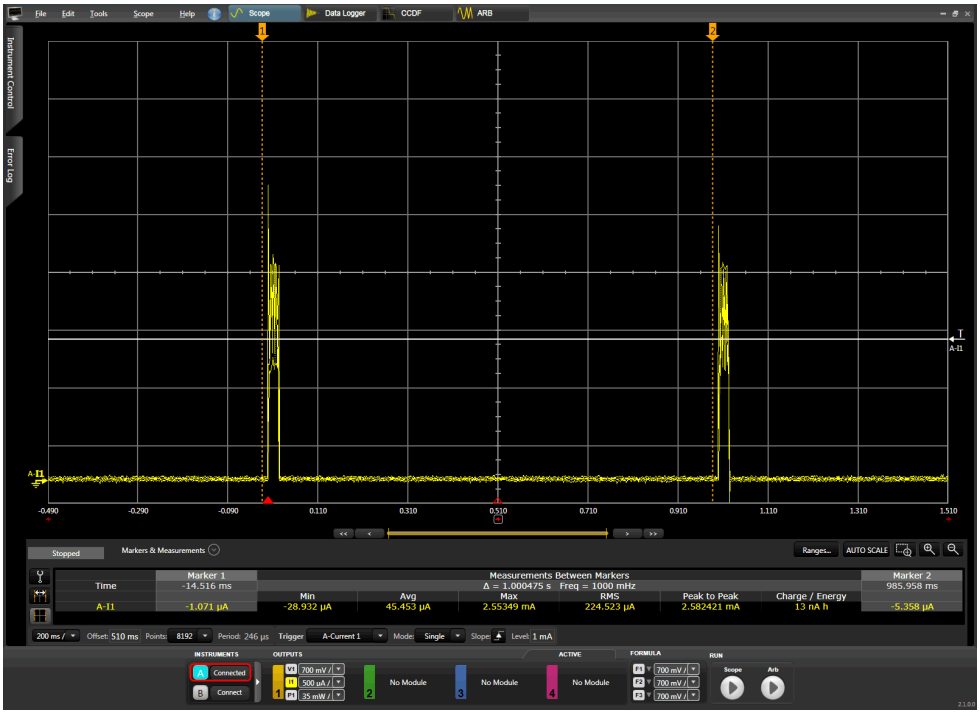

Figure 7. 1-Second Period

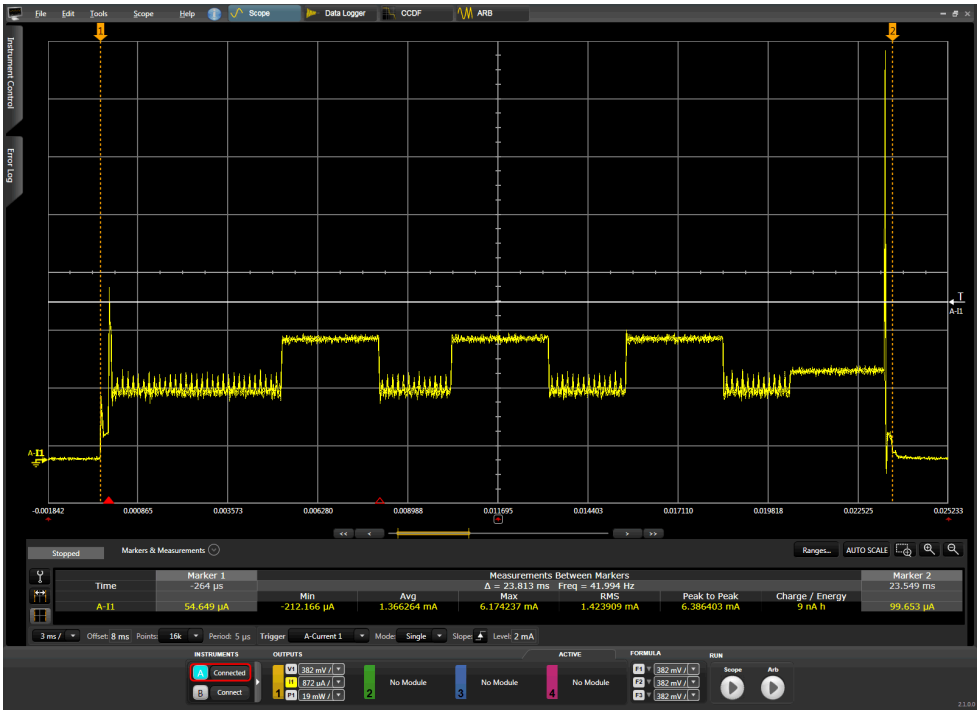

Figure 8. Data Acquisition and Capture

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Table 1. Average Current

Application	LPM3	LPM0 + Active	Average Current
1 second, 200 ksps, 4K samples	0.737 µA × (1000 ms – 23.8 ms)	1366 µA × 23.8 ms	33.23 µA
1 second, 100 ksps, 2K samples	0.737 µA × (1000 ms – 23.8 ms)	1060 µA × 23.8 ms	25.95 µA
1 second, 50 ksps, 1K samples	0.737 µA × (1000 ms – 23.8 ms)	904 µA × 23.8 ms	22.23 µA
2 seconds, 50 ksps, 1K samples	0.737 µA × (2000 ms – 23.8 ms – 0.42 ms)	904 µA × 23.8 ms + 272 µA × 0.420 ms	13.4 µA

6 Conclusion

The low-power mode of the precision ADC peripheral in conjunction with the low-power features of the MSP432 MCU enable a wide range of low-power applications. This example shows how to achieve 1 year of battery life using a 220-mAh battery while continuously measuring once a second. At a slower rate of 2 seconds and 50 ksps, a longer battery life of 1.8 years could be achieved. These techniques can easily scale to any low-power MSP432 application.

7 References

1. MSP432P401R, MSP432P401M SimpleLink™ Mixed-Signal Microcontrollers
2. MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual
3. Using the CMSIS DSP Library in Code Composer Studio for TM4C MCUs

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8 Appendix A. CMSIS DSP Library

The CMSIS DSP Library is utilized for some of the math functions to calculate the RMS of the measured waveform. This appendix, in addition to Reference 3, explains how to create and include the library in CCS.

9 Appendix B. Current Profiles

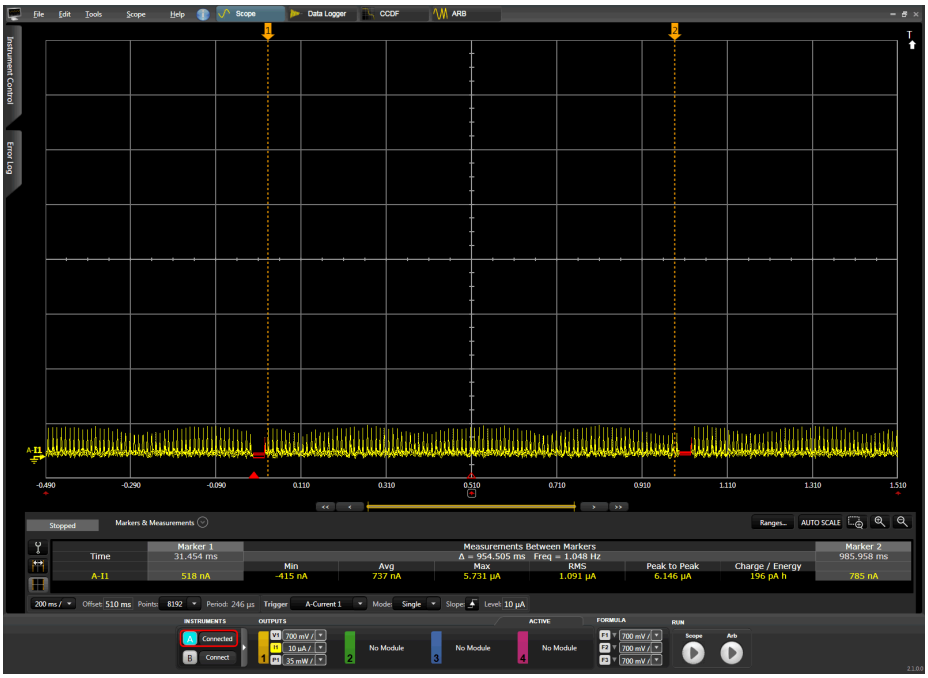

Figure 9. LPM3 Current, 740 nA

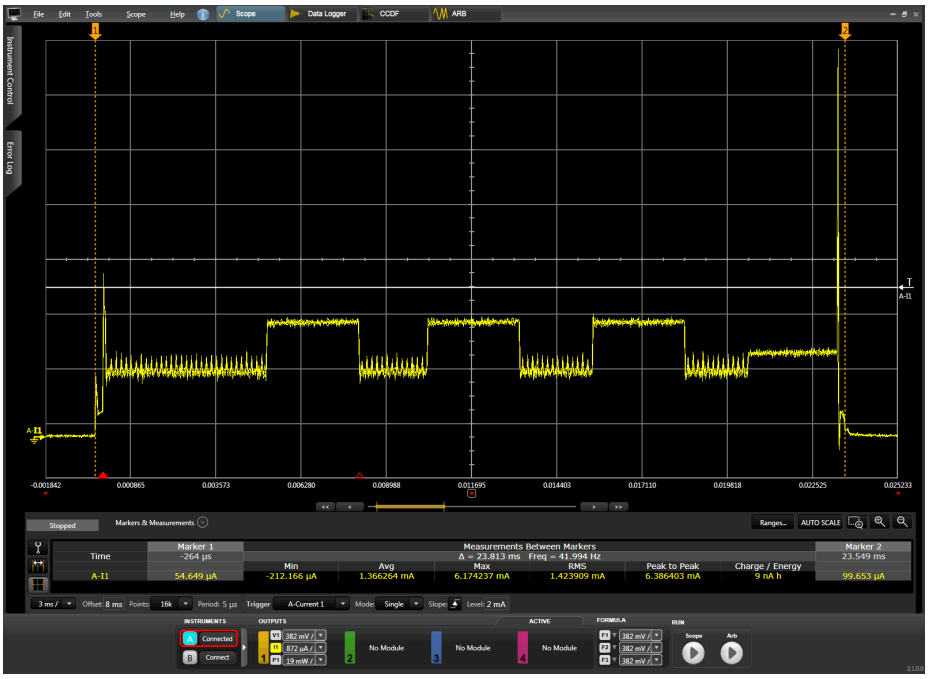

Figure 10. LPM0 and AM, 200 ksps, 4K Samples, 1.37 mA

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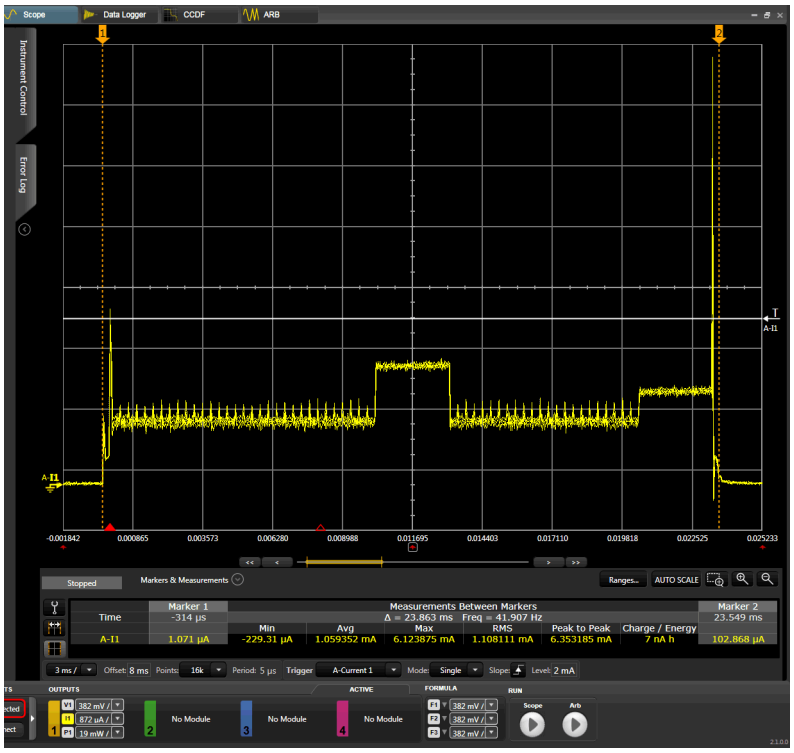

Figure 11. LPM0 and AM, 100 ksps, 2K Samples, 1.06 mA

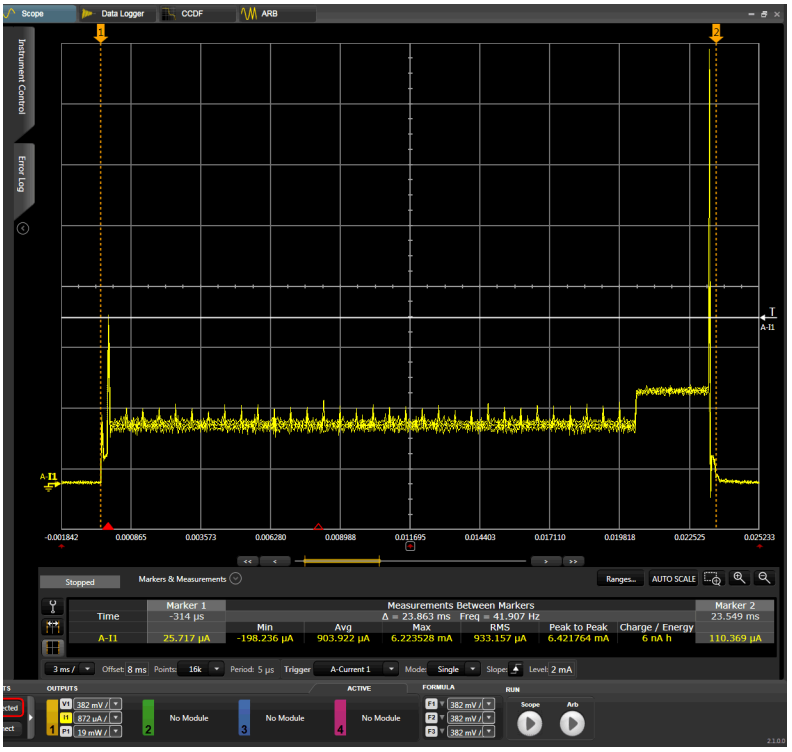

Figure 12. LPM0 and AM, 50 ksps, 1K Samples, 904 µA

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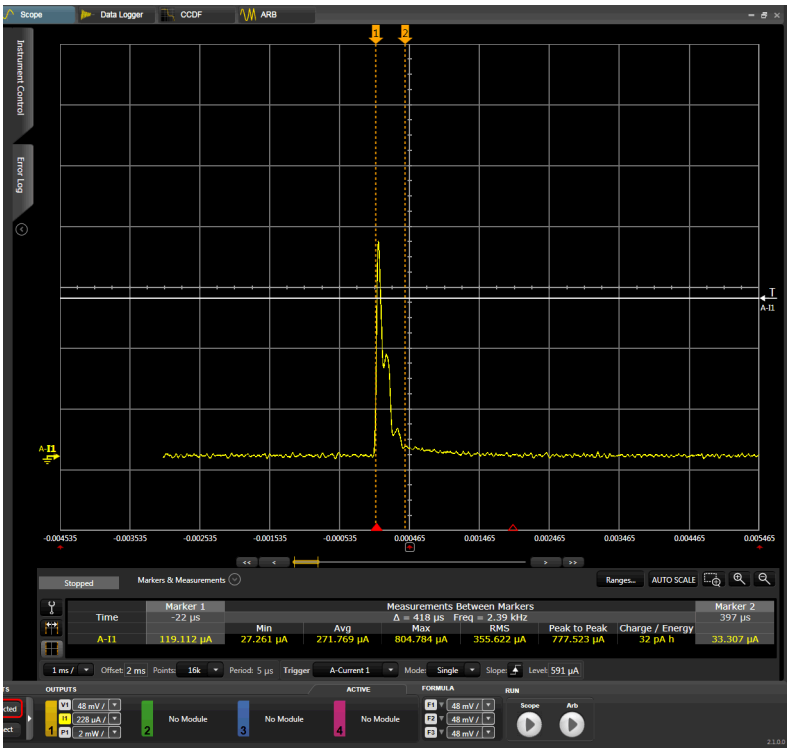

NOTE: A simple counter is added to the example to extend the LPM3 period to 2 seconds. The waveform is the time and associated current profile to service the interrupt.

Figure 13. WDT Interrupt to Extend Interval to 2 Seconds

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from June 30, 2017 to October 19, 2017	Page
• Changed the name of the ADC module from *ADC14* to *precision ADC* throughout document	1

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