Application Report
SLAA821–January 2018

Precision ADC With 16-Bit Performance

Connected MCU/MSP432

ABSTRACT

The precision ADC with 16-bit performance is a unique analog-to-digital converter (ADC) found in the SimpleLink™ MSP432P4 family of MCUs. This ADC provides a host of flexibility without compromising on performance. This application note walks though the different performance corners of the ADC in addition to providing examples for testing these different levels of performance. This will include the software infrastructure to show 16-bit performance as well as low-power (200-ksps, 12-bit) performance and high-speed (1.5-Msps, 8-bit) performance.

The software associated with this application report can be downloaded from http://www.ti.com/lit/zip/slaa821.

Contents

List of Figures

List of Tables

Trademarks

1 Introduction

This application report is split into two main themes. The first is a guided overview of how the precision ADC is presented in the data sheet. This overview includes some of the philosophy behind what is included and what is not. Of those parameters that are included, a differentiation is made between parameters that can be mitigated or even calibrated out in the application and parameters that cannot. These parameters that cannot be mitigated provide a good basis for comparing relative performance of an ADC. Additionally, Typical Performance Curves (TPCs) are provided to understand how parameters may vary within the bounds provided in the tables over temperature or supply voltage. These TPCs can in turn be used to help design the previously mentioned calibration.

The goal of this first section is to promote understanding and the application of the data sheet information. One of the parameters highlighted in the first section is the low system noise exemplified in the SINAD parametrics. This is the emphasis of the second section, which shows the resulting performance for the included firmware examples.

The ability to reach 16-bit performance with a 14-bit ADC is possible because of the extremely low amount of noise introduced by the converter. The examples and results show a continuity of performance between 8-, 12-, and 14-bit modes even as the 8-bit mode is increased in sampling rate or the 12-bit mode is throttled down to a low-power ADC mode. Finally, 16-bit performance is demonstrated with a simple window filter and also the CMSIS DSP Library decimation API. The contrast of the different implementations highlights the trade-offs between performance and resources.

2 Utilizing Data Sheet Parametric Values and Typical Curves to Assess ADC Performance

To facilitate the assessment of the Precision ADC, the MSP432P4 data sheet provides seven parametric tables and 40 TPCs to communicate the timing and switching characteristics of the ADC. This section highlights the linearity and dynamic parameters as figures of merit for choosing an ADC. In this section is also addressed the seemingly ad hoc choice of when or when not to delineate performance for various permutations and combinations of settings. Finally, this section identifies secondary parameters which can be addressed with external solutions such as a cleaner power supply or calibration techniques.

2.1 Tables

The values provided in the data sheet parametric tables are intended to cover all operating conditions and use cases unless a specific operating condition or use case is given. For example, the differential linearity error (DNL) is specified as having maximum error of less than one LSB. This means that there are no missing codes. Moreover there will be no missing codes across operating conditions such as temperature or V_{CC}, nor will there be any missing codes due to a particular configuration (resolution, reference, clock, and so on). In contrast, the gain and offset error (and E_T) [(1)] performance is delineated as a function of the reference configuration selected, see Figure 1. In the case of the gain and offset error the variation in performance is significant and therefor a separate test condition is provided. This is why the MSP432P4 data sheets specify some parameters with test conditions and some parameters without test conditions. If a specific test case is missing, then this should not be considered an omission, but a test case that does not cause the performance to deviate from what is provided.

(1) E_T is the root sum of the squares of all the errors, see ADC Performance Parameters - Convert the Units Correctly!.

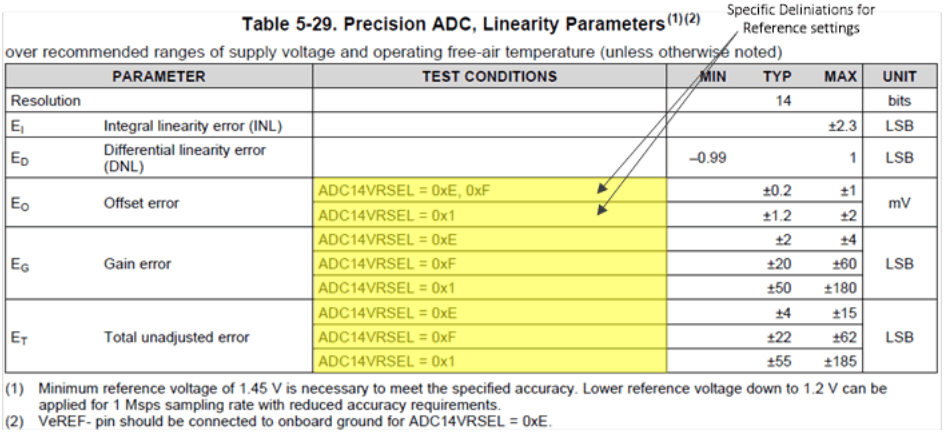


Table 5-29. Precision ADC, Linearity Parameters(1)(2)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

Specific Deliniations for Reference settings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Resolution				14		bits
E_I	Integral linearity error (INL)				±2.3	LSB
E_D	Differential linearity error (DNL)		–0.99		1	LSB
E_O	Offset error	ADC14VRSEL = 0xE, 0xF		±0.2	±1	mV
		ADC14VRSEL = 0x1		±1.2	±2	
E_G	Gain error	ADC14VRSEL = 0xE		±2	±4	LSB
		ADC14VRSEL = 0xF		±20	±60	
		ADC14VRSEL = 0x1		±50	±180	
E_T	Total unadjusted error	ADC14VRSEL = 0xE		±4	±15	LSB
		ADC14VRSEL = 0xF		±22	±62	
		ADC14VRSEL = 0x1		±55	±185	

(1) Minimum reference voltage of 1.45 V is necessary to meet the specified accuracy. Lower reference voltage down to 1.2 V can be applied for 1 Msps sampling rate with reduced accuracy requirements.
(2) VeREF- pin should be connected to onboard ground for ADC14VRSEL = 0xE.

Figure 1. Parameters With Specific Test Conditions

Within the tables, a good starting point for evaluating the performance of the ADC is the linearity and the signal-to-noise ratio.

2.1.1 Linearity Parameters

Integrated linearity error (INL) and DNL are very common and understood ADC parameters. In addition to the INL and DNL, other static parameters supplied in the data sheet are offset error, gain error, and total unadjusted error (E_T). While important, these other factors are considered secondary and application dependent because of the ability to remove these errors with calibration and compensation techniques.

Both the INL and DNL are provided across recommended operating conditions and operating modes. The gain and offset errors are provided for different types of reference configurations. The gain error is provided in mV, whereas the INL, DNL, and gain error are given in units of least significant bit (LSB). The definition of an LSB is dependent upon the mode, single-ended or differential, as shown in Equation 1 and Equation 2, respectively. The 2 raised to the 14th power represents the number of codes provided by the 14-bit ADC core. V_R represents the reference voltage.

$$1\ LSB_{single\text{-}ended} = \frac{V_{R+} - V_{R-}}{2^{14}} \quad (1)$$

$$1\ LSB_{differential\text{-}ended} = \frac{2 \times \left(V_{R+} - V_{R-}\right)}{2^{14}} \quad (2)$$

As an example, the external 2.5-V reference has been selected (ADC14VRSEL = 0x1). This reference has an error of ±1%, according to the data sheet. Using the equations found in How the voltage reference affects ADC performance, Part 1, Table 1 shows the voltage error for the precision ADC operating in 14-bit single-ended mode and differential modes.

Table 1. Linearity of Precision ADC With Internal 2.5-V Reference

Parameter	Mode	LSB	Volts
INL	SE	±2.3	±0.00035
	DE		±0.00070
DNL	SE	–0.99 to 1	±0.00015
	DE		±0.00030
Offset error (ADC14VRSEL = 0x1)	SE		±0.002
	DE		
Gain error	SE	±180	±0.027
	DE		±0.055
Total unadjusted error	SE	±185	±0.027
	DE		±0.055

It is important to remember that the gain and offset error can be compensated (adjusted) after the conversion so that only the INL and DNL error remain. This requires calibration of the ADC which is outside of the scope of this document, but it is important to note a couple of points about calibration. First, the offset error is a more easily compensated for in differential mode (1) typically requiring a single measurement at 0 V (by shorting the input to ground). Second, the two point calibration to determine slope (gain error) is applicable to both the single-ended and differential modes. Finally, another consideration for calibration is how the error changes or drifts over operating conditions. The TPCs found in the data sheet provide both gain and offset error over temperature.

Table 2 shows the performance with an exact external 2.5-V reference and no reference error. When comparing these numbers it is important to remember that the error associated with the reference affects the accuracy of the measurement. In the case of Table 1, a 1% error from the internal reference results in a gain error of 164 LSB (2) and is included in the total error. In Table 2, the error associated with the reference needs to be added to the total adjusted error or more precisely a root sum of the squares with the ADC gain error.

(1) In single-ended mode it is not possible to measure negative offset errors by simply applying 0 V to the input. The input voltage would need to be swept to determine where the first code is measured relative to the ideal 0.5 LSB (see ADC Performance Parameters - Convert the Units Correctly!).

(2) Theoretical, not measured

Table 2. Linearity of Precision ADC With External 2.5-V Reference

Parameter	Mode	LSB	Volts
INL	SE	±2.3	±0.00035
	DE		±0.00070
DNL	SE	–0.99 to 1	±0.00015
	DE		±0.00030
Offset error (ADC14VRSEL = 0x1)	SE		±0.001
	DE		
Gain error	SE	±4	±0.00061
	DE		±0.0012
Total unadjusted error	SE	±15	±0.0012
	DE		±0.0017

The linearity measurements found in the data sheet are associated with DC performance and complimenting these measures are the Dynamic Parameters associated with AC performance.

2.1.2 Dynamic Parameters

The INL and DNL are relative to the ideal transfer function of the ADC while the signal-to-noise and distortion (SINAD) (1) can be thought of in terms of the ideal error introduced from the quantization error (noise) and the FFT processing gain. Figure 2 shows one of the MSP432 ADC TPCs with the ideal noise floor (2) of a 14-bit ADC overlayed on the original data sheet graphic.

(1) Effective number of bits is also provided which is related to SINAD by the following equation: ENOB = (SINAD – 1.76 dB) / 6.02 dB

(2) This is the combination of the SINAD of an ideal 14-bit ENOB, 14 × 6.02 + 1.76 dB and the FFT process gain, 10 × log(M/2), where M is the sample size.

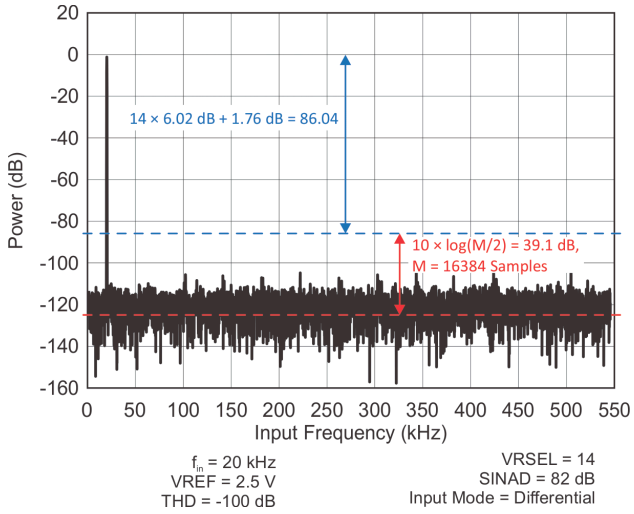


Figure 2. SINAD Description With Theoretical Limit Overlay

An ideal 14-bit ADC would only have noise associated with the quantization error of ±0.5LSB, and the SINAD can be calculated, as shown in Equation 3. As shown in Figure 2, applying this to one of the TPCs in the data sheet graphically demonstrates that the performance is within 5 dB (ENOB less than 1LSB) from the theoretical limit.

$$\text{SINAD} = 14 \times 6.02\ \text{dB} + 1.76\ \text{dB} = 86.04 \quad (3)$$

The dynamic parameters provided are common-mode rejection ratio (CMRR), and power supply rejection ratio (PSRR). Just as with the gain and offset error, the PSRR and CMRR are important but they are also factors that can be mitigated by controlling the common-mode input as well as the power supply noise. Again, these are application dependent features. For example, a differential amplifier can be used to keep the common-mode input seen by the ADC relatively constant and therefor any common-mode acceptance can be kept as a constant offset which can be easily calibrated for. Similarly, the use of an external regulator can eliminate power supply noise before it gets to the MCU and ADC.

2.1.3 Power and Timing

Following the performance requirements, the next logical evaluation is of the system resource requirements and determine whether the ADC can still perform within those resource requirements. This is most often a consideration of time and power. The input conditions and power consumption of the ADC are fairly straight forward. The main components of the current consumption are the ADC core and the ADC reference buffer. It is important to note that the ADC does provide a low power option which reduces the current consumption by over 50%. With this option the maximum signaling rate is reduced to 200Ksps and the maximum resolution to 12-bit.

The timing requirements are provided, however, the required sampling time is a function of several components. These components include the input capacitance and series on resistance of the ADC, the IO capacitance, as well as the impedance of the voltage source being measured. As shown in Appendix A, the sample-and-hold time can be controlled through firmware to accommodate a wide range of times, however, it should be understood that any increase in the minimum sample-and-hold time of 4 ADC clock cycles will impact the maximum achievable sampling rate.

2.2 Typical Curves

In addition to the tables describing performance and operating conditions, the data sheet also provides typical curves. These curves help provide a more complete picture of the performance ADC and how the performance can vary over specific operating conditions.

The first set of graphs, rather predictably, show the increase in current consumption with increased signaling rate. As shown in Figure 3, what is not as predictable is the difference between power consumption between the normal and low-power modes (ADC14PWRMD) of operation and the utilization of different references.

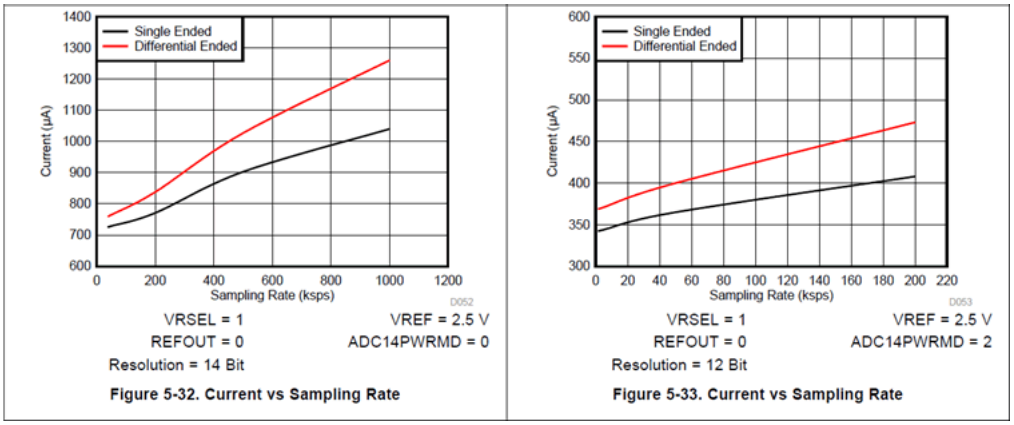


Figure 3. Example Current vs Sampling Rate Typical Curves

The second set of graphs show INL and DNL over the entire set of output codes of the ADC. For both the INL and DNL, the graphs represent a specific set of conditions and therefor well within the bounds described in the tables. Also, these graphs help illustrate the improvement in performance when using the differential mode of the single-ended mode, as shown in Figure 4.

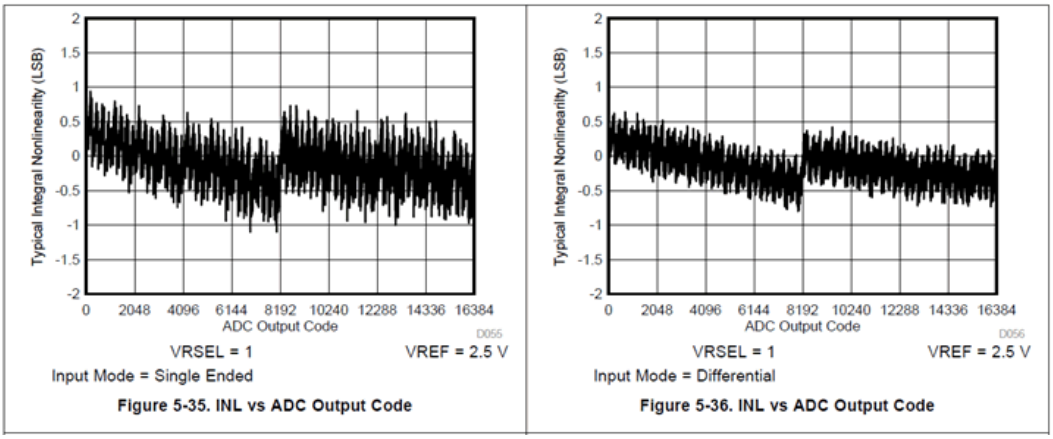


Figure 4. Linearity Typical Curves

The next set of graphs includes THD as well as the SINAD previously described in the table in the context of a 20-kHz input measured at 1 Msps. Again the benefit of differential mode and a nonbuffered external reference can be identified in the decreased noise floor and improved SINAD and THD.

Another set of graphs illustrates dynamic parameters SINAD (ENOB), THD, and SFDR, over the external reference voltage range. In most applications, the reference voltage is constant, but these graphs are helpful in understanding and selecting a reference voltage.

The final set of graphs help show the drift over temperature for the various performance parameters. This is especially important in calibrated systems to understand how good the calibration will apply over temperature or when another calibration should be applied as the temperature in the application environment changes. As an example, Figure 5 shows that above 40°C, the offset increases with temperature. Beyond this temperature, calibration for offset error should take place more frequently as temperature increases.

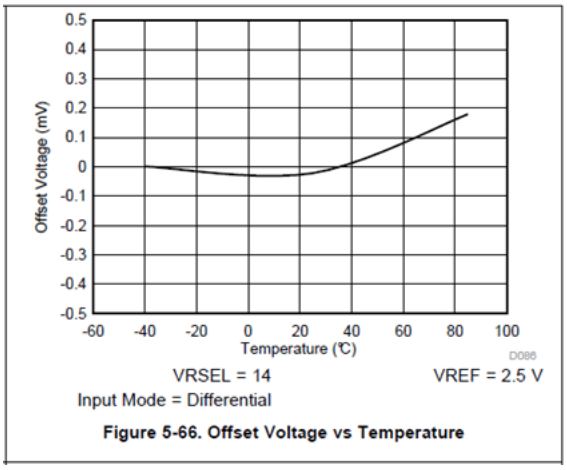


Figure 5. Offset Voltage vs Temperature Typical Curve

2.3 Specific Features

The last category to consider in ADC selection is special features. The MSP432P4 family Precision ADC provides an integrated window comparator as well as two internal sensors, one for temperature and one for AVcc/2. The temperature sensor, as described in the data sheet [3] , can be calibrated with the constants found in the internal memory (TLV).

3 Application

Sample code is provided with this application report with the intent to enable recreation of the test data shown as well as provide a code base from which to develop firmware. The examples are repeated single-channel conversions with manual trigger. The 12-bit resolution example incorporates the low-power feature and, therefore, the maximum signaling rate is limited to 200 ksps. The rest of the examples operate at 1 Msps, although the effective sample rate for the decimated examples is 31.25 ksps, with an oversampling rate (OSR) of 32.

All of the examples utilize the DMA in ping-pong mode to transfer data from the ADC to memory. The DMA typically transitions from the primary to secondary transfers (buffers) at 1024 sample boundaries. This enables 1-Msps operation and, as will be shown in the decimation example, the 1-ms period allows the previously acquired data block to be processed while the next block is being acquired.

The SINAD results shown are from data collected with the Precision Signal Injector (PSI) and the SimpleLink™ MSP432P401R LaunchPad™ Development Kit. The PSI is part of the ADS8900B Fully-Differential Input, 20-Bit SAR ADC EVM Performance Demonstration Kit (PDK). The combined performance of the PSI and the ADS8900B is typically an SNR of 100 dB and a total harmonic distortion of –120 dB.

The differential, 2-kHz sine wave [4], signal from the PSI is connected to the ADC inputs on the LaunchPad™ development kit. To most closely represent the data sheet use case, an external reference is used in addition to the 48-MHz oscillator found on the LaunchPad development kit. The only deviation from this test setup is the low-power mode case where the internal reference and internal 5-MHz system oscillator (SYSOSC) are used.

Each section is for a specific resolution. The 8-, 12-, and 14-bit resolutions are provided by the precision ADC hardware, and the greater than 14-bit examples are a combination of hardware and firmware.

[3] See Precision ADC, Temperature Sensor and Built-In $V_{1/2}$. The notes in this section further describe the use of the calibration values.
[4] The PSI can support various frequencies; however, the filters are designed to provide maximum fidelity at 2 kHz.

3.1 8-Bit Resolution

The 8-bit resolution provided by the precision ADC is still a low noise and high performance ADC. What is interesting about reducing the resolution is the reduction in the conversion time and consequently the ability to sample at a faster signaling rate. So, while the voltage resolution is reduced when compared to the 14-bit mode, the frequency resolution is slightly increased because the maximum sampling rate can be increased to 1.5 Msps. Because of the lower resolution, the internal reference can used as well as the voltage rail supplied by the LaunchPad development kit without affecting the quality of the conversion result. The 8-bit 1.5-Msps data collection results in an ENOB of 7.9, as shown in Figure 6.

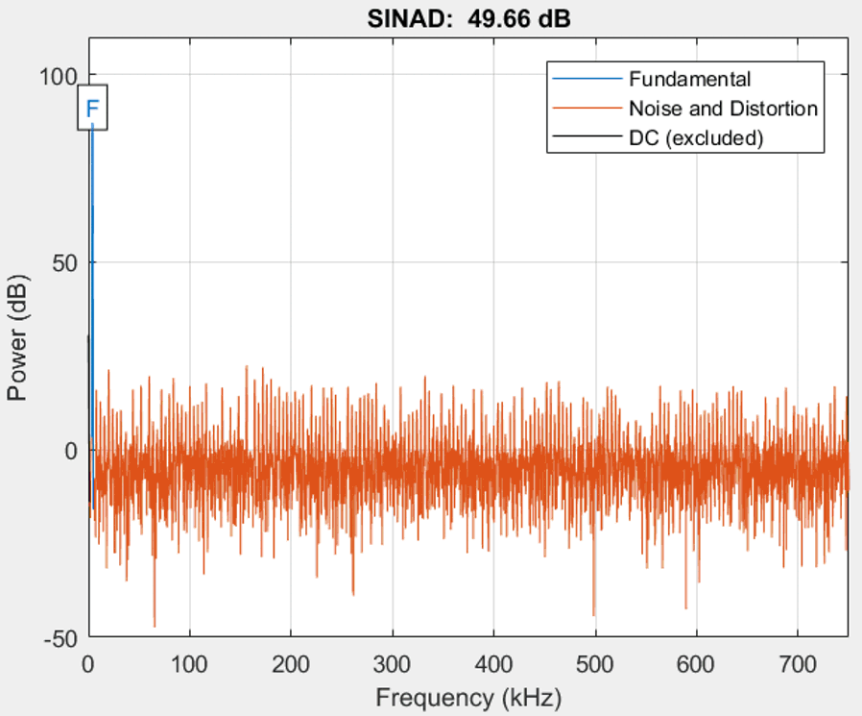


Figure 6. 8-Bit, 1.5 Msps, 2-kHz Input, ENOB 7.95

3.2 12-Bit Resolution

Another unique feature of the precision ADC is the low-power mode. This reduces the power consumption of the ADC core while still providing good ADC performance. The power reduction does limit the operating conditions to 200-ksps sampling rate and 12-bit resolution. As shown in the data sheet, the current consumption is nearly cut in half, and Figure 7 shows that the ENOB (11.7) is still within 1 LSB of the ideal resolution (12).

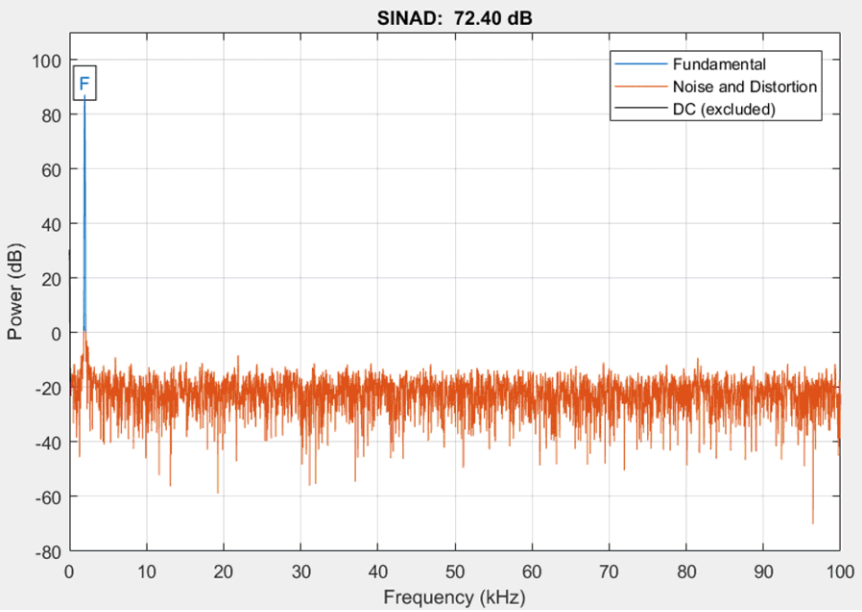


Figure 7. 12-Bit, 200-ksps, 2-kHz Input, ENOB 11.73

3.3 14-Bit Resolution

The 14-bit mode is the highest native resolution of the precision ADC, and as shown in the data sheet the typical ENOB is 13.2. This mode was also tested with the precision signal injector and the SINAD analysis is shown in Figure 8.

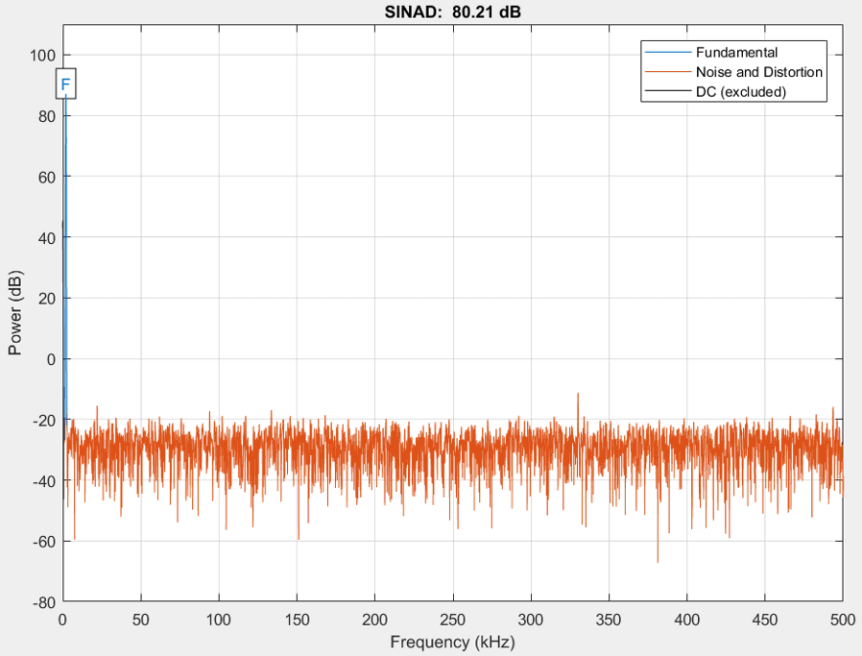


Figure 8. SINAD of 14-Bit, 1-Msps, 2-kHz Input, ENOB 13.03

3.4 15-Bit and 16-Bit Resolution

As seen in Figure 2 and Figure 8, the noise floor is quite low in the precision ADC. However, gains in ENOB can still be realized with software signal processing. 16-bit performance can be achieved with a smoothing window, a rolling summation of 32 samples. The benefit of the summation is two-fold; a gain of the signal and a reduction of the noise floor. The flow of the example firmware is shown in Figure 9.

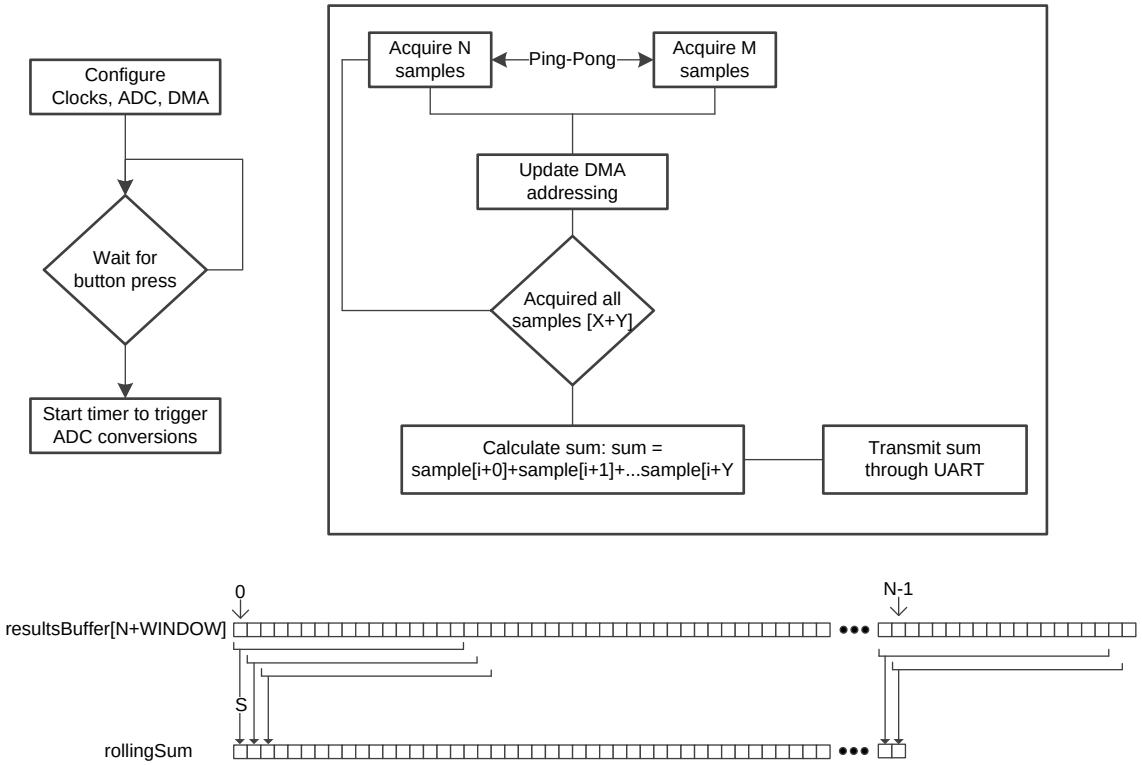


Figure 9. Rolling Sum Overview

The resulting SINAD result in Matlab is shown in Figure 10. Using Equation 3, 95 dB translates to an ENOB of 15.5 bits.

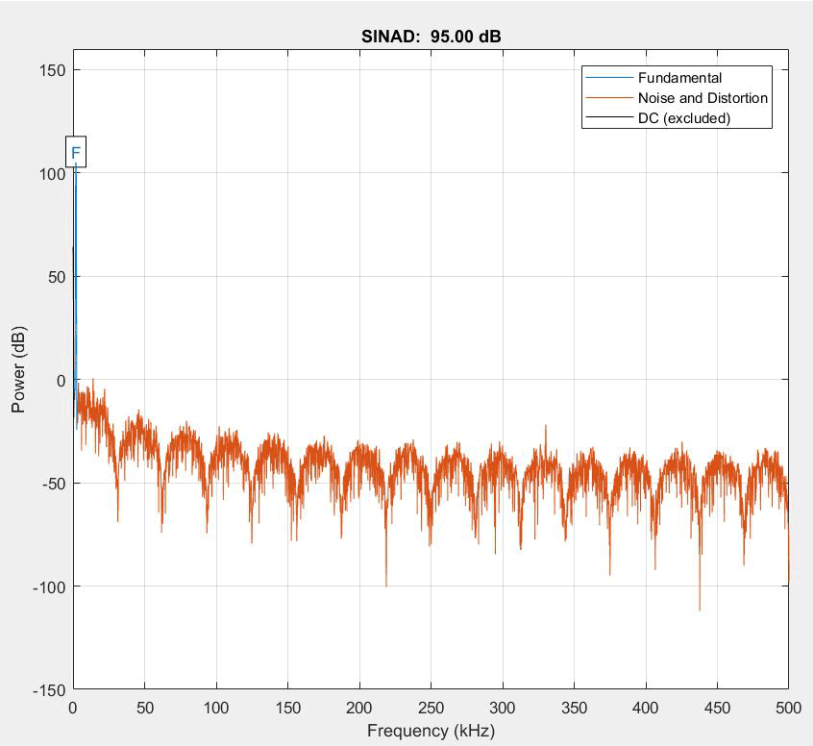


Figure 10. SINAD With 32-Sample Window, 2-kHz Input, ENOB 15.5

A similar approach can be made with an FIR filter and decimation. In this case, the CMSIS DSP Library is used and the conversion result of the ADC is provided in a signed binary left-aligned format which is treated as the ARM q15 format. The library provides a combined FIR filter and decimator which is used to take the 1 Msps and decimate to 31.25Khz (OSR=32). The resulting ENOB is 14.5.

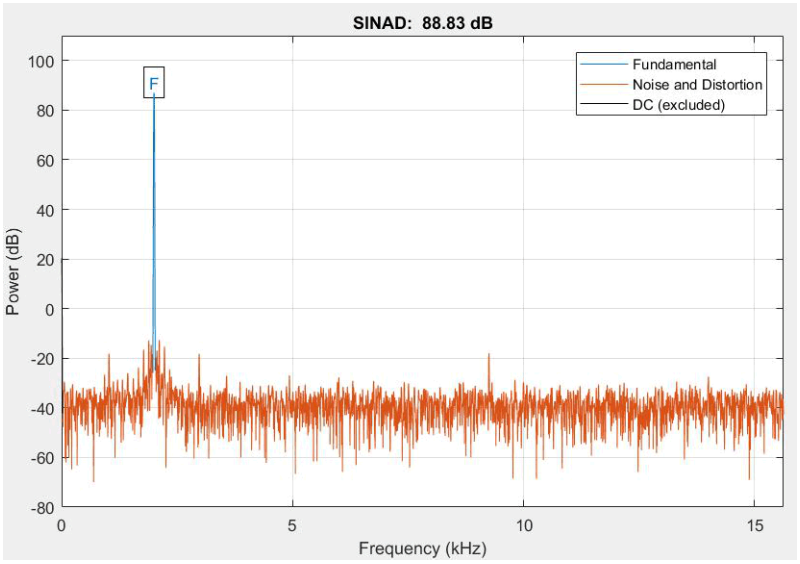


Figure 11. SINAD, CMSIS, 32x Decimation of 1 MSPS, ENOB 14.5

Because the rolling sum performs the same number of summations (adding 32 samples 1024 times) as the ADC is collecting data (1024 samples) it is impractical to apply the window while concurrently sampling as in the decimation example. The decimation example, however, consumes about 50% (535us) of the 1ms window before the next data block is ready. Instead of using the CMSIS DSPLIB API, arm_fir_decimate_q15, a simple average can be taken of each 32 samples (see firmware example adc14_15b_AVGDEC.c). This reduces the processing time to 25% and the ENOB is 13.6.

4 Conclusion

Two of the key characteristics of an ADC are the linearity and the ENOB. The precision ADC found in the MSP432P4 family of microcontrollers provides an exceptional ENOB that is less than 1 LSB from the ideal resolution of the ADC, indicating a very clean design with respect to noise. This ENOB can be further improved with post processing techniques such as windowing and decimation with filtering. Table 3 summarizes the scalability of the precision ADC from an 8-bit ADC to a 16-bit ADC, while maintaining an ENOB within 1 LSB of the ideal.

Table 3. Performance Summary

Resolution Setting	Sampling Rate: Actual / Effective	ENOB	Time to Collect 4k Samples (ms)	Current (mA)	Memory (SRAM) (KB)
8 bit	1.5 Msps / 1.5 Msps	7.9	2.73	1.37	8
12 bit	200 ksps / 200 ksps	11.7	20.48	0.98	8
14 bit	1 Msps / 1 Msps	13.2	4.10	1.36	8
16 bit	1 Msps / 31 ksps	14.5	131.07(1)	3.06(2)	16(3)
16 bit	1 Msps / 1 Msps	15.5	4.10 + 86.4	2.98(4)	10(5)

(1) 128k samples actually taken at 1 Msps and then decimated to 4k. 50% of data acquisition time is used to process previous sample set.
(2) CMSIS library functions run from flash.
(3) 4KB is used for primary (ping) and secondary (pong) DMA destination locations, and another 4KB is used by the decimation state machine.
(4) Window function runs from SRAM.
(5) If separate 16-bit and 32-bit arrays are used then the memory increases to 26KB. There are more efficient approaches that reuse the 16-bit raw conversion space to store the 32-bit windowed result.

5 References

1. Selecting an A/D Converter
2. ADC Performance Parameters - Convert the Units Correctly!
3. How the voltage reference affects ADC performance, Part 1
4. MSP432P401R, MSP432P401M SimpleLink™ Mixed-Signal Microcontrollers data sheet
5. MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual
6. ADS7056 Ultra-Low Power, Ultra-Small Size, 14-Bit, High-Speed SAR ADC data sheet, Section 9.2.1.2.1
7. General Oversampling of MSP ADCs for Higher Resolution
8. Oversampling the ADC12 for Higher Resolution
9. ADS8900BEVM-PDK User's Guide

Sample and Hold Time

The sample and hold time can be adjusted to support a range of impedances. Typically an external operation amplifier is used to buffer the signal and provide the required source impedance. By enabling a variable sample and hold time, there is potential that the additional circuitry could be omitted, provided the sampling requirements of the application are still met.

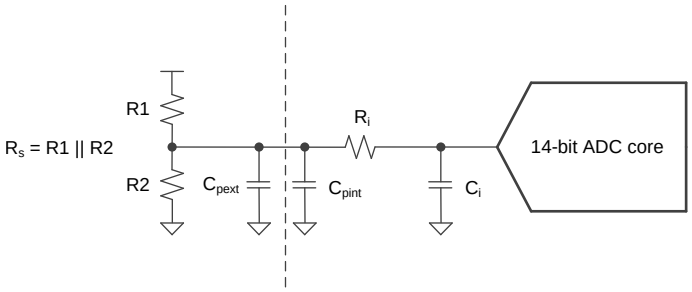


Figure 12. ADC Equivalent Circuit for Sample Time Calculation

Equation 4 is taken from the MSP432P401R, MSP432P401M SimpleLink™ Mixed-Signal Microcontrollers data sheet and is used to calculate the minimum sample time for the given source resistance and capacitance for a 14-bit conversion in Reference 4. There is also a requirement that the sampling time be at least 4 ADC clock cycles. To achieve 1 Msps with 14-bit resolution, the sample-hold time must be set to this minimum value as the remainder of the sample period is consumed with the conversion, (see the *Sample and Conversion Timing* section of the MSP432P4xx SimpleLink™ Microcontrollers Technical Reference Manual).

$$t_{SAMPLE} \geq (n + 1) \times \ln[2] \times \left[(R_s + R_i) \times C_i + R_s \times (C_{pext} + C_{pint})\right] \quad \text{where, } R_s < 100\ k\Omega \tag{4}$$

$$f_{Antialias} = \frac{1}{(2 \times \pi \times R_S \times C_{pext})} \tag{5}$$

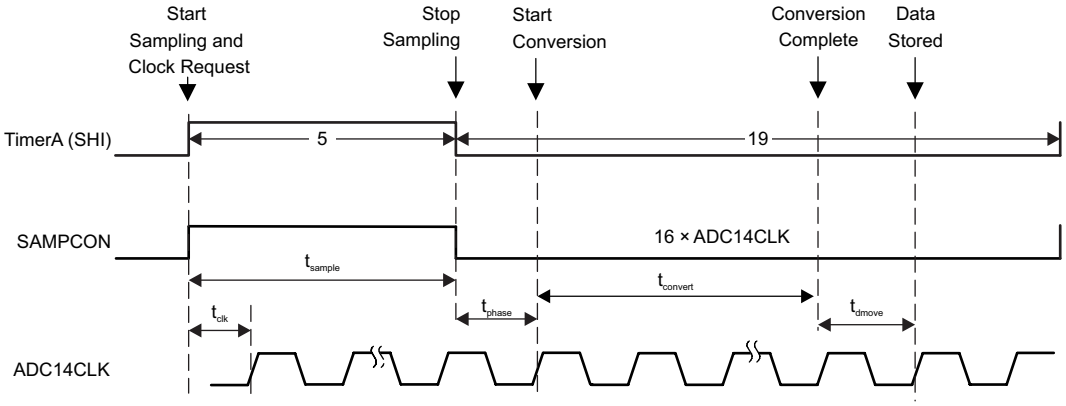
Table 4. Sample Time vs Impedance

R_s (Ω)	C_{pext} (nF)[1]	Device Dependent[2]			Minimum t_{Sample} (µs)	Number of ADCCLK Cycles When ADCCLK = 24 MHz
		C_{pint} (pF)	R_i (Ω)	C_I (pF)		
100k	0.15	5	1000	15	174	4170 (4170)
10k	0.15				17.4	417 (417)
1k	0.15				1.75	43 (42.1)
100	0.1				0.138	4 (3.32)

(1) Some design guides recommend using a capacitance of 20 times the sample-and-hold capacitance of the ADC when designing the drive circuit (see the ADS7056 Ultra-Low Power, Ultra-Small Size, 14-Bit, High-Speed SAR ADC data sheet).
(2) See the MSP432P401R, MSP432P401M SimpleLink™ Mixed-Signal Microcontrollers data sheet.

An ADC sample timer is provided in the precision ADC to allow for easy configuration of the sample-time as a function of the ADC timer. As a minimum, the sample-and-hold time, should be four ADC clock cycles which is the minimum and default setting for the sample timer. This timer can be programmed in multiples of the ADC clock (4,8,16,32,64, etc). Using the sample timer is referred to as pulse sample mode in the TRM. Pulse sample mode yields both the fastest and slowest sampling rates depending upon if the ADC is triggered automatically or manually. In the manual trigger mode (triggered from software or a timer), the overhead associated with synchronizing the trigger and the ADC clock can reduce the maximum sample rate to 700 ksps, while in auto-mode, the conversions are started immediately following completion of the previous and requiring no synchronization. This enables signaling rates of approximately 1.1 Msps.

The pulse sample timer can be disabled. This is referred to as extended pulse sample mode in the TRM. In the extended pulse sample mode, the sample-and-hold time is a function of the delay between trigger source edges. This is typically accomplished with a timer PWM where the duty cycle of the timer determines the sample and hold time, and the period determines the sampling rate. So for example, with a 1-Msps data acquisition, the timer would have a period of 24 clock cycles (1) , and a duty cycle of 5(19) clocks.



Note: If internal ADC reference buffers are used, the SHI signal is gated while ADC14RDYIFG = 0.

Figure 13. Extended Sample Mode

(1) Timer period is +1 so a value of 23 in CCR0 would result in a period of 24 timer clocks. 24 MHz is the maximum peripheral frequency and provides the most resolution in controlling the ADC trigger. 5 clocks are provided to the ADC for the sample and hold to maximize the use of the time. This could be reduced to 4.

Importing Software in Code Composer Studio™ IDE

The code provided with this application report utilizes the MSP432 driver library, which is part of the software development kit (SDK).

B.1 Downloading the Latest SDK

The SDK and quick start guide are available at the following links:

- SimpleLink MSP432 SDK
- Quick start guide for SimpleLink MSP432P4 SDK

  This quick start guide includes additional information for downloading CCS.

B.2 Importing into CCS

CCS provides an import function which recognizes the .projectSpec file found in the download. Follow the same instructions found in the Quick Start Guide:

1. Open CCS.
2. Choose Project → Import CCS project for the menu.
3. Browse to the installed directory.

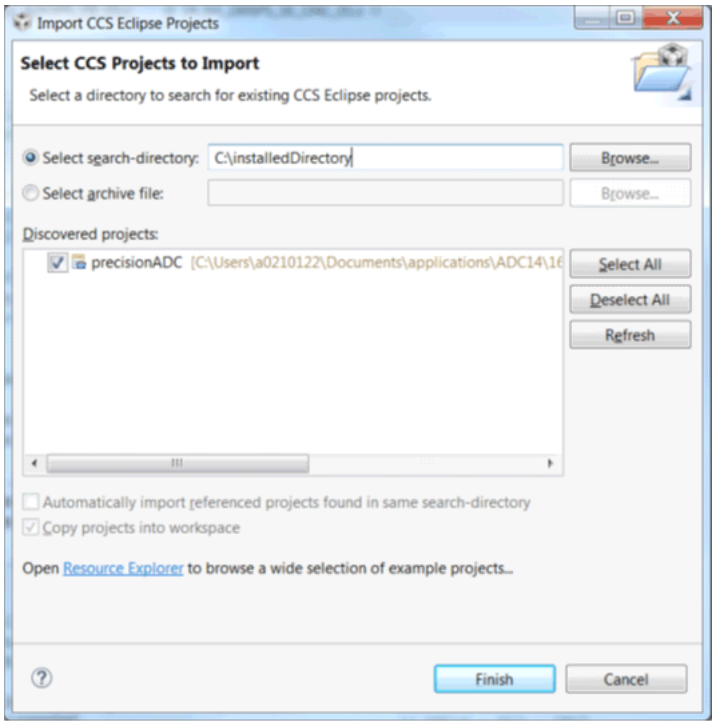


Figure 14. CCS Project Import Window

Source files are provided for the various examples; however, only one source is included in the build at a time.

IMPORTANT NOTICE FOR TI DESIGN INFORMATION AND RESOURCES

Texas Instruments Incorporated ('TI") technical, application or other design advice, services or information, including, but not limited to, reference designs and materials relating to evaluation modules, (collectively, "TI Resources") are intended to assist designers who are developing applications that incorporate TI products; by downloading, accessing or using any particular TI Resource in any way, you (individually or, if you are acting on behalf of a company, your company) agree to use it solely for this purpose and subject to the terms of this Notice.

TI's provision of TI Resources does not expand or otherwise alter TI's applicable published warranties or warranty disclaimers for TI products, and no additional obligations or liabilities arise from TI providing such TI Resources. TI reserves the right to make corrections, enhancements, improvements and other changes to its TI Resources.

You understand and agree that you remain responsible for using your independent analysis, evaluation and judgment in designing your applications and that you have full and exclusive responsibility to assure the safety of your applications and compliance of your applications (and of all TI products used in or for your applications) with all applicable regulations, laws and other applicable requirements. You represent that, with respect to your applications, you have all the necessary expertise to create and implement safeguards that (1) anticipate dangerous consequences of failures, (2) monitor failures and their consequences, and (3) lessen the likelihood of failures that might cause harm and take appropriate actions. You agree that prior to using or distributing any applications that include TI products, you will thoroughly test such applications and the functionality of such TI products as used in such applications. TI has not conducted any testing other than that specifically described in the published documentation for a particular TI Resource.

You are authorized to use, copy and modify any individual TI Resource only in connection with the development of applications that include the TI product(s) identified in such TI Resource. NO OTHER LICENSE, EXPRESS OR IMPLIED, BY ESTOPPEL OR OTHERWISE TO ANY OTHER TI INTELLECTUAL PROPERTY RIGHT, AND NO LICENSE TO ANY TECHNOLOGY OR INTELLECTUAL PROPERTY RIGHT OF TI OR ANY THIRD PARTY IS GRANTED HEREIN, including but not limited to any patent right, copyright, mask work right, or other intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information regarding or referencing third-party products or services does not constitute a license to use such products or services, or a warranty or endorsement thereof. Use of TI Resources may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

TI RESOURCES ARE PROVIDED "AS IS" AND WITH ALL FAULTS. TI DISCLAIMS ALL OTHER WARRANTIES OR REPRESENTATIONS, EXPRESS OR IMPLIED, REGARDING TI RESOURCES OR USE THEREOF, INCLUDING BUT NOT LIMITED TO ACCURACY OR COMPLETENESS, TITLE, ANY EPIDEMIC FAILURE WARRANTY AND ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, AND NON-INFRINGEMENT OF ANY THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

TI SHALL NOT BE LIABLE FOR AND SHALL NOT DEFEND OR INDEMNIFY YOU AGAINST ANY CLAIM, INCLUDING BUT NOT LIMITED TO ANY INFRINGEMENT CLAIM THAT RELATES TO OR IS BASED ON ANY COMBINATION OF PRODUCTS EVEN IF DESCRIBED IN TI RESOURCES OR OTHERWISE. IN NO EVENT SHALL TI BE LIABLE FOR ANY ACTUAL, DIRECT, SPECIAL, COLLATERAL, INDIRECT, PUNITIVE, INCIDENTAL, CONSEQUENTIAL OR EXEMPLARY DAMAGES IN CONNECTION WITH OR ARISING OUT OF TI RESOURCES OR USE THEREOF, AND REGARDLESS OF WHETHER TI HAS BEEN ADVISED OF THE POSSIBILITY OF SUCH DAMAGES.

You agree to fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of your non-compliance with the terms and provisions of this Notice.

This Notice applies to TI Resources. Additional terms apply to the use and purchase of certain types of materials, TI products and services. These include; without limitation, TI's standard terms for semiconductor products http://www.ti.com/sc/docs/stdterms.htm), evaluation modules, and samples (http://www.ti.com/sc/docs/sampterms.htm).

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265