How Far, How Fast Can You Operate M-LVDS Transceivers?

Multipoint Low Voltage Differential Signaling (M-LVDS) devices give LVDS benefits to the multipoint data transmission world. In a multipoint configuration, transmitters/drivers and receivers are interconnected on a single transmission line. The line is doubly terminated on both ends with matching impedance (usually 100Ω), see Figure 1. This technical note shows the performance in maximum data rates and distances connecting M-LVDS transceivers.

The test setup shown in Figure 2 connects a pseudo-random binary sequence (PRBS) source with two M-LVDS Evaluation Module (EVM) Boards to an oscilloscope. The three parts that use the half duplex configuration in Figure 4 are: SN65MLVD201, SN65MLVD206, and the SN65MLVD206B. The test set up for the full duplex configuration of the SN65MLVD207 is shown in Figure 2. The tests were conducted at the following cable lengths: 1m, 5m, 10m, 50m, and 100m; and each Cat-5e cable was modified with female headers to connect to the male headers on the EVM boards. A Bit Error Rate Tester (BERT) generates a $2^{31} - 1$ PRBS pattern, it is sent to the system and loops back to the analyzer, which compares to the generated signal. If the pattern matches, the system is said to have no errors. The error margin to not be surpassed in this lab experiment was $1 \times 10^{-12}$ for the bit error rate.

Figure 1. Multipoint Typical Application

The signal passing through the driver and receiver is connected to an oscilloscope to be observed as an eye diagram. Eye diagrams are made when a signal is repeatedly sampled over itself and is used to measure jitter. Jitter is the measured “error” in time difference of when a system cannot tell the difference between a high or a low bit. It is measured at the crossing point of the bits in an eye diagram as shown in Figure 3.

Figure 3. Eye Diagram

Jitter percentage is valuable when seeing what percentage of the eye will be open, providing a window of bit time to correctly sample the signal. To better understand jitter, Figure 5 shows examples of what 5%, 10%, 20% jitter. Up to 20% jitter, the signal should be clean enough to get readings with no errors. Above 20% it is not ensured that the signal is error free; however, higher jitter percentages were shown to be below the error margin of $1 \times 10^{-12}$ bit error rate using the BERT.

Figure 2. Full Duplex M-LVDS Test Setup

Figure 4. Half Duplex M-LVDS Test Setup
All of the parts chosen for this experiment (SN65MLVD201, SN65MLVD206, SN65MLVD206B, SN65MLVD207) have data sheet specifications of being able to achieve signaling rates up to 200 Mbps. As you can see, in Figure 6, Figure 7, and Figure 8, all devices meet and exceed the specified up to 200 Mbps signaling rates from the data sheets.

**Figure 6. SN65MLVD201 Results**

SN65MLVD201 operates up to 300 Mbps at short distances, 100 Mbps above what is specified on the data sheet. At a longer distance of 50m, the SN65MLVD201 is able to function up to 50 Mbps.

**Figure 7. SN65MLVD206**

SN65MLVD206 operates up to 450 Mbps at short distances, 250 Mbps above what is specified on the data sheet. The limitation of M-LVDS standard is 500 Mbps. At a longer distance of 50m, the SN65MLVD206 is able to function up to 50 Mbps.

**Figure 8. SN65MLVD206B**

SN65MLVD206B operates up to 300 Mbps at short distances, 100 Mbps above what is specified on the data sheet up to 10m.

**Figure 9. SN65MLVD207**

SN65MLVD207 performed above the 200 Mbps at short distances, and in longer distances like 5m it could handle a data rate of 60 Mbps.

### Table 1. Final Results

<table>
<thead>
<tr>
<th>Jitter</th>
<th>5%</th>
<th>10%</th>
<th>20%</th>
<th>Max Below Error Margin</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>EVM</td>
<td>201</td>
<td>206</td>
<td>206B</td>
</tr>
<tr>
<td>1m</td>
<td>90</td>
<td>140</td>
<td>75</td>
<td>90</td>
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<tr>
<td>50m</td>
<td>15</td>
<td>9</td>
<td>7</td>
<td>11</td>
</tr>
<tr>
<td>100m</td>
<td>4</td>
<td>3</td>
<td>2</td>
<td>3</td>
</tr>
</tbody>
</table>

(1) All data values are in Mbps.

(2) '201' is representative of the SN65MLVD201; '206' is representative of the SN65MLVD206; '206B' is representative of the SN65MLVD206B; '207' is representative of the SN65MLVD207
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