Programmable low-side current sink circuit

Garrett Satterfield

Design Goals

<table>
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<tr>
<th>VCC</th>
<th>DAC Output Voltage</th>
<th>Output Current</th>
<th>Error</th>
<th>Maximum Resistive Load</th>
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<tr>
<td>5V</td>
<td>0mV – 510mV</td>
<td>0mA – 100mA</td>
<td>&lt;0.25% FSR</td>
<td>44.9Ω</td>
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Design Description

The programmable low-side current sink sets the current through a load based on the DAC output voltage. The current is sensed through $R_{\text{SET}}$ and the op amp biases a transistor regulate the current through the load. Components $C_F$, $R_{\text{ISO}}$, and $R_{\text{FB}}$ provide compensation to ensure stability of the circuit.

Design Notes

1. Choose a DAC with low offset error, gain error, and drift. RRIO op amps should be used to reduce error near the rails and maximize resistive load drive. An op amp with low offset voltage should be chosen to minimize error.
2. Use a high-precision, low-drift resistor for $R_{\text{SET}}$ for accurate current regulation.
3. $R_{\text{SET}}$ should be minimized for efficiency and power dissipation. Most of the power dissipation should occur through $R_{\text{LOAD}}$.
4. To drive large $R_{\text{LOAD}}$, a separate high voltage supply may be used for driving the current to the load.
Design Steps

1. Calculate the $R_{SET}$ value for the maximum DAC output voltage and desired maximum output current.
\[
R_{SET} = \frac{V_{DAC,\text{max}}}{I_{OUT,\text{max}}} = \frac{510\text{mV}}{100\text{mA}} = 5.1\Omega
\]

2. The maximum resistive load is given by:
\[
R_{LOAD,\text{max}} = \frac{V_{cc} - I_{SET,\text{max}} R_{SET}}{I_{SET,\text{max}}} = \frac{5V - 100\text{mA} \times 5.1}{100\text{mA}} = 44.9\Omega
\]

3. Ensure Q1 is rated for the power dissipation at maximum current.
\[
P_{\text{Diss,Q2}} = V_{cc} \times I_{SET,\text{max}} - I_{SET,\text{max}}^2 \times (R_{LOAD} + R_{SET}) = 5V \times 100\text{mA} - 100\text{mA}^2 \times (25\Omega + 5.1\Omega) = 0.2W
\]

4. The output error can be approximated based on DAC TUE, amplifier offset voltage, resistor tolerance, and reference initial accuracy using root sum square (RSS) analysis.
\[
\text{Output TUE(%FSR)} = \sqrt{TUE_{DAC}^2 + \left(\frac{V_{OS,\text{Amplifier}}}{FSR} \times 100\right)^2 + TOL_{\text{SET}}^2 + \text{Accuracy}_{\text{Ref}}^2} = \sqrt{0.1^2 + \left(\frac{0.3\text{mV}}{510\text{mV}} \times 100\right)^2 + 0.1^2 + 0.1^2} = 0.183\% \text{ FSR}
\]
AC Loop Gain Analysis

Gain (dB)

Phase [deg]

Phase margin: 63.77 at frequency (Hz): 6.30MEG

Gain (dB)

Phase [deg]

Frequency (Hz)

10 100 1k 10k 100k 1MEG 10MEG 100MEG

Phase margin: 63.77 at frequency (Hz): 6.30MEG
## Devices

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<td><strong>DACs</strong></td>
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<tr>
<td>DAC8830</td>
<td>16-bit resolution, single channel, ultra-low power, unbuffered output, 1 LSB INL, SPI, 2.7-V to 5.5-V supply</td>
<td><a href="http://www.ti.com/product/DAC8830">http://www.ti.com/product/DAC8830</a></td>
<td><a href="http://www.ti.com/pdacs">http://www.ti.com/pdacs</a></td>
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<td><strong>Amplifiers</strong></td>
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<td>TLV9061</td>
<td>Ultra-Small, 0.3-mV Offset, Rail-to-Rail I/O, 1.8-V to 5.5-V supply</td>
<td><a href="http://www.ti.com/product/TLV9061">http://www.ti.com/product/TLV9061</a></td>
<td><a href="http://www.ti.com/opamps">http://www.ti.com/opamps</a></td>
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### Design References

See [Analog Engineer's Circuit Cookbooks](http://www.ti.com) for TI's comprehensive circuit library.

### Links to Key Files

- **TI Precision Labs - Op Amps: Stability 6**

### For direct support from TI Engineers use the E2E community

- [e2e.ti.com](http://e2e.ti.com)

### Other Links

- **Precision DAC Learning Center**
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