Programmable low-side current sink circuit

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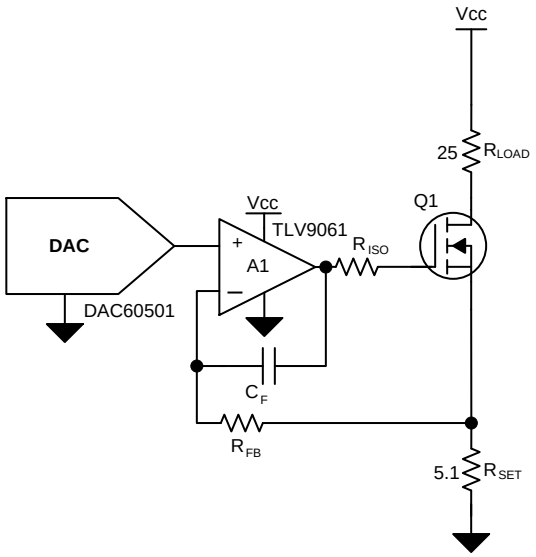
Design Goals

VCC	DAC Output Voltage	Output Current	Error	Maximum Resistive Load
5V	0mV – 510mV	0mA – 100mA	<0.25% FSR	44.9Ω

Design Description

The programmable low-side current sink sets the current through a load based on the DAC output voltage. The current is sensed through R_{SET} and the op amp biases a transistor regulate the current through the load. Components C_F, R_{ISO}, and R_{FB} provide compensation to ensure stability of the circuit.



Design Notes

1. Choose a DAC with low offset error, gain error, and drift. RRIO op amps should be used to reduce error near the rails and maximize resistive load drive. An op amp with low offset voltage should be chosen to minimize error.
2. Use a high-precision, low-drift resistor for R_{SET} for accurate current regulation.
3. R_{SET} should be minimized for efficiency and power dissipation. Most of the power dissipation should occur through R_{LOAD}
4. To drive large R_{LOAD}, a separate high voltage supply may be used for driving the current to the load.

Design Steps

1. Calculate the R_{SET} value for the maximum DAC output voltage and desired maximum output current.

$$R_{SET} = \frac{V_{DAC,max}}{I_{OUT,max}} = \frac{510mV}{100mA} = 5.1\Omega$$

2. The maximum resistive load is given by:

$$R_{LOAD,max} = \frac{Vcc - I_{SET,max}R_{SET}}{I_{SET,max}} = \frac{5V - 100mA \times 5.1}{100mA} = 44.9\Omega$$

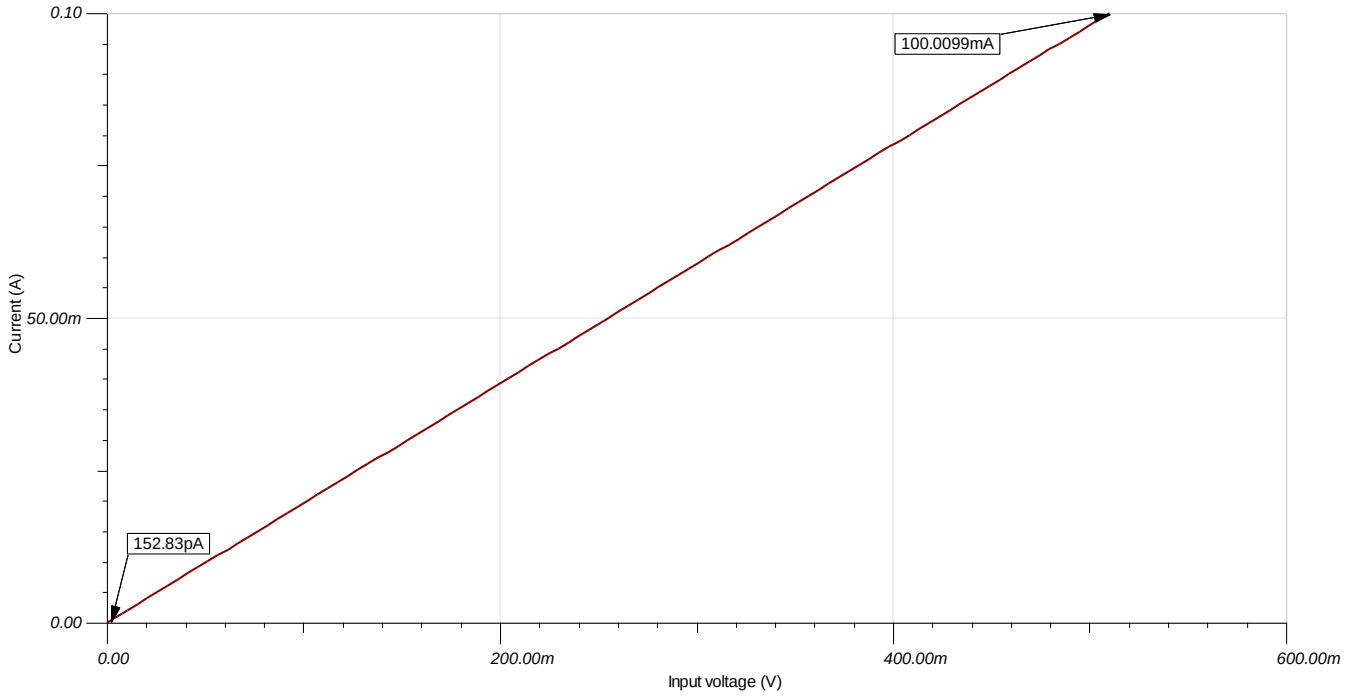
3. Ensure Q1 is rated for the power dissipation at maximum current.

$$P_{Diss,Q2} = Vcc \times I_{SET,max} - I_{SET,max}{}^2 \times (R_{LOAD} + R_{SET}) = 5V \times 100mA - 100mA^2 \times (25\Omega + 5.1\Omega) = 0.2W$$

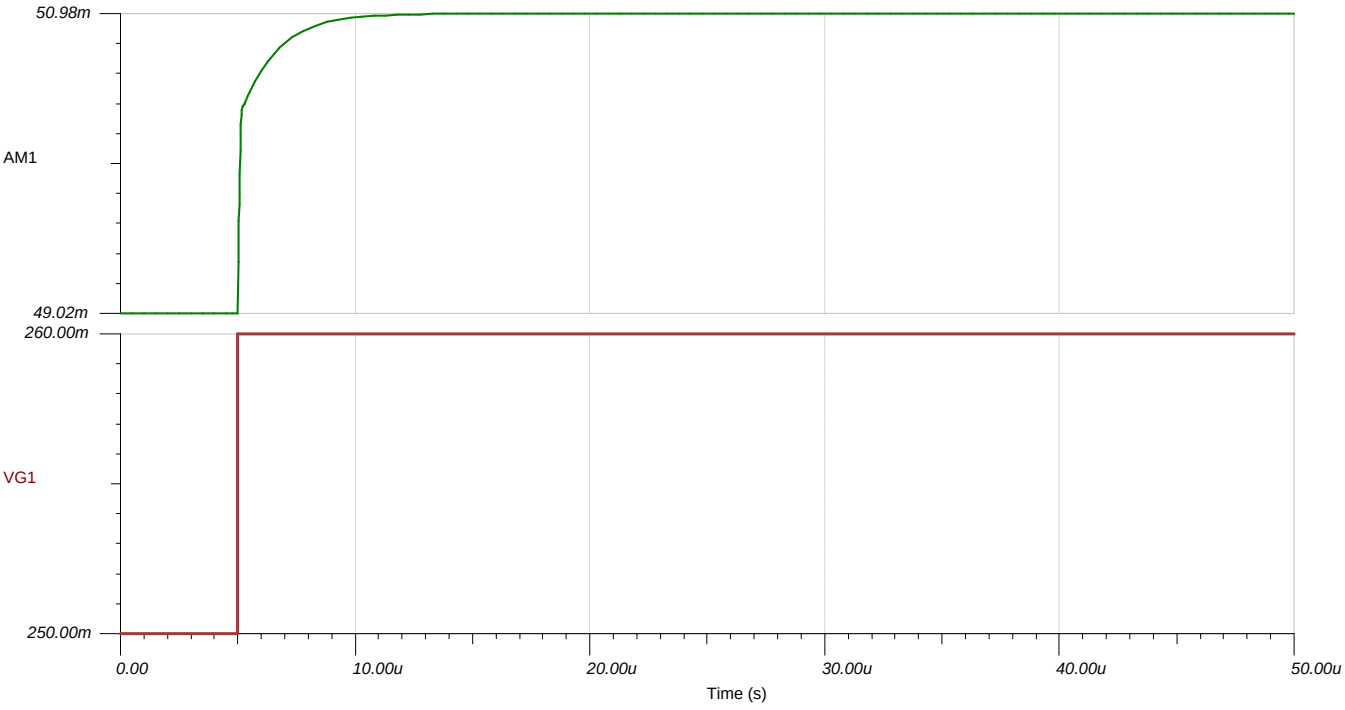
4. The output error can be approximated based on DAC TUE, amplifier offset voltage, resistor tolerance, and reference initial accuracy using root sum square (RSS) analysis.

$$\text{Output TUE(\%FSR)} = \sqrt{TUE_{DAC}^2 + \left(\frac{V_{OS,Amplifier}}{FSR} \times 100\right)^2 + Tol_{R_{SET}}^2 + Accuracy_{Ref}^2} = \sqrt{0.1^2 + \left(\frac{0.3mV}{510mV} \times 100\right)^2 + 0.1^2 + 0.1^2} = 0.183\% \text{ FSR}$$

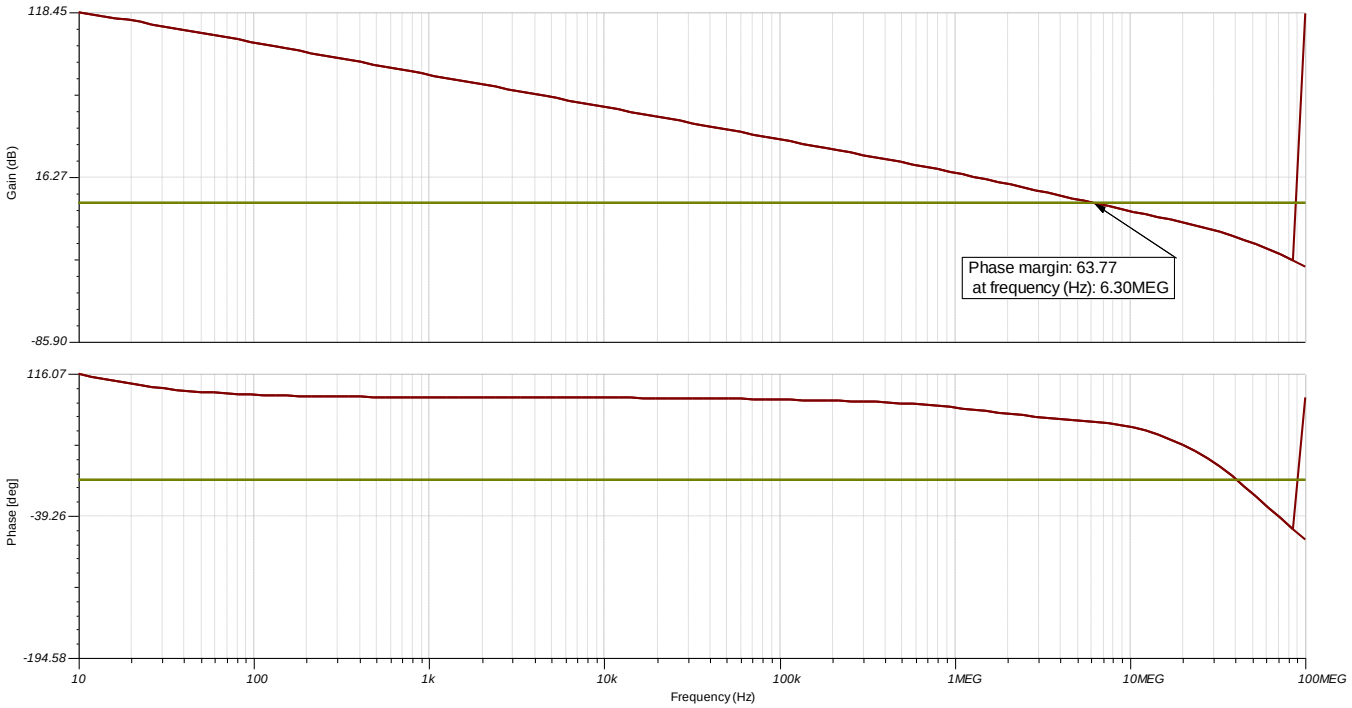
DC Transfer Characteristic



Small Signal Step Response



AC Loop Gain Analysis



Devices

Device	Key Features	Link	Other Possible Devices
DACs			
DAC60501	12-bit resolution, 1LSB INL, Single-Channel, Voltage Output DAC with 5 ppm/°C Internal Reference	http://www.ti.com/product/DAC60501	http://www.ti.com/pdacs
DAC80501	16-bit resolution, 1LSB INL, Single-Channel, Voltage Output DAC with 5 ppm/°C Internal Reference	http://www.ti.com/product/DAC80501	http://www.ti.com/pdacs
DAC8830	16-bit resolution, single channel, ultra-low power, unbuffered output, 1 LSB INL, SPI, 2.7-V to 5.5-V supply	http://www.ti.com/product/DAC8830	http://www.ti.com/pdacs
Amplifiers			
TLV9061	Ultra-Small, 0.3-mV Offset, Rail-to-Rail I/O, 1.8-V to 5.5-V supply	http://www.ti.com/product/TLV9061	http://www.ti.com/opamps
OPA317	Zero-Drift, Low-Offset, Rail-to-Rail I/O, 35-µA supply current max, 2.5-V to 5.5-V supply	http://www.ti.com/product/OPA317	http://www.ti.com/opamps
OPA388	Precision, Zero-Drift, Zero-Crossover, Low Noise Rail-to-Rail I/O, 2.5-V to 5.5-V supply	http://www.ti.com/product/OPA388	http://www.ti.com/opamps

Design References

See *Analog Engineer's Circuit Cookbooks* for TI's comprehensive circuit library.

Links to Key Files

Source Files for *Low-Side Current Sink* – http://www.ti.com/lit/zip/slac784.

TI Precision Labs - Op Amps: Stability 6

For direct support from TI Engineers use the E2E community

e2e.ti.com

Other Links

Precision DAC Learning Center

http://www.ti.com/data-converters/dac-circuit/precision/overview.html

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