Application Report

Applications of Logic and Translation in IP Cameras

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ABSTRACT

Logic and translation devices can be found in the majority of electronic systems. IP Cameras integrate numerous subsystems together that often require additional signal interfacing, such as when the image capture sensor needs to operate at a different voltage than the system controller and translation must be used for the serialized image data, or when a button requires a hardware debounce circuit. All of the use cases shown in the *Block Diagram* and *Logic and Translation Use Cases* sections of this document are commonly seen in IP Camera designs.

Logic gates, voltage translators, and other logic devices are utilized for many purposes throughout modern electronic systems. This document provides example solutions for common design challenges that can be solved using logic and translation. Not all of the solutions here appear in every system, however all solutions shown are commonly used and effective.

There are dozens of logic families available from Texas Instruments, and it can be difficult to select the right one for the application. IP Cameras are generally very small, and prefer low power solutions, which makes it easier to identify an appropriate family for this application. Refer to *Recommended Logic and Translation Families for IP Cameras* in this document for help finding the right logic family for your use case.

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Trademarks

1 Block Diagram

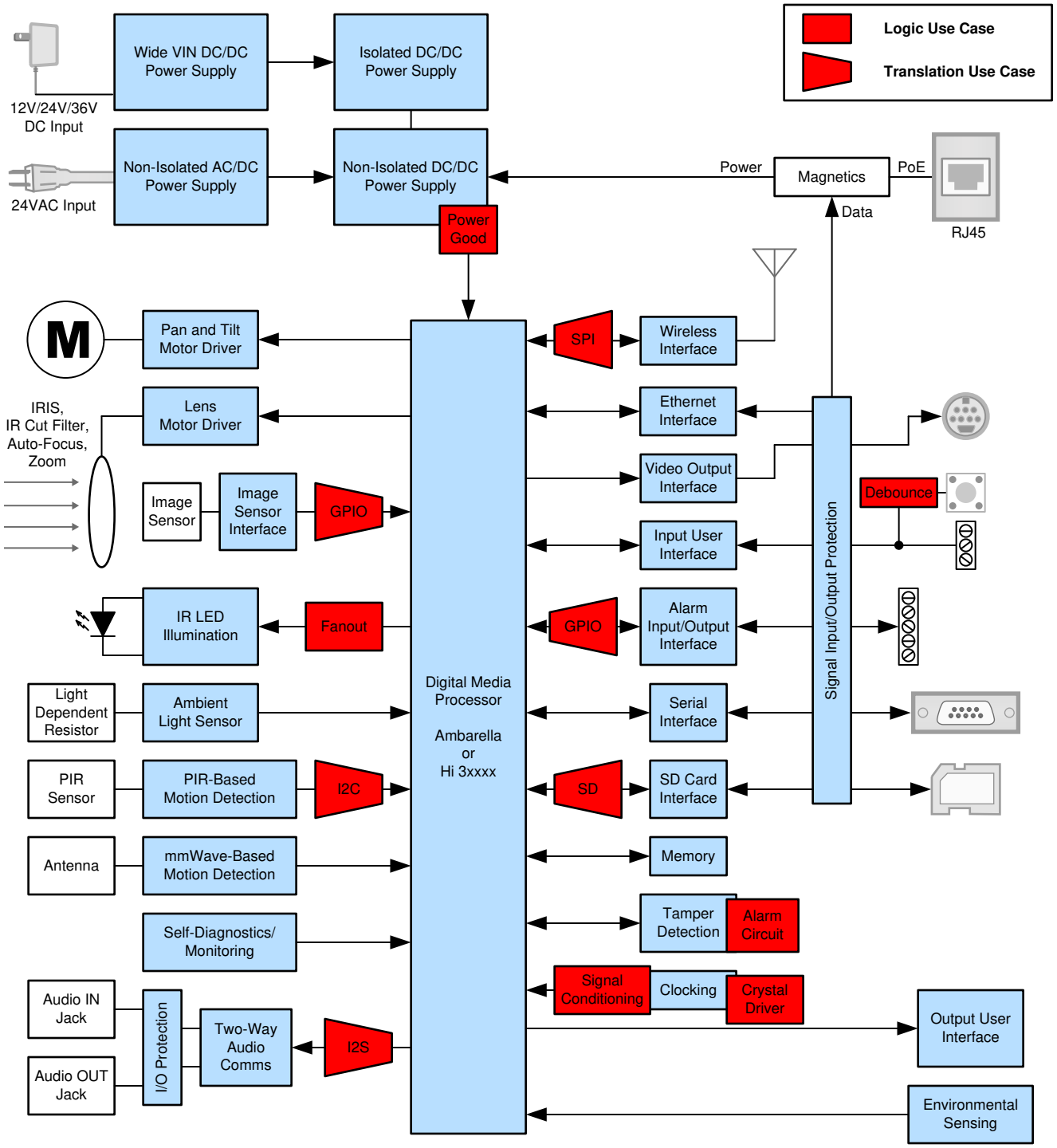

Figure 1-1. Simplified Block Diagram for IP Cameras

See the interactive online *End Equipment Reference Diagram* for a more complete view.

2 Logic and Translation Use Cases

2.1 Logic Use Cases

2.1.1 Combine Power Good Signals

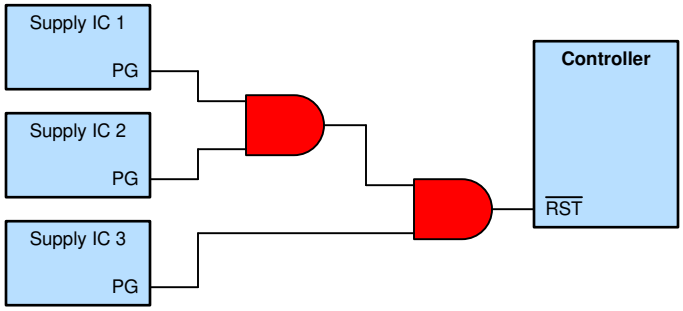

Figure 2-1. Using Logic to Combine Multiple Power-Good Signals

- Add system indicators without software or system controller interaction
- Most logic gates can drive low current indicator LEDs (1 mA to 25 mA)
- Logic functions add configurability
- See more about this use case in the Logic Minute video *Combining Power Good Signals*
- Find the right AND gate through the *online parametric search tool*

2.1.2 Debounce Switches and Buttons

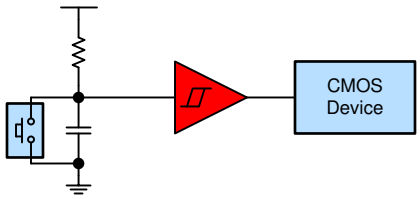

Figure 2-2. Using Logic to Prevent Multiple Triggers of a CMOS Input Due to Switch Bounce

- Prevents multiple triggers of CMOS inputs due to switch bounce
- Works when the system controller is asleep
- Works without a system controller
- Reduces controller code complexity, no software debounce required
- See more about this use case in the Logic Minute video *Debounce a Switch*
- Find the right Schmitt-trigger buffer through the *online parametric search tool*

2.1.3 Fanout Signals to Multiple Receivers

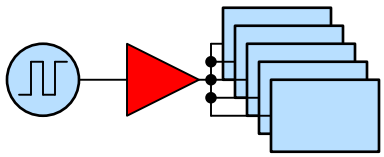

Figure 2-3. Using Logic to Redrive a Signal Into Multiple Receiving Devices.

- Most logic gates can drive 8+ CMOS inputs
- Reduce loading on key components
- Ensure clean clock signals reach all system components
- Find the right buffer/driver through the *online parametric search tool*

2.1.4 Latching Alarm Circuit with Reset

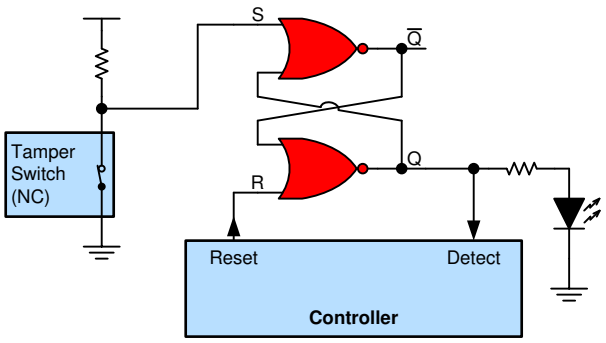

Figure 2-4. Using Logic to Monitor a Normally Closed (NC) Tamper Switch

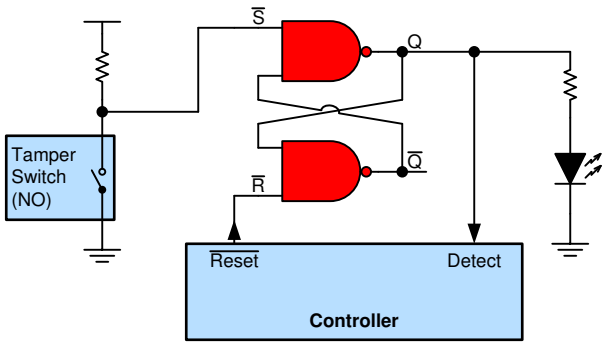

Figure 2-5. Using Logic to Monitor a Normally Open (NO) Tamper Switch

- Flags any tampering
- Extremely low power
- Works while the controller sleeps
- Can be used without a controller
- See more about this use case in the Logic Minute video *Using an S-R Latch in Alarm Circuitry*
- Find the right NOR or NAND gate through the *online parametric search tool*

2.1.5 Generate a Clock Signal from a Crystal Oscillator

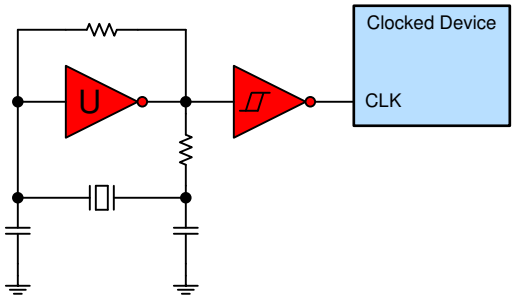

Figure 2-6. Using an Unbuffered Inverter and Schmitt-trigger Inverter to Generate a Clock Signal From a Crystal Oscillator

- Drive crystal oscillators directly
- Can be disabled with added logic
- Allows for selectable system clocks with multiple crystals
- Outputs a clean and reliable square wave
- See more about this use case in the application report *Use of the CMOS Unbuffered Inverter in Oscillator Circuits*
- Find the right inverter through the *online parametric search tool*

2.1.6 Condition Digital Signals

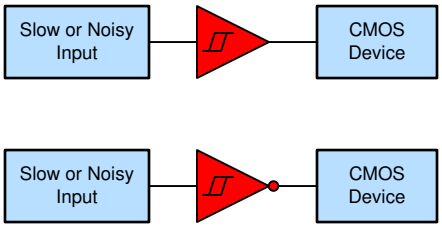

Figure 2-7. Using Schmitt-Trigger Drivers to Remove Noise or Slow Edges from Digital Signals

- Removes moderate noise from digital signals
- Prevents multiple switching events for CMOS inputs
- Speeds up slow input edges to meet input transition rate requirements
- See more about this use case in the Logic Minute video *Eliminate Slow or Noisy Input Signals*
- Find the right Schmitt-trigger buffer or inverter through the *online parametric search tool*

2.2 Voltage Translation Use Cases

2.2.1 SPI Communication

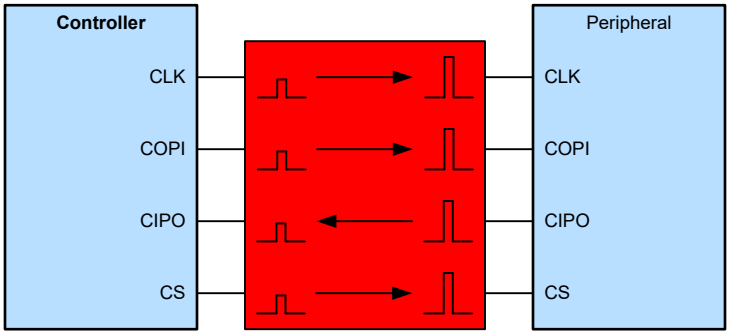

Figure 2-8. Using Voltage Translation with a SPI-communication Bus

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Provides protection from disconnected peripherals
- Find the right voltage level translator through the *online parametric search tool*

2.2.2 GPIO Communication

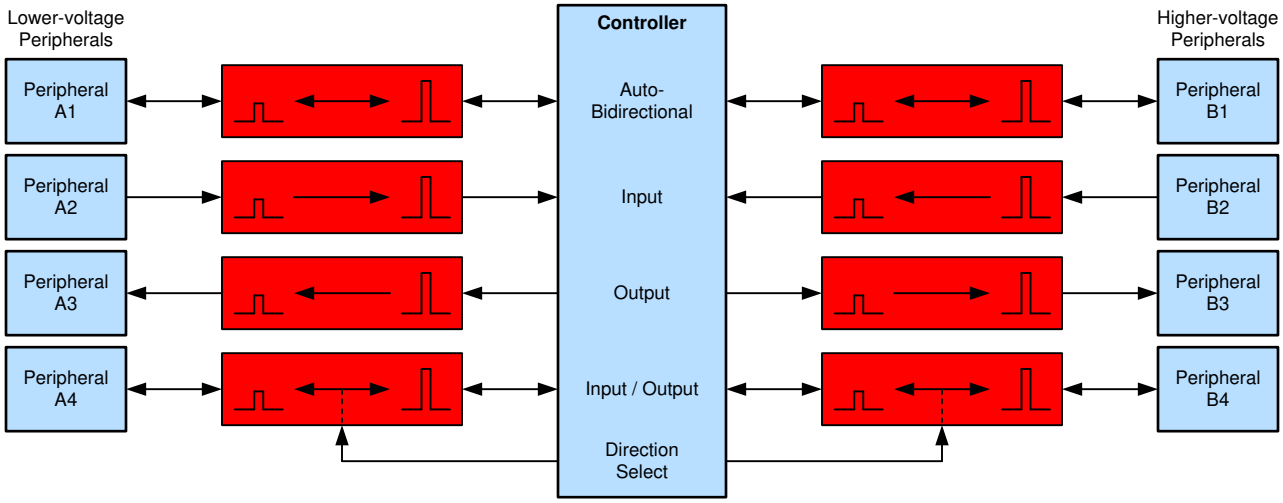

Figure 2-9. Using Voltage Translation with GPIO Communications

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Provides protection from disconnected peripherals
- Find the right voltage level translator through the *online parametric search tool*

2.2.3 I²C Communication

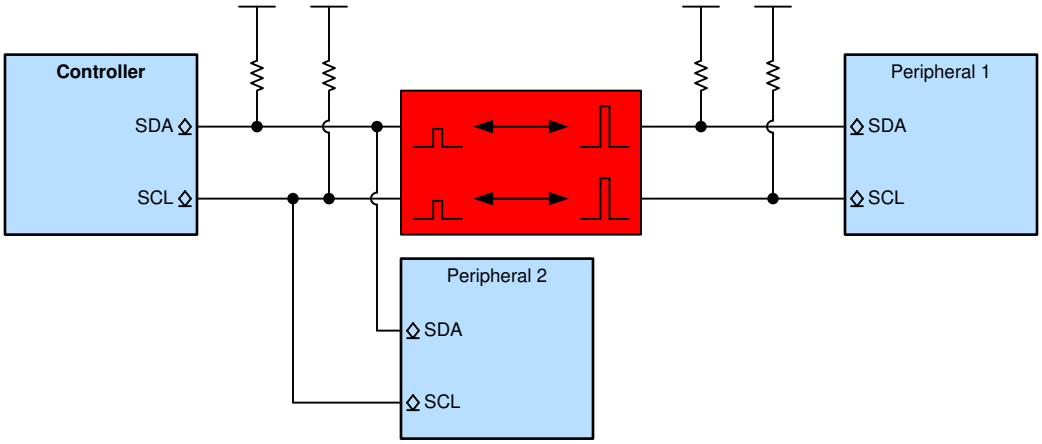

Figure 2-10. Using Voltage Translation with an I² Communication Bus

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Find the right voltage level translator through the *online parametric search tool*

2.2.4 SD Card Communication

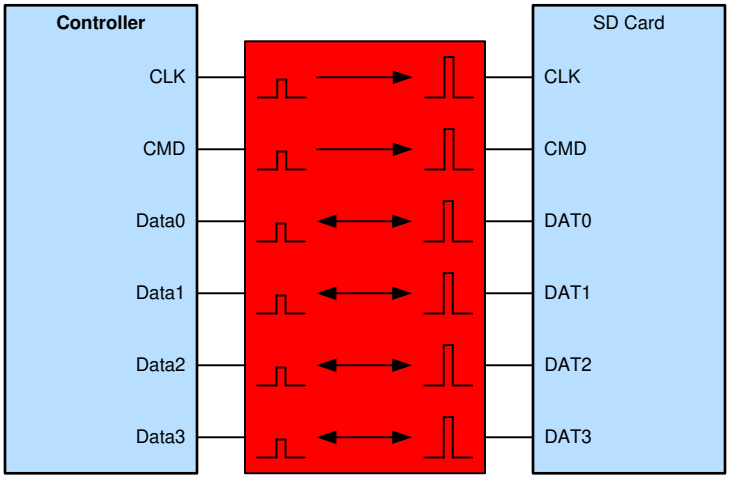

Figure 2-11. Using Voltage Translation with an SD Card Communication Bus

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while SD Card is not connected
- Find the right voltage level translator through the *online parametric search tool*

2.2.5 I2S Communication

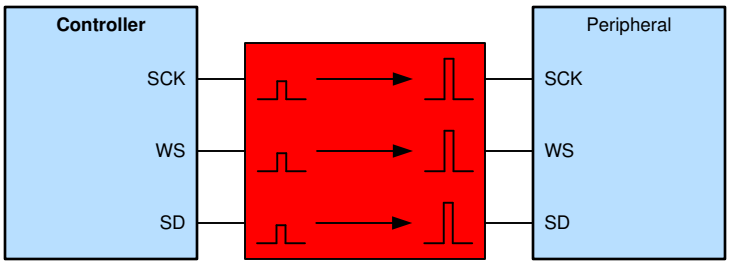

Figure 2-12. Using Voltage Translation with an I2S Communication Bus

- Enable communication when devices have mismatched logic voltage levels
- Prevent damage to devices that cannot support higher voltage inputs
- Improve data rates over discrete translation solutions
- Protect controller while peripheral is not connected
- Find the right voltage level translator through the *online parametric search tool*

3 Recommended Logic and Translation Families for IP Cameras

3.1 AUP: Advanced Ultra-Low-Power CMOS Logic and Translation

Key Features: SN74**AUPxG**xxxx

- Low static-/dynamic-power consumption
- Wide V_{CC} operating range: 0.8 V to 3.6 V
- Input hysteresis allows for slow input transition rate
- Best in class for speed-power optimization
- I_{off} specification for partial power down support
- Packaging Options: DSBGA, SC70, SM8, SON, SOT-23, SOT, UQFN, US8, and X2SON

Key Features: SN74**AUPxT**xxxx

- Low static-/dynamic-power consumption
- 1.65-V to 3.6-V translation range
- Best in class for speed-power optimization
- I_{off} specification for partial power down support

Find the right AUP family logic and voltage level translation devices through the *online parametric search tool*

3.2 AXC: Advanced eXtremely Low-Voltage CMOS Translation

Key Features

- Up and Down Translation Across 0.65 V to 3.6 V
- Designed with glitch suppression circuitry to improve power sequencing performance
- Maximum Quiescent Current (I_{CCA} + I_{CCB}) of 6 µA (85°C Maximum) and 14 µA (125°C Maximum)
- Up to 500-Mbps support when translating from 1.8 to 3.3V
- V_{CC} Isolation Feature – If either V_{CC} input is Below 100 mV, all I/Os outputs are disabled and become high impedance
- I_{off} supports partial-power-down mode operation
- Operating Temperature: –40°C to +125°C
- Packaging Options: DSBGA, SC70, SM8, SON, SOT-23, SOT, UQFN, US8, and X2SON

Find the right AXC family voltage level translation devices through the *online parametric search tool*

3.3 LVC: Low-Voltage CMOS Logic and Translation

Key Features: SN74**LVC**xxxx

- Huge portfolio of logic functions
- LVC: 4+ channels per package
- Over-voltage tolerant inputs allow unidirectional down-translation with any function
- High-drive outputs (up to 32 mA)
- Up to 250 Mbps operation
- I_{off} supports partial-power-down mode operation
- Packaging Options: SOIC, TSSOP, VQFN, SOP, and SSOP

Key Features: SN74**LVCxG**xxxx

- Put 1, 2, or 3 channels of any logic function right where you need them
- Configurable gates available ('57, '58, '97, '98, and '99 functions)
- Over-voltage tolerant inputs allow unidirectional down-translation with any gate or buffer
- High-drive outputs (up to 32 mA)
- Up to 250 Mbps operation
- I_{off} supports partial-power-down mode operation
- Packaging Options: SOT-23, SC70, X2SON, SOT-5X3, SON, and DSBGA

Key Features: SN74**LVCxT**xxxx

- LVCxT: Up and Down Translation Across 1.65 V to 5.5 V
- 1, 2, 8, or 16 channels per device
- High-drive outputs (up to 32 mA)
- Up to 250 Mbps operation
- I_{off} supports partial-power-down mode operation

Find the right LVC family logic and voltage level translation devices through the *online parametric search tool*

4 Related Documentation

- Texas Instruments, *Use of the CMOS Unbuffered Inverter in Oscillator Circuits* application report

5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (January 2019) to Revision A (March 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document	2
• Updated SPI terminology for the *Using Voltage Translation with a SPI-communication Bus* figure	5

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