

# Voltage margining and scaling circuit with current output smart DAC



Smart DAC

Katlynn Jones

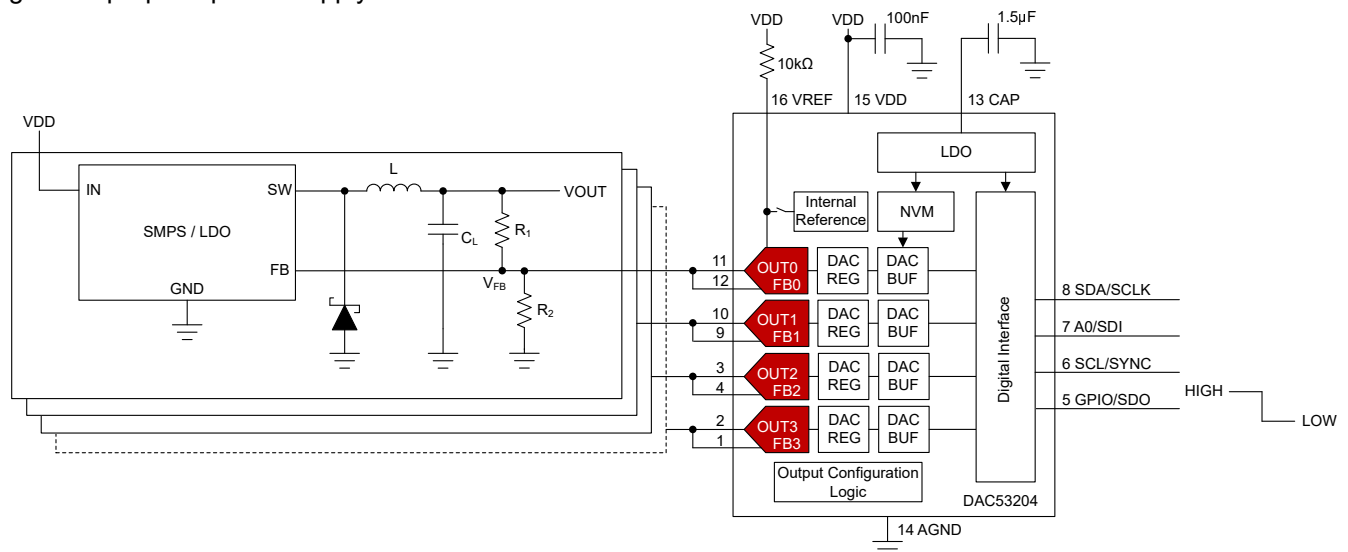
## Design Objective

Key Input Parameter	Key Output Signal	Recommended Device
SPI or I2C communication	$\pm 12\text{-}\mu\text{A}$ analog DAC output, 3.3-V $\pm 10\%$ SMPS output	DAC43204, DAC53204, DAC53004

**Objective:** Provide a margin voltage for an SMPS output of  $\pm 10\%$  the nominal value.

## Design Description

This circuit uses a four-channel buffered current output DAC to voltage margin a switch-mode power supply (SMPS). A voltage margining circuit is used to trim, scale, or test the output of a power converter. Adjustable power supplies, such as low dropout regulators (LDOs), DC/DC converters, or SMPS provide a feedback (FB) input that is used to control the desired output. A precision smart DAC, such as the DAC43204, provides linear control of the power supply output when the DAC is supplied and the output is powered on. Most DACs include an internal pull-down resistor at the voltage output when the DAC is supplied but the output is in power down mode. Also, when most DACs are completely powered off, the ESD cells on the output pin conduct current if the output is pulled away from ground which is the case in voltage margining circuits. The DAC43204 provides a high-impedance (Hi-Z) output when the DAC is powered off or when the output channel is in power down mode, meaning that the DAC draws very little current through the FB pin of the SMPS and the output is set at the nominal voltage. The DAC43204 has a general-purpose input (GPI) pin that allows the DAC output to be toggled between a high- and low-current output. This allows the SMPS to be toggled within  $\pm 10\%$  of the nominal output value. All register settings can be saved using the non-volatile memory (NVM) on the DAC43204 meaning that the device can be used without a processor, even after a power cycle. This circuit can be used in applications such as [communications equipment](#), [enterprise systems](#), [test and measurement](#), and general-purpose power-supply modules.



## Design Notes

- The [DACx3204 12-Bit, 10-Bit, and 8-Bit, Quad Voltage and Current Output Smart DACs With Auto-Detected I2C, PMBus™, or SPI Interface Data Sheet](#) recommends using a 100-nF decoupling capacitor for the VDD pin and a 1.5-μF or greater bypass capacitor for the CAP pin. The CAP pin is connected to the internal LDO. Place these capacitors close to the device pins.
- The nominal voltage of the SMPS is set by resistors R<sub>1</sub> and R<sub>2</sub>. The SMPS uses an internal 600-mV reference voltage at the FB pin to determine the voltage at the output. Calculate R<sub>1</sub> and R<sub>2</sub> using the following equations:

$$R_1 = \frac{V_{NOMINAL} - V_{FB}}{I_{NOMINAL}}$$

$$R_2 = \frac{R_1 \times V_{FB}}{V_{NOMINAL} - V_{FB}}$$

A nominal current of 100μA through R<sub>1</sub> and R<sub>2</sub> and 3.3-V nominal output voltage is used. With these values the equations become:

$$R_1 = \frac{3.3V - 0.6V}{100\mu A} = 27k\Omega$$

$$R_2 = \frac{27k\Omega \times 0.6V}{3.3V - 0.6V} = 6k\Omega$$

- To achieve the desired margin, the DAC43204 must sink or source additional current through R<sub>1</sub>. This current (I<sub>MARGIN</sub>) is calculated by:

$$I_{MARGIN} = \frac{V_{NOMINAL} \times (1 + MARGIN) - V_{FB}}{R_1} - I_{NOMINAL}$$

For a ±10% margin, the equation becomes:

$$I_{MARGIN} = \frac{3.3V \times (1 + 0.10) - 0.6V}{27k\Omega} - 100\mu A = 12\mu A$$

- The DAC codes for ±I<sub>MARGIN</sub> are stored in the DAC-MARGIN-HIGH and DAC-MARGIN-LOW registers. The codes programmed to these registers, in decimal, is calculated using:

$$DAC\_MARGIN\_HIGH = \frac{I_{DAC,MAX} - I_{MIN}}{I_{MAX} - I_{MIN}} \times 256$$

$$DAC\_MARGIN\_LOW = \frac{I_{DAC,MIN} - I_{MIN}}{I_{MAX} - I_{MIN}} \times 256$$

Using an I<sub>OUT</sub> range of ±25μA, the equation becomes:

$$DAC\_MARGIN\_HIGH = \frac{12\mu A - (-25\mu A)}{25\mu A - (-25\mu A)} \times 256 = 189.44d$$

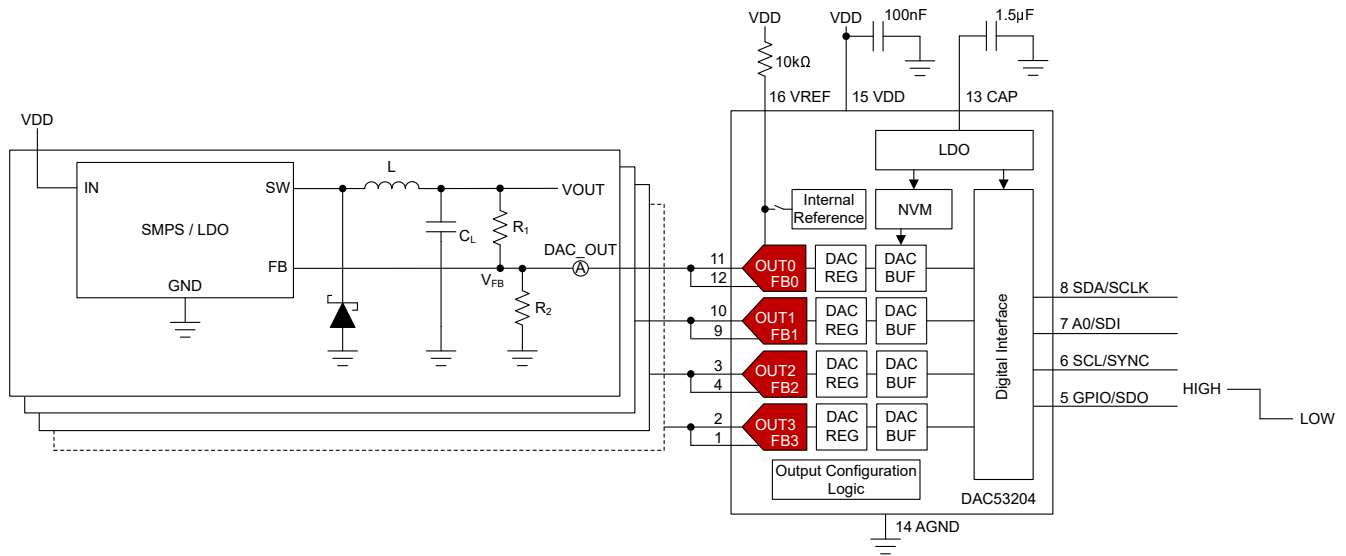
$$DAC\_MARGIN\_LOW = \frac{-12\mu A - (-25\mu A)}{25\mu A - (-25\mu A)} \times 256 = 66.56d$$

This is rounded to 189d and 67d to give a I<sub>DAC,MAX</sub> of 11.9μA and a I<sub>DAC,MIN</sub> of -11.9μA.

- In this design, GPI is used for Margin High, Low function. A high on GPI sets the DAC output to I<sub>DAC,MAX</sub> and the SMPS V<sub>OUT</sub> to margin high, or 3.63V. A low on GPI sets the DAC output to I<sub>DAC,MIN</sub> and the SMPS V<sub>OUT</sub> to margin low, or 2.97V.
- The DAC43204 can be programmed with the initial register settings described in the [Register Settings](#) section using I2C or SPI. Save the initial register settings in the NVM by writing a 1 to the NVM-PROG field of the COMMON-TRIGGER register. After programming the NVM, the device loads all registers with the values stored in the NVM after a reset or a power cycle.

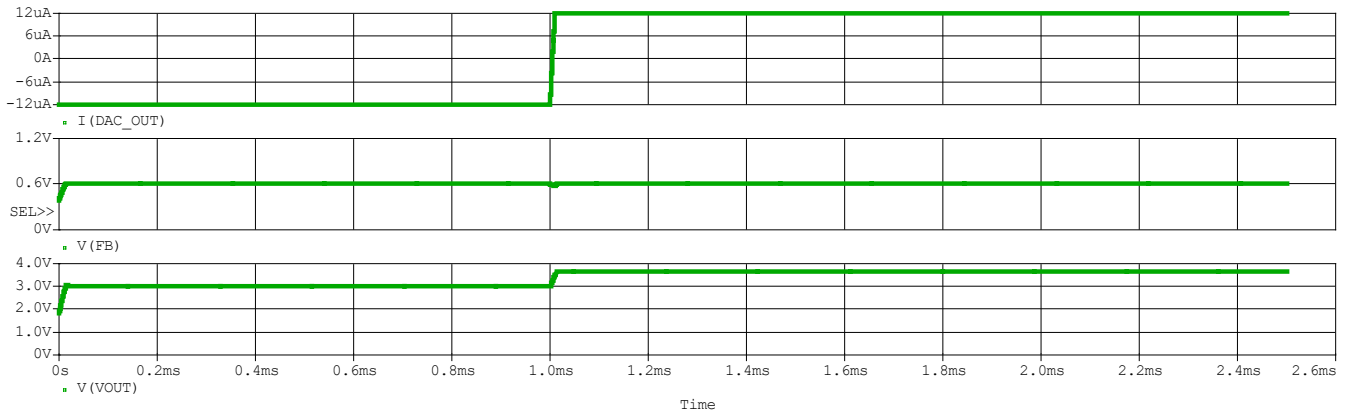
## Design Simulations

This schematic is used for the following simulation of the DAC43204.



## Transient Simulation Results

The simulation shows the SMPS output ( $V_{OUT}$ ) responding to the changes on the DAC43204 output (DAC\_OUT). When DAC\_OUT is at  $I_{DAC,MAX}$  the SMPS  $V_{OUT}$  goes to margin high, or 3.63V. When DAC\_OUT is at  $I_{DAC,MIN}$  the SMPS  $V_{OUT}$  goes to margin low, or 2.97V.



## Register Settings

### Register Settings for DAC43204 Voltage Margining

Register Address	Register Name	Setting	Description
0x1F	COMMON-CONFIG	0x1DB6	[15] 0b0: Write 0b1 to set window-comparator output to a latching output
			[14] 0b0: Write 0b1 to lock device. Unlock by writing 0b0101 to DEV-UNLOCK field in the COMMON-TRIGGER register
			[13] 0b0: Write 0b1 to set fault-dump read enable at address 0x01
			[12] 0b1: Enables the internal reference
			[11:10] 0b11: Powers-down VOUT3
			[9] 0b0: Powers-up IOUT3
			[8:7] 0b11: Powers-down VOUT2
			[6] 0b0: Powers-up IOUT2
			[5:4] 0b11: Powers-down VOUT1
			[3] 0b0: Powers-up IOUT1
			[2:1] 0b11: Powers-down VOUT0
			[0] 0b0: Powers-up IOUT0
0x24	GPIO-CONFIG	0x01F5	[15] 0b0: Write 0b1 to enable glitch filter on GPI
			[14] 0b0: Don't care
			[13] 0b0: Write 0b1 to enable output mode on GPIO pin
			[12:9] 0b0000: Selects the STATUS function setting mapped to GPIO as output
			[8:5] 0b1111: Enables GPI function on all channels
			[4:1] 0b1010: Selects GPI to trigger margin-high, margin-low
			[0] 0b1: Enables input mode for GPIO pin
0x20	COMMON-TRIGGER	0x0002	[15:12] 0b0000: Write 0b0101 to unlock the device
			[11:8] 0b0000: Write 0b1010 to trigger a POR reset
			[7] 0b0: Write 0b1 to trigger LDAC operation if the respective SYNC-CONFIG-X bit in the DAC-X-FUNC-CONFIG register is 1
			[6] 0b0: Write 0b1 to set the DAC registers and outputs to zero-code or mid-code based on the respective CLR-SEL-X bit in the DAC-X-FUNC-CONFIG register
			[5] 0b0: Don't care
			[4] 0b0: Write 0b1 to trigger fault-dump sequence
			[3] 0b0: Write 0b1 to trigger PROTECT function
			[2] 0b0: Write 0b1 to read one row of NVM for fault-dump
			[1] 0b1: Write 0b1 to store applicable register settings to the NVM
			[0] 0b0: Write 0b1 to reload applicable registers with existing NVM settings
0x01, 0x07, 0x0D, 0x13	DAC-X-MARGIN-HIGH	0xBD00	[15:8] 0xBD: 8-bit data updates the MARGIN-HIGH code
			[7:0] 0x00: Don't care
0x02, 0x08, 0x0E, 0x14	DAC-X-MARGIN-LOW	0x4300	[15:8] 0x43: 8-bit data updates the MARGIN-LOW code
			[5:0] 0x00: Don't care

## Pseudo Code Example

The following shows a pseudo code sequence to program the initial register values to the NVM of the DAC43204. The values given here are for the design choices made in the [Design Notes](#).

### Pseudo Code Example for GPI to PWM

```
//SYNTAX: WRITE <REGISTER NAME (Hex code)>, <MSB DATA>, <LSB DATA>
//Power-up current output on all channels, enables internal reference
WRITE COMMON-CONFIG(0x1F), 0x1D, 0xB6
//Configure GPI for Margin-High, Low function
WRITE GPIO-CONFIG(0x24), 0x01, 0xF5
//Write DAC margin high code (repeat for all channels)
WRITE DAC-0-MARGIN-HIGH(0x01), 0xBD, 0x00
//Write DAC margin low code (repeat for all channels)
WRITE DAC-0-MARGIN-LOW(0x02), 0x43, 0x00
//Save settings to NVM
WRITE COMMON-TRIGGER(0x20), 0x00, 0x02
```

## Design Featured Devices

Device	Key Features	Link
DAC43204	4-channel, 8-bit, VOUT and IOUT smart DAC with I2C, SPI and Hi-Z out during power off	<a href="http://www.ti.com/product/DAC43204">www.ti.com/product/DAC43204</a>
DAC53204	4-channel, 10-bit, VOUT and IOUT smart DAC with I2C, SPI and Hi-Z out during power off	<a href="http://www.ti.com/product/DAC53204">www.ti.com/product/DAC53204</a>
DAC53004	Ultra-low-power, 4-channel, 10-bit, VOUT and IOUT smart DAC with I2C, SPI and Hi-Z out during power off	<a href="http://www.ti.com/product/DAC53004">www.ti.com/product/DAC53004</a>

Find other possible devices using the [Parametric search tool](#).

## Design References

See [Analog Engineer's Circuit Cookbooks](#) for TI's comprehensive circuit library.

### Additional Resources

- Texas Instruments, [DAC53204 Evaluation Module](#)
- Texas Instruments, [DAC53204 EVM User's Guide](#)
- Texas Instruments, [Precision Labs - DACs](#)

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