Application Report

Layout Guidelines of PCIe® Gen 4.0 Application With the TMUXHS4412 Multiplexer

ABSTRACT

The Peripheral Component Interface Express (PCIe®) standard continues to be the primary input/output (IO) interconnect within the server and PC environment. With more channels in the system, PCB layout designs become more challenging. This document provides guidelines on how to achieve a robust PCIe® PCB design with the TMUXHS4412 multichannel multiplexer device.

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Trademarks

1 Introduction

PCB layout becomes more and more important for computer systems because of the trend to faster, higher integrated, smaller form factors,and lower power systems using the PCIe® interface. The higher the switching frequencies are, the more radiation occurs on a PCB. With good layout, many EMI problems like reflection or crosstalk can be minimized to meet the required specifications.

2 Practical PCB Design Rules

Many things can affect PCB transmission lines, like impedance mismatch or intra-pair skew and inter-pair skew of trace, EMI problems can occur. To reduce these problems, good PCB design is important, and with some simple design rules,the PCB designer can minimize these problems.

2.1 PCIe® Specific Standard

There are many differences in the various high-speed standards that need to be taken into account when designing the layout of a system. These differences include parameters like data-rates/frequency, AC coupling capacitors, inter-pair skew, intra-pair skew and trace impedance. Table 2-1 lists the standard values for PCIe standard.

Table 2-1. Parameters of PCIe® Standard

Parameter	Value
Frequency	PCIe® Gen 1: 1.25 GHz (2.5 Gbps)
	PCIe® Gen 2: 2.5 GHz (5 Gbps)
	PCIe® Gen 3: 4 GHz (8 Gbps)
	PCIe® Gen 4: 8 GHz (16 Gbps)
AC Coupling Capacitors	AC capacitors required: 75 nF–220 nF
Polarity Reversal	Allowed
Max Intra-Pair Skew	5 mils
Max Inter-Pair Skew	No Inter-pair specification
Trace Impedance	PCIe® Gen 1 and 2:100 Ω ±5% differential; 50 Ω ±5% single ended
	PCIe® Gen 3 and 4: 85 Ω ±5% differential; 42.5 Ω ±5% single ended

2.2 PCIe® High-Speed Signal Layout Guidelines

1. For PCIe® high-speed signals, design *trace impedance* so as to minimize the reflections in traces. Control the trace impedance to be as close as possible to the recommended values in Table 2-1.
2. Keep the total *trace length* for signal pairs to a *minimum*.
3. Match the etch lengths of the relevant differential pair traces. Make sure *intra-pair skew* is within *5 mils* for the PCIe® standard. There is no need to match inter-pair skew.

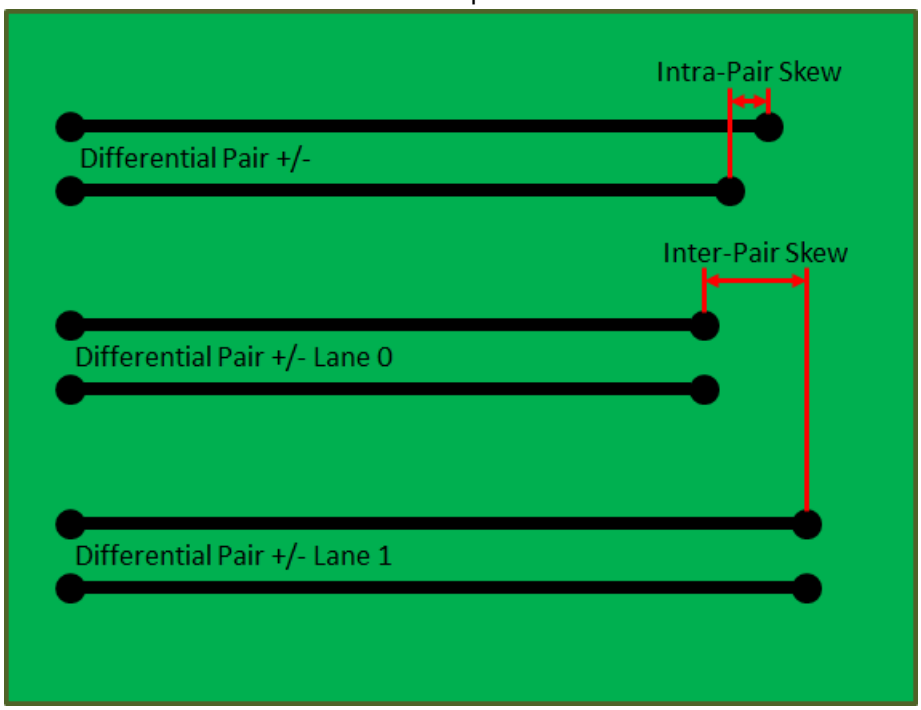

Figure 2-1. Differential Pair Intra-Pair Skew and Inter-Pair Skew

4. To minimize crosstalk in high-speed interface implementations, the *spacing* between the signal pairs must be a minimum of *5* times the width of the trace.
5. When possible, route high-speed differential pair signals on the *top or bottom layer* of the PCB with an adjacent GND layer. TI does not recommend stripline routing of the high-speed differential signals.
6. Void right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing is a round bend (see Figure 2-2)

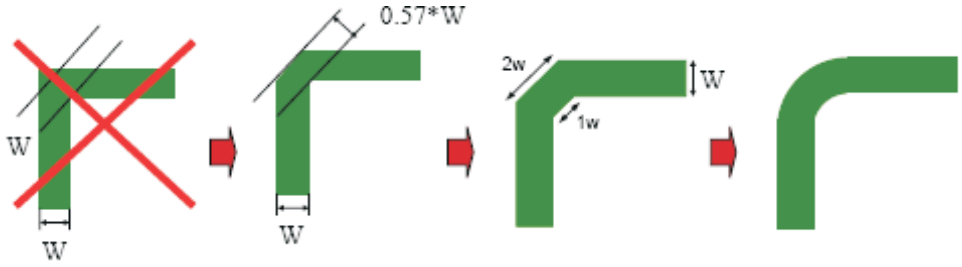

Figure 2-2. Poor and Good Right Angle Bends

2.3 Vias, Stub, and ESD/EMI Layout Guidelines

1. The use of vias is essential in most routings, but vias add additional inductance and capacitance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length.

   If possible, avoid routing high-speed traces through the *vias*.

   If it is impossible to avoid vias:

   - Ensure that the via count on each member of the differential pair is equal and that the vias are as equally spaced as possible. A maximum of two vias are recommended for high-speed trace over 5Gbps.
   - Be careful with the return current when changing the layers. Use ground vias around the signal via to make sure that the return current can flow as close as possible to the signal (see Figure 2-3)

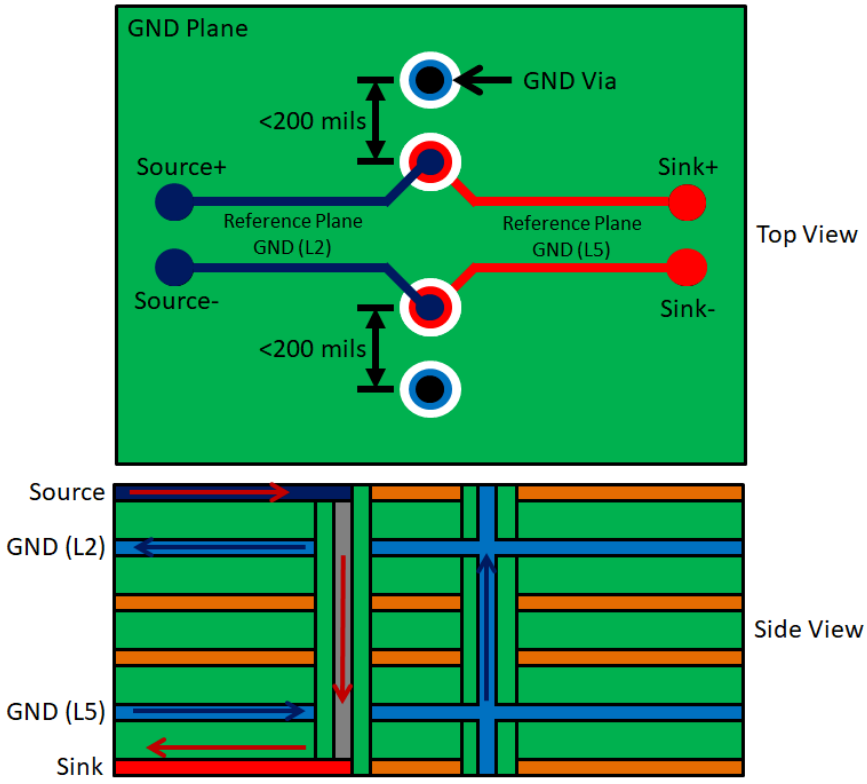

Figure 2-3. Differential Pair Via Return Path With GND Vias

   - Longer via stubs resonate at lower frequencies and increase insertion loss, keep these stubs as short as possible. TI recommends keeping via stubs to less than 15 mils. Longer stubs must be *back-drilled* (see Figure 2-4).

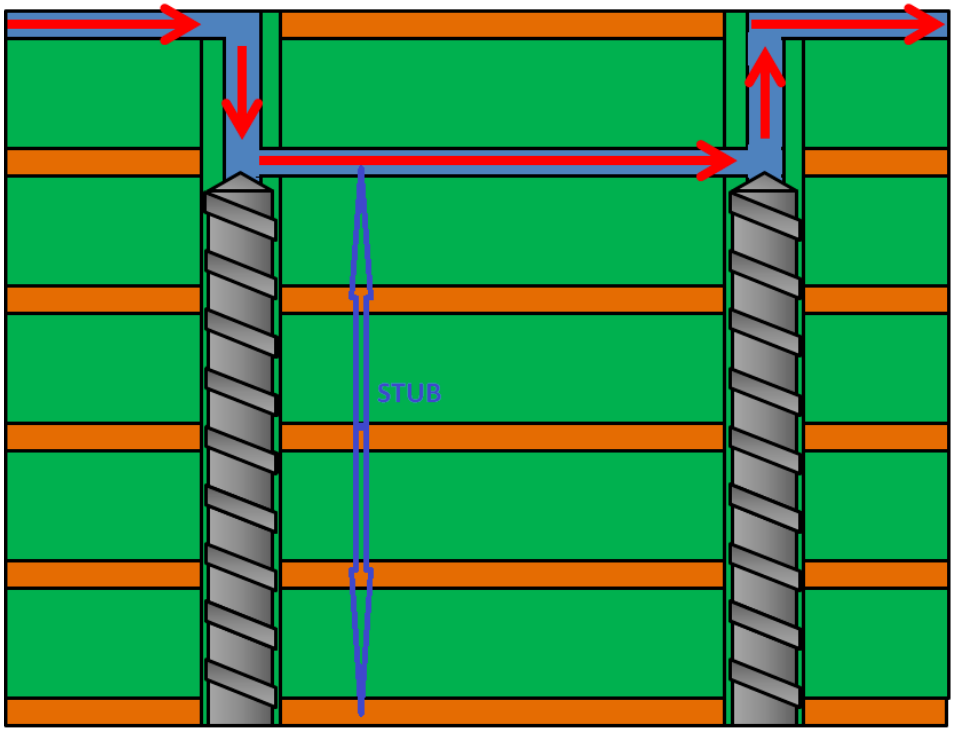

Figure 2-4. Long Vias With Back-Drilled Stubs

2. Do not place probe or test points on any high-speed differential signals.
3. Do not route high-speed traces under or near crystals, oscillators, clock signal generators, switching power regulators, mounting holes, magnetic devices, or integrated circuits (IC) that use or duplicate clock signals.
4. When choosing *ESD/EMI* components, TI recommends selecting devices that permit flow-through routing of the differential signal pair because they provide the cleanest routing.
   - Incorporate voids under the ESD/EMI component signal pads to reduce losses (see Figure 2-5).

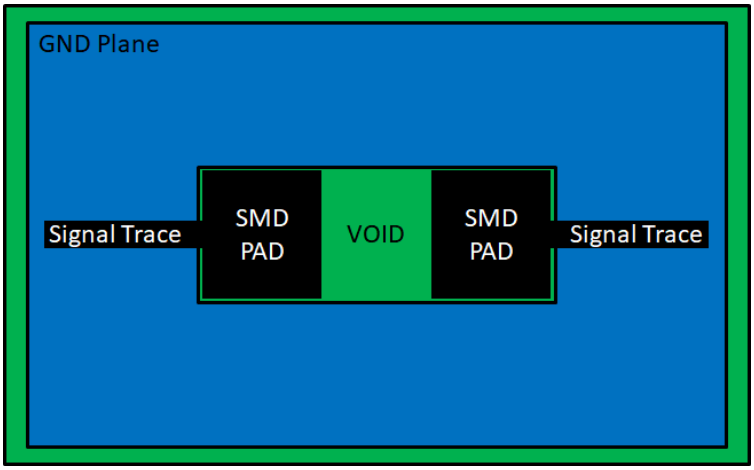

Figure 2-5. Void Below Surface Mount Devices

   - Use 0402 0-Ω resistors for common-mode filter (CMF) no-stuff options because larger components will typically introduce more loss that the CMF itself.
   - Keep the overall routing of AC coupling capacitors+ CMF+ ESD protection as short and as close as possible to the connector.

2.4 Power and Grounding Layout Guidelines

1. Use a complete ground plane and a complete power plane to avoid noise coupling. But in most cases, split ground planes cannot be avoided. If split ground planes are essential:
   - Do not route signals over a gap. Always strive for the return current flow with the smallest loop area.
   - Connect split ground planes only at one point. More common-ground connections can create ground loops, and this increases radiation.
   - Power planes should only reference their own ground plane. They should not overlap with another ground plane.
   - Do not connect bypass capacitors between a power plane and an unrelated ground plane. Again, noise can be coupled from one supply system into the other.
2. Separate digital and analog power supplies with filtering and bypassing.
3. Put the largest-value filter capacitors near a power connector and supply inputs.
4. Place high-quality X7R decoupling capacitors close to device pins.
   - Use multiple capacitors (0.1 µF, 0.01 µF, and 1 µF) in parallel to offer low impedance over higher frequency ranges.
   - Place the smallest-value capacitors closest to the power pin.
   - Connect the pad of the capacitor directly to a via to the ground plane. Use two or three vias to get a low-impedance connection to ground.
   - Keep the traces from decoupling caps to ground as short and wide as possible

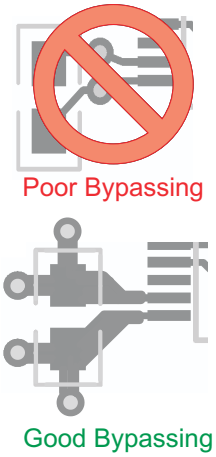

Figure 2-6. Poor and Good Placement and Routing of Bypass Capacitors

3 Layout Examples

Figure 3-1 shows a TMUXHS4412 layout example.

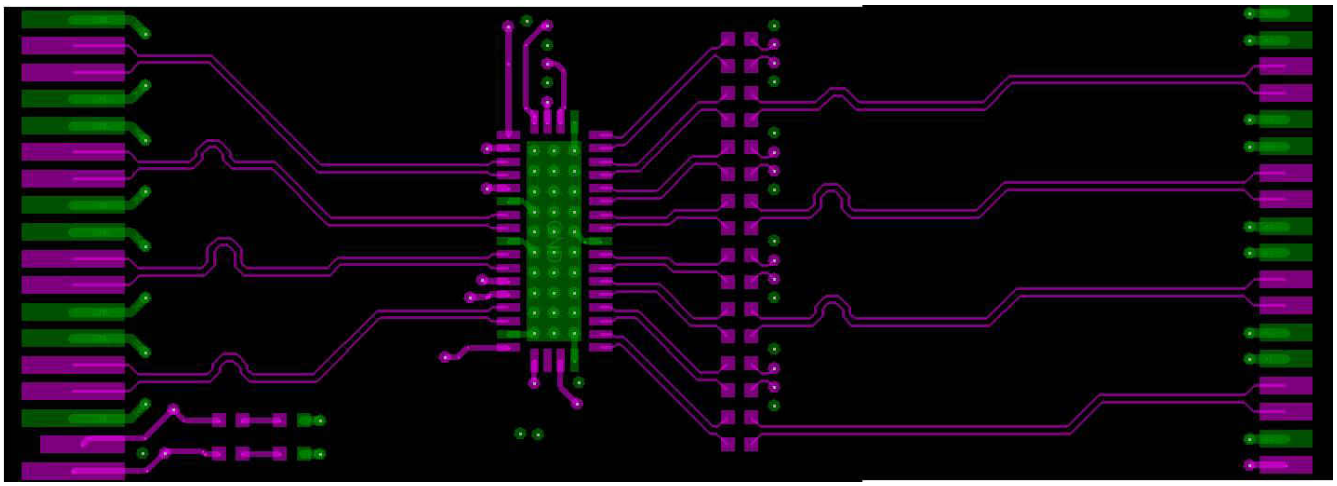

Figure 3-1. TMUXHS4412 Layout Example

Figure 3-2 shows a layout illustration where four TMUXHS4412 are used to switch eight PCIe® lanes between two PCIe® connectors.

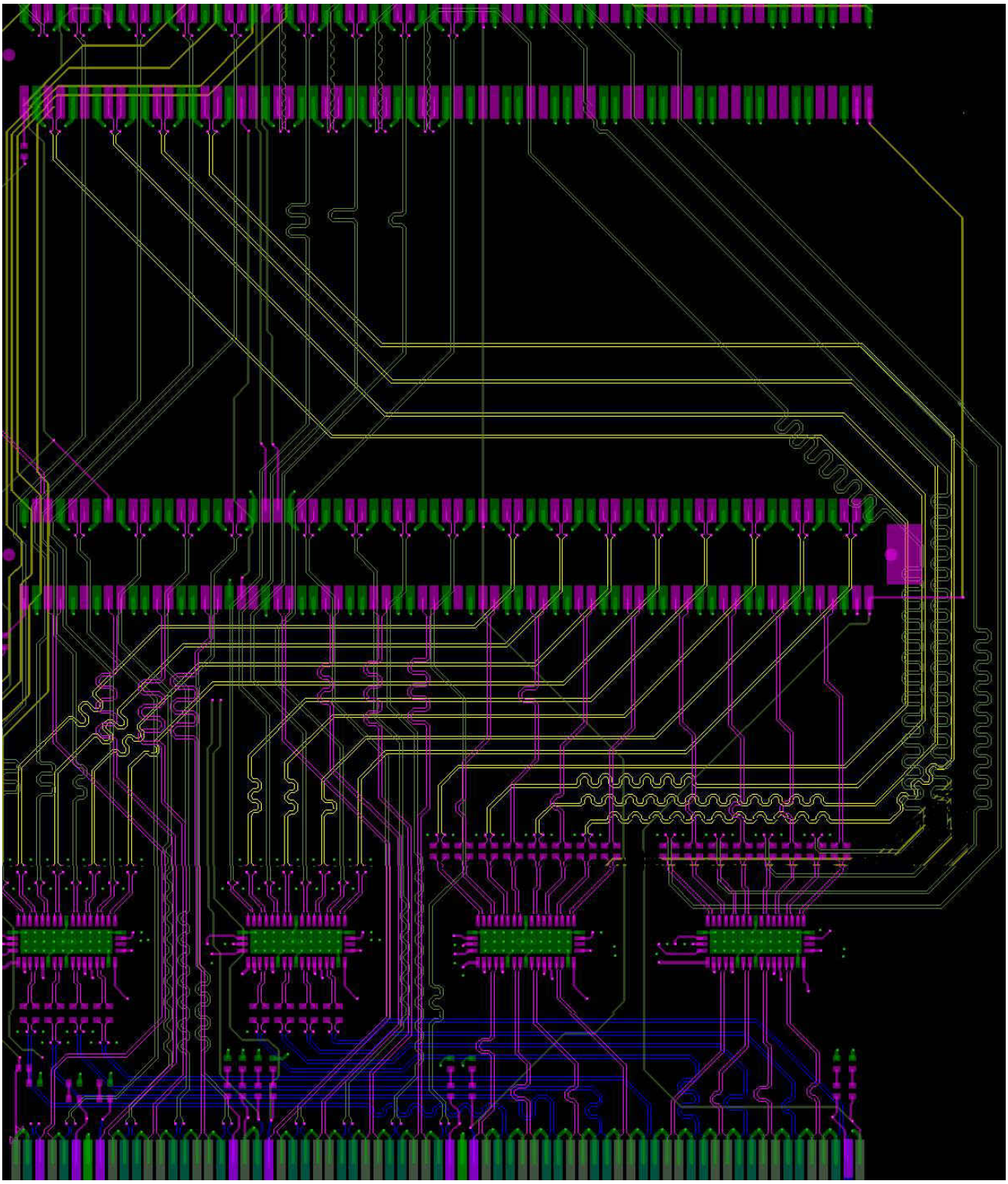

Figure 3-2. Layout Example for PCIe® Lane MUXing Application

4 Summary

This user guide summarized the PCB layout guidelines for high-speed differential signals like PCIe® interface. It also showed some layout examples of PCIe® lane MUXing application with TI multiplexer device TMUXHS4412.

5 References

- Texas Instruments, *High-Speed Layout Guidelines for Signal Conditioners and USB Hubs*
- Texas Instruments, *High-Speed Layout Guidelines Application Report*

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