Controlling TAS5026 Volume After Error Recovery

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ABSTRACT

The TAS5026 monitors the relationship between its MCLK, SCLK and LRCLK. If the TAS5026 detects clock errors, it will automatically perform a clock error recovery sequence. When the execution of the clock error recovery sequence is combined with the /ERR_RCVRY terminal being asserted or the I^2C individual channel error recovery bits being cleared, the error recovery sequence may be modified resulting in the volume not being restored to its pre-error setting. The user can control these side affects on volume by appropriately setting the error recovery register and the test register x1F.

1 Introduction

The TAS5026 monitors the relationship between its MCLK, SCLK and LRCLK. If the TAS5026 detects clock errors, it will automatically perform a clock error recovery sequence. The clock errors detected by the TAS5026 include the following:

1. Any of the clocks are missing.
2. LRCLK rate changes more than ±10 MCLKS cycles since the last device reset or clock error recovery sequence.
3. MCLK frequency changes substantially with respect to the PLL frequency.

The clock error recovery sequence temporarily suspends processing, places the PWM outputs in a hard mute (PWM_P outputs are low; PWM_M outputs are high, and all VALID_x signals are low), resets all internal processes, sets the volume to mute and suspends all I^2C operations. When the clock error has been corrected, the TAS5026 performs a 4.3 ms partial re-initialization, noiselessly restarts the PWM outputs, and softly ramps the volume up to the level specified in the volume control registers over a 43 ms interval.

When the error recovery register (x04) is in its default configuration and there are no clocks errors, asserting /ERR_RCVRY terminal or clearing one of the individual channel error recovery bits will result in a hard mute being applied to the appropriate PWM outputs. When the /ERR_RCVRY terminal or an individual channel error recovery bits is de-asserted, the volume will be restored to the level specified in the volume configuration registers. When one introduces clock errors into the equation, the TAS5026 may start reacting a little different then expected when either /ERR_RCVRY terminal or the I^2C individual channel error recovery bits are asserted. This application note describes the effect that unstable clocks have on the error recovery sequence and how to work around these issues by using the error recovery register and the test register x1F.

2 Error Recovery Register and its Affect on Post Error Recovery Sequence Volume

For purposes of this discussion, we are interested in bits 6 and 7 (D6 and D7 respectively) of the error recovery register (x04). D6 and D7 of the error recovery register combined with specific settings of test register x1F can control the volume ramp up following an error recovery sequence. We will consider cases where the user places the TAS5026 in error recovery mode by either asserting /ERR_RCVRY or by using the individual channel recovery bits (bits 0..5) of the error recovery register (both /ERR_RCVRY terminal and the I^2C error recovery mode bits are active low). The table below defines the effect D6 and D7 of the error recovery register in combination with the values of test register x1F have on volume following the error recovery sequence. It is not recommended that test register x1F be programmed to any other value other than those presented below.

Table 1. Error Recovery Register (x04) and Test Register x1F Settings

D7	D6	Test Register x1F	Function
1	1	x00 or default setting.	Default setting. If clock error occurs while the /ERR_RCVRY pin is asserted, the TAS5026 performs the error recovery sequence up to the unmute sequence. The volume remains at full attenuation with the PWM ouputs at a 50% duty cycle.
0	-	x84	Volume ramp up is **enabled** after an error recovery sequence initiated by either the /ERR_RCVRY terminal or the I^2C error recovery command bit (bit 2 of register x03).
1	-	x84	Volume ramp up is **disabled** after an error recovery sequence initiated by either the /ERR_RCVRY terminal or the I^2C error recovery command bit (bit 2 of register x03).
-	0	x84	Volume ramp up is **enabled** after an error recovery sequence initiated by setting bits 0 to 5 of the error recovery register (x04).
-	1	x84	Volume ramp up is **disabled** after an error recovery sequence initiated by setting bits 0 to 5 of the error recovery register (x04).

2.1 Error Recovery Register and Test Register Setting Examples

The following examples are presented only to illustrate the effect that different register configurations and clock errors have on post error recovery volume levels. We will take a look at four configurations and see the effect on volume when the /ERR_RCVRY terminal or I^2C bits is asserted.

1. Volume ramp is always disabled regardless of means of initiating the error recovery sequence.

2. Volume ramp is disabled when the error recovery sequence is initiated by using the /ERR_RCVRY terminal, but is enabled when using the individual channel error recovery mode I^2C bits.

3. Volume ramp is disabled when the error recovery sequence is initiated using the individual channel error recovery mode I^2C bits, but is enabled when the /ERR_RCVRY terminal is used.

4. Volume ramp is always enabled regardless of means of initiating the error recovery sequence.

Please refer to the TAS5026 Data Manual for recommend procedures to use during start up, data sample rate changes and master/slave clock mode changes.

2.1.1 Volume Ramp is Always Disabled

The first configuration deals with what essentially is the default behavior of the TAS5026. D7 and D6 of Register x04 are both set to 1 (the default values) and test register x1F is set to its default value of x00. In this configuration, the volume following the error recovery sequence will vary depending on whether a clock error is detected while in the user initiated error recovery mode.

Whether the user initiates error recovery by using the /ERR_RCVRY terminal or the individual channel error recovery mode bits of the error recovery register, the effect is the same. When /ERR_RCVRY goes LOW, the TAS5026 will place the PWM outputs in a hard mute. If clocks are stable while /ERR_RCVRY is LOW, the volume will be restored, without a soft ramp, to the level specified in the volume control registers (see Figure 1). If clocks are unstable while /ERR_RCVRY is LOW, the TAS5026 will perform the error recovery sequence up to the unmute sequence. Consequently, the volume will remain muted (see Figure 2).

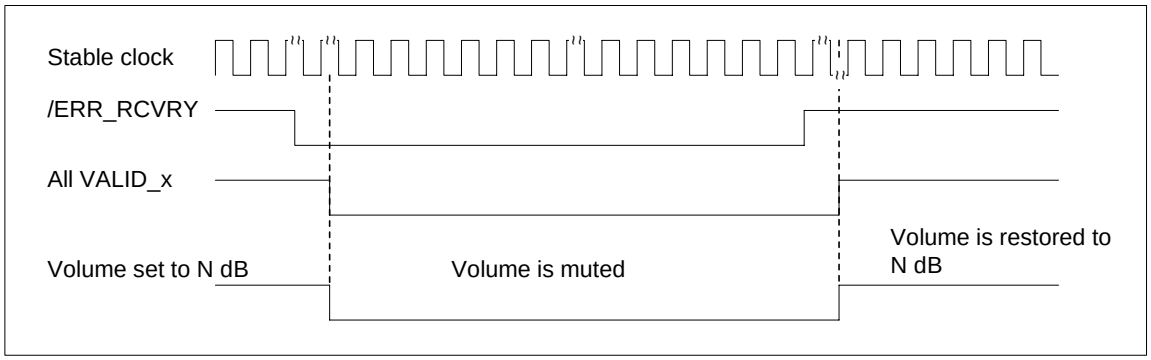

Figure 1 - Reg. x04 D7 = 1 and D6 = 1 and test register x1F set to x00; error recovery via /ERR_RCVRY; stable clocks

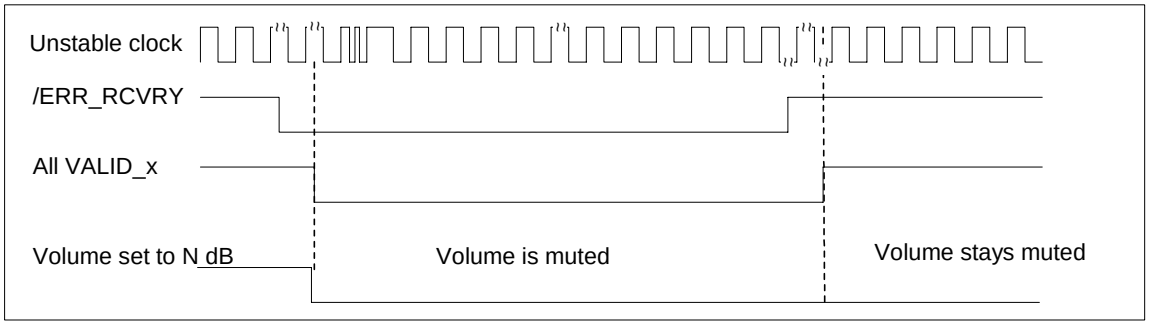

Figure 2 - Reg. x04 D7 = 1 and D6 = 1 and test register x1F set to x00; error recovery via /ERR_RCVRY; unstable clocks

In the case that the user uses the individual error recovery mode bits to initiate the error recovery on a specific channel, the associated bit (bit 0..5 of the error recover register) is set to 0 via I^2C and the TAS5026 will place the corresponding PWM output in a hard mute. If clocks are stable while the individual channel error recovery mode bit is 0, the volume will be restored, without a soft ramp, to the level specified in the volume control registers (see Figure 3). If clocks are unstable while the associated bit is 0, the TAS5026 will perform the error recovery sequence up to the unmute sequence. Consequently, the volume will remain muted (see Figure 4).

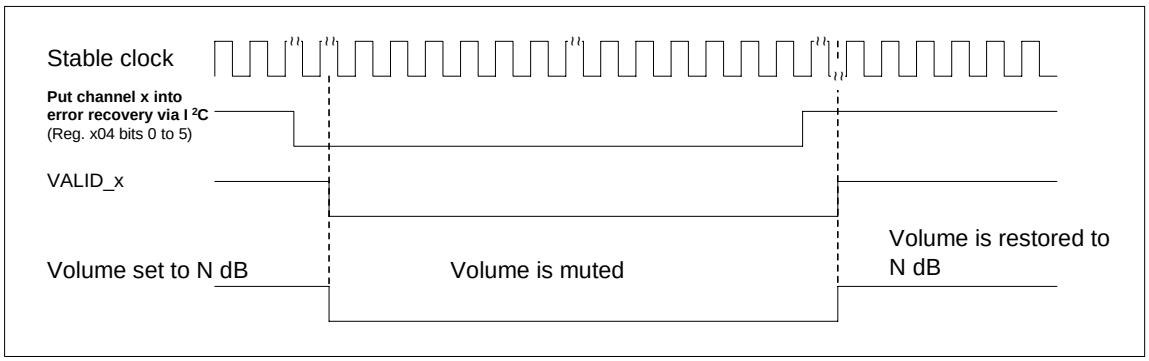

Figure 3 - Reg. x04 D7 = 1 and D6 = 1 and test register x1F set to x00; error recovery on individual channel via Reg. x04; stable clocks

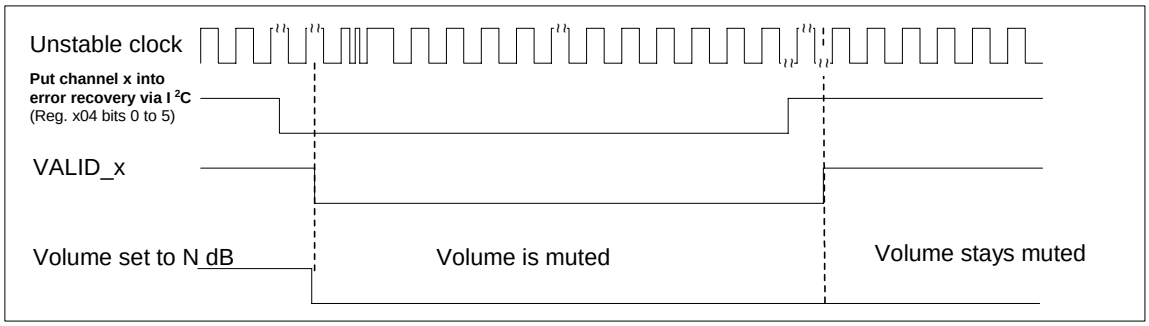

Figure 4 - Reg. x04 D7 = 1 and D6 = 1 and test register x1F set to x00; error recovery on individual channel via Reg. x04; unstable clocks

2.1.2 Volume Ramp Enabled Only for Individual Channel Error Recovery Mode I^2C Bits

In this second case, we configure the error recovery register bits (D7 = 1 and D6 = 0) so that the TAS5026 still disables the volume ramp up after an error recovery sequence is initiated by the /ERR_RCVRY terminal and enables the soft volume ramp up when the error recovery sequence is initiated by the individual channel error recovery mode bits of the error recovery register. The setting for test register x1F will be modified from its default value to x84.

When the /ERR_RCVRY terminal is used to initiate the error recover sequence, the TAS5026 will react in the same way as it did in the default case. If clocks are stable while the /ERR_RCVRY terminal is LOW, the volume will be restored, without a soft ramp, to the level specified in the volume control registers (see Figure 5). If clocks are unstable while the /ERR_RCVRY terminal is LOW, the TAS5026 will perform the error recovery sequence up to the unmute sequence (see Figure 6). At that point the volume will remain at mute until the /MUTE terminal is brought low and then high or the /MUTE I^2C bit is cleared and then set to 1.

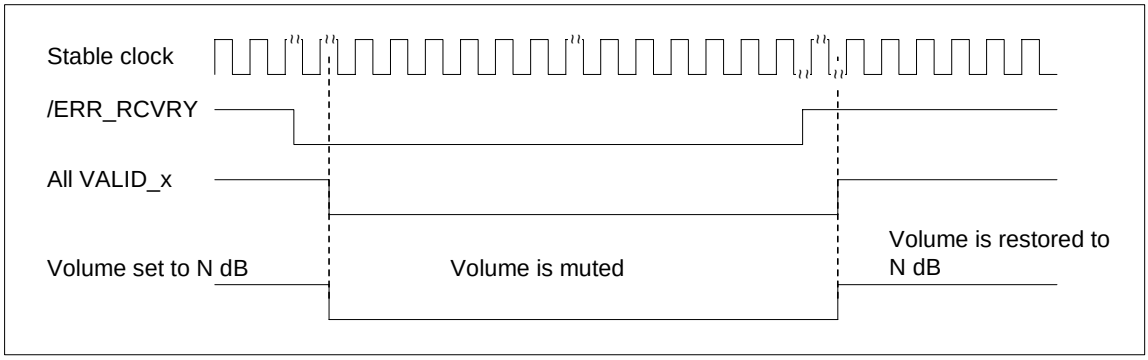

Figure 5 - Reg. x04 D7 = 1 and D6 = 0 and test register x1F set to x84; error recovery via /ERR_RCVRY; stable clocks

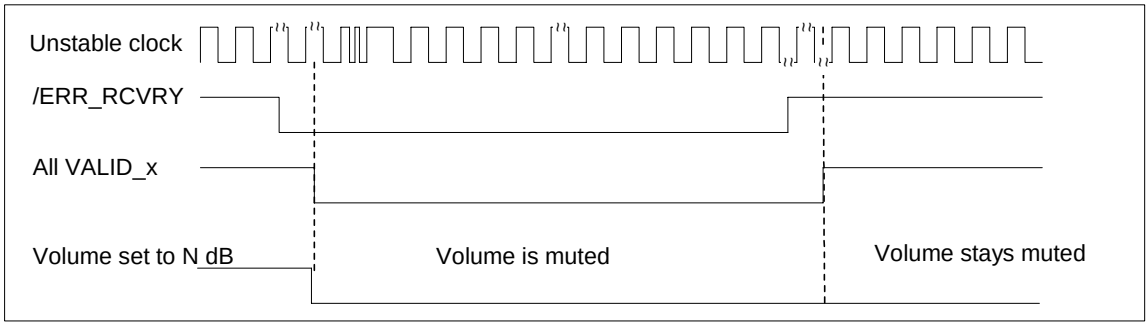

Figure 6 - Reg. x04 D7 = 1 and D6 = 0 and test register x1F set to x84; error recovery via /ERR_RCVRY; unstable clocks

With D6 = 0, the TAS5026 will react differently when the individual error recovery mode bits are used to initiate the error recovery sequence verses when the /ERR_RCVRY terminal is used to initiate the sequence. Regardless of whether the clocks are stable while an individual channel error recovery bit is 0, the TAS5026 will softly ramp the volume to the level specified in the volume control registers over a 42 to65 ms interval at the end of the error recovery sequence (see Figure 7 and Figure 8).

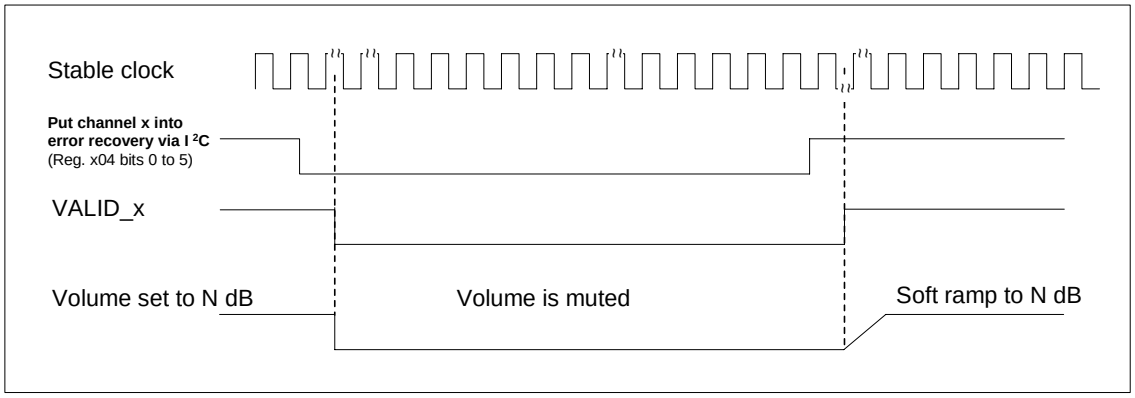

Figure 7 - Reg. x04 D7 = 1 and D6 = 0 and test register x1F set to x84; error recovery on individual channel via Reg. x04; stable clocks

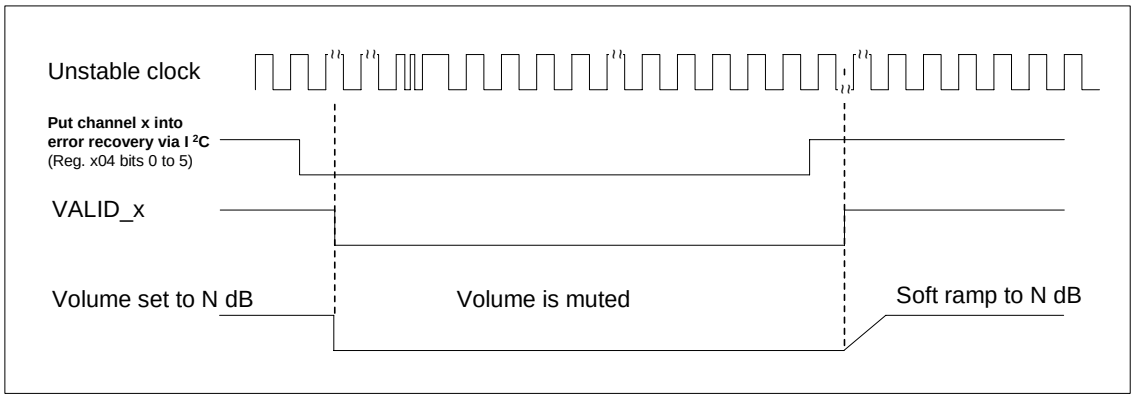

Figure 8 - Reg. x04 D7 = 1 and D6 = 0 and test register x1F set to x84; error recovery on individual channel via Reg. x04; unstable clocks

2.1.3 Volume Ramp Enabled Only for /ERR_RCVRY

In this third case, we configure the error recovery register bits (D7 = 1 and D6 =0) so that the TAS5026 enables the volume ramp up after an error recovery sequence when the sequence is initiated by the /ERR_RCVRY terminal and disables the volume ramp up when the error recovery sequence is initiated by the individual channel error recovery mode bits of the error recovery register. The setting for the test register x1F will again be modified from its default value to x84.

The TAS5026 will react differently when the /ERR_RCVRY terminal is used to initiate the sequence verses when the individual error recovery mode bits are use to initiate the error recovery sequence. The difference in this case is that TAS5026 will react the same regardless of whether the clocks are stable when the /ERR_RCVRY terminal is LOW. Whether clocks are stable or not, the TAS5026 will softly ramp the volume to the level specified in the volume control registers over a 42 to 65 ms interval at the end of the error recovery sequence (see Figure 9 and Figure 10).

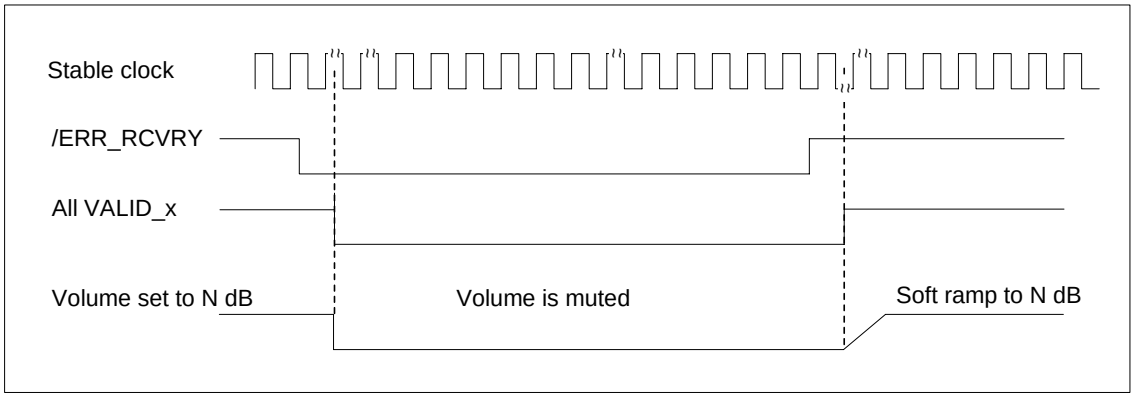

Figure 9 - Reg. x04 D7 = 0 and D6 = 1 and test register x1F set to x84; error recovery via /ERR_RCVRY; stable clocks

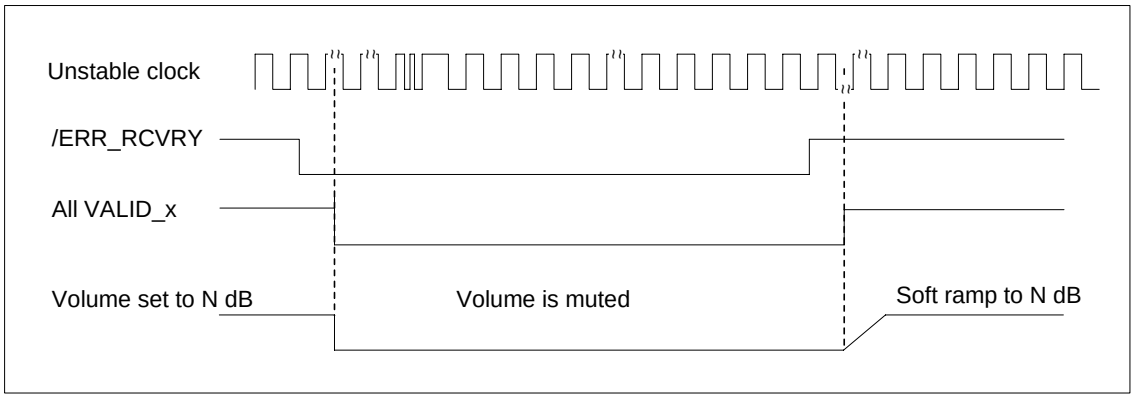

Figure 10 - Reg. x04 D7 = 0 and D6 = 1 and test register x1F set to x84; error recovery via /ERR_RCVRY; unstable clocks

In this configuration, the TAS5026 will react as it did in the default case when the individual error recovery mode bits are used to initiate the error recovery sequence. If clocks are stable while the individual error recovery mode bit is 0, the volume will be restored, without a soft ramp, to the level specified in the volume control registers (see Figure 11). If the clocks are unstable, the TAS5026 will perform the error recovery sequence up to the unmute sequence (see Figure 12).

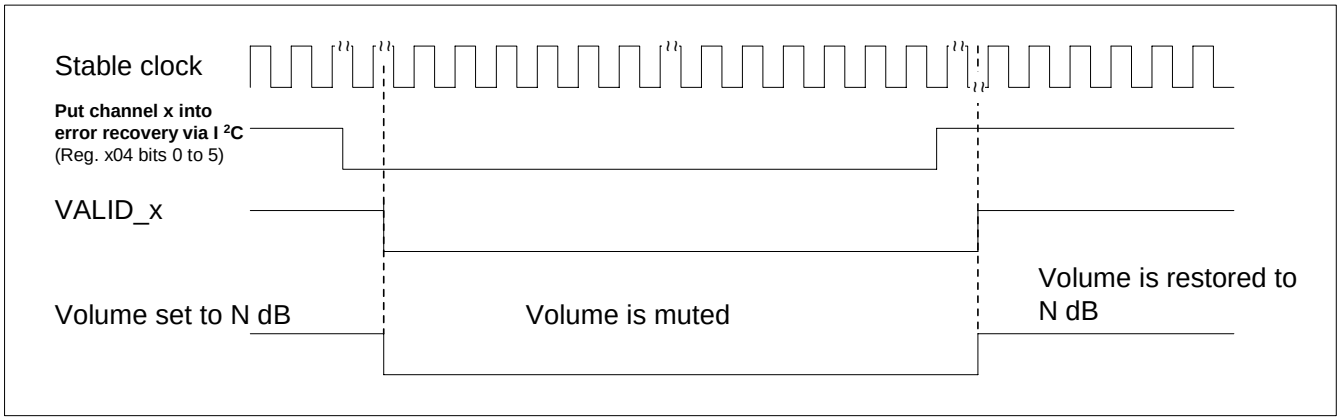

Figure 11 - Reg. x04 D7 = 0 and D6 = 1 and test register x1F set to x84; error recovery on individual channel via Reg. x04; stable clocks

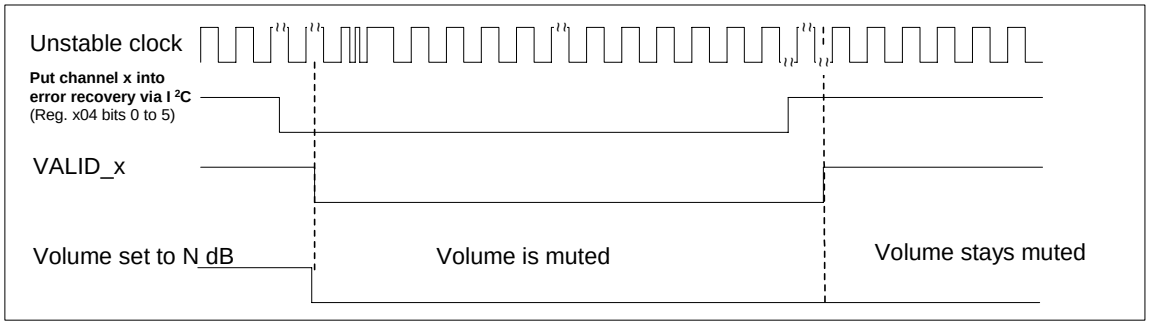

Figure 12 - Reg. x04 D7 = 0 and D6 = 1 and test register x1F set to x84; error recovery on individual channel via Reg. x04; unstable clocks

2.1.4 Volume Ramp Always Enabled

Finally we consider the case where the error recover register bit (D7 = 0, D6 = 0) are configured so that the TAS5026 will do a soft ramp of the volume regardless of whether the user uses the /ERR_RCVRY terminal or the individual channel error recovery bits to initiate the error recovery sequence. Again, the setting for test register x1F will be modified from its default value to x84. In this final case, the TAS5026 is configured so that at the end of the error recovery sequence it will softly ramp the volume to the level specified in the volume control registers over a 42 to 65 ms interval. As illustrated in the figures below, the TAS5026 will do a soft volume ramp at the end of the error recovery sequence regardless of the means the user used to initiate the error recovery sequence or the state of the clocks.

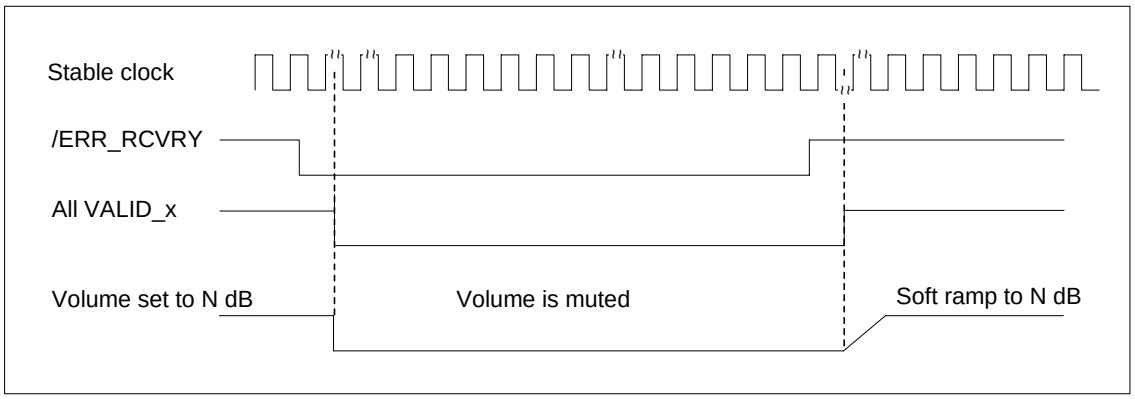

Figure 13 - Reg. x04 D7 = 0 and D6 = 0 and test register x1F set to x84; error recovery via /ERR_RCVRY; stable clocks

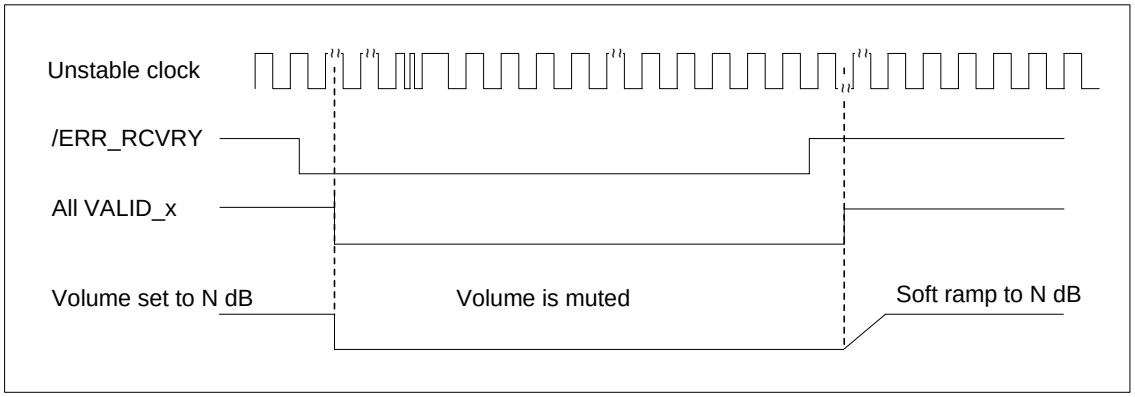

Figure 14 - Reg. x04 D7 = 0 and D6 = 0 and test register x1F set to x84; error recovery via /ERR_RCVRY; unstable clocks

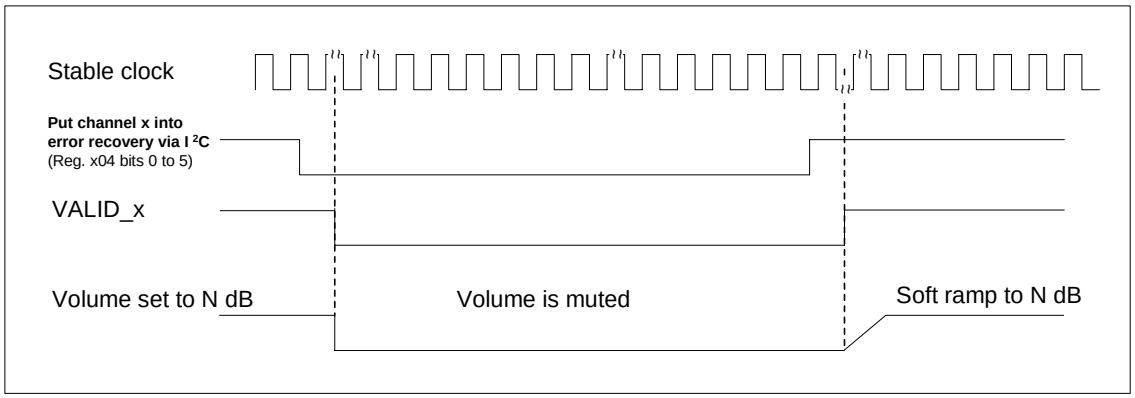

Figure 15 - Reg. x04 D7 = 0 and D6 = 0 and test register x1F set to x84; error recovery on individual channel via Reg. x04; stable clocks

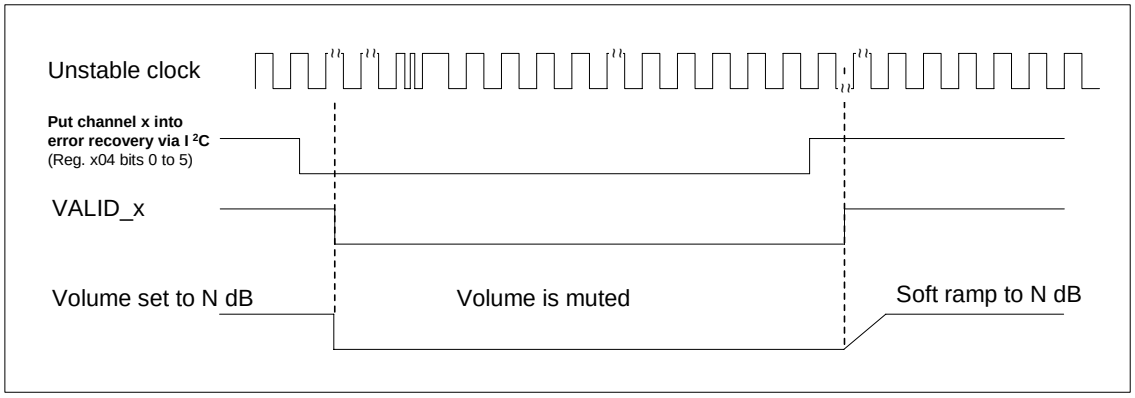

Figure 16 - Reg. x04 D7 = 0 and D6 = 0 and test register x1F set to x84; error recovery on individual channel via Reg. x04; unstable clocks

3 Conclusions

The resulting volume level following an error recovery sequence initiated by either the /ERR_RCVRY terminal or the individual channel error recovery mode bits of the error recovery register can be affected by the state of the clocks. By configuring the error recovery register and the less documented test register x1F, the user can specify how the TAS5026 will restore the volume level after the /ERR_RCVRY terminal goes HIGH or an individual channel error recovery mode bit is set to 1. By setting the error recovery register to enable volume ramp up after an error recovery sequence initiated by the user, as well as setting the test register x1F to x84, the user can configure the TAS5026 so that the volume will always be softly ramped regardless of the state of the clocks while the /ERR_RCVRY terminal is LOW or the individual channel error mode bits is set to 0.

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