Application Report Title

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ABSTRACT

The Texas Instruments TAS3103EVM is an evaluation module designed to support Texas Instruments' TAS3103 Digital Audio Processor. This EVM houses two TAS3103 audio processing chips, allowing the EVM to implement and evaluate 6 channel audio applications. The TAS3103 chip is a highly configurable audio processor that can serve many applications and circuit topologies. To support such a wide range of applications and circuit topologies, it is necessary that the EVM also be highly configurable. This application report is intended to serve as a startup document. Four commonly used EVM topologies are presented, with the required EVM switch settings, shunt installations and TAS3103 configuration files to implement each topology included.

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1 INTRODUCTION

The TAS3103EVM has two TAS3103 audio processing chips, three Texas Instruments PCM1802 stereo ADCs, one 6-channel Texas Instruments PCM1606 DAC, one S/PDIF receiver (with both coax and optical ports) and one S/PDIF transmitter (with both coax and optical ports). In addition, the TAS3103EVM provides input and output headers for routing I^2S data directly to and from the TA3103 chips. An I^2C port provides the ability to configure (and re-configure) each TAS3103 chip via an I^2C bus.

Audio can be input into the TAS3103EVM via the three DACs (analog input), the S/PDIF Rx (S/PDIF stereo input) or the I^2S Input Header (digital input). The two TAS3103 chips can output processed audio to the 6-channel PCM1606 DAC (analog output), the S/PDIF Tx (S/PDIF stereo output), and the I^2S Output Header (digital output).

Clock management is also provided on the TAS3103EVM. TAS3103-U1 can be configured as an I^2S master device, which means that it can source the sample clock (LRCLK) and the serial data bit clock (SCLK). To provide these two clocks, TAS3103-U1 can use either an externally provided MCLK or an external crystal reference to derive LRCLK and SCLK. The S/PDIF Rx and the I^2S Input Header can also serve as I^2S masters and source LRCLK and SCLK.

Clock management separate from that used to control SCLK and LRCLK is provided for the master clock MCLK. The S/PDIF Rx and the I^2S Input Header can both source MCLK. In addition, TAS3103-U1, when configured either as an I^2S master device or as an I^2S slave device, can source MCLK using an external crystal frequency reference. This means that TAS3103-U1 can source MCLK yet be slaved to external SCLK and LRCLK clocks. The TAS3103EVM, as well as the TAS3103 chips, does not require MCLK to be synchronous with SCLK and LRCLK.

Fifteen switches and fifteen removable shunts are included on the TAS3103EVM to control the array of choices in data and clocking topologies. This application report is intended to aid the user in setting the switches and installing the shunts to arrive at a topology that implements the application to be evaluated.

2 COMMON EVM TOPOLOGIES

To illustrate the setting of the switches and shunts on the EVM, four example EVM topologies are presented.

S/PDIF In - S/PDIF Out

- S/PDIF Single Stereo Input
- S/PDIF Single Stereo Output
- Single I^2S Stereo Data Output Stream
- Single Stereo DAC Output

Analog In – Analog Out

- Up To Three Analog Stereo Inputs
- Up to Three Analog Stereo Outputs
- Up To Three I^2S Stereo Data Output Streams
- S/PDIF Single Stereo Output

I^2S In - I^2S Out

- Up To Three I^2S Stereo Data Input Streams
- Up to Three Analog Stereo Outputs
- Up To Three I^2S Stereo Data Output Streams
- S/PDIF Single Stereo Output

TDM In – Analog Out

- Single TDM Input Data Stream (Containing Up To Three Stereo Signals)
- Up to Three Analog Stereo Outputs
- Up To Three I^2S Stereo Data Output Streams
- S/PDIF Single Stereo Output

On the input side, these four topologies address analog stereo input applications (up to three stereo analog input channels), S/PDIF single stereo input applications, serial I^2S stereo input data stream applications (up to four stereo input channels), and serial TDM input data stream applications.

On the output side, the four chosen topologies address stereo analog output applications (up to three stereo analog output channels), single stereo S/PDIF output applications, and serial I^2S stereo output data stream applications (up to three stereo output channels).

The .cfg configuration file for each of the four topologies is presented in the Appendix.

3 S/PDIF IN - S/PDIF OUT

Figure 1 shows the signal flow for this single S/PDIF stereo input configuration. The S/PDIF source can be input using the optical TOSLINK connector OPTO1 or the coaxial connector J4. The input is routed through monaural channels CH1 and CH2 of TAS3103-U1. The monaural channels are set up by configuration file SPDIF_IN_OUT.cfg as pass-through channels with a volume attenuation of -12 dB. Volume adjustments can be made via I^2C bus commands.

TAS3103-U1 outputs the stereo signal on pin 20 - SDOUT1. This output is routed to both S/PDIF output ports - the TOSLINK connector OPTO2 and the coaxial connector J5, the analog line out jacks J8 and J9, and the I^2S Output Header J2B (where it is output as a serial data stream). MCLK, SCLK, and LRCLK are also provided on the I^2S Output Header.

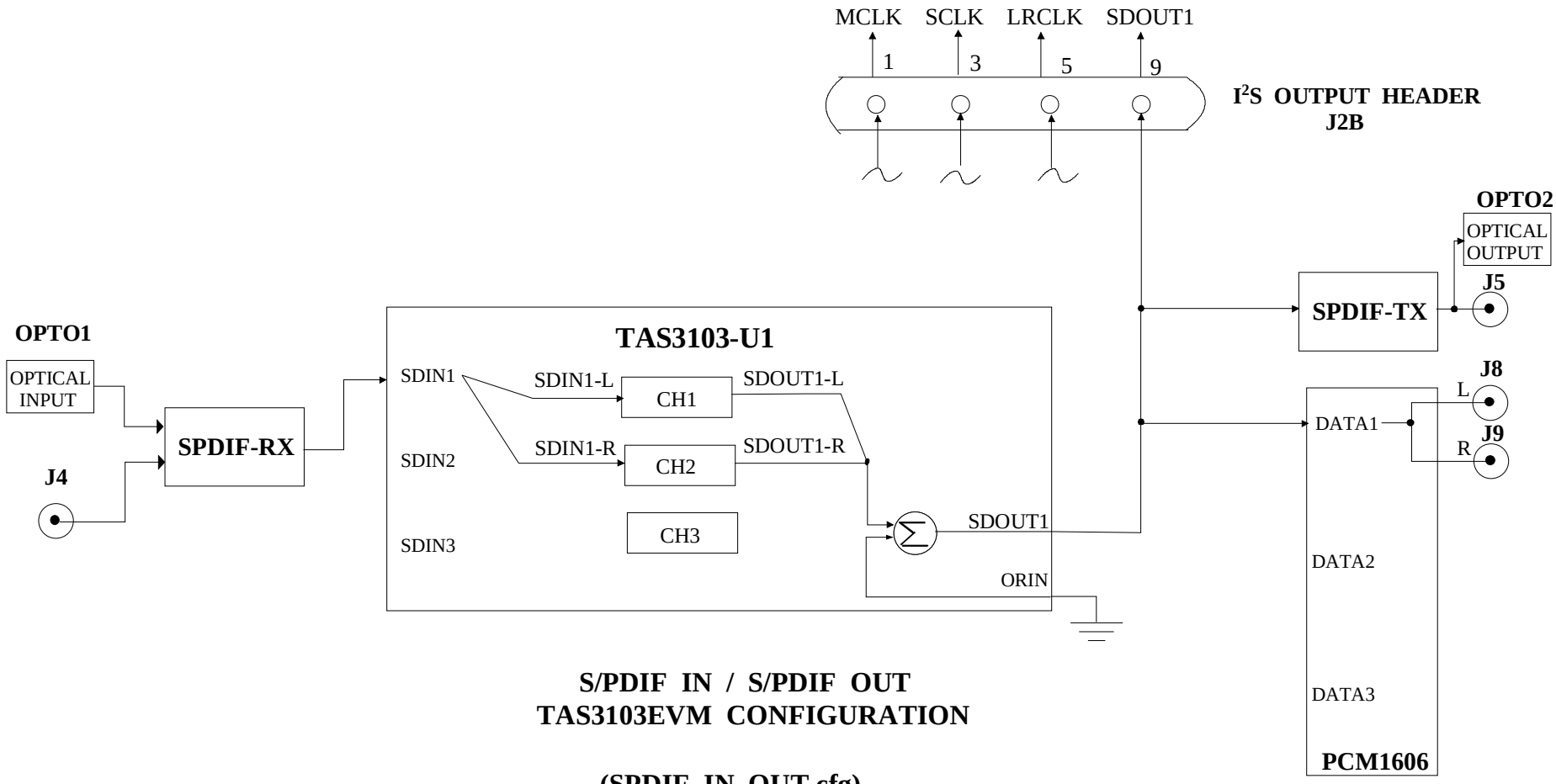
For this configuration, the S/PDIF Rx serves as the I^2S master, sourcing MCLK, SCLK, and LRCLK to TAS3103-U1, TAS3103-U2, the output DAC, and the S/PDIF Tx.

The TAS3103EVM switch settings required for Figure 1 are given in Table 1. Two shunts - JP11 and JP09 - must be installed on the TAS3103 EVM. All other shunts must be removed.

Table 1. TAS3103EVM Switch Settings For SPDIF In / SPDIF Out

Switch No.	Setting
S1	H
S2	Don't Care
S3	H
S4	L
S5	L
S6	Don't Care
S7	L
S8	H

Switch No.	Setting
S9	H
S10 (Reset)	Not Activated
S11	Don't Care
S12	Don't Care
S13	Don't Care
S14	Don't Care
S18	L



S/PDIF IN / S/PDIF OUT
TAS3103EVM CONFIGURATION

(SPDIF_IN_OUT.cfg)

Figure 1. TAS3103EVM TOPOLOGY - SPDIF IN / SPDIF OUT

4 ANALOG IN - ANALOG OUT

Up to three analog stereo inputs can be accommodated with the signal flow established by configuration file ANALOG_IN_OUT.cfg, and shown in Figure 2. The analog audio connected to input jacks J6L and J6R is routed to input port SDIN2 of both TAS3103s, but is processed only by monaural channels CH1 and CH2 in TAS3103-U1. The analog audio connected to input jacks J7L and J7R is routed to input port SDIN3 of both TAS3103s, but is only processed by monaural channels CH1 and CH2 in TAS3103-U2. The analog audio connected to input jacks J5L and J5R is routed to input port SDIN1 of both TAS3103s. However, the left monaural channel - input jack J5L - is processed only by monaural channel CH3 in TAS3103-U1, and the right monaural channel - input jack J5R - is only processed by monaural channel CH3 in TAS3103-U2.

Monaural channels CH1 and CH2 share the same dynamic range block. Typically, monaural channels CH1 and CH2 are used to process left / right surround and left / right front audio. Monaural channel CH3 has its own dedicated dynamic range block, and is typically used to process center and sub-woofer audio.

The configuration of Figure 2 retains the signal assignments of the input - although this is not a requirement when using the TAS3103s. The output port SDOUT2-U1 outputs the processed audio input into port SDIN2, and becomes the serial output SDOUT2. The output port SDOUT2-U2 outputs the processed audio input into port SDIN3, and becomes the serial output SDOUT3, after passing through a multiplexer controlled by switch S6 (S6 = H).

Both TAS3103 devices are required to process the audio into input port SDIN1 as each TAS3103 has but one monaural channel (CH3) left to process audio. The audio into input port SDIN1 then must be split between the two TAS3103s. The left monaural channel of SDIN1 is routed to CH3 of TAS3103-U1. The right monaural channel of SDIN1 is routed to CH3 of TAS3103-U2. The output of CH3 in TAS3103-U2 is routed to SDOUT1-U2. SDOUT1-U2 then contains the right monaural channel of the audio input into SDIN1. Output port SDOUT1-U2 is then routed to the ORIN port of TAS3103-U1, where it is combined with the output from CH3 in TAS3103-U1. Since CH3 in TAS3103-U1 contains the left monaural channel of the audio input into SDIN1, the combination (summation) reconstructs the audio input into input port SDIN1. The output of the summation node is routed to SDOUT1-U1. SDOUT1-U1 then contains the processed audio input into port SDIN1, and becomes the serial output SDOUT1.

The volume level is set to -12 dB for all channels.

For this configuration, TAS3103-U1 serves as an I^2S master, sourcing MCLK, SCLK, and LRCLK to the input ADCs, TAS3103-U2, the output DAC, and the S/PDIF Tx. The 12.288 MHz crystal (Y1) is used as the frequency reference.

All three output channels - SDOUT1, SDOUT2, and SDOUT3 - are routed to the 6-channel PCM1606 DAC and the I^2S Output Header J2B. MCLK, SCLK, and LRCLK are also provided on the I^2S Output Header. In addition, SDOUT1 is routed to the S/PDIF Tx, and the S/PDIF output is available on both the optical TOSLINK connector OPTO2 and the coaxial connector J5.

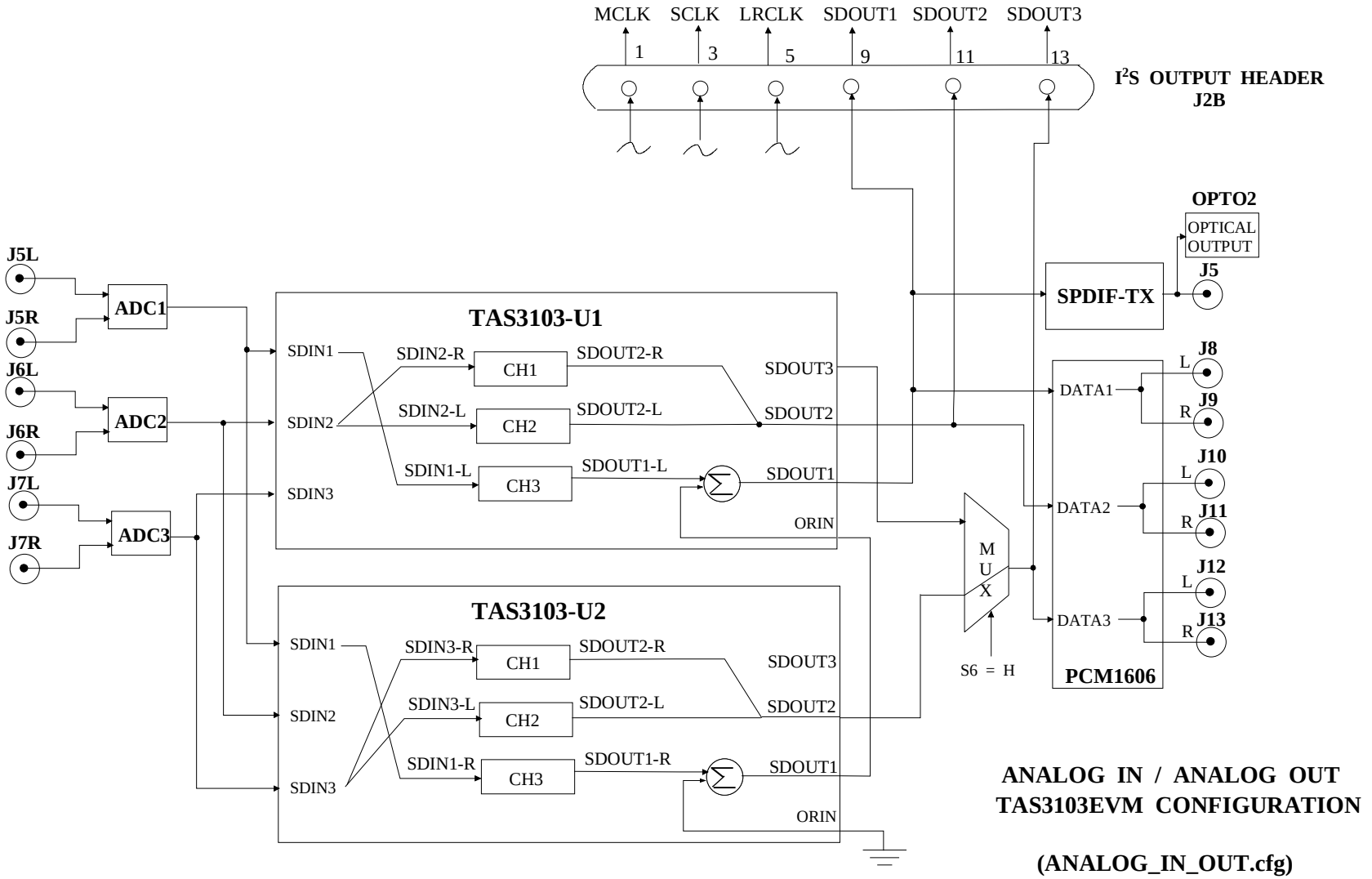


Figure 2. TAS3103EVM TOPOLOGY - ANALOG IN / ANALOG OUT

The TAS3103EVM switch settings required for Figure 2 are given in Table 2.

Table 2. TAS3103EVM Switch Settings For Analog In / Analog Out

Switch No.	Setting
S1	L
S2	H
S3	Don't Care
S4	H
S5	Don't Care
S6	H
S7	H
S8	H

Switch No.	Setting
S9	H
S10 (Reset)	Not Activated
S11	L
S12	H
S13	Don't Care
S14	H
S18	H

For this configuration only one shunt should be installed on the TAS3103 EVM - shunt JP9. If shunt JP11 is installed, it must be removed to enable the 12.288 MHz crystal used by TAS3103-U1 to derive the I^2S clocks.

5 I^2S IN - I^2S OUT

The TAS3103EVM can accommodate up to four stereo I^2S input data streams. The example shown in Figure 3 only processes three stereo I^2S input data streams, input via the I^2S Input Header (J1B). The processing flow through the two TAS3103s is identical to the previous ANALOG IN – ANALOG OUT example. This example then assumes that I^2S ports SDIN2 and SDIN3 are left / right surround audio and left / right front audio respectively, and I^2S input port SDIN1 is sub-woofer / center audio. Twenty four bit I^2S formatted audio data is assumed.

The output audio flow from the two TAS3103s is also identical to that for the ANALOG IN – ANALOG OUT case, and the volume level is set to -12 dB for all channels (as was also the case for the ANALOG IN – ANALOG OUT configuration).

One option for this configuration is to have the I^2S Input Header source MCLK, SCLK, and LRCLK. In this case, the two TAS3103s are configured as I^2S slave devices.

The TAS3103EVM switch settings required for this case are given in Table 3. Two shunts - JP11 and JP09 - must be installed on the TAS3103 EVM. All other shunts must be removed. Configuration file I^2S_IN_OUT.cfg supports this option.

Table 3. TAS3103EVM Switch Settings For I^2S In / I^2S Out – External MCLK

Switch No.	Setting
S1	H
S2	L
S3	L
S4	H
S5	H
S6	H
S7	L
S8	H

Switch No.	Setting
S9	H
S10 (Reset)	Not Activated
S11	L
S12	H
S13	Don't Care
S14	H
S18	H

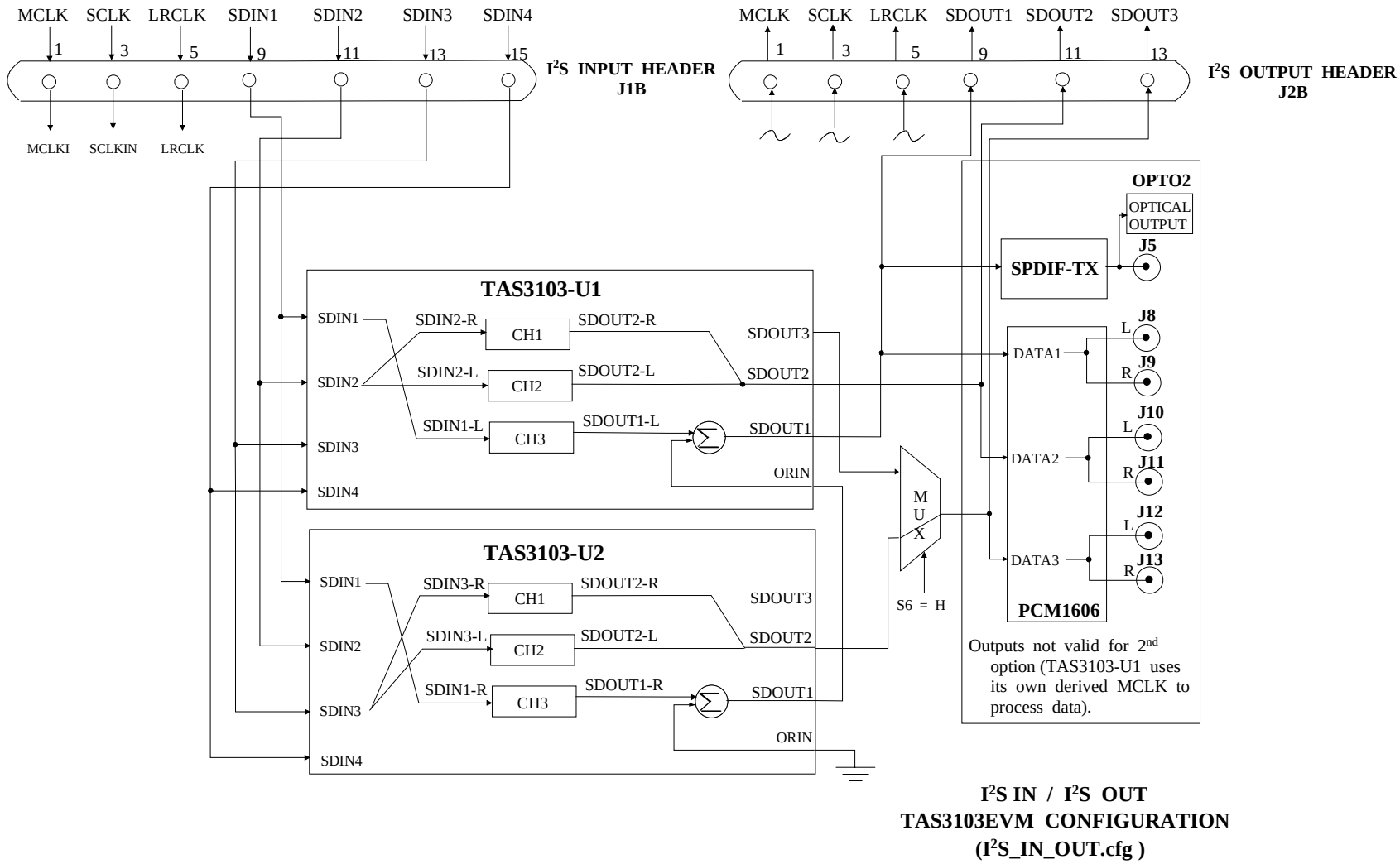


Figure 3. TAS3103EVM TOPOLOGY – I²S IN / I²S OUT

It may not be convenient to route MCLK to the TAS3103 EVM. The TAS3103 can derive its own MCLK from an external crystal, even when in the I^2S slave mode, leaving the I^2S Input Header to source only SCLK and LRCLK. (The TAS3103 is capable of generating its own MCLK – using an external crystal as a frequency reference - when in either the I^2S slave mode or the I^2S master mode. This capability means that the TAS3103 does not require MCLK be synchronous to SCLK or LRCLK). The switch settings given in Table 4 configure the TAS3103EVM to source MCLK (via TAS3103-U1).

Table 4. TAS3103EVM Switch Settings For I^2S In / I^2S Out – No External MCLK

Switch No.	Setting
S1	L
S2	L
S3	L
S4	H
S5	Don't Care
S6	H
S7	L
S8	H

Switch No.	Setting
S9	H
S10 (Reset)	Not Activated
S11	L
S12	H
S13	Don't Care
S14	H
S18	H

For this option to the configuration of Figure 3, only one shunt is installed on the TAS3103 EVM - shunt JP9. If shunt JP11 is installed, it must be removed.

Configuration file I^2S_IN_OUT.cfg also supports this option. The only valid processed output data on the TAS3103EVM for this second option is the data routed to the I^2S Output Header J2B. The S/PDIF output and the analog output channels are not valid, as the S/PDIF Tx and the 6 channel DAC use MCLKO from TAS3103-U1, which is not synchronous to the incoming data (SCLK and LRCLK).

The second option also supports applications where MCLK is sourced by TAS3103-U1 and routed to external audio sources via the I^2S Output Header (J2B). The audio, derived from this supplied MCLK, is then routed into I^2S Input Header where it is received by the two TAS3103s as per Figure 3. In this scenario, the S/PDIF output and the analog output channels would be valid outputs.

6 TDM IN - ANALOG OUT

The TAS3103 can accommodate multiple TDM (time-division-multiplex) serial digital data formats (see Section 2.1 in the TAS3103 Data Manual – SLES038A). The topology example given in Figure 4 assumes a 6 channel I^2S TDM input (8 channel I^2S TDM format) via the I^2S Input Header (J1B) and a 6 channel analog output. Twenty four bit I^2S formatted audio data is assumed.

The processing flow through the two TAS3103s is very similar to the previous ANALOG IN – ANALOG OUT and I^2S IN – I^2S OUT examples. The only difference, as shown in Figure 4, is that the 6 channels are all extracted from SDIN1. The assumed placement of left / right surround audio, left / right front audio, and sub-woofer / center audio in the TDM data stream, for this example, is also shown in Figure 4.

The discrete output audio flow from the two TAS3103s is identical to previous ANALOG IN – ANALOG OUT and I^2S IN – I^2S OUT examples, and the volume level is set to -12 dB for all channels.

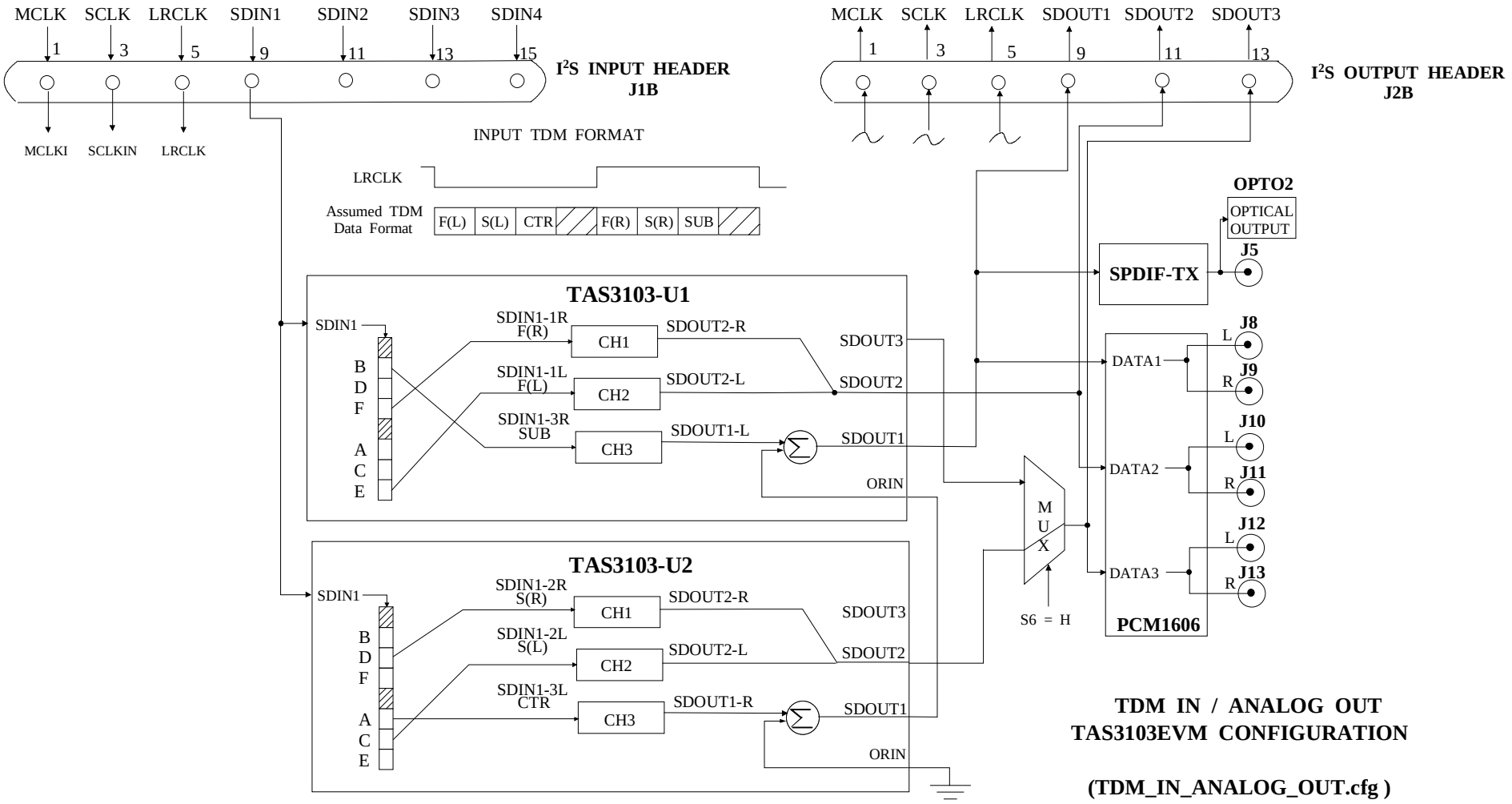


Figure 4. TAS3103EVM TOPOLOGY – TDM IN / ANALOG OUT

This example assumes that the I^2S Input Header sources MCLK, SCLK, and LRCLK. The configuration file for this example is TDM_IN_ANALOG_OUT.cfg.

The TAS3103EVM switch settings required for this case are identical to those for the first option in the previous I^2S IN - I^2S OUT case, and are repeated in Table 5.

Table 5. TAS3103EVM Switch Settings For TDM In / Analog Out

Switch No.	Setting	Switch No.	Setting
S1	H	S9	H
S2	L	S10 (Reset)	Not Activated
S3	L	S11	L
S4	H	S12	H
S5	H	S13	Don't Care
S6	H	S14	H
S7	L	S18	H
S8	H		

Two shunts - JP11 and JP09 - must be installed on the TAS3103 EVM. All other shunts must be removed.

APPENDIX A

Figures 5 - 11 are the TAS3103EVM configuration files for the topologies covered in this Application Note. Only those sub-addresses that require changes from the initial chip state set after power turn-on or after a reset are included in these files. Sub-addresses are also included to provide the same resulting configuration if the file is downloaded from the state set by the TAS3103 GUI upon activation.

```
// I2S Command Word
Xf9
01 01 24 33

// Input Mixers
// Mix A to a - SDIN1 -
X01
00 80 00 00
// Mix B to b - SDIN1 - R
X08
00 80 00 00
// Mix C to f - SDIN2 - L
X12
00 00 00 00
// Mix D to f - SDIN2 - R
X18
00 00 00 00

// Reverb Mixers
// ByPass (Rg0) / InLine (Rg1)
// a_de path (CH1 Reverb)
X4c
00 80 00 00
00 00 00 00
// b_de path (CH2 Reverb)
X4d
00 80 00 00
00 00 00 00
// f_CH3 path (CH3 Reverb)
X4e
00 80 00 00
00 00 00 00

// Bass and Treble Mixers
// CH1  - Bypass / InLine
X73
00 80 00 00
00 00 00 00
// CH2  - Bypass / InLine
X74
00 80 00 00
00 00 00 00
// CH3  - Bypass / InLine
X75
00 80 00 00
00 00 00 00

// Output Mixers
// Mix x to W- SDOUT2 - L
X99
00 00 00 00
// Mix r to X- SDOUT2 - R
X9e
00 00 00 00

// CH1 Volume
Xf2
00 20 00 00

// CH2 Volume
Xf3
00 20 00 00

// CH3 Volume
Xf4
00 20 00 00

// Bass Filter Set Selection
Xf5
00 03 03 03

// Treble Filter Set Selection
Xf7
00 03 03 03
```

Figure 5. S/PDIF_IN_OUT_U1.cfg

```
// I2S Command Word
Xf9
01 42 24 33

// Input Mixers
// Mix A to a - SDIN1 - L
X01
00 00 00 00
// Mix A to f - SDIN1 -
X06
00 80 00 00
// Mix B to b - SDIN1 -
X08
00 00 00 00
// Mix C to b - SDIN2 -
X0e
00 80 00 00
// Mix C to f - SDIN2 -
X12
00 00 00 00
// Mix D to a - SDIN2 -
X13
00 80 00 00
// Mix D to f - SDIN2 -
X18
00 00 00 00

// Reverb Mixers
//ByPass (Rg0) / InLine (Rg1)
// a_de path (CH1 Reverb)
X4c
00 80 00 00
00 00 00 00
// b_de path (CH2 Reverb)
X4d
00 80 00 00
00 00 00 00
// f_CH3 path (CH3 Reverb)
X4e
00 80 00 00
00 00 00 00

// Bass and Treble Mixers
// CH1  - Bypass / InLine
X73
00 80 00 00
00 00 00 00
// CH2  - Bypass / InLine
X74
00 80 00 00
00 00 00 00
```

```
// CH3  - Bypass / InLine
X75
00 80 00 00
00 00 00 00

// Output Mixers
// Mix z to X - SDOUT2 - R
X8c
00 80 00 00
// Mix z to U - SDOUT1 - L
X8f
00 00 00 00
// Mix y to W - SDOUT2 - L
X93
00 80 00 00
// Mix y to V - SDOUT1 - R
X94
00 00 00 00
// Mix x to W- SDOUT2 - L
X99
00 00 00 00
// Mix x to U - SDOUT1 - L
X9b
00 80 00 00
// Mix r to X- SDOUT2 - R
X9e
00 00 00 00

// CH1 Volume
Xf2
00 20 00 00

// CH2 Volume
Xf3
00 20 00 00

// CH3 Volume
Xf4
00 20 00 00

// Bass Filter Set Selection
Xf5
00 03 03 03

// Treble Filter Set Selection
Xf7
00 03 03 03
```

Figure 6. ANALOG_IN_OUT_U1.cfg

```
// I2S Command Word
Xf9
01 01 24 33

// Input Mixers
// Mix A to a - SDIN1 - L
X01
00 00 00 00
// Mix B to b - SDIN1 - R
X08
00 00 00 00
// Mix B to f - SDIN1 - R
X0c
00 80 00 00
// Mix C to f - SDIN2 - L
X12
00 00 00 00
// Mix D to f - SDIN2 - R
X18
00 00 00 00
// Mix E to b - SDIN3 - L
X1a
00 80 00 00
// Mix F to a - SDIN3 - R
X1f
00 80 00 00

// Reverb Mixers
// ByPass (Rg0) / InLine (Rg1)
// a_de path (CH1 Reverb)
X4c
00 80 00 00
00 00 00 00
// b_de path (CH2 Reverb)
X4d
00 80 00 00
00 00 00 00
// f_CH3 path (CH3 Reverb)
X4e
00 80 00 00
00 00 00 00

// Bass and Treble Mixers
// CH1  - Bypass / InLine
X73
00 80 00 00
00 00 00 00
```

```
// CH2  - Bypass / InLine
X74
00 80 00 00
00 00 00 00
// CH3  - Bypass / InLine
X75
00 80 00 00
00 00 00 00

// Output Mixers
// Mix z to X - CH1 to SDOUT2 - R
X8c
00 80 00 00
// Mix z to U - CH1 to SDOUT1 - L
X8f
00 00 00 00
// Mix y to W - CH2 to SDOUT2 - L
X93
00 80 00 00
// Mix y to V - CH2 to SDOUT1 - R
X94
00 00 00 00
// Mix x to W- CH3 to SDOUT2 - L
X99
00 00 00 00
// Mix x to V- CH3 to SDOUT1 - R
X9a
00 80 00 00
// Mix r to X- CH1 + CH2 combination to
SDOUT2 - R
X9e
00 00 00 00

// CH1 Volume
Xf2
00 20 00 00

// CH2 Volume
Xf3
00 20 00 00

// CH3 Volume
Xf4
00 20 00 00

// Bass Filter Set Selection
Xf5
00 03 03 03

// Treble Filter Set Selection
Xf7
00 03 03 03
```

Figure 7. ANALOG_IN_OUT_U2.cfg

```
// I2S Command Word
Xf9
01 01 24 33

// Input Mixers
// Mix A to a - SDIN1 - L
X01
00 00 00 00
// Mix A to f - SDIN1 - L
X06
00 80 00 00
// Mix B to b - SDIN1 - R
X08
00 00 00 00
// Mix C to b - SDIN2 - L
X0e
00 80 00 00
// Mix C to f - SDIN2 - L
X12
00 00 00 00
// Mix D to a - SDIN2 - R
X13
00 80 00 00
// Mix D to f - SDIN2 - R
X18
00 00 00 00

// Reverb Mixers
// ByPass (Rg0) / InLine (Rg1)
// a_de path (CH1 Reverb)
X4c
00 80 00 00
00 00 00 00
// b_de path (CH2 Reverb)
X4d
00 80 00 00
00 00 00 00
// f_CH3 path (CH3 Reverb)
X4e
00 80 00 00
00 00 00 00

// Bass and Treble Mixers
// CH1  - Bypass / InLine
X73
00 80 00 00
00 00 00 00
```

```
// CH2  - Bypass / InLine
X74
00 80 00 00
00 00 00 00
// CH3  - Bypass / InLine
X75
00 80 00 00
00 00 00 00

// Output Mixers
// Mix z to X - SDOUT2 - R
X8c
00 80 00 00
// Mix z to U - SDOUT1 - L
X8f
00 00 00 00
// Mix y to W - SDOUT2 - L
X93
00 80 00 00
// Mix y to V - SDOUT1 - R
X94
00 00 00 00
// Mix x to W- SDOUT2 - L
X99
00 00 00 00
// Mix x to U - SDOUT1 - L
X9b
00 80 00 00
// Mix r to X- SDOUT2 - R
X9e
00 00 00 00

// CH1 Volume
Xf2
00 20 00 00
// CH2 Volume
Xf3
00 20 00 00
// CH3 Volume
Xf4
00 20 00 00

// Bass Filter Set Selection
Xf5
00 03 03 03

// Treble Filter Set Selection
Xf7
00 03 03 03
```

Figure 8. I2S_IN_OUT_U1.cfg

```
// I2S Command Word
Xf9
01 01 24 33

// Input Mixers
// Mix A to a - SDIN1 - L
X01
00 00 00 00
// Mix B to b - SDIN1 - R
X08
00 00 00 00
// Mix B to f - SDIN1 - R
X0c
00 80 00 00
// Mix C to f - SDIN2 - L
X12
00 00 00 00
// Mix D to f - SDIN2 - R
X18
00 00 00 00
// Mix E to b - SDIN3 - L
X1a
00 80 00 00
// Mix F to a - SDIN3 - R
X1f
00 80 00 00

// Reverb Mixers
// ByPass (Rg0) / InLine (Rg1)
// a_de path (CH1 Reverb)
X4c
00 80 00 00
00 00 00 00
// b_de path (CH2 Reverb)
X4d
00 80 00 00
00 00 00 00
// f_CH3 path (CH3 Reverb)
X4e
00 80 00 00
00 00 00 00

// Bass and Treble Mixers
// CH1  - Bypass / InLine
X73
00 80 00 00
00 00 00 00
// CH2  - Bypass / InLine
X74
00 80 00 00
00 00 00 00
// CH3  - Bypass / InLine
X75
00 80 00 00
00 00 00 00

// Output Mixers
// Mix z to X - SDOUT2 - R
X8c
00 80 00 00
// Mix z to U - SDOUT1 - L
X8f
00 00 00 00
// Mix y to W - SDOUT2 - L
X93
00 80 00 00
// Mix y to V - SDOUT1 - R
X94
00 00 00 00
// Mix x to W- SDOUT2 - L
X99
00 00 00 00
// Mix x to V- SDOUT1 - R
X9a
00 80 00 00
// Mix r to X- SDOUT2 - R
X9e
00 00 00 00

// CH1 Volume
Xf2
00 20 00 00
// CH2 Volume
Xf3
00 20 00 00
// CH3 Volume
Xf4
00 20 00 00

// Bass Filter Set Selection
Xf5
00 03 03 03

// Treble Filter Set Selection
Xf7
00 03 03 03
```

Figure 9. I2S_IN_OUT_U2.cfg

```
// I2S Command Word
Xf9
04 01 24 EE

// Input Mixers
// Mix A to a - SDIN1 - L
X01
00 00 00 00
// Mix B to b - SDIN1 - R
X08
00 00 00 00
// Mix B to f - SDIN1 - R
X0c
00 80 00 00
// Mix C to f - SDIN2 - L
X12
00 00 00 00
// Mix D to f - SDIN2 - R
X18
00 00 00 00
// Mix E to b - SDIN3 - L
X1a
00 80 00 00
// Mix F to a - SDIN3 - R
X1f
00 80 00 00

// Reverb Mixers
//ByPass (Rg0) / InLine (Rg1)
// a_de path (CH1 Reverb)
X4c
00 80 00 00
00 00 00 00
// b_de path (CH2 Reverb)
X4d
00 80 00 00
00 00 00 00
// f_CH3 path (CH3 Reverb)
X4e
00 80 00 00
00 00 00 00

// Bass and Treble Bypass / InLine Mixers
// CH1  - Bypass / InLine
X73
00 80 00 00
00 00 00 00
```

```
// CH2  - Bypass / InLine
X74
00 80 00 00
00 00 00 00
// CH3  - Bypass / InLine
X75
00 80 00 00
00 00 00 00

// Output Mixers
// Mix z to X - SDOUT2 - R
X8c
00 80 00 00
// Mix z to U - SDOUT1 - L
X8f
00 00 00 00
// Mix y to W - SDOUT2 - L
X93
00 80 00 00
// Mix y to V - SDOUT1 - R
X94
00 00 00 00
// Mix x to W - SDOUT2 - L
X99
00 00 00 00
// Mix x to U - SDOUT1 - L
X9b
00 80 00 00
// Mix r to X - SDOUT2 - R
X9e
00 00 00 00

// CH1 Volume
Xf2
00 20 00 00
// CH2 Volume
Xf3
00 20 00 00
// CH3 Volume
Xf4
00 20 00 00

// Bass Filter Set Selection
Xf5
00 03 03 03

// Treble Filter Set Selection
Xf7
00 03 03 03
```

Figure 10. TDM_IN_ANALOG_OUT_U1.cfg

```
// I2S Command Word
Xf9
04 01 24 EE

// Input Mixers
// Mix A to a - SDIN1 - L
X01
00 00 00 00
// Mix A to f - SDIN1 - L
X06
00 80 00 00
// Mix B to b - SDIN1 - R
X08
00 00 00 00
// Mix C to b - SDIN2 - L
X0e
00 80 00 00
// Mix C to f - SDIN2 - L
X12
00 00 00 00
// Mix D to a - SDIN2 - R
X13
00 80 00 00
// Mix D to f - SDIN2 - R
X18
00 00 00 00

// Reverb Mixers
//ByPass (Rg0) / InLine (Rg1)
// a_de path (CH1 Reverb)
X4c
00 80 00 00
00 00 00 00
// b_de path (CH2 Reverb)
X4d
00 80 00 00
00 00 00 00
// f_CH3 path (CH3 Reverb)
X4e
00 80 00 00
00 00 00 00

// Bass and Treble Bypass / InLine Mixers
// CH1  - Bypass / InLine
X73
00 80 00 00
00 00 00 00
```

```
// CH2  - Bypass / InLine
X74
00 80 00 00
00 00 00 00
// CH3  - Bypass / InLine
X75
00 80 00 00
00 00 00 00

// Output Mixers
// Mix z to X - SDOUT2 - R
X8c
00 80 00 00
// Mix z to U - SDOUT1 - L
X8f
00 00 00 00
// Mix y to W - SDOUT2 - L
X93
00 80 00 00
// Mix y to V - SDOUT1 - R
X94
00 00 00 00
// Mix x to W - SDOUT2 - L
X99
00 00 00 00
// Mix x to V - SDOUT1 - R
X9a
00 80 00 00
// Mix r to X - SDOUT2 - R
X9e
00 00 00 00

// CH1 Volume
Xf2
00 20 00 00
// CH2 Volume
Xf3
00 20 00 00
// CH3 Volume
Xf4
00 20 00 00

// Bass Filter Set Selection
Xf5
00 03 03 03

// Treble Filter Set Selection
Xf7
00 03 03 03
```

Figure 11. TDM_IN_ANALOG_OUT_U2.cfg

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