TVP5146 Frequently Asked Questions

HPA Digital Audio Video

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ABSTRACT

The following frequently asked questions (FAQ) on the TVP5146 are from a variety of sources covering many aspects of the device itself, its features, application and EVM. This document is organized into sections related to different areas of the TVP5146. Questions related to multiple areas are shown in each area along with the corresponding answer.

The size of this document and the number of questions covered may make it difficult to locate an FAQ. If this is the case, try using the Search tool to locate specific words associated with the FAQ.

Questions not covered in this document may be available by referring to the TVP5146 Data Manual, SLES084, as well as the various application notes and user guides available at www.ti.com.

1 Input and Output Formats and Standards

1. What inputs are supported with the TVP5146?

   The TVP5146 supports composite (CVBS), S-Video, component YPbPr (480i, 576i), component RGB and SCART. It also supports digital RGB inputs for character data overlay from a Line 21 decoder or other VBI data decoder.

2. What is the difference between YCbCr and YPbPr?

   These two are sometimes used incorrectly in datasheets, application notes and even customer user manuals. YPbPr and YCbCr by definition are respectively, the analog and digital representations of the same color space, YUV.

   YPbPr is the three signal analog video component interface specified in EIA-770. It is the analog representation of YCbCr.

   YCbCr is a scaled and offset version of the YUV digital color space. It is YCbCr that is used in the ITU-R BT.601 and ITU-R BT.656 specifications.

3. When using YPbPr or RGB component video inputs, which filters are bypassed?

   When using analog component video inputs, the decimation remains active and all other filters are automatically bypassed so that bandwidth is preserved.

4. What is SCART?

   SCART is a connection interface used primarily in Europe. It uses the component RGB inputs and a CVBS input. Some SCART connections may incorporate a fast switch overlay signal that can be connected to the FSS pin of the TVP5146.

5. What is the difference between FSO and FSS?

   FSO is the Fast Switch Overlay input signal for the digital RGB overlay feature (the TVP5146 pin 57). This allows the digital RGB data from a Line 21 decoder or other VBI decoder to be soft mixed onto any selected analog input into the TVP5146.

   FSS, the TVP5146 pin 35, is the Fast Switch SCART input signal for the analog component RGB overlay feature of the TVP5146. This allows, for example, a CVBS input to be overlaid onto a component RGB input for a SCART interface.

6. What input video formats are supported with the TVP5146?

The TVP5146 supports the following video formats:

- NTSC (J, M, 4.43)
- PAL (B, D, G, H, I, M, N, Nc, 60)
- SECAM (B, D, G, K, K1, L)

7. Does the TVP5146 autoswitch or auto-detect? What is the difference?

   The TVP5146 performs autoswitch meaning that it automatically detects and then reinitializes itself to decode the input video standard without reprogramming I2C register settings.

   Autoswitch is the ability for a video decoder to detect and then automatically reconfigure itself to adapt to an input video standard. Auto-detect only detects the video standard and then relies on a backend to reinitialize it.

8. Do all of the video standards autoswitch by default?

   No, by default only the following video standards are supported in the autoswitch.

   - NTSC (J, M)
   - PAL (B, D, G, H, I)
   - SECAM (B, D, G, K, K1, L)

   The remaining video standards (PAL-M, N, and NTSC 4.43) are masked off and require a register write to enable them in the autoswitch process. Once they are enabled in the autoswitch process, it is not necessary to enable them again unless a HW reset is performed.

9. Does the TVP5146 support EDTV (480p, 576p) or HDTV (720i, 720p, 1080i)?

   No, the TVP5146 does not support EDTV or HDTV modes.

10. What alternatives do I have if I need to support HDTV?

    We recommend looking into the Texas Instruments Triple Video ADCs. These devices support both VESA mode graphics and HD inputs.

11. Does the TVP5146 support VESA mode (PC graphic) inputs?

    No, the TVP5146 does not support VESA mode inputs.

12. What alternatives do I have if I need to support VESA mode inputs?

    We recommend looking into the Texas Instruments Triple Video ADCs. These devices support both VESA mode graphics and HD inputs.

13. What outputs does the TVP5146 support?

    The TVP5146 supports the following user programmable video output formats:

    - 8/10-bit ITU-R BT.656 4:2:2 YCbCr with embedded syncs
    - 8/10-bit 4:2:2 YCbCr with discrete syncs
    - 16/20-bit 4:2:2 YCbCr with discrete syncs
    - 2x sampled raw VBI data in active video during a vertical blanking period
    - Sliced VBI data during a vertical blanking period or active video period (Full Field mode)

14. Can I use ITU-R BT.656 and still use the HSYNC and VSYNC outputs?

    Yes, the HSYNC and VSYNC outputs from the TVP5146 are still available when outputting ITU-656 digital video outputs.

15. Does the TVP5146 have a built in scaler?

    No, the TVP5146 does not have a built in scaler. The TVP5146 does however support AVID cropping. While all of the video data is still output from the TVP5146, AVID, a programmable signal representing the active video data, can be used to gate the amount of active data taken into a backend device. This signal would work similar to a Write Enable on a backend processor.

16. Does the TVP5146 support 4:2:0 outputs?

    No, the TVP5146 does not support 4:2:0 sampled digital video outputs.

17. When switching between inputs, how many fields does it take to lock? Is it possible to enable a faster lock speed?

    The TVP5146 takes approximately 12 fields when switching between inputs. The fast lock speed within the TVP5146 is optimized by default.

18. Will the TVP5146 automatically detect whether composite (CVBS), S-Video or component video input are connected?

No, the TVP5146 does not automatically detect inputs. It only detects and autoswitchs input video standards on the selected video input.

19. Does the TVP5146 have an external output enable (OE) pin?

No, the TVP5146 does not have an external OE pin. The OE enable for the digital data output and the clocks is available via the Output Formatter 2 Register, 34h, bit 4 and bit 0, respectively. By default both the data outputs and clock outputs are high impedance.

20. Can the TVP5146 detect sync on green/luma?

Yes, the TVP5146 can detect sync on green from YPbPr or component RGB analog inputs supporting SDTV (480i, 576i) resolutions only. The TVP5146 does not detect sync on green for standards supporting EDTV and HDTV resolutions.

21. What happens to SCLK and the sync outputs when no video signal is present on the inputs?

If no video signal is present on the input selected into the TVP5146, the DATACLK and sync information is still valid for the last detected video standard, and the video data output is black.

22. Does the TVP5146 oversample the input? How does it meet the 13.5-MHz output from the ITU-R BT.601 specification?

Yes, the TVP5146 performs 2x oversampling on all analog input signals. The ADC outputs are then decimated to reduce the data rate to 1x the pixel rate. This oversampling and decimation technique effectively increases the overall SNR by approximately 3dB.

23. What is meant by “extended coding range”?

I2C register 33h, bit 6 controls the YCbCr coding range of the digital outputs. By default the coding range is set to 1, Extended Coding Range (4 – 1016 on Y, Cb and Cr). The ITU-R BT.601 specification only allows codes of 64-940 for Y and 64-960 for Cb and Cr. To avoid clipping, the extended coding range allows for overshoot outside of the ITU-R BT.601 specification. Within the output formatter of the TVP5146, the digital outputs are then rescaled to conform to the ITU-R BT.601 or ITU-R BT.656 outputs.

24. During the horizontal and vertical blanking periods, does the TVP5146 output the digital data?

Digital data is output during vertical blanking, but not during horizontal blanking. Data during the vertical blanking can have VBI information while output data during the horizontal period is black.

25. Is it possible to mask the output data during the horizontal and vertical blanking period?

    If using ITU-R BT.656 digital outputs, only the horizontal blanking data may be masked by using the AVID cropping feature. The AVID registers are AVID Start Pixel Register, 16h – 17h, and the AVID Stop Pixel Register, 18h - 19h. Masking the data during the vertical blanking period is not available since compliance with ITU-R BT.656 must be maintained.

    If using ITU-R BT.601 digital outputs with discrete syncs then data in both the horizontal and vertical blanking periods may be masked using the AVID Start and Stop registers and the VSYNC Start and Stop registers, respectively.

26. Can the TVP5146 generate an arbitrary number of samples per line?

    No, the TVP5146 generates the standard number of samples per line based on the input video standard.

2 Initializing the TVP5146

1. Once the TVP5146 is up and running, are there additional register settings that would further optimize its performance?

   By default the video performance of the TVP5146 is considered optimized. On power up the TVP5146 is configured to enable the following:

   - Ch1A CVBS input
   - Autoswitch between NTSC, PAL and SECAM video standards
   - ITU-R BT.656 digital outputs
   - Adaptive 5-line comb filter

2. What is the minimum register writes required to begin using the TVP5146?

   In many cases most TVP5146 registers can be left at their default settings. The simplest case requires only one register write to enable video data output. The below is another simple example: Assuming the following minimum configuration, the required register settings are below:

   - Input connector: Composite (VI_1_A) (default)
   - Video format: NTSC (J, M), PAL (B, G, H, I, N) or SECAM (default)
   - Output format: 10-bit ITU-R BT.656 with embedded syncs (default)

   NOTE: NTSC-443, PAL-Nc, and PAL-M are masked from the autoswitch process by default. See the autoswitch mask register at address 04h.

The recommended I2C register settings are this setup are:

Table 1. Recommended I2C Register Settings

1	Address	08h	Luminance Processing Control 3 Register
	Data	00h	Optimizes the trap filter selection for NTSC and PAL
2	Address	0Eh	Chrominance Processing Control 3 Register
	Date	04h	Optimizes the chrominance filter selection for NTSC and PAL
3	Address	34h	Output Formatter 2 Register
	Date	11h	Enables YCbCr output and the clock output

3 I2C Communication

1. How do I configure the TVP5146 for a specific I2C address?

   The I2C address for the TVP5146 is configured using I2CA, pin 37, on the TVP5146. When pulled high the I2C address is BAh, when the I2CA pin is pulled low the I2C address is B8h.

Table 2. I2C Address Selection

I2CA	I2C Base Address
IOGND	B8h
IOVDD	BAh

2. What is the maximum I2C speed the TVP5146 will support?

   The TVP5146 I2C operates at a maximum speed of 400Kbits/sec.

3. When using the TVP5146EVM I continue to get I2C error messages. What is wrong?

   See Table 10 for trouble shooting information.

4. Can the TVP5146 be programmed while in reset?

   No, the TVP5146 cannot be programmed while in reset.

5. Can I write to reserved register bits?

The reserved registers should never be programmed. If your system automatically increments through the I2C registers as they are programmed then it is highly recommended that the reserved registers be avoided when doing so.

The default values of the register bits within active registers are defined in the I2C register summary and the register description. The default value for each register is listed here including the reserved bits. When writing to active bits within registers, it is important that the default value of any reserved bits is maintained. Also, it is not safe to assume that all reserved bits are zero. Some reserved bits may actually have a default value of 1.

6. Does the TVP5146 auto increment the I2C registers when they are programmed?

   Yes, the TVP5146 auto increments the I2C register address if multiple bytes are written using one I2C transfer.

4 Device Registers

1. Are there status registers available that indicate the horizontal and vertical lock status, field rate, color subcarrier lock status, etc?

   Yes, there are multiple status registers within the TVP5146 that provide this information. The status registers begin with the Status 1 Register, 3Ah, and end with the Vertical Line Count Register, 43h.

2. Is there a pin on the TVP5146 that provides horizontal lock or vertical lock?

   No, horizontal and vertical lock status are only currently available with the I2C status registers mentioned previously.

3. Does the TVP5146 detect Macrovision and identify which type is present?

   Yes, the TVP5146 provides status registers that indicate the type of Macrovision detected on the analog input. The Status 2 Register, 3Bh, bits [2:0] provide this information. Please refer to the TVP5146 Data Manual, SLES084, for more information.

4. Does the TVP5146 support brightness, contrast, hue and sharpness controls via I2C?

   Yes, the TVP5146 does support brightness, contrast, hue and sharpness controls via I2C. The sharpness control within the TVP5146 register map is called luma peaking. Please refer to the TVP5146 Data Manual, SLES084, for more information.

5. What is the VBUS?

   The VBUS refers to the indirect registers available within the TVP5146. The registers available through the VBUS primarily include VBI registers.

6. How do I access indirect registers?

   Access to the VBUS indirect registers is provided using the method illustrated in Figure 1. The assumed I2C device address is B8h. Since the VBUS uses 24-bit addresses, three bytes must be sent beginning with the MSB byte as VA0.

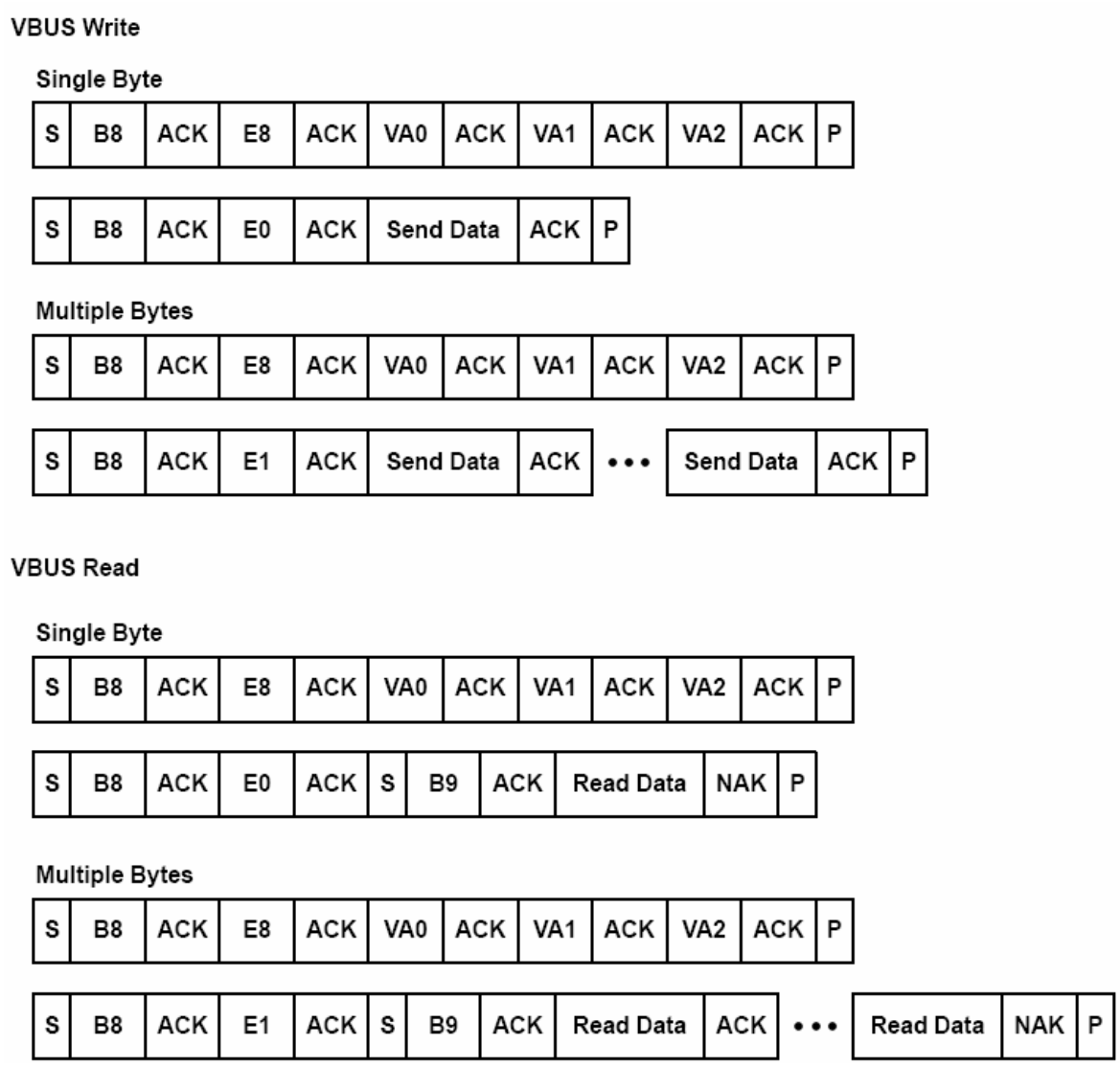

Figure 1. Access to VBUS Indirect Registers

7. Can the TVP5146 be programmed while in reset?

   No, the TVP5146 cannot be programmed while in reset.

8. Can I write to reserved register bits?

   The reserved registers should never be programmed. If your system automatically increments through the I2C registers as they are programmed then it is highly recommended that the reserved registers be avoided when doing so.

   The default values of the register bits within active registers are defined in the I2C register summary and the register description in the TVP5146 Data Manual, SLES084. The default value for each register is listed here including the reserved bits. When writing to active bits within registers, it is important that the default value of any reserved bits is maintained. Also, it is not safe to assume that all reserved bits are zero. Some reserved bits may actually have a default value of 1.

9. What is the difference between Power Save mode and Power Down mode?

   The Operation Mode Register, 03h, bits [1:0] controls the power down/save modes of the TVP5146. See Table 3 below.

   In the Power Save mode, the TVP5146 reduces the clock speed of the internal processor and powers down the ADCs. The I2C interface is active and all current registers are preserved.

   In the Power Down mode, the TVP5146 turns off all internal clocks and powers down the analog and digital cores. The I2C interface is also powered down. To power the TVP5146 back up, a hardware reset on RESETB, pin 34, is required. At this point the TVP5146 resumes operation in its default power up state. All I2C register settings also resume their default state.

Table 3. Power Down/Save Bit Selections, Register 03h, bits [1:0]

Bit 1	Bit 0	Result
0	0	Normal Operation
0	1	Power Save
1	0	Reserved
1	1	Power Down

10. Do the TVP5146 I2C registers auto increment when they are programmed?

    Yes, the TVP5146 auto increments the I2C register address if multiple bytes are written using one I2C transfer.

11. Does the TVP5146 have a software reset? Hardware reset?

Yes, the TVP5146 supports a hardware reset. An active low on RESETB, pin 34, for >200ns resets the TVP5146. A software reset within the TVP5146 is not available.

12. Are customerized register settings retained after an automatic standard switch?

Yes, internally four sets of register settings are maintained. These sets correspond to NTSC ITU-R BT.601, NTSC Square Pixel, PAL ITU-R BT.601 and PAL Square Pixel modes. Registers that are programmed to a value other than the default value retain their settings even after switching to one of the other three modes and back. These four sets of register settings are retained until a hardware reset occurs.

5 Application Circuit, Schematic and Layout

1. Do I need to use the AC coupling capacitor on the analog inputs?

Each analog input must be AC coupled through a 0.1-µF capacitor. Unused analog inputs must be AC coupled through a 0.1-µF capacitor to ground.

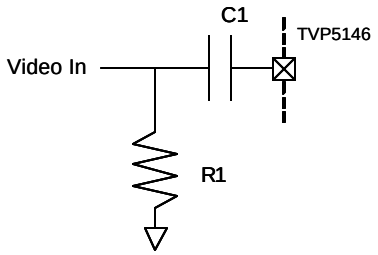

Figure 2. Recommended Analog Input Circuit

R1 = 75 Ohm

C1 = 0.1µF

2. What type of crystal should I use for the TVP5146?

We recommend using a 14.31818-MHz parallel-resonant, fundamental mode crystal, not a third-overtone crystal. The crystal tolerance should be 50ppm or better.

The manufacturer's load capacitance required should be carefully considered when designing the crystal circuit. The capacitors used on the TVP5146EVM, for instance, were chosen based on the specific crystal used.

3. Are both the 1.8-V and 3.3-V supplies required by the TVP5146?

   Yes, both voltage supplies are required to properly power the TVP5146. The 1.8-V supply is used for DVDD and AVDD18 while the 3.3-V supply is used for IOVDD and AVDD33.

4. What pins are required to be pulled up or pulled down on power up and what are their purpose? Can I still use the pin as intended without issues?

   Two pins require pull-up or pull-down resistors on power up. FID, pin 71, should always be pulled to ground through a 2.2-kOhm resistor. I2CA, pin 37, should be pulled up or down depending on the desired I2C address for the TVP5146.

   Also, it is important to note that SDA and SCL of the I2C bus require pull-ups resistors somewhere in your system's design.

5. Is a 0.1-µF decoupling capacitor required on each supply pin of the TVP5146?

   We highly recommend using a 0.1-µF capacitor on each power supply pin to reduce the level of noise in your system.

6. Can you recommend an anti-aliasing filter circuit for my design?

   Anti-alias filtering is recommended any time significant out-of-band noise is present on the inputs of the TVP5146. This noise could cause vertical or diagonal lines appear throughout picture. Important anti-alias filter characteristics:

   - Amplitude flat to Fc ~ 4.2 MHz NTSC, 5-6 MHz PAL
   - Amplitude minimal at (Fs-Fc)
   - Group delay small at subcarrier frequencies
   - For most applications they need to be inexpensive

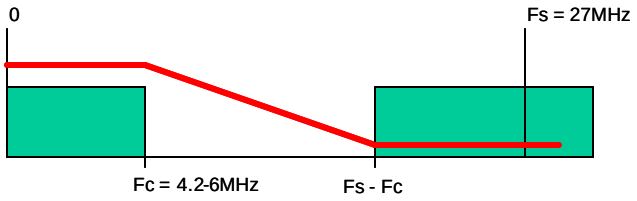

Figure 3. Anti-Aliasing – Frequency Response

The following is an inexpensive anti-alias filter that gives good results for TVP5146 inputs. This filter goes before the coupling capacitor:

- Only five components, only two inductors
- Standard values
- Excellent pass- and stop-band amplitude
- Excellent delay at Fsc for minimal chroma/luma delay

The Figure 4 presents the anti-alias filter schematics, and its characteristics are given in Table 4.

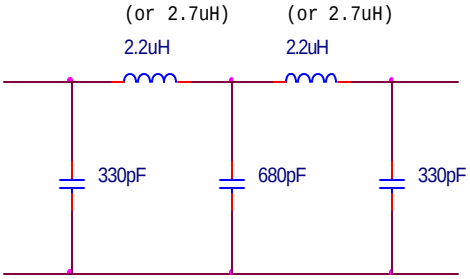

Figure 4. Anti-Aliasing Filter Example Circuit

Table 4. Anti-Aliasing Filter Design Characteristics

	With 2.2uH		With 2.7uH	
Freq (MHz)	Mag (dB)	Delay (ns)	Mag (dB)	Delay (ns)
0.01	0	0	0	0
3.58 Fsc NTSC	-0.1	5	0	11
4.2 Fc NTSC	-0.1	9	0	17
4.43 Fsc PAL	0	12	0	20
6.0 Fc PAL	0	34	-0.2	68
21.0 Fs-Fc PAL	-54		-57	
22.8 Fs-Fc NTSC	-57		-61	

7. What is the purpose of the GPIO pins?

The C bus of the digital video outputs, VS, HS, FID, FSS, and AVID pins may all be used as GPIOs. Access to these GPIO is available through I2C registers. When used as GPIO, these pins may either be configured as an input or as an output with a logic level high or low. By default, each GPIO pin is configured to be an input. If digital video outputs using ITU-R BT.601 with discrete syncs is selected, then the C bus, VS, and HS pins not available as GPIOs.

Table 5. GPIO Function Selection

GPIO Function	GPIO [1]	GPIO [0]
Logic 0 output	0	0
Logic 1 output	0	1
Reserved	1	0
Logic input (default)	1	1

8. How do I use an oscillator instead of a crystal in my design?

   To use a 14.31818-MHz oscillator instead, connect the oscillator output to the XTAL1 input. The capacitors used in the crystal circuit are not required.

9. How do I use a crystal instead of an oscillator in my design?

   The crystal design requires the use of XTAL1 and XTAL2 and two capacitors as seen in the following figure. C1 and C2 must be calculated based on the load capacitance requirements of the crystal selected. These requirements vary from manufacturer to manufacturer.

   The equation used to calculate the required capacitors is:

$$C1 = C2 = 2 \times C_{load} - C_{stray}$$

   where: C_{load} is the crystal manufacturer's load capacitance requirement

   C_{stray} is the stray capacitance (assume 3-8pF)

   Example: If C_{load} = 20pF, then C1 = 33pF, C2 = 33pF.

   Refer to Figure 5 below for TVP5146 crystal circuit information.

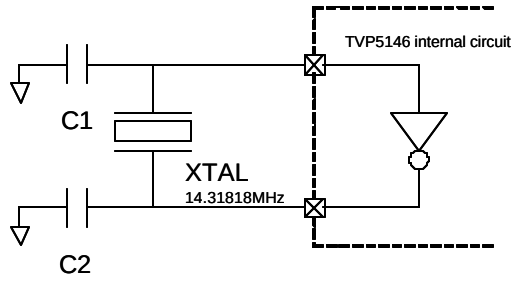

Figure 5. TVP5146 Crystal Circuit

10. How do I use the PowerPAD package for thermal dissipation?

    Please refer to *PowerPAD*™ *Thermally Enhanced Package,* SLMA002 and *PowerPAD* ™*Made Easy,* SLMA004. Information showing the thermal performance of the TVP5146 package is in SLMA002, Appendix A, under the PFP package designator.

6 System Applications & Interfaces

1. What applications or end equipments does the TVP5146 support?

   The TVP5146 supports a variety of end equipments not limited to the following:

   - Digital TV
   - LCD TV/Monitors
   - DVD Recorders (DVD-R)
   - Personal Video Recorders (PVR)
   - PC Video Cards
   - Video capture / Video editing

2. What is the purpose of the GPIO pins?

   The C bus of the digital video outputs, VS, HS, FID, FSS, and AVID pins may all be used as GPIOs. Access to these GPIO is available through I2C registers. When used as GPIO, these pins may either be configured as an input or as an output with a logic level high or low. By default, each GPIO pin is configured to be an input. If digital video outputs using ITU-R BT.601 with discrete syncs is selected, then the C bus, VS, and HS pins not available as GPIOs. See Table 5 for GPIO function selections.

3. How long must RESETB be held low in order to reset the TVP5146?

   RESETB is active low and must be pulled low for >200ns in order to reset the TVP5146.

4. I am looking for a low-power video decoder that is smaller and designed more for portable video applications. Does TI have a solution available for this?

Yes, the TVP5150A video decoder is designed specifically for portable video end equipments. This device consumes less than 150mW and is the smallest video decoder in a 32-pin QFP. Compared to typical video decoders the TVP5150A requires only 25% of the board space and consumes 20% of the power.

5. When switching between inputs, how many fields does it take to lock? Is it possible to enable a faster lock speed?

   The TVP5146 takes approximately 12 fields when switching between inputs. The fast lock speed within the TVP5146 is optimized by default.

6. My backend processor only supports 8-bits, the TVP5146 has 10-bits output. Which bits do I use to connect to my system?

   Use the MSB bits Y[9:2]. Leave the two remaining LSBs, bits Y[1:0], unconnected.

7. How do I interface the TVP5146 to my backend?

   Using the ITU-R BT.656 digital video outputs and DATACLK is the simplest interface to a backend. The required number of pins is at a minimum and no additional clocks are required. This interface only provides 8- or 10-bits of data out which includes the embedded sync information.

   If the backend does not support ITU-R BT.656 then it may be necessary to use ITU-R BT.601 digital video outputs with discrete syncs. There is no performance difference between these two interfaces. It is merely a difference in the number of required signals. With the ITU-R BT.601 interface, the backend requires the discrete HS and VS syncs as well as the digital video data and DATACLK.

8. How much current does the TVP5146 draw on the analog and digital supplies?

   The amount of current drawn on the supplies varies with the type of input being used. With a CVBS input, the typical current is shown in the following table:

Table 6. CVBS Input Current Draw

Supply	Description	Current
IOVDD	3.3-V IO digital supply current	6mA
DVDD	1.8-V digital supply current	66.2mA
AVDD33	3.3-V analog supply current	16mA
AVDD18	1.8-V analog supply current	79.3mA

9. How much current does the TVP5146 draw in the Power Down and Power Save modes?

   The amount of current drawn by the TVP5146 in the Power Down and Power Save modes is shown in the following table across each supply.

Table 7. Power Save and Power Down Mode Current Draw

Supply	Description	Power Save Current	Power Down Current
IOVDD	3.3-V IO digital supply current	1.2mA	1.2mA
DVDD	1.8-V digital supply current	15.8mA	0mA
AVDD33	3.3-V analog supply current	0mA	0mA
AVDD18	1.8-V analog supply current	9.5mA	0mA

10. Does the TVP5146 have to be the clock master?

    Yes, the TVP5146 must always provide the DATACLK, HSYNC, and VSYNC signals to the backend. The TVP5146 is not capable of receiving these signals as inputs.

11. How would a GPIO be used as a sync lock control and why?

    Using a backend device and I2C to monitor various status registers within the TVP5146, a GPIO pin could be used as a indicator flag or signal to a microprocessor or another device in the system.

7 Chrominance and Luminance

1. There are faint vertical lines in bright areas with strong color (e.g. cyan or yellow color bars). What is causing this? How do I fix it?

   This is called Chroma Clipping. The TVP5146 has protection to reduce or eliminate chroma clipping for non-standard signals. It can still show up under some circumstances though. Chroma clipping occurs when the input signal exceeds the range of the ADC which can occur when:

   - AGC turned off
   - Peak protection turned off
   - Very high amplitude signal

   It causes faint vertical lines in bright areas with highly saturated color. Example (See Figure 6): 100% color bars cyan and yellow.

   To confirm this is the problem:

- Lower saturation and/or brightness of the source and verify lines go away.
- Check amplitude of source and verify it does not exceed input range of the TVP5146.
- Turn TVP5146 AGC and peak protection back on if they are off (default is on).

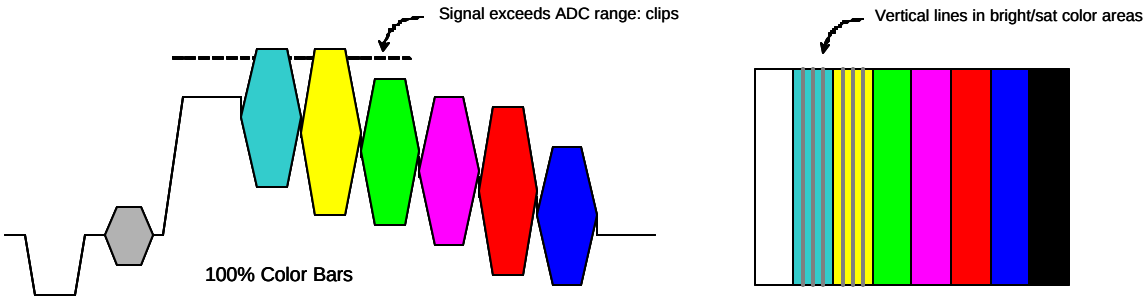

Figure 6. Faint Vertical Lines in 100% Color Bar

2. The colors on the output of the TVP5146 are reversed or improper. What is the cause and how do I fix it?

   This problem is often caused by alignment or Genlock issues. These can be very easy to diagnose with a color bar test pattern.

   Picture is entirely magenta and green: Luma and chroma are reversed. Possible reasons:

   - 10- or 20-bit mode is selected incorrectly. The decoder output and back-end input must be set to the same format, either 10-bit (8-bit) mode with multiplexed luma and chroma (includes ITU-R BT.656 mode); or 20-bit (16-bit) mode with separate luma and chroma buses.
   - Multiplexed luma and chroma are reversed. This may be affected by TVP5146 AVID Start/Stop or HSYNC, or encoder horizontal alignment adjustments.

   Red and blue color bars are reversed order: Cb and Cr are reversed. Possible reason:

   - This may be affected by TVP5146 AVID Start/Stop or HSYNC, or encoder horizontal alignment adjustments.

3. There is no color or the color is intermittent on the output of the TVP5146. What is the cause and how do I fix it?

   This is typically caused by an improperly designed crystal circuit. The load capacitance requirements from the manufacturer of the crystal are very important and must be considered when designing the crystal circuit. See previous discussions of crystal circuits.

   This issue can also be caused by the improper use of genlock/RTC. See the following Genlock and RTC section.

4. There is not a pedestal present on the output video waveform. Why is this?

   By default the TVP5146 Luminance Processing Control 1 Register, 06h, bit 6, supports a pedestal on the analog video input signal. If a pedestal is not present and this setting has not changed, then most likely the video source does not support a pedestal or the pedestal has been disabled on the video source.

5. What is CTI? How do I use it?

   Chroma (or Color) Transient Improvement (CTI) enhances horizontal color transients by delay modulation for both color difference signals. The operation should only be performed on YCbCr formatted data. The color difference signals are virtually kept constant at the start and end of a color transient, whereas time is appropriately compressed at the center of color transitions. For signals from CVBS and S-video sources the color bandwidth is limited and CTI helps to increase the perceived spatial resolution of color. Figure 7 shows the possible effect of color transient improvement.

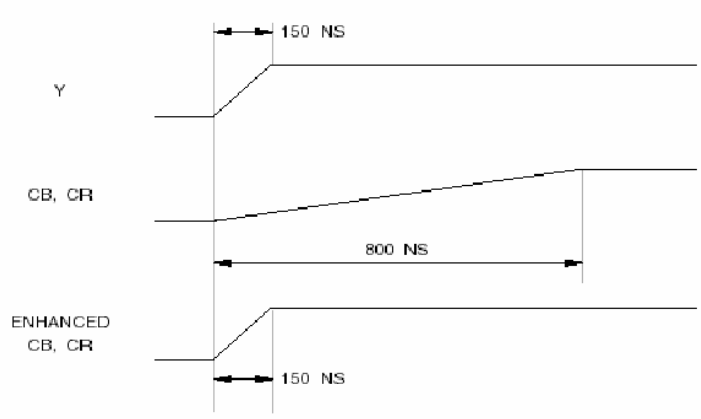

Figure 7. Color Transient Improvement

8 Genlock and RTC

1. Does my system require the use of the Genlock (RTC) or GLCO pin?

   This depends on the system. Proper composite (modulated) color requires an extremely accurate subcarrier frequency. An encoder using a line-locked clock must know when its input clock frequency changes in response to horizontal sync frequency changes at the decoder input.

The decoder and encoder use a serial data stream to transfer the color discrete-time oscillator (DTO) increment value between them, to compensate for the changing clock frequency. This data stream is called Genlock or RTC. An alternative is to use a time base corrector to change clocks.

If neither of these techniques is used, the color with a noisy or unstable signal will be streaky, flash on and off, or be absent entirely on the re-encoded composite output of the encoder.

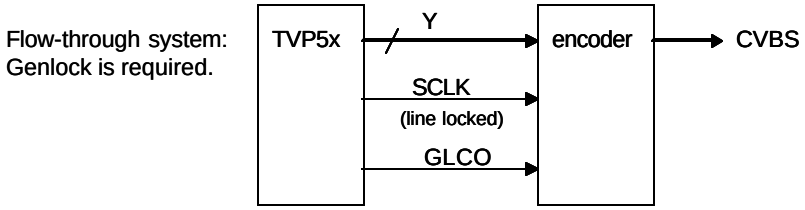

Figure 8. TVP5146 to Encoder Flow Through System – GLCO Required

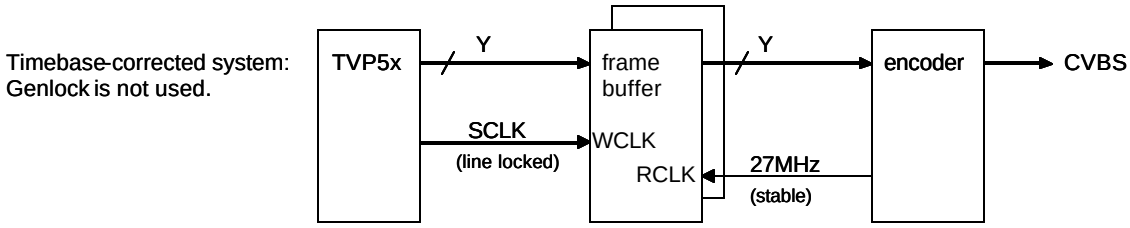

Figure 9. TVP5146 to Time Base Corrector to Encoder – GLCO Not Required

9 PLL and Sync Information

1. Can the TVP5146 be slaved to an external clock?

   No, the TVP5146 video decoder generates a clock that is locked to the sync frequency of the incoming video and cannot function as a slave to an external clock. The TVP5146 uses an external clock (crystal or oscillator) only as a reference for the PLL circuitry that generates its own clock. This clock must be 14.31818 MHz.

2. Does the TVP5146 have a built in time base corrector (TBC)?

   No, the TVP5146 does not have a built in TBC.

3. How does the TVP5146 lock to the incoming video input?

The TVP5146 line locks to the incoming analog video input. This allows the TVP5146 to track the input signal, maintain horizontal and vertical sync, and provide an equal number of pixels per line.

4. Does TVP5146 sample asynchronous to the incoming analog video?

No, by means of internal clock generation (PLL) the analog input signal is sampled synchronously (line-locked). Each horizontal line yields an integer number of samples. The video signal is two-fold over-sampled to avoid the need for sharp cut-off analog anti-aliasing filters. A digital decimation filter converts two samples to one pixel. Dependent on video standard and the choice of pixel aspect ratio (ITU-R BT.601 or square-pixel) the number of samples per line and the sampling rate amount to:

Table 8. Video Standards Information

Standard	Pixel Aspect Ratio	Samples per Line	Sample Rate [MHz]
NTSC	Square Pixel	1560	24.545
NTSC	ITU-R BT.601	1716	27
PAL / SECAM	ITU-R BT.601	1728	27
PAL / SECAM	Square Pixel	1888	29.5

The TVP5146 uses a line-locked clock to sample and output data. The clock frequency varies to ensure a constant number of pixels per line (858 NTSC, 864 PAL). Clock frequency is nominally 27 MHz but changes depending on the horizontal sync frequency. Worst case is usually VCR input with non-standard (and changing) HSYNC frequency.

TVP5146 clock is generated by the internal PLL. It is not synchronous with the reference clock on XTAL pin.

TVP5146 clock output **must** be used to drive the back end unless a time base corrector (FIFO or frame buffer) is used. If a time base corrector is used, the TVP5146 output clock must be used for its write timing.

Note: Pixel numbers and clock frequencies given are for ITU-R BT.601 sampling.

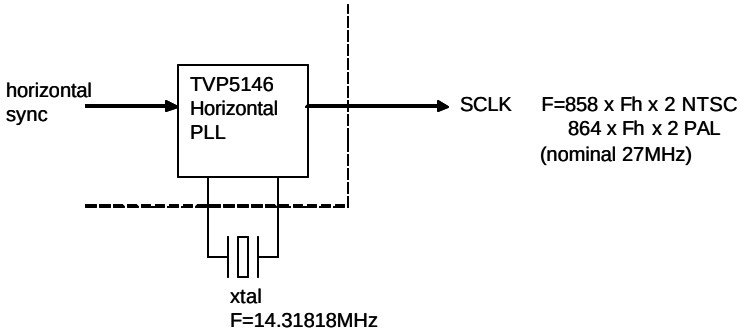

Figure 10. Line-Locked Sampling

5. Does the TVP5146 have to be the clock master?

   Yes, the TVP5146 must always provide the SCLK, HSYNC, and VSYNC signals to the backend. The TVP5146 is not capable of receiving these signals as inputs.

6. How to use a GPIO pin to control backend processor?

   Using a backend device as an I2C master to monitor various status registers within the TVP5146, normally a GPIO pin could be used as an indicator flag or signal to a microprocessor or another device in the system.

10 VBI Data Processing

1. What is the VBI data processor (VDP) and how does it work?

   VBI data is digital data that is encoded onto an analog video signal, usually transmitted in the non-active video region, vertical blanking interval (VBI). The VBI information includes many data types, current time, program info, VCR/PVR recording info, aspect ratio, etc. Some VBI information can be displayed on-screen (e.g., closed caption).

   The Vertical Blanking Interval (VBI) data processor slices various data services like teletext and closed caption that are available during the vertical blanking interval.

   These data services are acquired by programming the VDP via I2C. The results can be stored in a FIFO and made available via I2C or ancillary data.

   VBI data processing stages in a video system

   1. Capture analog waveform
   2. Slice analog waveform into data bytes
   3. Parse data bytes
   4. Decode data bytes
   5. Actions based on the data

   The TVP5146 performs only a portion of the total work required to fully decode VBI data. The TVP5146 can process VBI data up to and including step 2. Additional processing (step 3) can be applied to those with error detection/protection (e.g., Teletext: filtering of magazine/articles). The TVP5146 can perform step 4 for some VBI data (e.g., TVP5146 for V-chip info).

Other devices in a video system need to perform the full decode & actions of the VBI data. Examples: OSD display for CC, Block a channel/program based on V-chip info, Record a program according to VPS, etc.

The TVP5146 slices this digital information from the input video and supplies it to the user for processing.

The TVP5146 does **not** automatically generate overlay graphics or OSD from sliced data. An external processor or OSD controller must be used to process and display sliced OSD data.

6. What VBI data formats does the TVP5146 support?

The TVP5146 VDP supports the following formats. The User defined VBI System at the bottom of the following table is used to indicate that the VDP of the TVP5146 may be customized to support non-standard VBI systems.

Table 9. Supported VBI Data Formats

VBI SYSTEM	STANDARD
Teletext WST A	SECAM
Teletext WST B	PAL
Teletext NABTS C	NTSC
Teletext NABTS D	NTSC-J
Closed Caption	PAL
Closed Caption	NTSC
WSS	PAL
WSS-CGMS	NTSC
VITC	PAL
VITC	NTSC
VPS (PDC)	PAL
V-CHIP (Decoded)	NTSC
Gemstar 1x	NTSC
Gemstar 2x	NTSC
User	Any

7. How would I use the VDP in my application?

The Figure 11 shows one example: TVP5146 + video processor (VP) + OSD controller (OSD). In this implementation, the TVP5146 supplies VBI data, e.g., closed caption (CC) and V-chip data, to the backend video processor VP. The VP performs the VBI decoding and then the OSD controller performs the OSD operations to display CC on top of the video images.

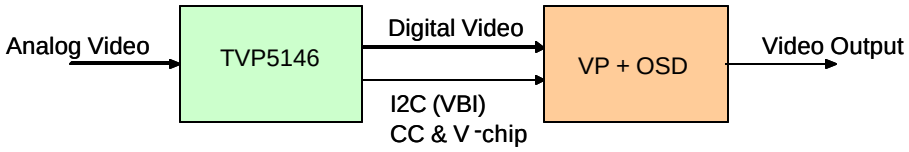

Figure 11. Example System Interface Using the VDP

8. Does VBI data processing mean the TVP5146 performs as a full Line 21 decoder or other VBI data decoding?

   No, the TVP5146 does not perform full decode of captured VBI data. It only captures, slices, and parses the VBI data bytes. It does not decode the VBI data bytes or perform actions based on them.

   The TVP5146 can perform full decode of V-Chip data. The TV Rating and MPAA Rating provided by the V-Chip data are available by reading indirect addresses 800540h – 800543h.

9. How do I access indirect registers?

   Access to the VBUS indirect registers is provided using the method illustrated in Figure 1. The assumed I2C device address is B8h. Since the VBUS uses 24-bit addresses, three bytes must be sent beginning with the MSB byte as VA0.

11 Macrovision

1. What version of Macrovision™ does the TVP5146 support?

   The TVP5146 is capable of detecting Type 1, Type 2 and Type 3 Macrovision™ as well as color striping. The detection of these different types is provided in the Status 2 Register, 3Bh, bits [2:0].

12 RGB Overlay

1. What is the difference between the analog RGB overlay and the digital RGB overlay?

   The analog RGB overlay is a feature designed to support SCART. Using the FSS input, a CVBS input can be soft mixed with the RGB input all within the TVP5146.

The digital RGB overlay is a feature designed to support the digital character data from a Line 21 decoder or other VBI decoders. The digital character data using the FSO input, can be soft mixed onto any selected input.

While both of the features were designed for specific uses, their flexibility makes it possible to use them in a variety of ways.

2. What is digital RGB overlay and how does it work?

   The RGB overlay allows the TVP5146 to accept digital inputs from a Line 21 decoder or other VBI data decoders in order to overlay the character data onto the designated video input. The required inputs into the TVP5146 for the RGB overlay are DR, DG, DB, and FSO. The FSO is the fast switch signal used to indicate to the TVP5146 when the digital RGB character should be mixed with the video input on a pixel basis.

3. What inputs can I overlay data onto?

   The TVP5146 is unique from other video decoders that support RGB overlay in that you can overlay your data onto any analog input, CVBS, SV, YPbPr/RGB component and SCART.

4. What is the difference between FSO and FSS?

   FSO is the Fast Switch Overlay input signal for the digital RGB overlay feature. This allows the digital RGB data from a Line 21 decoder or other VBI decoder to be soft mixed onto any selected analog input into the TVP5146.

   FSS is the Fast Switch SCART input signal for the analog component RGB overlay feature of the TVP5146. This allows, for example, a CVBS input to be overlayed onto a component RGB input for a SCART interface.

13 Automatic Gain Control (AGC)

1. Does the TVP5146 support manual gain and offset control?

   The TVP5146 only supports manual gain control. Manual offset control is not supported. In order to enable manual gain, the AFE Gain Control Register, 01h, must be set to 0Ch. The manual gain control registers begin with the AFE Coarse Gain for Ch1 Register at 46h and ends with the AFE Fine Gain for CVBS_Luma Register at 51h.

14 Audio Clocks

1. Does the TVP5146 support audio clocks?

   No, the TVP5146 does not directly support audio clocks. However, we recommend using the low-cost PLL1708 to generate synchronized audio clocks from the DATACLK output of the TVP5146.

2. Since the TVP5146 does not support audio clocks, what device(s) do you recommend to generate these clocks?

   We recommend using the low-cost PLL1708 to generate synchronized audio clocks from the DATACLK output of the TVP5146.

15 TVP5146EVM and WinVCC4 Questions

1. When using WinVCC4, I get I2C communication errors. What is the problem?

   Please refer to the following table (Table 10) to resolve any I2C communication errors.

Table 10. I2C Communications Errors

No I2C communication.	I2C slave address is wrong.	Close and restart WinVCC4. Choose the alternate slave address in the WinVCC4 Configuration dialog.
	Parallel cable is not connected from PC parallel port to the EVM DB25 connector.	Connect cable.
	EVM is not powered on.	Power supply must be plugged into a 110V/60Hz power source and the cord must be plugged into the power connector on the EVM.
	Wrong type of parallel cable.	Some parallel cables are not wired straight through pin-for-pin. Use the cable supplied with the EVM.
	PC parallel port mode is not set correctly.	Reboot PC, enter BIOS setup program, set parallel port LPT1 mode (Addr 378h) to DCP mode or bidirectional mode (sometimes called PS/2 mode or byte mode). If already set to one of these two modes, switch to the other setting.
	Device was placed in power-down mode.	Press the reset button on the TVP5146EVM.
	EVM was configured for an external I2C master.	Re-install 0-ohm resistors R5 and R6. Control EVM using the PC parallel port.
	Still no I2C communication	PC may not be capable of operating in the required parallel port mode. This is true of some laptop computers. Use a different computer, preferably a desktop PC.

2. What Windows operating systems does WinVCC4 support?

   WinVCC4 supports Win95, Win98, WinME, WinNT, Win2000 and WinXP operating systems. Port95nt.exe must be installed regardless of the OS.

3. I have the TVP5146 powered up with everything connected. I2C communication is okay and I loaded the dataset from the CMD file, but there is no video.

Typically this can be resolved by verifying the WinVCC4 default input connection with the physical input connection on the TVP5146EVM.

4. What is the Port95nt.exe and is it required in order to use the TVP5146EVM?

   Port95nt.exe is a parallel port I/O driver and is required for WinVCC4 to operate correctly. The order of installation is not important as long as both Port95nt and WinVCC4 are running on the same PC.

5. Can I use WinVCC4 to communicate with devices not listed in the I2C Address Configuration screen?

   Yes, WinVCC4 is capable of supporting I2C devices that are not listed in the I2C Address Configuration screen. Once the configuration of the TI devices is complete, click on Edit->Register Map->Generic I2C. From this window it is possible to specify any I2C slave address, register address or data. WinVCC4 supports I2C read and write capability for Generic I2C devices.

6. Do I need to supply 5 V to each DC supply jack on the TVP5146EVM?

   No, only one DC supply jack should be installed and powered up. The 5-V supply is then shared across the 120-pin connector interface to supply the other board.

7. Do I need to connect a parallel port cable to each DB25 connector on the TVP5146EVM in order to communicate with both devices?

   No, only one DB25 connector should be installed. The I2C SDA and SCL signals are then shared across the 120-pin connector interface in order to provide I2C communication to both boards. Also, SCL and SDA testpoints are available on both boards of the TVP5146EVM.

8. How many PCB layers does the TVP5146EVM use?

   The TVP5146EVM uses four layers on each board. There is a top and bottom signal layer, a split power plane, and a semi-split ground plane. A semi-split ground plane is technically one plane but the analog and digital areas on the board are isolated by a 30mil trace. The analog and digital areas of the ground plane are connected under the TVP5146.

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